



### DESCRIPTION

The MPQ6631H is a three-phase, brushless DC (BLDC) motor driver with integrated power MOSFETs. The device supports a single external Hall sensor or three external Hall-effect sensors to drive a three-phase BLDC motor, with up to 3A of peak phase current and an input voltage ( $V_{IN}$ ) range between 3.6V and 35V.

The MPQ6631H controls the motor speed through the pulse-width modulation (PWM) signal or the DC signal on the PWM/DC pin with closed-/open-loop control. The device features a built-in, configurable speed curve function. It also features a sinusoidal drive for maximum torque, as well as low speed ripple and noise across the full speed range.

The MPQ6631H provides rotational speed detection. The rotational speed detector (the FG/RD pin) is an open-drain output. It outputs a high or low voltage relative to the Hall comparator's output. Direction control is achieved via the DIR pin's input.

Rich protection features include input over-voltage protection (OVP), under-voltage lockout (UVLO), locked-rotor protection, over-current protection (OCP), and thermal shutdown protection.

The MPQ6631H is available in a TQFN-26 (3mmx4mm) package with wettable flanks. It is available in AEC-Q100 Grade 1.

### FEATURES

- 3.6V to 35V Operating Input Voltage ( $V_{IN}$ ) Range
- Up to 3A of Peak Phase Current
- Integrated 160m $\Omega$  High-Side MOSFETs (HS-FETs) and Low-Side MOSFETs (LS-FETs)
- Sinusoidal Drive
- Supports a 0V to 1.2V DC Input or 1kHz to 100kHz Pulse-Width Modulation (PWM) Input
- Supports Triple-Hall or Single-Hall Inputs
- Closed-/Open-Loop Speed Control
- Direction/Brake Input
- Power-Save Mode
- 0.5s/4.5s Lock Protection
- Over-Current Protection (OCP)
- Single-Pulse or Triple-Pulse FG Output per Electrical Cycle
- FG Signal: Rotational Speed Indication
- Soft Start (SS) for Low Noise and Current Overshoot
- Available in a TQFN-26 (3mmx4mm) Package with Wettable Flanks
- Available in AEC-Q100 Grade 1

### APPLICATIONS

- Fans
- Automotive Fans
- General Three-Phase Brushless DC (BLDC) Motors
- Pumps

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## TYPICAL APPLICATION

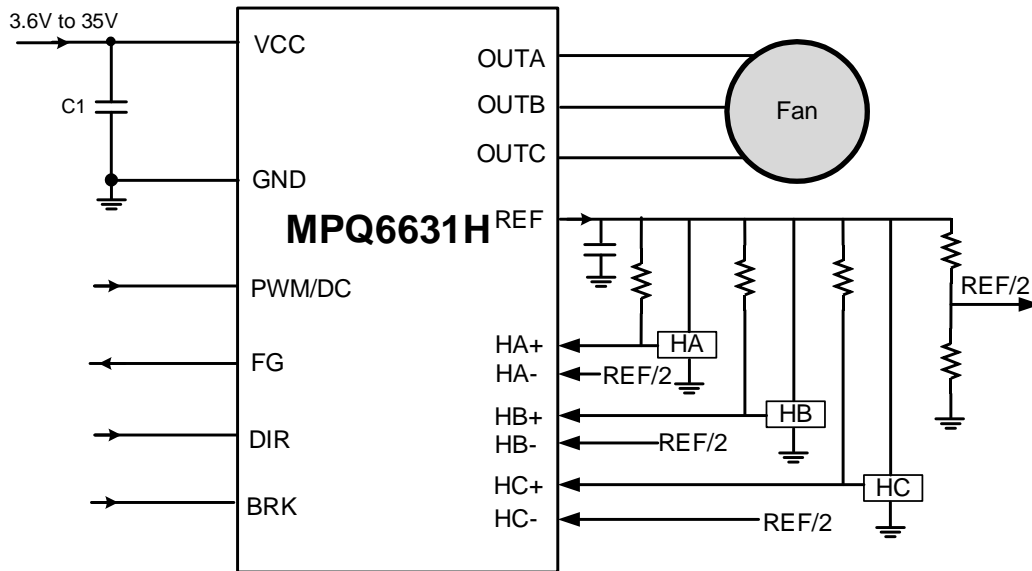


Figure 1: Triple Hall-Effect Sensor Application

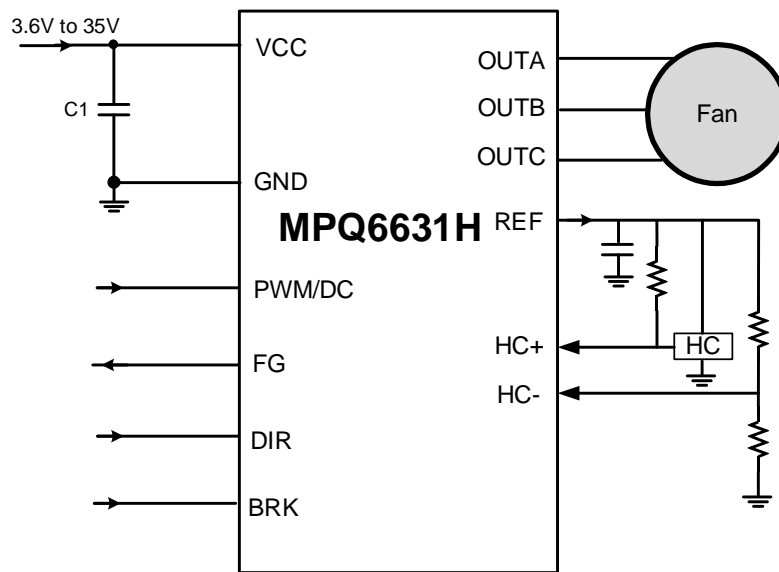


Figure 2: Single Hall-Effect Sensor Application

## ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Level
MPQ6631HGLTE-xxxx-AEC1**	TQFN-26 (3mmx4mm) with wettable flank	See Below	1

\* For Tape & Reel, add suffix -Z (e.g. MPQ6631HGLTE-xxxx-AEC1-Z).

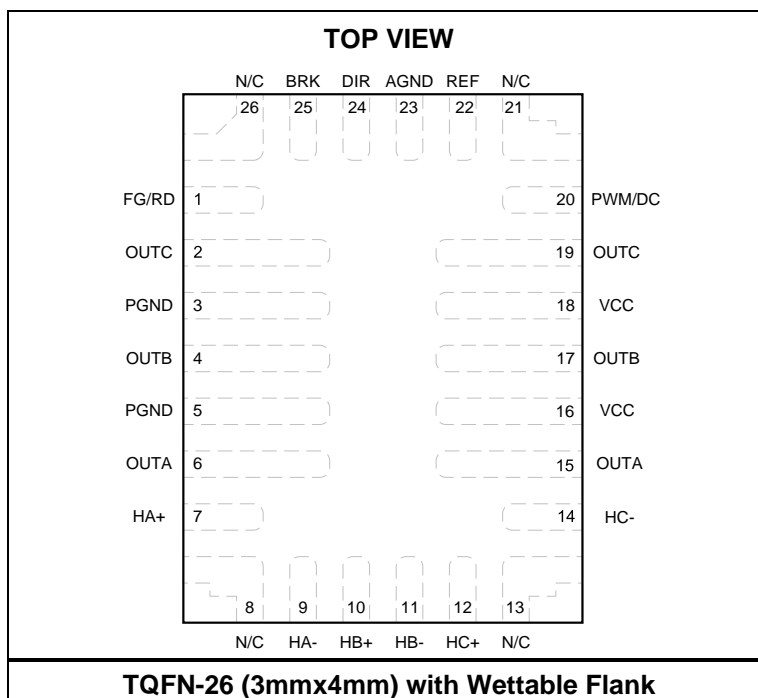
\*\* “xxxx” is the configuration code identifier. The first four digits of the suffix (“xxxx”) can be a hexadecimal value between 0 and F. Work with an MPS FAE to create this unique number for non-default options. The default code is “0000”.

## TOP MARKING

**MPYW**  
**6631**  
**HLLL**  
**E**

MP: MPS prefix  
Y: Year code  
W: Week code  
6631H: Part number  
LLL: Lot number  
E: Wettable flank

## PACKAGE REFERENCE



## PIN FUNCTIONS

Pin #	Name	Description
1	FG/RD	<b>Speed or rotor lock indication.</b> Open-drain output. FG/RD can be used for speed indication (FG) or rotor lock indication (RD). Pull up this pin externally.
2, 19,	OUTC	<b>Phase C terminal.</b>
3, 5	PGND	<b>Power ground.</b>
4, 17	OUTB	<b>Phase B terminal.</b>
6, 15	OUTA	<b>Phase A terminal.</b>
7	HA+	<b>Phase A's positive Hall input terminal.</b>
9	HA-	<b>Phase A's negative Hall input terminal.</b>
10	HB+	<b>Phase B's positive Hall input terminal.</b>
11	HB-	<b>Phase B's negative Hall input terminal.</b>
12	HC+	<b>Phase C's positive Hall input terminal.</b>
14	HC-	<b>Phase C's negative Hall input terminal.</b>
16, 18	VCC	<b>Input voltage supply pin.</b> The VCC pin must be locally bypassed.
20	PWM/DC	<b>Rotational speed control input pin.</b> Pull the PWM/DC pin high internally with a 500kΩ resistance. When DC_PWM = 0, apply a 1kHz to 100kHz pulse-width modulation (PWM) signal to this pin for speed control. When DC_PWM = 1, apply a 0V to 1.2V DC voltage to this pin for speed control.
22	REF	<b>5V LDO output.</b> The REF pin must be locally bypassed.
23	AGND	<b>Analog ground.</b>
24	DIR	<b>Direction control pin.</b> Pull the DIR pin low for forward rotation (A → B → C); pull it high for reverse rotation (A → C → B). Internally pull this pin down with a resistor.
25	BRK	<b>Brake pin.</b> Pull BRK high to brake the motor; pull it low internally using a resistor.
8, 13, 21, 26	NC	<b>No connection.</b>

## ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

Supply voltage ( $V_{CC}$ ) ..... -0.3V to +38V  
OUTA, OUTB, OUTC ..... -0.3V to  $V_{CC} + 0.3V$   
All other pins ..... -0.3V to +5.8V  
Lead temperature ..... 260°C  
Continuous power dissipation ( $T_A = 25^\circ C$ ) <sup>(2)</sup>  
..... 2.6W  
Junction temperature ( $T_J$ ) ..... 150°C  
Storage temperature ..... -60°C to +150°C

## ESD Ratings

Human body model (HBM) ..... 2kV  
Charged-device model (CDM) ..... 2kV

## Recommended Operating Conditions <sup>(3)</sup>

Supply voltage ( $V_{CC}$ ) ..... 3.6V to 35V  
Operating junction temp ( $T_J$ ) .... -40°C to +150°C

## Thermal Resistance <sup>(4)</sup> $\theta_{JA}$ $\theta_{JC}$

TQFN-26-WF (3mmx4mm) ..... 48 ..... 11... °C/W

### Notes:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature,  $T_J$  (MAX), the junction-to-ambient thermal resistance,  $\theta_{JA}$ , and the ambient temperature,  $T_A$ . The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_D$  (MAX) =  $(T_J(\text{MAX}) - T_A) / \theta_{JA}$ . Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- The device is not guaranteed to function outside of its operating conditions.
- Measured on a JESD51-7, 4-layer PCB.

## ELECTRICAL CHARACTERISTICS

$V_{CC} = 12V$ ,  $T_J = -40^{\circ}C$  to  $+150^{\circ}C$ , unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input under-voltage lockout (UVLO) rising threshold	$V_{UVLO}$		3	3.3	3.5	V
Input UVLO hysteresis				360		mV
Operating supply current	$I_{CC}$			6.7		mA
Standby current	$I_{STANDBY}$			130		$\mu A$
DIR input high voltage	$V_{DIR\_H}$		1.5			V
DIR input low voltage	$V_{DIR\_L}$				0.4	V
BRK input high voltage	$V_{BRK\_H}$		1.5			V
BRK input low voltage	$V_{BRK\_L}$				0.4	V
Pulse-width modulation (PWM) input high voltage	$V_{PWM\_H}$	DC_PWM = 0	1.5			V
PWM input low voltage	$V_{PWM\_L}$	DC_PWM = 0			0.4	V
PWM pull-up resistance	$R_{PWM}$	DC_PWM = 0		500		k $\Omega$
DC input high voltage	$V_{DC\_H}$	DC_PWM = 1	1.08	1.2	1.32	V
DC input low voltage	$V_{DC\_L}$	DC_PWM = 1		0		V
REF output voltage	$V_{REF}$			5.24		V
REF load regulation	$I_{REF\_LO}$	$I_{REF} = 30mA$		5.2		V
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)\_HS}$	$I_{OUT} = 100mA$		85		m $\Omega$
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)\_LS}$	$I_{OUT} = 100mA$		75		m $\Omega$
Cycle-by-cycle current limit	$I_{OCP}$	OCP_SEL = 11	2.7	3		A
PWM output frequency	$f_{SW}$	$T_J = 25^{\circ}C$	24.5	25	25.8	kHz
FG output low-level voltage	$V_{FG\_L}$	$I_{FG/RD} = 3mA$		0.2	0.4	V
Locked rotor detection time	$t_{RD}$			0.5		sec
Zero-current detection (ZCD) threshold	$I_{ZCD}$			5		mA
Hall sensor input low voltage, common mode	$V_{HCM\_LO}$			1		V
Hall sensor input high voltage, common mode	$V_{HCM\_HI}$			4.5		V
Hall sensor input voltage, differential mode	$V_{HDM}$	$V_{HCM} = 1V$ to $4.5V$		30		mV
Thermal shutdown threshold <sup>(5)</sup>				180		$^{\circ}C$
Thermal shutdown hysteresis <sup>(5)</sup>				25		$^{\circ}C$

### Note:

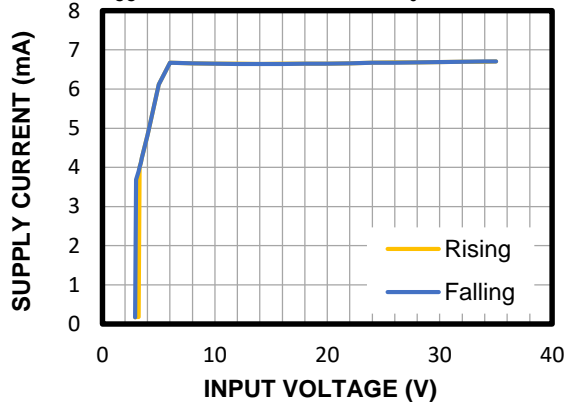
5) Guaranteed by design.

# TYPICAL CHARACTERISTICS

$V_{CC} = 12V$ ,  $T_J = -40^{\circ}C$  to  $+150^{\circ}C$ , unless otherwise noted.

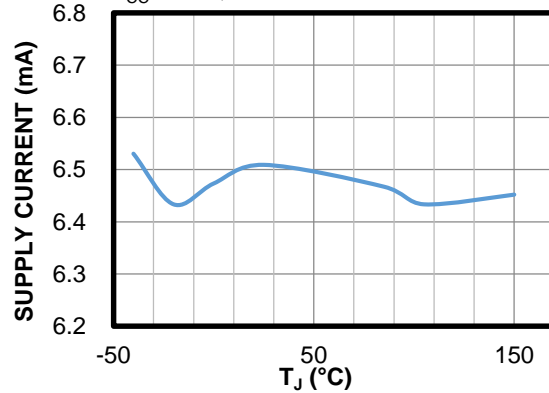
## Supply Current vs. Input Voltage

$V_{CC} = 2.9V$  to  $35V$ , no load,  $T_J = 25^{\circ}C$

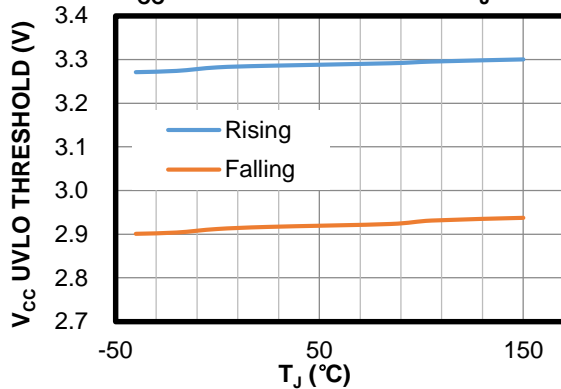


## Supply Current vs. $T_J$

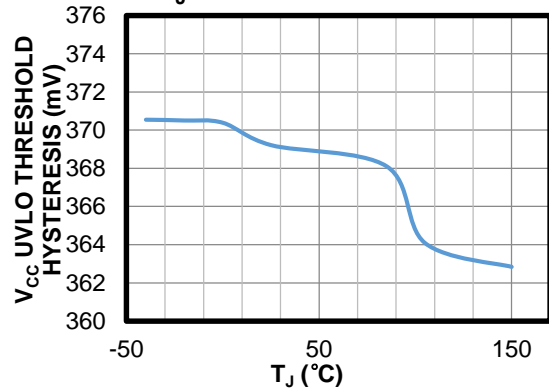
$V_{CC} = 12V$ , no load



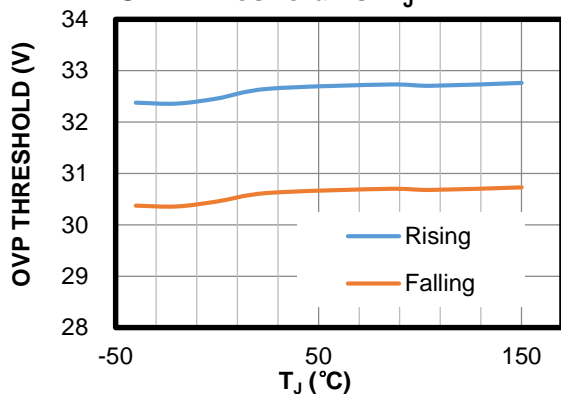
## $V_{CC}$ UVLO Threshold vs. $T_J$



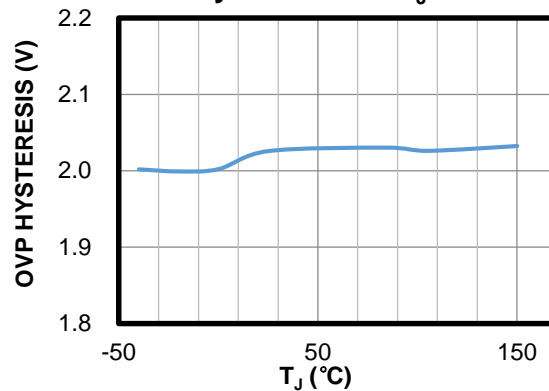
## $V_{CC}$ UVLO Threshold Hysteresis vs. $T_J$



## OVP Threshold vs. $T_J$

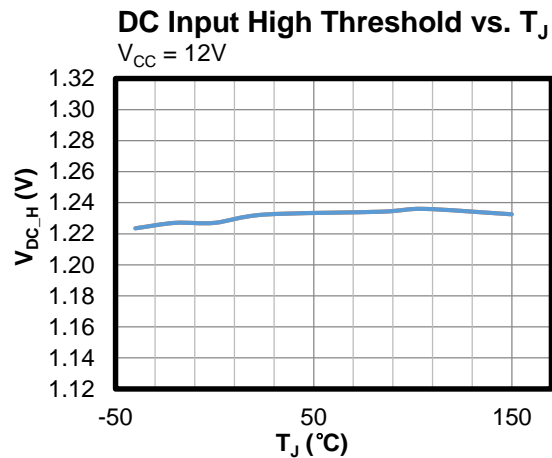
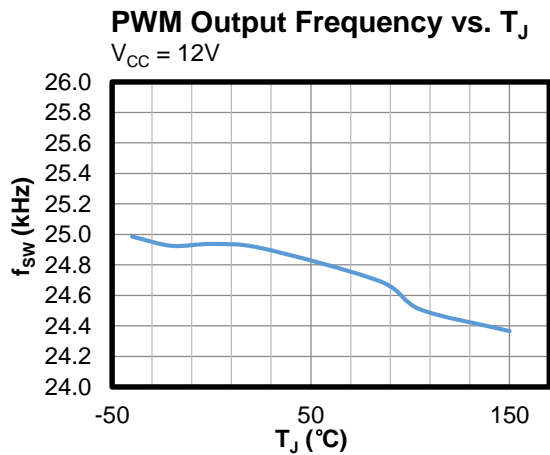
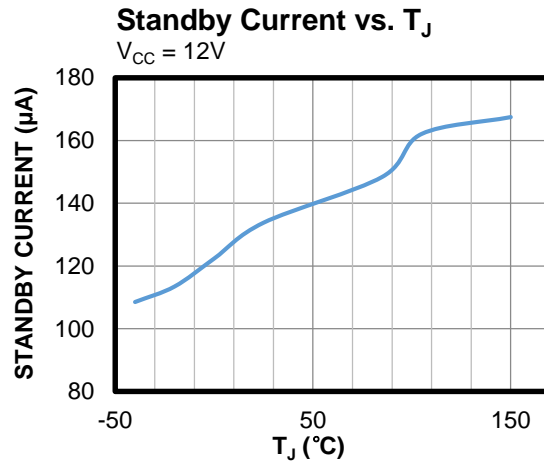
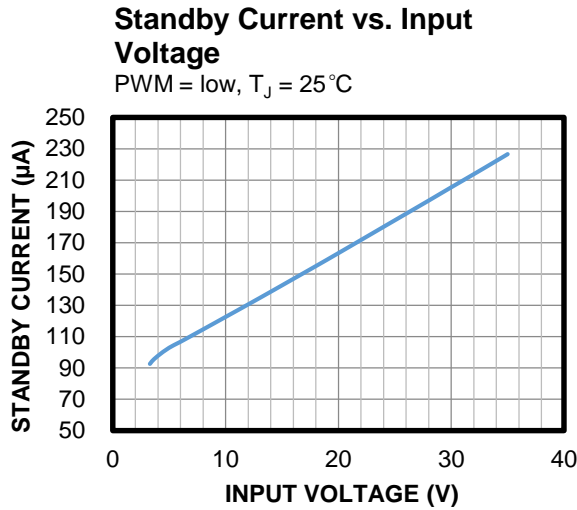
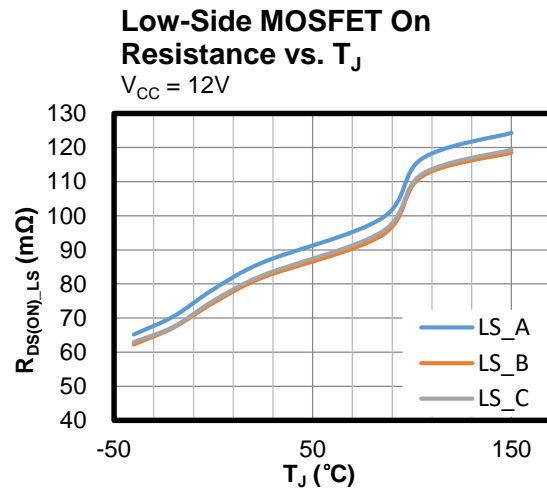
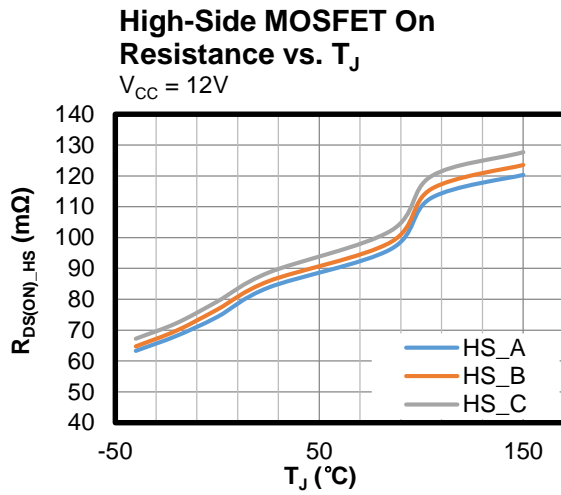


## OVP Hysteresis vs. $T_J$



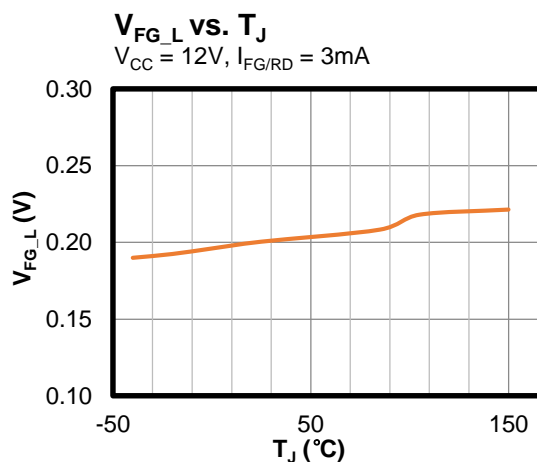
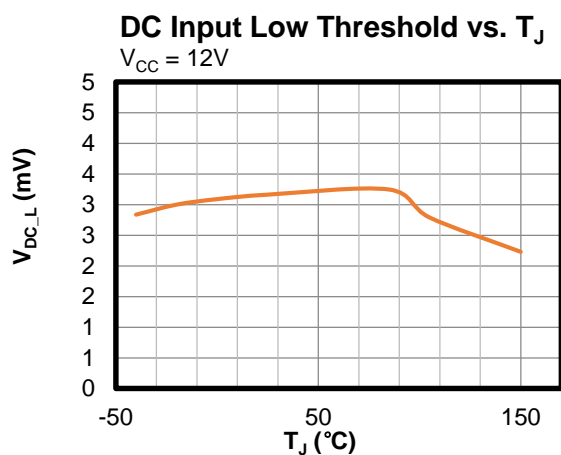
# TYPICAL CHARACTERISTICS (continued)

$V_{CC} = 12V$ ,  $T_J = -40^{\circ}C$  to  $+150^{\circ}C$ , unless otherwise noted.



# TYPICAL CHARACTERISTICS *(continued)*

$V_{CC} = 12V$ ,  $T_J = -40^{\circ}C$  to  $+150^{\circ}C$ , unless otherwise noted.



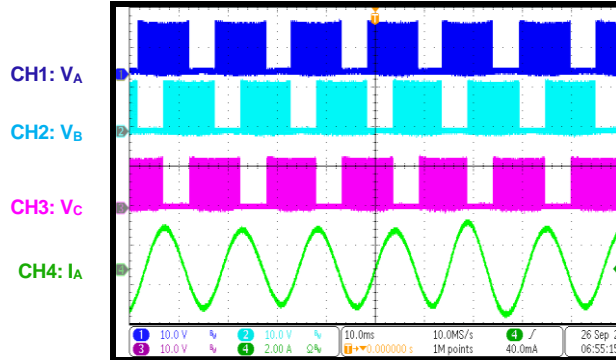


## TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board.  $V_{IN} = 12V$ , PWM frequency = 20kHz, with a single external Hall-effect sensor or three external Hall-effect sensors.

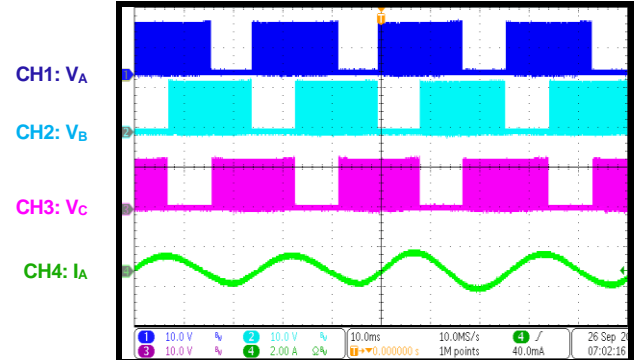
### Steady State

PWM duty cycle = 100%, DIR = low, counterclockwise



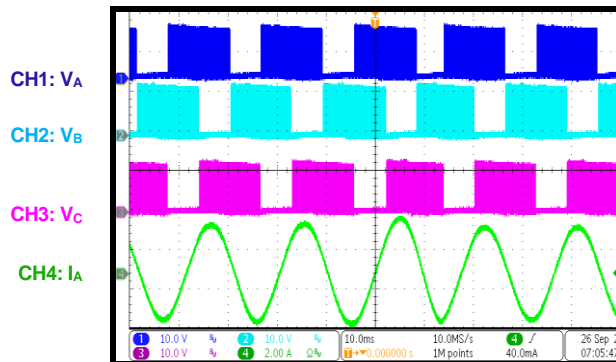
### Steady State

PWM duty cycle = 50%, DIR = low, counterclockwise



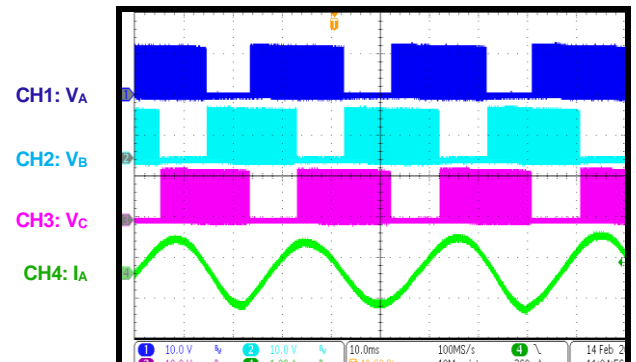
### Steady State

PWM duty cycle = 100%, DIR = high, clockwise



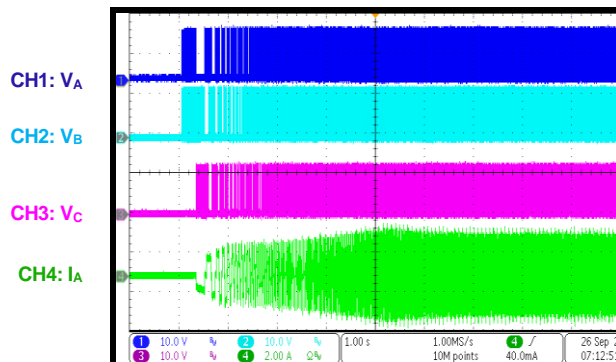
### Steady State

PWM duty cycle = 50%, DIR = high, clockwise



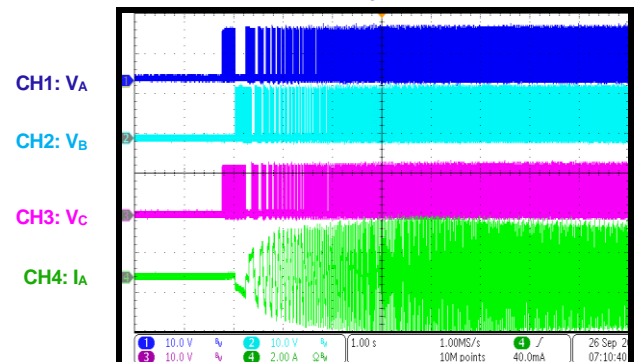
### PWM On

PWM duty cycle = 0% to 100%, three Hall-effect sensors, DIR = low, counterclockwise



### PWM On

PWM duty cycle = 0% to 100%, three Hall-effect sensors, DIR = high, clockwise

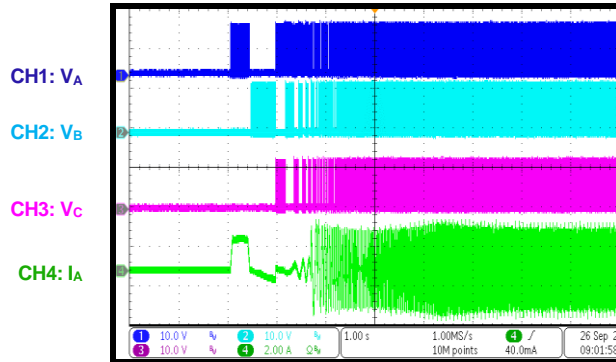


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board.  $V_{IN} = 12V$ , PWM frequency = 20kHz, with a single external Hall-effect sensor or three external Hall-effect sensors.

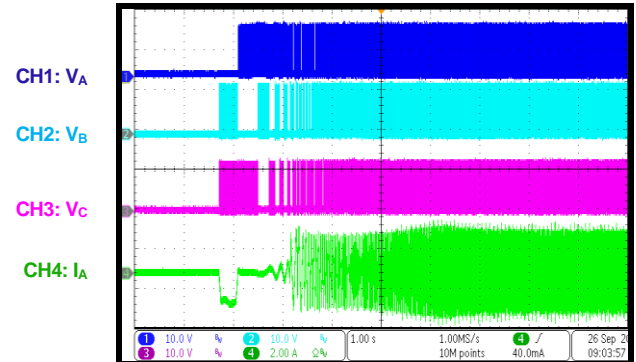
### PWM On

PWM duty cycle = 0% to 100%, single Hall-effect sensor, DIR = low, counterclockwise



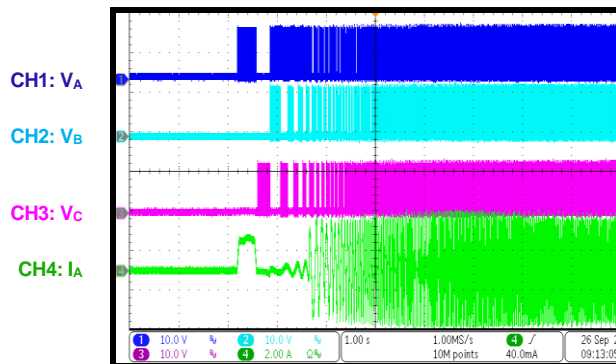
### PWM On

PWM duty cycle = 0% to 100%, single Hall-effect sensor, DIR = low, counterclockwise



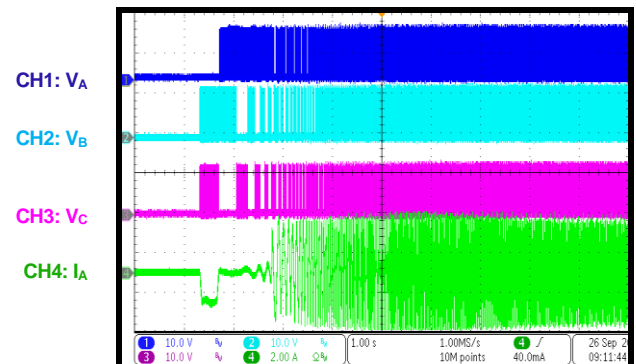
### PWM On

PWM duty cycle = 0% to 100%, single Hall-effect sensor, DIR = high, clockwise



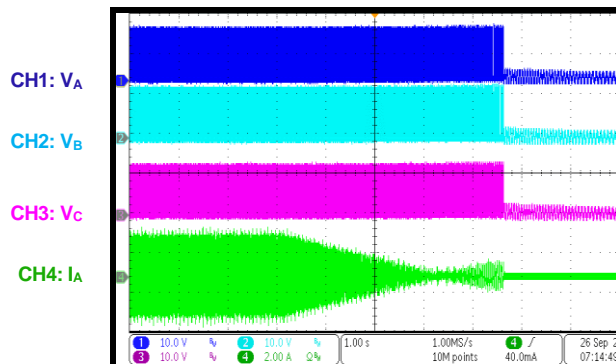
### PWM On

PWM duty cycle = 0% to 100%, single Hall-effect sensor, DIR = high, clockwise



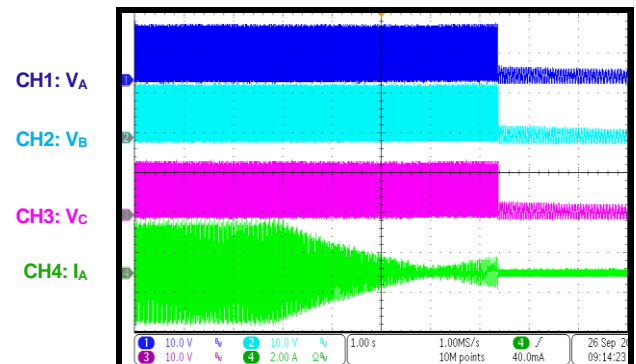
### PWM Off

PWM duty cycle = 100% to 0%, DIR = low, counterclockwise



### PWM Off

PWM duty cycle = 100% to 0%, DIR = high, clockwise

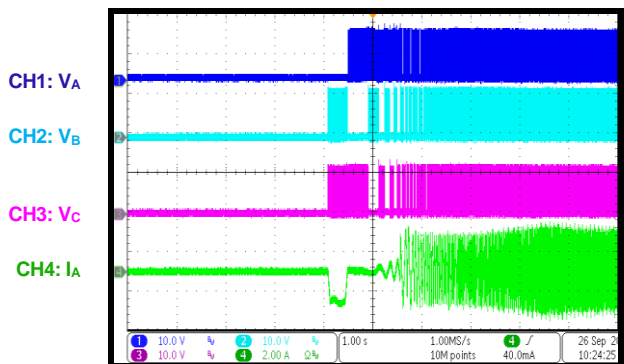


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board.  $V_{IN} = 12V$ , PWM frequency = 20kHz, with a single external Hall-effect sensor or three external Hall-effect sensors.

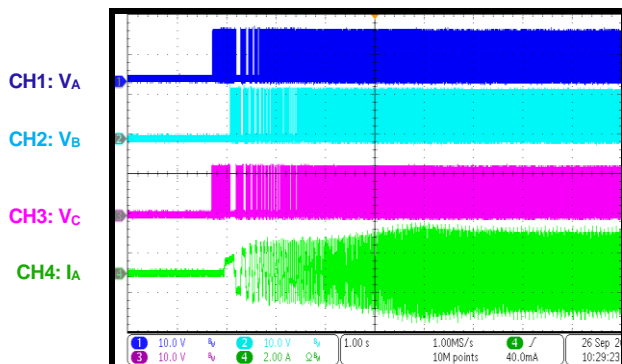
### Start-Up with VCC

$V_{CC} = 0V$  to 12V, PWM duty cycle = 100%, single Hall-effect sensor, DIR = low, counterclockwise



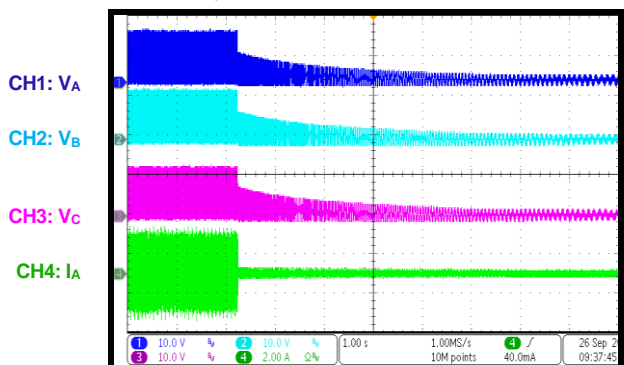
### Start-Up with VCC

$V_{CC} = 0V$  to 12V, PWM duty cycle = 100%, three Hall-effect sensors, DIR = low, counterclockwise



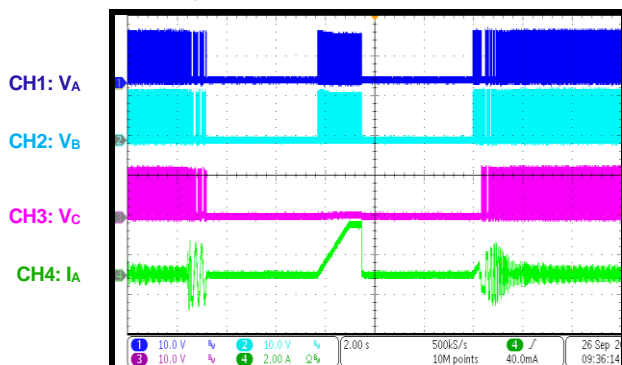
### Shutdown with VCC

$V_{CC} = 0V$  to 12V, PWM duty cycle = 100%, DIR = low, counter-clockwise



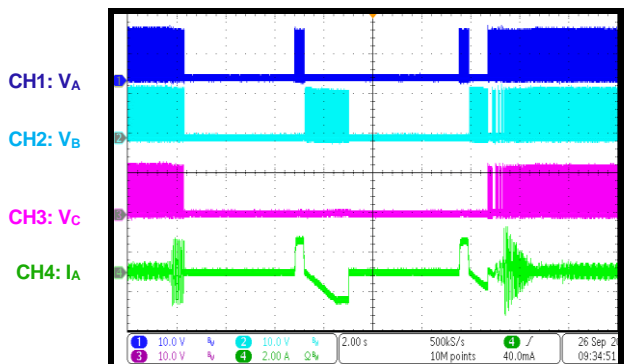
### Rotor Lock and Retry

PWM duty cycle = 25%, three Hall-effect sensors, lock rotor then release



### Rotor Lock and Retry

PWM duty cycle = 25%, single Hall-effect sensor, lock rotor then release



## FUNCTIONAL BLOCK DIAGRAM

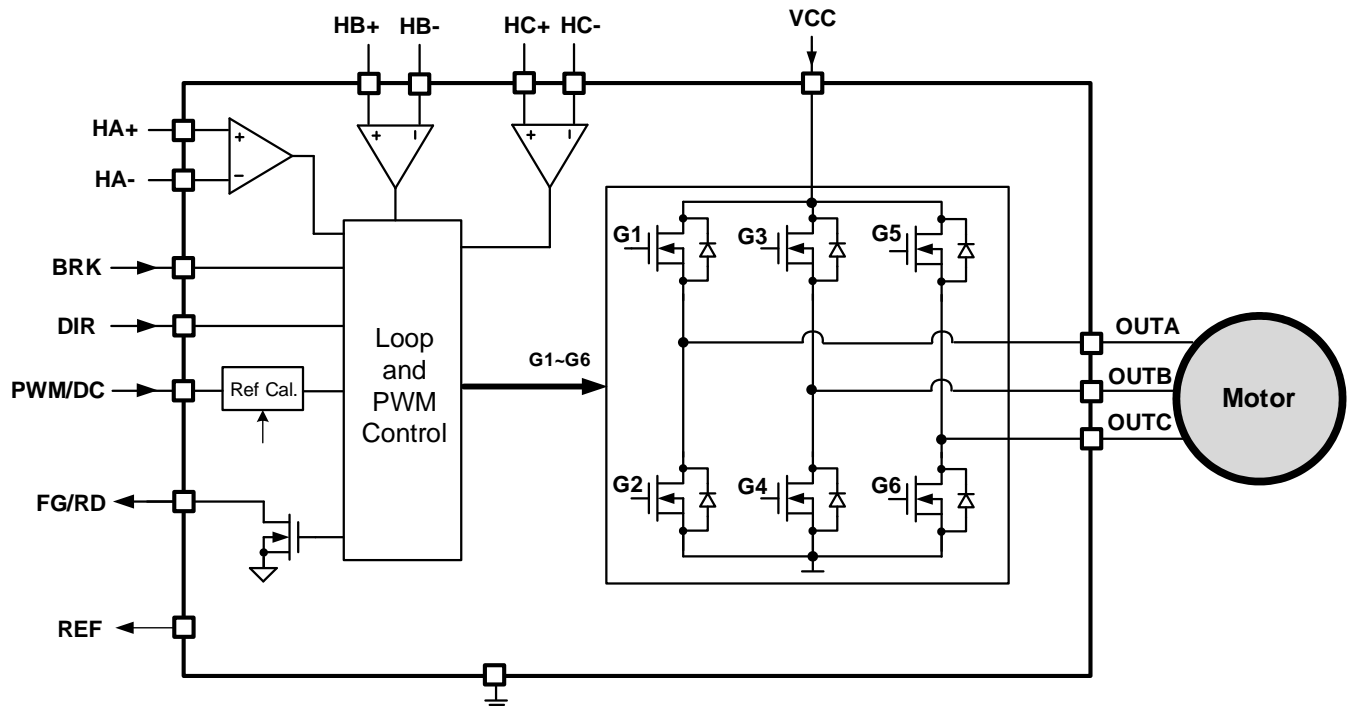


Figure 3: Functional Block Diagram

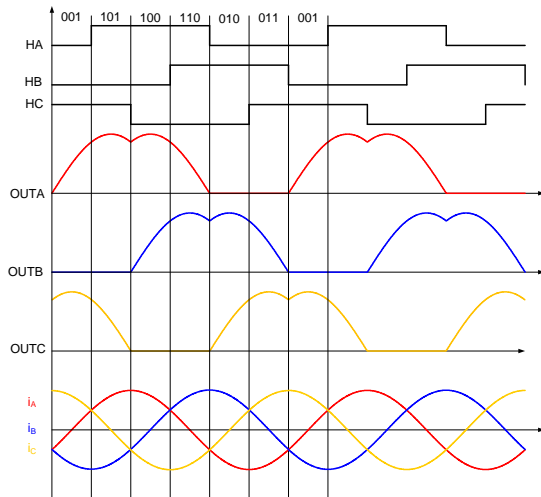
## OPERATION

The MPQ6631H is a three-phase brushless DC (BLDC) motor driver with integrated power MOSFETs. The MPQ6631H controls the motor speed via the pulse-width modulation (PWM) signal or the DC voltage on the PWM/DC pin, with closed-/open-loop speed control and a built-in, configurable speed curve function.

The MPQ6631H also features a rotational speed detector. The rotational speed detector (the FG/RD pin) is an open-drain output. It outputs a high or low voltage relative to the external Hall signal. Additionally, direction control is achieved via the DIR pin's input, and the BRK pin is used to brake the motor.

Rich protection features include input over-voltage protection (OVP), under-voltage lockout (UVLO), locked-rotor protection, over-current protection (OCP), and thermal shutdown protection.

A sinusoidal drive is employed in the MPQ6631H. Figure 4 shows the MPQ6631H's output drive, where HA, HB, and HC are the output of Hall A, Hall B, and Hall C, respectively. OUTA, OUTB, and OUTC are the output duty of the OUTA, OUTB, and OUTC pins, respectively.



**Figure 4: MPQ6631H Hall Output and Output Drive**

## Speed Control

The PWM/DC pin controls the motor speed in an open loop or closed loop via the PWM signal or the DC voltage. PWM/DC accepts a wide

input frequency range (1kHz to 100kHz) or a voltage between 0V and 1.2V.

If DC\_PWM = 1, then the motor speed is controlled via the DC voltage on the PWM/DC pin.

If DC\_PWM = 0, then the motor speed is controlled via the PWM input signal's duty cycle.

## Starting Duty and Minimum Speed

The starting duty cycle is configured by the DIN\_MIN bits. When the PWM input duty cycle is below the duty cycle set by DIN\_MIN, the fan speed supports two modes:

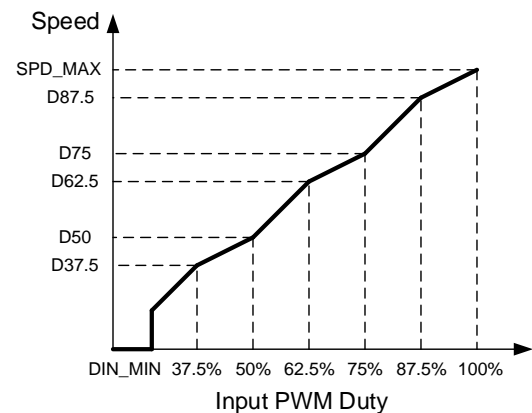
1. The speed maintains the minimum speed when SPD\_ZERO is set to 0.
2. The speed is at 0 when SPD\_ZERO is set to 1.

## Speed Curve Configuration

The SPD\_MAX registers configure the speed when the input duty cycle is at 100%. Otherwise, the MPQ6631H provides a five-point curve configuration function where the output speed can be configured when the input duty cycle is 37.5%, 50%, 62.5%, 75%, or 87.5%. Linear interpolation occurs between the adjacent duty cycles.

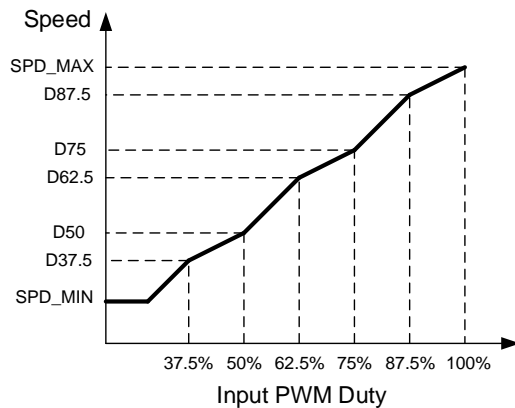
The DIN\_MIN register sets the minimum input duty cycle, and SPD\_MIN sets the minimum output duty cycle and minimum speed.

Figure 5 shows the curve configuration when SPD\_ZERO = 1.



**Figure 5: Curve Configuration when SPD\_ZERO = 1**

Figure 6 shows the curve configuration when SPD\_ZERO = 0.



**Figure 6: Curve Configuration when SPD\_ZERO = 0**

### Speed Open-/Closed-Loop Control

In closed-loop mode (OPEN\_L = 0, CLOSE\_H = 1), the MPQ6631H internally detects the Hall signal's speed and feedback to the control loop, which adjusts the PWM output duty cycle in a closed loop. By doing this, the motor speed follows the reference exactly.

In open-loop mode (OPEN\_L = 1), the OUT1 and OUT2 output duty cycles directly depend on the PWM input duty cycle.

In mixed mode (OPEN\_L = 0, CLOSE\_H = 0), the MPQ6631H operates in closed-loop mode when the PWM input duty cycle is below 87.5%, and the device operates in open-loop mode when the input duty cycle exceeds 87.5%.

### Soft-Start Time (t<sub>ss</sub>)

To reduce the input inrush current during start-up, the MPQ6631H provides the reference speed's configurable soft-start time (t<sub>ss</sub>) by setting register bits TDYN[1:0]. This time can be configured from 1.3s to 10.4s.

### Closed-Loop Integrator Gain

In closed-loop mode, the closed-loop integrator gain depends on registers KI and KP.

Higher KI and KP values lead to quick loop response. KI and KP should be adjusted according to the dynamic response and steady state operation.

### Single-Hall or Triple-Hall Input Mode

The MPQ6631H supports either a single or triple Hall-effect sensor. If a single Hall-effect sensor is employed, the Hall selection bit must set to support a single Hall sensor, and Hall C is used as the control.

### Direction Control

The direction is controlled by the DIR pin's polarity. When DIR is pulled low, the MPQ6631H operates in forward rotation in the following sequence: A to B to C to A.

When DIR is pulled high, the MPQ6631H operates in reverse rotation in the following sequence: A to C to B to A.

### Alignment

At the beginning of start-up in single Hall sensor applications, the MPQ6631H aligns the rotor in certain positions depending on the Hall outputs. After the alignment time set by the TPOS register is complete, the MPQ6631H enters pre start-up. This function is only enabled in single Hall sensor applications.

### Pre Start-Up Timer

During pre start-up, the MPQ6631H gradually increases the output duty cycle with the timer set by the TPRES[1:0] bits. This provides a sufficient torque for robust start-up and avoids current overshoot during start-up.

- TPRES = 0: the timer period is 2.5ms
- TPRES = 1: the timer period is 5ms
- TPRES = 2: the timer period is 10ms
- TPRES = 3: the timer period is 20ms

A higher timer period leads to a lower soft pre start-up current, but it increases the pre start-up time.

### Cycle-by-Cycle Over-Current Protection (OCP)

During normal switching, if the current flowing through the MOSFET exceeds the threshold set by bits OCP[1:0] after a set blanking time, then the high-side MOSFETs (HS-FETs) turn off and the low-side MOSFETs (LS-FETs) turn on immediately. The MPQ6631H resumes normal switching during the next switching cycle.



**Maximum Peak Current Limit**

If the load current is not limited by over-current protection (OCP) and the current exceeds the maximum peak current limit threshold (typically 6A), all MOSFETs turn off and the MPQ6631H tries to re-enable after a lock-retry time.

**Speed Detection**

The FG signal on the FG/RD pin outputs an internal Hall-changing signal for speed indication. Different FG signal frequencies are provided. The frequencies are selected by setting the FGRD bit to 00, 01, or 10.

FG/RD is an open-drain output, and it must be pulled up externally by a resistor.

**Locked-Rotor Protection**

If the motor rotor is locked and the Hall signal edge is not detected during the 0.5s detection time, then the MPQ6631H turns on all LS-FETs and automatically restarts after the recovery time (4.5s). By setting the FGRD bit to 11, the signal on FG/RD is set to locked-rotor indication. During a locked-rotor fault status, FG/RD remains low.

**Over-Voltage Protection (OVP)**

If the voltage on the VCC pin ( $V_{CC}$ ) exceeds the over-voltage (OV) threshold (34V), the MPQ6631H turns off the HS-FETs and turns on the LS-FETs. Once  $V_{CC}$  drops below 32V, the device resumes normal operation.

**Thermal Shutdown**

The MPQ6631H also provides thermal monitoring. If the MPQ6631H's die temperature exceeds 160°C, then the output duty cycle decreases to reduce power consumption until the die temperature drops below 135°C.

**Under-Voltage Lockout (UVLO)**

If the voltage on the VCC pin ( $V_{CC}$ ) falls below the UVLO threshold, all circuitry in the device is disabled and the internal logic is reset. Once  $V_{CC}$  exceeds the UVLO threshold, the device resumes normal operation.

**Test Mode and Factory Mode**

To configure the internal registers, the MPQ6631H supports test mode. In test mode, all internal registers can be read/written. After the design is finalized, the register value can be configured via the non-volatile memory (NVM), which can be configured twice. Refer to the MPS Fan Driver GUI Software for easy parameter changes and memory configuration.

## REGISTER MAP

Address	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
00h (OTP/REG)	SPD_MAX[7:0]							
01h (OTP/REG)	SPD_MAX[15:8]							
02h (OTP/REG)	SPD_MIN[7:0]							
03h (OTP/REG)	HI_FREQ	RESERVED	DIN_MIN[5:0]					
04h (OTP/REG)	OVP_EN	WAIT_TM[1:0]		RESERVED	MAX_EN	CLOSE_H	OPEN_L	RESERVED
05h (OTP/REG)	RESERVED	TDYN[1:0]		TPRE[1:0]		SPD_ZERO	SINGLE	RESERVED
06h (OTP/REG)	RESERVED		DC_PWM	FGRD[1:0]		ILIM[1:0]		TPOS
07h (OTP/REG)	RESERVED	SW_SEL	THETA_COMP[5:0]					
08h (OTP/REG)	KI[7:0]							
09h (OTP/REG)	KP[7:0]							
0Ah (OTP/REG)	RESERVED		WAIT_SEL	RESERVED		OCP_EN	OCP_BH	OVP_BH
0Bh (OTP/REG)	D37.5							
0Ch (OTP/REG)	D50							
0Dh (OTP/REG)	D62.5							
0Eh (OTP/REG)	D75							
0Fh (OTP/REG)	D87.5							
10h (REG)	RESERVED		OTP_PAGE[1:0]		RESERVED			DEBUG



## REGISTER DESCRIPTION

### MAX\_SPEED\_1 (0x00)

The MAX\_SPEED\_1 command sets maximum speed in close-loop control.

Bits	Access	Bit Name	Default	Description
7:0	R/W	SPD_MAX[7:0]	0xFF	Sets the maximum speed when the input duty cycle is 100%. These 8 bits are the least significant bit (LSB). The electrical speed = 7.5rpm/LSB. These bits are combined with SPD_MAX[15:8] to set the maximum speed (electrical speed).

### MAX\_SPEED\_2 (0x01)

The MAX\_SPEED\_2 command sets maximum speed in close-loop control.

Bits	Access	Bit Name	Default	Description
7:0	R/W	SPD_MAX[15:8]	0x08	Sets the maximum speed when the input duty cycle is 100%. These 8 bits are the most significant bit (MSB). These bits are combined with SPD_MAX[7:0] to set the maximum speed (electrical speed).

### MIN\_SPEED COMMAND (0x02)

The MIN\_SPEED command sets the minimum speed in closed-loop mode or the minimum output duty cycle in open-loop mode.

Bits	Access	Bit Name	Default	Description
7:0	R/W	SPD_MIN[7:0]	0x20	Sets the minimum speed or minimum output duty cycle. In closed-loop mode, this bit sets the minimum speed (electrical speed), depending on the HI_FREQ, where: HI_FREQ = 0, 60rpm/LSB HI_FREQ = 1, 480rpm/LSB In open-loop mode, this bit sets the minimum output duty cycle, where the minimum output duty cycle = SPD_MIN[7:0] / 255, and the default is 12.5%.

### CFR\_1 (0x03) (Control Function Register)

The CFR\_1 command sets the switching frequency and starting duty cycle.

Bits	Access	Bit Name	Default	Description
7	R/W	HI_FREQ	0	Selects the high frequency. The SW_SEL bit must be set to 1 if HI_FREQ = 1. 0: High frequency is not selected (default) 1: High frequency is selected
6	R	RESERVED	N/A	Reserved.
5:0	R/W	DIN_MIN[5:0]	0x10	Sets the starting duty cycle, where the starting duty cycle = DIN_MIN / 128, and the default is 12.5%.

### CFR\_2 (0x04)

The CFR\_2 command enables over-voltage protection (OVP), and sets the wait status, maximum speed below the starting duty cycle, and open-/closed-loop control.

Bits	Access	Bit Name	Default	Description
7	R/W	OVP_EN	0	Enables OVP. 0: Disabled (default) 1: Enabled

6:5	R/W	WAIT_TM[1:0]	00	<p>Selects the waiting time or speed threshold at start-up. Combined with WAIT_SEL, these bits can select the fixed time during which the IC waits before output switching, or they can select the motor speed threshold at which the IC starts driving the motor. This is active for triple Hall sensor applications.</p> <p>The waiting time or speed threshold can be selected as follows:</p> <p>If WAIT_SEL = 1, wait for a fixed time.</p> <p>00: 1.2s 01: 1.8s 10: 3s 11: 4.2s</p> <p>If WAIT_SEL = 0, wait for the motor speed to drop to a certain speed.</p> <p>00: 1000rpm (electrical speed) 01: 600rpm 10: 150rpm 11: 60rpm</p>
4	R	RESERVED	N/A	Reserved.
3	R/W	MAX_EN	0	<p>Enables the maximum speed when the PWM input duty cycle &lt; DIN_MIN. Active only when SPD_ZERO = 0.</p> <p>0: Disabled (default) 1: Maximum output speed or maximum output duty when PWM input duty &lt; DIN_MIN</p>
2	R/W	CLOSE_H	0	<p>Enables closed-loop speed control when the PWM input duty cycle &gt; 87.5%.</p> <p>0: Open-loop speed control when the PWM input duty cycle &gt; 87.5% (default) 1: Closed-loop speed control when the PWM input duty cycle &gt; 87.5%</p>
1	R/W	OPEN_L	1	<p>Enables open-loop speed control.</p> <p>1: Open-loop speed control (default) 0: Closed-loop speed control when the PWM input duty cycle &lt; 87.5%</p>
0	R	RESERVED	N/A	Reserved.

### START\_HALL (0x05)

The START\_HALL command sets the start-up, Hall, and dynamic operations.

Bits	Access	Bit Name	Default	Description
7	R	RESERVED	N/A	Reserved.
6:5	R/W	TDYN[1:0]	00	<p>Sets the soft dynamic time. The output duty cycle reference time determines how long it takes to rise from a 0% to 100% duty cycle.</p> <p>00: 1.3s (default) 01: 2.6s 10: 5.2s 11: 10.4s</p>

4:3	R/W	TPRE[1:0]	10	Sets the pre start-up time. The output duty cycle's time duration increases by 1 step. 00: 2.5ms 01: 5ms 10: 10ms (default) 11: 20ms
2	R/W	SPD_ZERO	1	Enables zero speed. 0: Maintains the minimum speed when the PWM input duty cycle < DIN_MIN 1: Stops when the PWM input duty cycle < DIN_MIN
1	R/W	SINGLE	1	Selects the number of Hall sensors. 0: Triple Hall sensor application 1: Single Hall sensor application (default)
0	R	RESERVED	N/A	Reserved.

### CFR\_3 (0x06)

The CFR\_3 command sets the PWM input, FG/RD output, current-limit threshold, and alignment time.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5	R/W	DC_PWM	0	Selects the DC input or PWM input for the PWM/DC pin. 0: PWM input (default) 1: DC input
4:3	R/W	FGRD[1:0]	00	Selects the FG/RD pin's output. 00: 1x (default) 01: 1/2x 10: 1/4x for single Hall sensor applications, 3x for triple Hall sensor applications 11: RD
2:1	R/W	ILIM[1:0]	11	Sets the current-limit threshold. 00: 0.7A 01: 1.5A 10: 2.2A 11: 3A (default)
0	R/W	TPOS	0	Sets the alignment time. 0: 320ms (default) 1: 650ms

### PWM\_SW\_COMP (0x07)

The PWM\_SW\_COMP command sets the switching frequency and the compensation angle.

Bits	Access	Bit Name	Default	Description
7	R	RESERVED	N/A	Reserved.
6	R/W	SW_SEL	0	Selects the output switching frequency ( $f_{sw}$ ). 0: 25kHz (default) 1: 50kHz

5:0	R/W	THETA_COMP[5:0]	0x00	<p>Sets the leading/lag compensation angle.</p> <p>0x00: Auto compensation</p> <p>The non-zero value sets the fixed compensation. The MSB is the signed bit.</p> <p>MSB = 0: leading. The compensation angle can be calculated with the following equation:</p> $\text{Compensation Angle} = \text{THETA\_COMP}[5:0] \times 15 / 8^\circ + 0.94^\circ$ <p>MSB = 1 lag. The compensation angle can be calculated with the following angle:</p> $\text{Compensation Angle} = 119.06^\circ - \text{THETA\_COMP}[5:0] \times 15 / 8^\circ$
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### KI (0x08)

The KI command configures the integral parameter in closed-loop control.

Bits	Access	Bit Name	Default	Description
7:0	R/W	KI[7:0]	0x01	Sets the integral parameter for closed-loop speed control.

### KP (0x09)

The KP command configures the gain parameter in closed-loop control.

Bits	Access	Bit Name	Default	Description
7:0	R/W	KP[7:0]	0x01	Sets the gain during closed-loop speed control.

### CFR\_4 (0x0A)

The CFR\_4 command sets the wait configuration as well as parameters for over-current protection (OCP) and over-voltage protection (OVP).

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5	R/W	WAIT_SEL	0	<p>Selects the waiting function at start-up.</p> <p>0: The IC does not drive until the speed drops below the threshold speed during start-up (default)</p> <p>1: The IC does not drive for a fixed time during start-up</p>
4:3	R	RESERVED	N/A	Reserved.
2	R/W	OCP	0	<p>Enables OCP.</p> <p>0: Enabled</p> <p>1: Disabled</p>
1	R/W	OCP_BH	0	<p>Selects the OCP response.</p> <p>0: Turn on the LS-FETs and resume switching during the next switching cycle (default)</p> <p>1: Decrease the output duty</p>
0	R/W	OVP_BH	0	<p>Selects the OVP response.</p> <p>0: Turn on the LS-FETs when OVP is triggered</p> <p>1: Turn off all the MOSFETs</p>

### SPEED\_CURVE\_1 (0x0B)

The SPEED\_CURVE\_1 command configures the speed when the PWM input duty cycle is 37.5%.

Bits	Access	Bit Name	Default	Description
7:0	R/W	D37.5[7:0]	0x60	<p>Sets the speed or output duty cycle when the PWM input duty cycle is 37.5%.</p> <p>For open-loop control, set the output duty cycle when the PWM input duty cycle is 37.5%. The output duty cycle can be calculated with the following equation:</p> $\text{Output Duty Cycle} = \text{D37.5}[7:0] / 256$ <p>For closed-loop control, set the speed reference when the PWM input duty cycle is 37.5%. The speed can be calculated with the following equation:</p> $\text{Speed} = \text{D37.5}[7:0] / 256 \times \text{SPD\_MAX}[15:0]$

### SPEED\_CURVE\_2 (0x0C)

The SPEED\_CURVE\_2 command configures the speed when the PWM input duty cycle is 50%.

Bits	Access	Bit Name	Default	Description
7:0	R/W	D50[7:0]	0x80	<p>Sets the speed or output duty cycle when the PWM input duty cycle is 50%.</p> <p>For open-loop control, set the output duty cycle when the PWM input duty cycle is 50%. The output duty cycle can be calculated with the following equation:</p> $\text{Output Duty Cycle} = \text{D50}[7:0] / 256$ <p>For closed-loop control, set the speed reference when the PWM input duty cycle is 50%. The speed can be calculated with the following equation:</p> $\text{Speed} = \text{D50}[7:0] / 256 \times \text{SPD\_MAX}[15:0]$

### SPEED\_CURVE\_3 (0x0D)

The SPEED\_CURVE\_3 command configures the speed when the PWM input duty cycle is 62.5%.

Bits	Access	Bit Name	Default	Description
7:0	R/W	D62.5[7:0]	0xA0	<p>Sets the speed or output duty when the PWM input duty cycle is 62.5%.</p> <p>For open-loop control, set the output duty cycle when the PWM input duty cycle is 62.5%. The output duty cycle can be calculated with the following equation:</p> $\text{Output Duty Cycle} = \text{D62.5}[7:0] / 256$ <p>For closed-loop control, set the speed reference when the PWM input duty cycle is 62.5%. The speed can be calculated with the following equation:</p> $\text{Speed} = \text{D62.5}[7:0] / 256 \times \text{SPD\_MAX}[15:0]$

### SPEED\_CURVE\_4 (0x0E)

The SPEED\_CURVE\_4 command configures the speed when the PWM input duty cycle is 75%.

Bits	Access	Bit Name	Default	Description
7:0	R/W	D75[7:0]	0xC0	<p>Sets the speed or output duty cycle when the PWM input duty cycle is 75%.</p> <p>For open-loop control, set output duty cycle when the PWM input duty cycle is 75%. The output duty cycle can be calculated with the following equation:</p> $\text{Output Duty Cycle} = \text{D75}[7:0] / 256$ <p>In closed-loop control, set the speed reference when the PWM input duty cycle is 75%. The speed can be calculated with the following equation:</p> $\text{Speed} = \text{D75}[7:0] / 256 \times \text{SPD\_MAX}[15:0]$

### SPEED\_CURVE\_5 (0x0F)

The SPEED\_CURVE\_5 command configures the speed when the PWM input duty cycle is 87.5%.

Bits	Access	Bit Name	Default	Description
7:0	R/W	D87.5[7:0]	0xE0	<p>Sets the speed or output duty cycle when the PWM input duty is 87.5%.</p> <p>For open-loop control, set the output duty cycle when the PWM input duty cycle is 87.5%. The output duty cycle can be calculated with the following equation:</p> $\text{Output Duty Cycle} = \text{D87.5}[7:0] / 256$ <p>For closed-loop control, set the speed reference when the PWM input duty cycle is 87.5%. The speed can be calculated with the following equation:</p> $\text{Speed} = \text{D87.5}[7:0] / 256 \times \text{SPD\_MAX}[15:8]$

### CFR\_5 (0x10)

The CFR\_5 command indicates the one-time programmable (OTP) memory page and sets the debugging mode.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:4	R	OTP_PAGE[1:0]	00	<p>Indicates the OTP page indicator.</p> <p>00: No OTP configured 01: OTP Page 1 is configured 10: OTP Page 2 is configured</p>
3:1	R	RESERVED	N/A	Reserved.
0	R/W	DEBUG	0	Debugging bit. Write 1 to this bit to exit debugging mode.

## APPLICATION INFORMATION

### Selecting the Input Capacitor

Place an input capacitor ( $C_{IN}$ ) as close to the VCC and GND pins as possible. A sufficient capacitance must be applied to maintain a stable input voltage ( $V_{IN}$ ) and reduces input switching voltage noise and ripple.  $C_{IN}$ 's impedance must be low at the switching frequency ( $f_{SW}$ ). Ceramic capacitors with X7R dielectrics are recommended for their low-ESR characteristics.

The capacitance depends on the DC voltage applied on the capacitor. A ceramic capacitor can lose more than 50% of its capacitance when the voltage is close to the voltage rating. Leave a sufficient voltage rating margin when selecting the capacitor.

It is recommended to use an additional electrolytic capacitor to absorb chargeback energy.

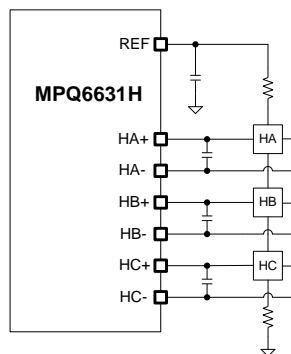
### Selecting the Input Clamping TVS Diode

High-voltage spikes are created when the energy stored in the motor charges back to  $C_{IN}$ . To avoid these spikes, a voltage-clamping transient voltage suppressor (TVS) diode is recommended. The maximum clamping voltage should be below the MPQ6631H's maximum operating  $V_{IN}$ .

### Hall Placement and Connection

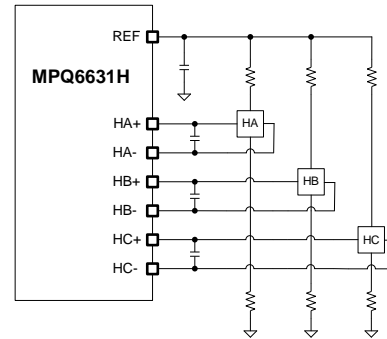
Hall sensors are required to operate the MPQ6631H, which supports Hall elements with differential inputs. When Hall elements are used, the Hall sensors can be connected in series or in parallel.

Figure 7 shows the Hall sensors connected in series.



**Figure 7: Series Hall Elements Connection**

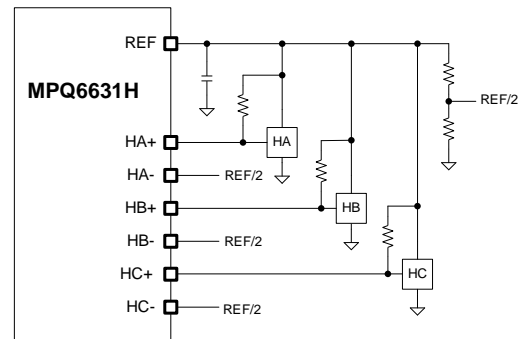
Figure 8 shows the Hall sensors connected in parallel.



**Figure 8: Parallel Hall Elements Connection**

The MPQ6631H's Hall-sensor IC outputs logic polarity with an open-drain output, and it requires an external pull-up resistor.

Figure 9 shows the Hall-sensor IC connection.



**Figure 9: Hall Sensor Connection**

### Hall Sensor Placement Example

The MPQ6631H supports either a single Hall-effect sensor or three Hall-effect sensors. Consider the Hall sensor placement for a 4-pole, 6-slot motor. There are two conditions to evaluate:

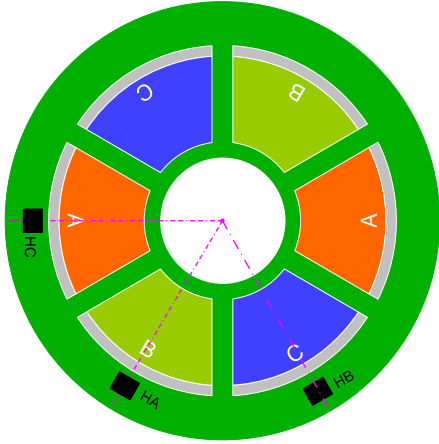
1. When the current flows into the stator phase winding, the north magnetic field is generated.
2. If the Hall sensor's output is high when the north pole is close to the Hall sensor's branded side.

If both conditions are satisfied, then the Hall sensor placement is as follows:

- Hall A is aligned with phase B's central line.
- Hall B is aligned with phase C's central line.

- Hall C is aligned with phase A's central line. In single Hall sensor applications, Hall C is the active Hall sensor.

Figure 10 shows the first Hall sensor placement option.

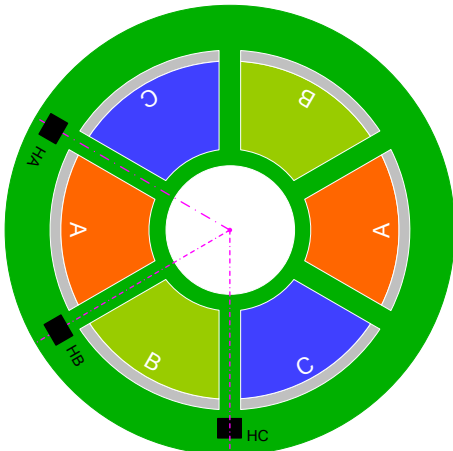


**Figure 10: First Hall Sensor Placement Option**

If one of these conditions is not satisfied, then the Hall sensor placement can be shifted 180° into an electrical angle, resulting in the following Hall sensor placement:

- Hall A is aligned with the central line of phase A and phase C.
- Hall B is aligned with the central line of phase A and phase B.
- Hall C is aligned with the central line of Phase B and Phase C.

Figure 11 shows the second Hall sensor placement option.

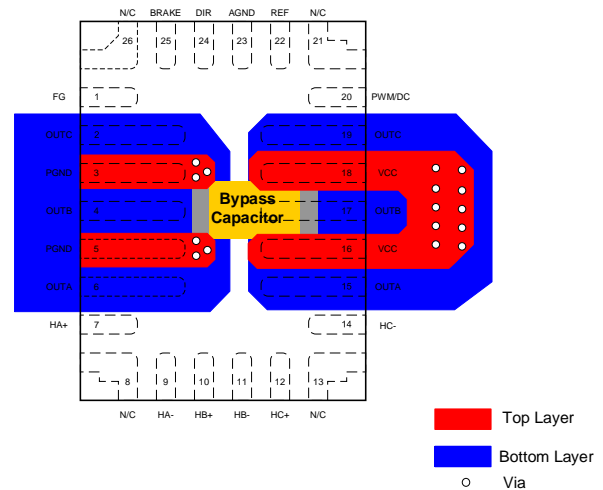


**Figure 11: Second Hall Sensor Placement Option**

## PCB Layout Guidelines

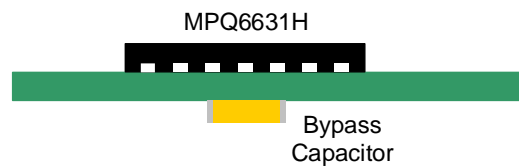
Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 12 and Figure 13, and follow the guidelines below:

- After selecting  $C_{IN}$ , place a 100nF/X7R bypass capacitor as close to the VCC and GND pins as possible.
- Figure 12 shows the recommended PCB layout when the MPQ6631H is placed on the top layer and the bypass capacitor is placed on the bottom layer.



**Figure 12: Recommended PCB Layout (Top View)**

- Figure 13 shows the side view of the MPQ6631H's recommended PCB layout.



**Figure 13: Recommended PCB Layout (Side View)**



## TYPICAL APPLICATION CIRCUIT

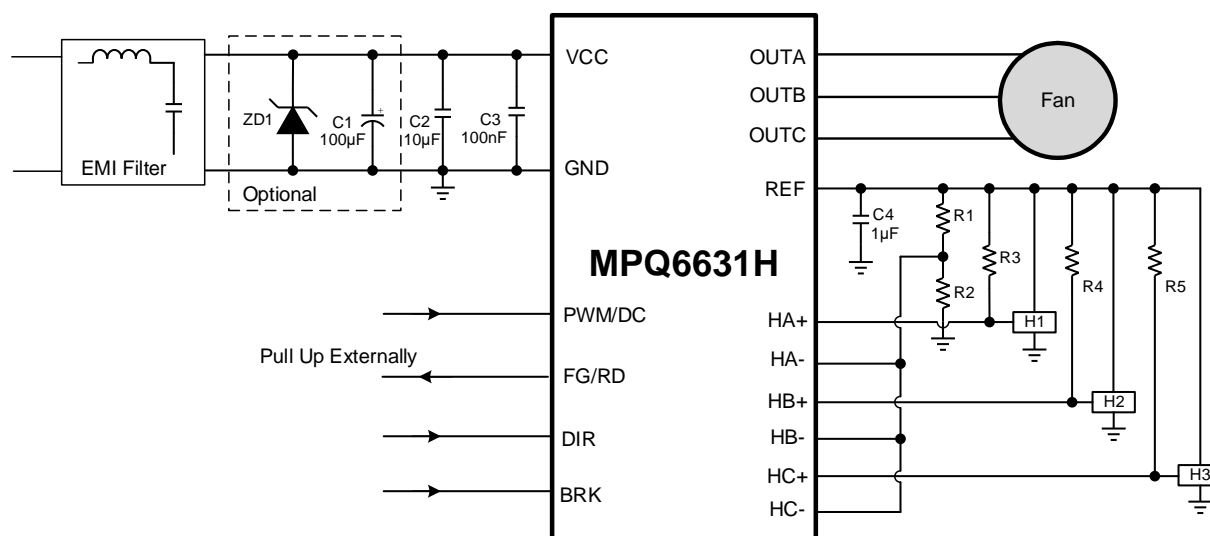
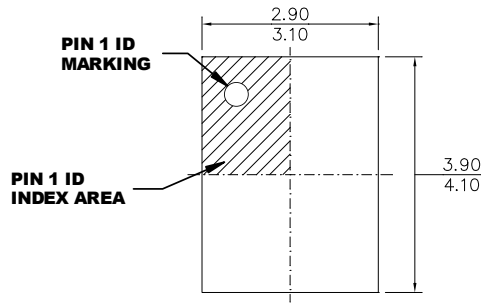


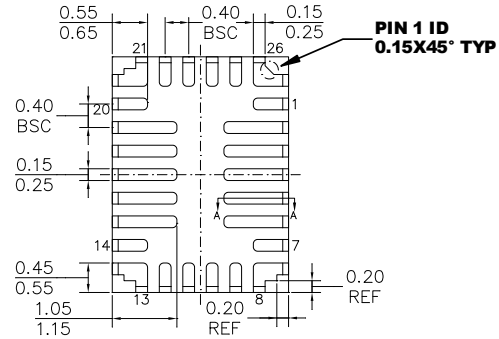
Figure 14: Typical Application Circuit (Triple Hall-Effect Sensor Application)

# PACKAGE INFORMATION

## TQFN-26 (3mmx4mm) with Wettable Flank



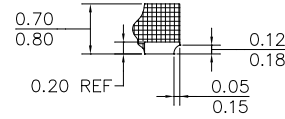
**TOP VIEW**



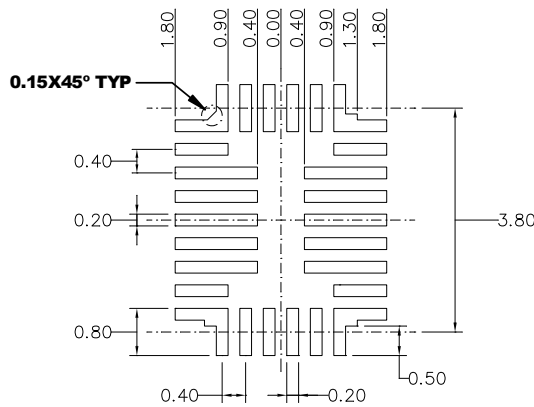
**BOTTOM VIEW**



**SIDE VIEW**



**SECTION A-A**

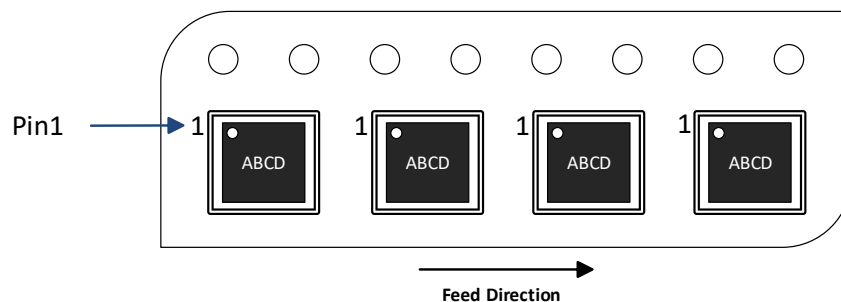
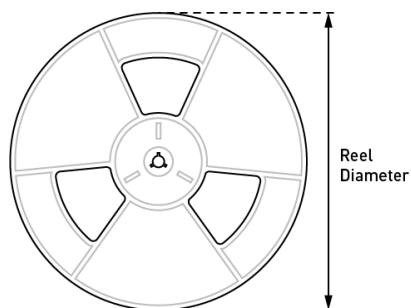


**RECOMMENDED LAND PATTERN**

### NOTE:

- 1) THE LEAD SIDE IS WETTABLE.
- 2) ALL DIMENSIONS ARE IN MILLIMETERS.
- 3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
- 4) JEDEC REFERENCE IS MO-220.
- 5) DRAWING IS NOT TO SCALE.

# CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ6631HGLTE-xxxx-AEC1-Z	TQFN-26-WF (3mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

## REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	3/13/2024	Initial Release	-

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