PCN Number:	20250430003.1	PCN Date:	May 01, 2025
Title:	Qualification of FFAB using qualified Process Technology, Die Revision, Datasheet and additional Assembly BOM options for select devices		
Customer Contact:	Change Management Team	Dept:	Quality Services
Proposed 1st Ship Date:	July 30, 2025	Sample requests accepted until:	June 30, 2025*

***Sample requests received after June 30, 2025 will not be supported.**

Change Type:

☐	Assembly Site	☒	Design	☐	Wafer Bump Material
☒	Assembly Process	☒	Data Sheet	☐	Wafer Bump Process
☒	Assembly Materials	☐	Part number change	☒	Wafer Fab Site
☐	Mechanical Specification	☐	Test Site	☒	Wafer Fab Material
☒	Packing/Shipping/Labeling	☐	Test Process	☒	Wafer Fab Process

PCN Details

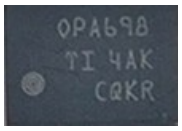
Description of Change:

Texas Instruments is pleased to announce the addition of FFAB using the BICOMHD qualified process technology and additional Assembly Site/BOM options for the devices listed below.

Current Fab Site			Additional Fab Site		
Current Fab Site	**Process**	**Wafer Diameter**	**Additional Fab Site**	**Process**	**Wafer Diameter**
SFAB	CBC10	150 mm	FFAB	BICOMHD	200 mm

The die was also changed as a result of the process change.

Construction differences are as follows:

	Current	Proposed
Passivation (PI) layer thickness	10um	20um
Wire bond diam/type	1.18mil Au	0.8mil Cu
Top side marking		

The datasheets will be changing as a result of the above mentioned changes. The datasheet change details can be reviewed in the datasheet revision history. The links to the revised datasheets are available in the table below.

TEXAS INSTRUMENTS

OPA698

SBOS258E – NOVEMBER 2002 – REVISED APRIL 2025

Changes from Revision D (December 2008) to Revision E (April 2025) **Page**

- Updated *Features*, *Applications*, and *Description* sections and with die redesign specifications; for updated specifications, see the *Specifications* section 1
- Updated the numbering format for tables, figures, and cross-references throughout the document 1
- Added *Pin Configuration and Functions* 2
- Changed the supply voltage specification from ±6.5V to 13V in *Absolute Maximum Ratings* 3
- Updated the table note in *Absolute Maximum Ratings* to add clarification 3
- Added Supply turn-on and turn-off rate and Continuous input current to *Absolute Maximum Ratings* 3
- Deleted soldering flow specification from *Absolute maximum specifications* 3
- Deleted machine model (MM) specification from *ESD Ratings* 3
- Added *Recommended Operating Conditions* 3
- Deleted minimum and overtemperature specifications in both *Electrical Characteristics AC Performance* 4
- Updated test conditions to both *Electrical Characteristics* for added clarity 4
- Updated table format for both *Electrical Characteristics* 4

- Deleted T_A = 0°C to +70°C specifications from all *Electrical Characteristics* 4
- Deleted Test Level column from all *Electrical Characteristics* 4
- Changed SSBW at G = 1V/V from 450MHz to 650MHz..... 4
- Added T_A = 25°C to the default test conditions to both *Electrical Characteristics*..... 4
- Updated *AC Performance* section with improved typical small signal bandwidth, slew rate, voltage noise, current noise, and distortion values in both *Electrical Characteristics* 4
- Changed Gain bandwidth product from 250MHz to 300MHz..... 4
- Changed typical Peaking at a gain of 1V/V from 5dB to 1.5dB..... 4
- Changed typical Slew rate from 1100V/µs to 1800V/µs..... 4
- Changed Rise and fall time at V_O = 0.2V Step from 1.6ns to 1.4ns..... 4
- Changed Settling time from 8ns to 25ns..... 4
- Changed typical 2nd-order harmonic distortion at R_L = 500Ω from –74dBc to –94dBc..... 4
- Deleted Differential gain and Differential phase specifications..... 4
- Changed typical 3rd-order harmonic distortion at R_L = 500Ω from –87dBc to –85dBc..... 4
- Changed typical Open-loop voltage gain from 63dB to 80dB..... 4
- Changed typical Input bias current from 3µA to ±0.2µA and Input offset current from ±0.3µA to ±0.1µA..... 4
- Changed typical Common-mode rejection ratio from 61dB to 82dB..... 4
- Changed Input impedance Differential-mode from 0.32 || 1MΩ || pF to 1 || 0.3MΩ || pF..... 4
- Changed the typical Input impedance common-mode from 3.5 || 1MΩ || pF to 33 || 1.4MΩ || pF..... 4
- Changed Current output sourcing and sinking from 120mA and –120mA to +190mA and –190mA..... 4
- Changed maximum Limiter input bias current magnitude, T_A = –40°C to +85°C from 64µA to 65µA..... 4
- Changed the typical Limiter input impedance from 3.4 || 1 MΩ || pF to 10 || 0.85 MΩ || pF..... 4
- Changed typical Limiter feedthrough from –68dB to –95dB..... 4
- Changed typical Limiter offset ±5mV from ±10mV..... 4
- Changed Op amp input bias current shift from 3µA to 0.15µA..... 4
- Changed Limiter small signal bandwidth from 600MHz to 700MHz..... 4
- Changed Limiter slew rate from 125V/µs to 175V/µs 4
- Changed maximum and minimum Quiescent current from 15.9mA to 17.3mA and 15.2mA to 13.8mA..... 4
- Changed minimum and maximum Quiescent current, T_A = –40°C to +85°C from 16.6mA to 17.7mA and 14.6mA to 13.4mA..... 4
- Changed typical Power-supply rejection ratio from 75dB to 90dB..... 4
- Moved *Thermal Characteristics* to *Thermal Information* table and *Recommended Operating Conditions* table 4
- Changed SSBW at G = 1V/V from 375MHz to 550MHz..... 6
- Changed Gain bandwidth product from 230MHz to 300MHz..... 6
- Changed typical Bandwidth for 0.1dB gain flatness typical value from 30MHz to 26MHz..... 6
- Changed typical Peaking at a gain of 1V/V from 7dB to 2.5dB..... 6
- Changed Rise and fall time at V_O = 0.2V step from 1.9ns to 1.4ns..... 6
- Changed Settling time from 12ns to 28ns..... 6
- Changed typical 2nd-order harmonic distortion at R_L = 500Ω from 69dBc to –95dBc..... 6
- Changed typical 3rd-order harmonic distortion at R_L = 500Ω from 73dBc to –81dBc..... 6
- Changed the typical Input voltage noise from 5.7nV/√Hz to 4nV/√Hz..... 6
- Changed the typical Input current noise from 2.3pA/√Hz to 1.4pA/√Hz..... 6
- Changed typical Open-loop voltage gain from 60dB to 77dB..... 6
- Changed typical Input bias current from ±3µA to ±0.5µA and Input offset current from ±0.4µA to ±0.1µA..... 6
- Changed typical Common-mode rejection ratio from 58dB to 82dB..... 6
- Changed Input impedance Differential-mode from 0.32 || 1 MΩ || pF to 0.77 || 0.3 MΩ || pF..... 6
- Changed the typical Input impedance common-mode from 3.5 || 1 MΩ || pF to 24 || 1.5MΩ || pF..... 6
- Changed Current output Sourcing and sinking from 70mA and –70mA to 170mA and –170mA..... 6
- Changed the typical closed-loop output impedance from 0.2Ω to 0.1Ω..... 6
- Changed Limiter Input Bias Current Magnitude from 16µA to 8µA..... 6
- Changed Limiter input impedance from 3.4 || 1 MΩ || pF to 1 || 7 MΩ || pF..... 6
- Changed typical Limiter feedthrough from –60dB to –92dB..... 6
- Deleted Bias current shift specification..... 6
- Changed Limiter small signal bandwidth from 450MHz to 515MHz..... 6
- Changed Limiter slew rate from 100V/µs to 150V/µs..... 6
- Changed Limited step response overshoot from 55mV to 40mV..... 6
- Changed Limited step response recovery time from 3ns to 2.5ns..... 6
- Changed maximum Quiescent current from 14.9mA to 17.2mA..... 6
- Changed typical quiescent current from 14.3mA to 15.6mA..... 6
- Changed maximum quiescent current, T_A = –40°C to +85°C from 15.3mA to 17.6mA..... 6
- Changed typical Power-supply rejection ratio from 70dB to 85dB..... 6
- Updated *Typical Characteristics: V_S = ±5V* with new die characteristics..... 8
- Updated *Typical Characteristics: V_S = 5V* with new die characteristics..... 14
- Updated *Typical Application* with data from *Electrical* and *Typical Characteristics* 23

Product Folder	Current Datasheet Number	New Datasheet Number	Link to full datasheet
OPA698	SBOS258D	**SBOS258E**	http://www.ti.com/product/OPA698

Qual details are provided in the Qual Data Section.

Reason for Change:

These changes are part of our multiyear plan to transition products from our 150-millimeter factories to newer, more efficient manufacturing processes and technologies, underscoring our commitment to product longevity and supply continuity.

Anticipated impact on Form, Fit, Function, Quality or Reliability (positive / negative):

None

Impact on Environmental Ratings:

Checked boxes indicate the status of environmental ratings following implementation of this change. If below boxes are checked, there are no changes to the associated environmental ratings.

RoHS	REACH	Green Status	IEC 62474
☒ No Change	☒ No Change	☒ No Change	☒ No Change

Changes to product identification resulting from this PCN:

Fab Site Information:

Chip Site	Chip Site Origin Code (20L)	Chip Site Country Code (21L)	Chip Site City
SH-BIP-1	SHE	USA	Sherman
FR-BIP-1	**TID**	**DEU**	**Freising**

Die Rev:

Current	New
Die Rev [2P]	**Die Rev [2P]**
B	**A**

Sample product shipping label (not actual product label):

Product Affected:

OPA698IDR

For alternate parts with similar or improved performance, please visit the product page on TI.com

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Name	Condition	Duration	Qual Device: OPA698IDR	QBS Process Reference: OPA2810IDGKR	QBS Package Reference: INA849DR	QBS Package Reference: OPA2991QDRQ1
HAST	A2	Biased HAST	130C/85%RH	96 Hours	-	3/231/0	-	3/231/0
HAST	A2	Temperature Humidity Bias	85C/85%RH	1000 Hours	-	-	3/231/0	-
UHAST	A3	Unbiased HAST	130C/85%RH	96 Hours	-	3/231/0	3/231/0	3/231/0
TC	A4	Temperature Cycle	-65C/150C	500 Cycles	-	3/231/0	3/231/0	3/231/0
HTSL	A6	High Temperature Storage Life	150C	1000 Hours	-	-	-	3/135/0
HTSL	A6	High Temperature Storage Life	170C	420 Hours	-	3/231/0	3/231/0	-
HTOL	B1	Life Test	100C[1]	300 Hours	-	-	1/77/0	-
HTOL	B1	Life Test	125C	1000 Hours	-	3/231/0	-	-
HTOL	B1	Life Test	150C	408 Hours	-	-	-	1/77/0
ELFR	B2	Early Life Failure Rate	125C	48 Hours	-	3/3000/0	-	-
PD	C4	Physical Dimensions	Cpk>1.67	-	-	-	-	3/30/0
ESD	E2	ESD CDM	-	250 Volts	1/3	3/9/0	1/3/0	-
ESD	E2	ESD CDM	-	500 Volts	-	-	-	1/3/0

Type	#	Test Name	Condition	Duration	Qual Device: OPA698IDR	QBS Process Reference: OPA2810IDGKR	QBS Package Reference: INA849DR	QBS Package Reference: OPA2991QDRQ1
ESD	E2	ESD HBM	-	1000 Volts	1/3	3/9/0	1/3/0	-
ESD	E2	ESD HBM	-	2000 Volts	-	-	-	1/3/0
LU	E4	Latch-Up	Per JESD78	-	1/3/0	3/9/0	1/6/0	1/6/0
CHAR	E5	Electrical Characterization	Per Datasheet Parameters	-	1/30/0	3/90/0	1/30/0	3/90/0

- QBS: Qual By Similarity, also known as Generic Data
- Qual Device OPA698IDR is qualified at MSL2 260C

- Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable
- The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours
- The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours
- The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles

Quality and Environmental data is available at TI's external Web site: http://www.ti.com/

TI Qualification ID: R-NPD-2402-063

[1] Tj-150C

In performing change qualifications, Texas Instruments follows integrated circuit industry standards in performing defect mechanism analysis and failure mechanism-based accelerated environmental testing to ensure wafer fab process, assembly process and product quality and reliability. As encouraged by these standards, TI uses both product-specific and generic (family) data in qualifying its changes. For devices to be categorized as a 'product qualification family' for generic data purposes, they must share similar product, wafer fab process and assembly process elements. The applicability of generic data (also known at TI as Qualification by Similarity (QBS)) is determined by the Reliability Engineering function following these industry standards. Generic data is shown in the qualification report in columns titled "QBS Process" (for wafer fab process), "QBS Package" (for assembly process) and "QBS Product" (for product family).

For questions regarding this notice, e-mails can be sent to the Change Management team or your local Field Sales Representative.

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