74AHC1G125-Q100; 74AHCT1G125-Q100

Bus buffer/line driver; 3-state

Rev. 6 — 19 September 2024 Product data sheet

1. General description

The 74AHC1G125-Q100/74AHCT1G125-Q100 is a single buffer/line driver with 3-state output. Inputs are overvoltage tolerant. This feature allows the use of these devices as translators in mixed voltage environments.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and -40 °C to +125 °C
- Wide supply voltage range from 2.0 V to 5.5 V
- Overvoltage tolerant inputs to 5.5 V
- High noise immunity
- Symmetrical output impedance
- CMOS low power dissipation
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level A
- Balanced propagation delays
- Input levels:
  - For 74AHC1G125-Q100: CMOS level
  - For 74AHCT1G125-Q100: TTL level
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AHC1G125GW-Q100 74AHCT1G125GW-Q100	-40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1
74AHC1G125GV-Q100 74AHCT1G125GV-Q100	-40 °C to +125 °C	SC-74A	plastic surface-mounted package; 5 leads	SOT753
74AHC1G125GZ-Q100	-40 °C to +125 °C	XSON5	plastic thermal enhanced extremely thin small outline package with side-wettable flanks (SWF); no leads; 5 terminals; body 1.1 × 0.85 × 0.5 mm	SOT8065-1

4. Marking

Table 2. Marking codes

Type number	Marking [1]
74AHC1G125GW-Q100	AM
74AHCT1G125GW-Q100	CM
74AHC1G125GV-Q100	A25
74AHCT1G125GV-Q100	C25
74AHC1G125GZ-Q100	AM

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

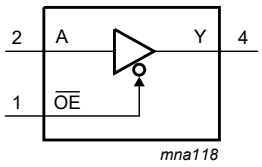


Fig. 1. Logic symbol

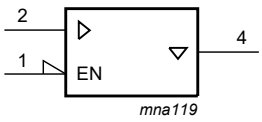


Fig. 2. IEC logic symbol

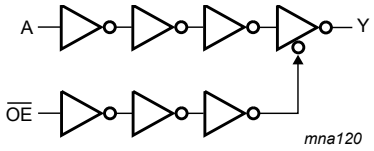
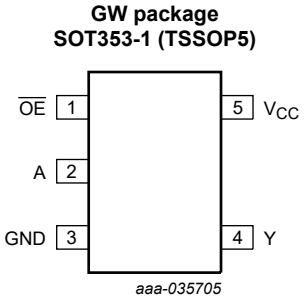
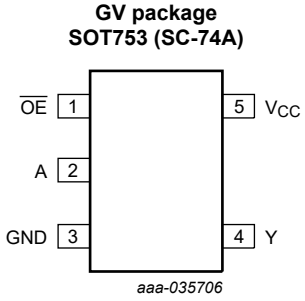


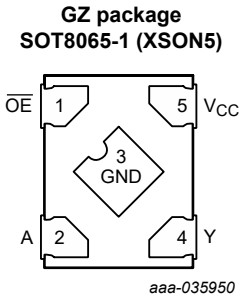
Fig. 3. Logic diagram

6. Pinning information

6.1. Pinning







Transparent top view

6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
$\overline{OE}$	1	output enable input
A	2	data input
GND	3	ground (0 V)
Y	4	data output
V_{CC}	5	supply voltage

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Inputs		Output
$\overline{OE}$	A	Y
L	L	L
L	H	H
H	X	Z

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+7.0	V
V_I	input voltage			-0.5	+7.0	V
I_{IK}	input clamping current	V_I < -0.5 V	[1]	-20	-	mA
I_{OK}	output clamping current	V_O < -0.5 V or V_O > V_{CC} + 0.5 V	[1]	-	±20	mA
I_O	output current	-0.5 V < V_O < V_{CC} + 0.5 V		-	±25	mA
I_{CC}	supply current			-	75	mA
I_{GND}	ground current			-75	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C	[2]	-	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For SOT353-1 (TSSOP5) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.
For SOT753 (SC-74A) package: P_{tot} derates linearly with 3.8 mW/K above 85 °C.
For SOT8065-1 (XSON5) package: P_{tot} derates linearly with 3.2 mW/K above 72 °C.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74AHC1G125-Q100			74AHCT1G125-Q100			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V_I	input voltage		0	-	5.5	0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 3.3 V ± 0.3 V	-	-	100	-	-	-	ns/V
		V_{CC} = 5.0 V ± 0.5 V	-	-	20	-	-	20	ns/V

10. Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74AHC1G125-Q100										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
		V_{CC} = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V_{CC} = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V_{CC} = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V_{CC} = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = -50 µA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = -50 µA; V_{CC} = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I_O = -50 µA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -4.0 mA; V_{CC} = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
		I_O = -8.0 mA; V_{CC} = 4.5 V	3.94	-	-	3.8	-	3.70	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = 50 µA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 50 µA; V_{CC} = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 50 µA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I_O = 8.0 mA; V_{CC} = 4.5 V	-	-	0.36	-	0.44	-	0.55	V
I_{OZ}	OFF-state output current	V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	-	0.25	-	2.5	-	10	µA
I_I	input leakage current	V_I = 5.5 V or GND; V_{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	1.0	-	10	-	40	µA
C_I	input capacitance		-	1.5	10	-	10	-	10	pF
74AHCT1G125-Q100										
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = -50 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -8.0 mA	3.94	-	-	3.8	-	3.70	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = 50 µA	-	0	0.1	-	0.1	-	0.1	V
		I_O = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
I_{OZ}	OFF-state output current	V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	-	0.25	-	2.5	-	10	µA
I_I	input leakage current	V_I = 5.5 V or GND; V_{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	1.0	-	10	-	40	µA
ΔI_{CC}	additional supply current	per input pin; V_I = 3.4 V; other inputs at V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
C_I	input capacitance		-	1.5	10	-	10	-	10	pF

11. Dynamic characteristics

Table 8. Dynamic characteristics

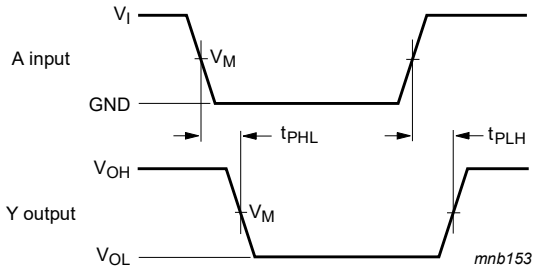
GND = 0 V; for test circuit see Fig. 6.

Symbol	Parameter	Conditions		25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
74AHC1G125-Q100											
t_{pd}	propagation delay	A to Y; see Fig. 4	[1]								
		V_{CC} = 3.0 V to 3.6 V; C_L = 15 pF	[2]	-	4.7	8.0	1.0	9.5	1.0	11.5	ns
		V_{CC} = 3.0 V to 3.6 V; C_L = 50 pF	[2]	-	6.6	11.5	1.0	13.0	1.0	14.5	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 15 pF	[3]	-	3.4	5.5	1.0	6.5	1.0	7.0	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 50 pF	[3]	-	4.8	7.5	1.0	8.5	1.0	9.5	ns
t_{en}	enable time	$\overline{OE}$ to Y; see Fig. 5	[1]								
		V_{CC} = 3.0 V to 3.6 V; C_L = 15 pF	[2]	-	5.0	8.0	1.0	9.5	1.0	11.5	ns
		V_{CC} = 3.0 V to 3.6 V; C_L = 50 pF	[2]	-	6.9	11.5	1.0	13.0	1.0	14.5	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 15 pF	[3]	-	3.6	5.1	1.0	6.0	1.0	6.5	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 50 pF	[3]	-	4.9	7.5	1.0	8.5	1.0	9.5	ns
t_{dis}	disable time	$\overline{OE}$ to Y; see Fig. 5	[1]								
		V_{CC} = 3.0 V to 3.6 V; C_L = 15 pF	[2]	-	6.0	9.7	1.0	11.5	1.0	12.5	ns
		V_{CC} = 3.0 V to 3.6 V; C_L = 50 pF	[2]	-	8.3	13.2	1.0	15.0	1.0	16.5	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 15 pF	[3]	-	4.1	6.8	1.0	8.0	1.0	8.5	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 50 pF	[3]	-	5.7	8.8	1.0	10.0	1.0	11.0	ns
C_{PD}	power dissipation capacitance	per buffer; C_L = 50 pF; f = 1 MHz; V_I = GND to V_{CC}	[4]	-	9	-	-	-	-	-	pF

Symbol	Parameter	Conditions		25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
74AHCT1G125-Q100											
t_{pd}	propagation delay	A to Y; see Fig. 4	[1]								
		V_{CC} = 4.5 V to 5.5 V; C_L = 15 pF	[3]	-	3.4	5.5	1.0	6.5	1.0	7.0	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 50 pF	[3]	-	4.8	7.5	1.0	8.5	1.0	9.5	ns
t_{en}	enable time	$\overline{OE}$ to Y; see Fig. 5	[1]								
		V_{CC} = 4.5 V to 5.5 V; C_L = 15 pF	[3]	-	3.9	5.1	1.0	6.0	1.0	6.5	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 50 pF	[3]	-	5.1	7.5	1.0	8.5	1.0	9.5	ns
t_{dis}	disable time	$\overline{OE}$ to Y; see Fig. 5	[1]								
		V_{CC} = 4.5 V to 5.5 V; C_L = 15 pF	[3]	-	4.5	6.8	1.0	8.0	1.0	8.5	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 50 pF	[3]	-	6.1	8.8	1.0	10.0	1.0	11.0	ns
C_{PD}	power dissipation capacitance	per buffer; C_L = 50 pF; f = 1 MHz; V_I = GND to V_{CC}	[4]	-	11	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.
[2] Typical values are measured at V_{CC} = 3.3 V.
[3] Typical values are measured at V_{CC} = 5.0 V.
[4] C_{PD} is used to determine the dynamic power dissipation P_D (µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V.

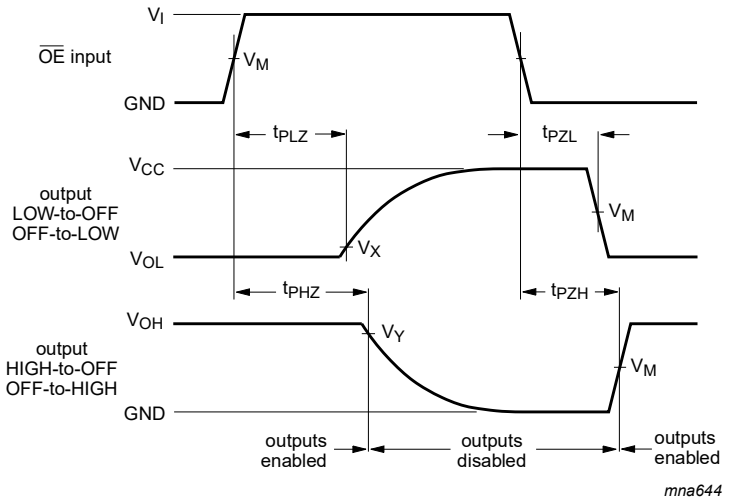
11.1. Waveforms and test circuit



Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 4. Input (A) to output (Y) propagation delays



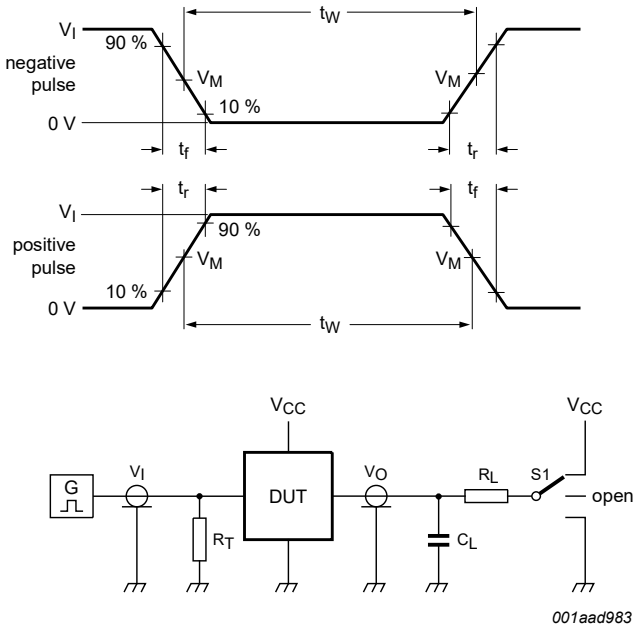
Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 5. Enable and disable times

Table 9. Measurement point

Type	Inputs		Output		
	V_I	V_M	V_M	V_X	V_Y
74AHC1G125-Q100	GND to V_{CC}	$0.5V_{CC}$	$0.5V_{CC}$	V_{OL} + 0.3 V	V_{OH} - 0.3 V
74AHCT1G125-Q100	GND to 3.0 V	1.5 V	$0.5V_{CC}$	V_{OL} + 0.3 V	V_{OH} - 0.3 V



Test data is given in Table 10.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

C_L = Load capacitance including jig and probe capacitance;

R_L = Load resistance;

S1 = Test selection switch

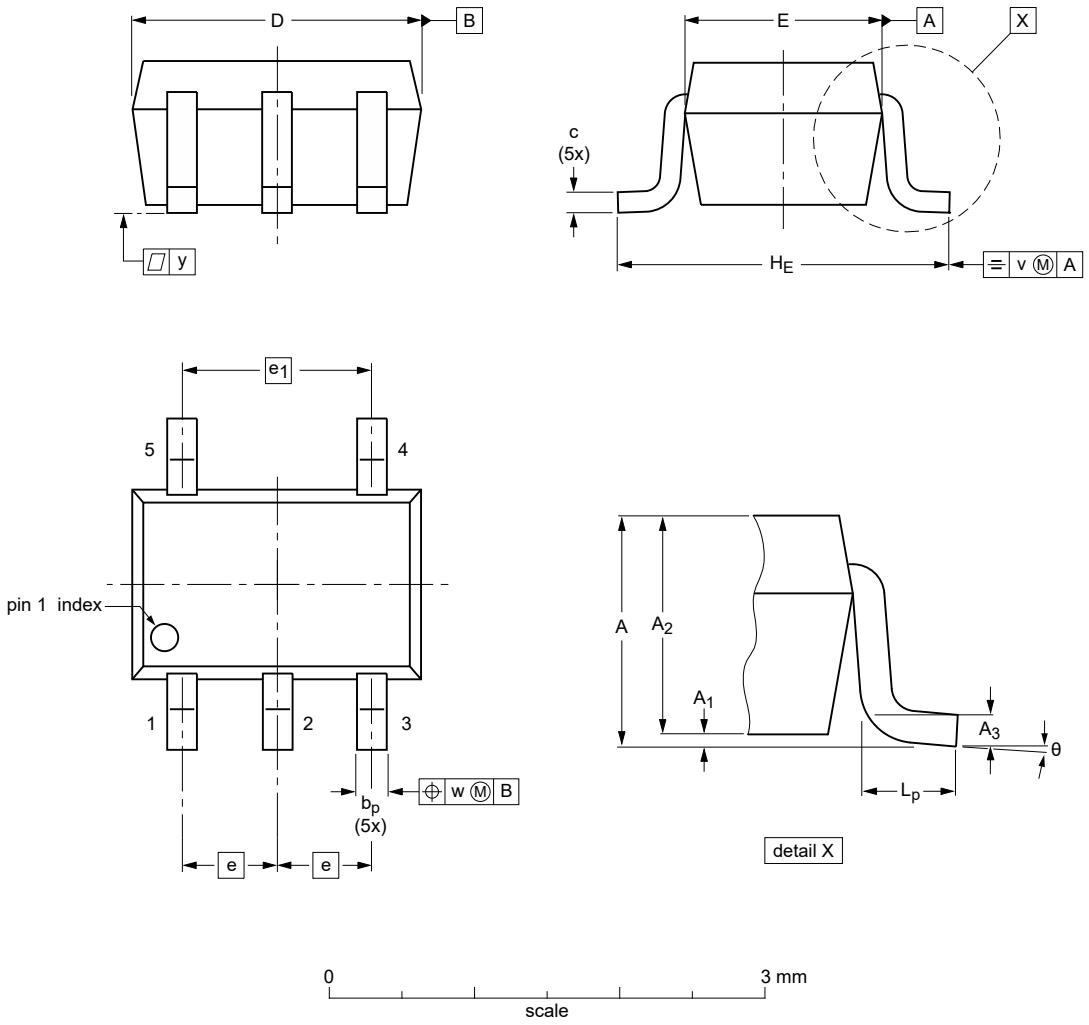
Fig. 6. Test circuit for measuring switching times

Table 10. Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74AHC1G125-Q100	V_{CC}	≤ 3 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}
74AHCT1G125-Q100	3 V	≤ 3 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}

12. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm **SOT353-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	e_1	H_E	L_p	v	w	y	θ
mm	max	1.1	0.1	1.0	0.15	0.30	0.25	2.2	1.35	0.65	1.3	2.4	0.46	0.3	0.1	0.1	8°
	min	0.8	0	0.8		0.15	0.08	1.8	1.15			1.8	0.26				0°

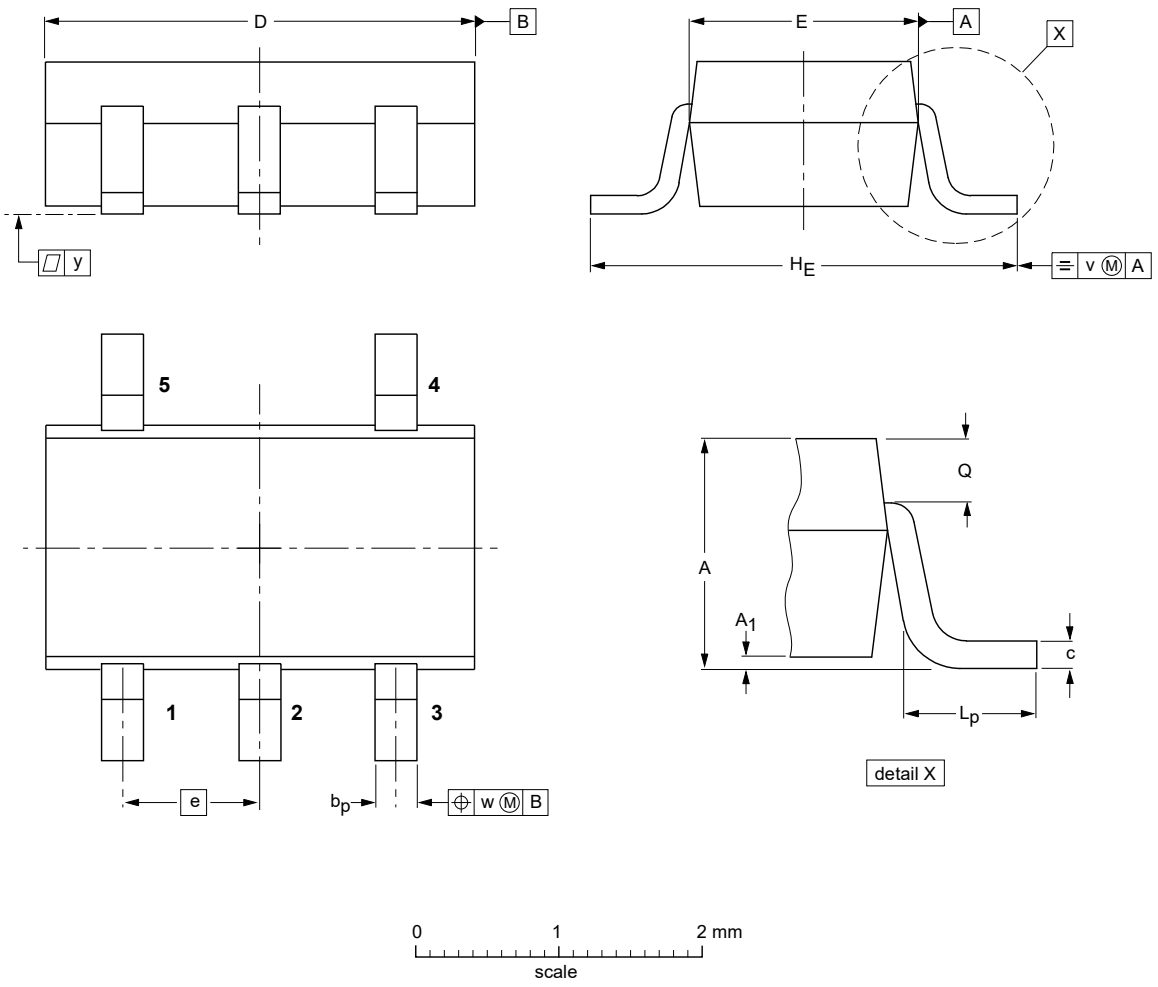
Note
1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

sot353-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT353-1		MO-203	SC-88A			~~21-12-15~~ 21-12-16

Fig. 7. Package outline SOT353-1 (TSSOP5)

Plastic surface-mounted package; 5 leads **SOT753**



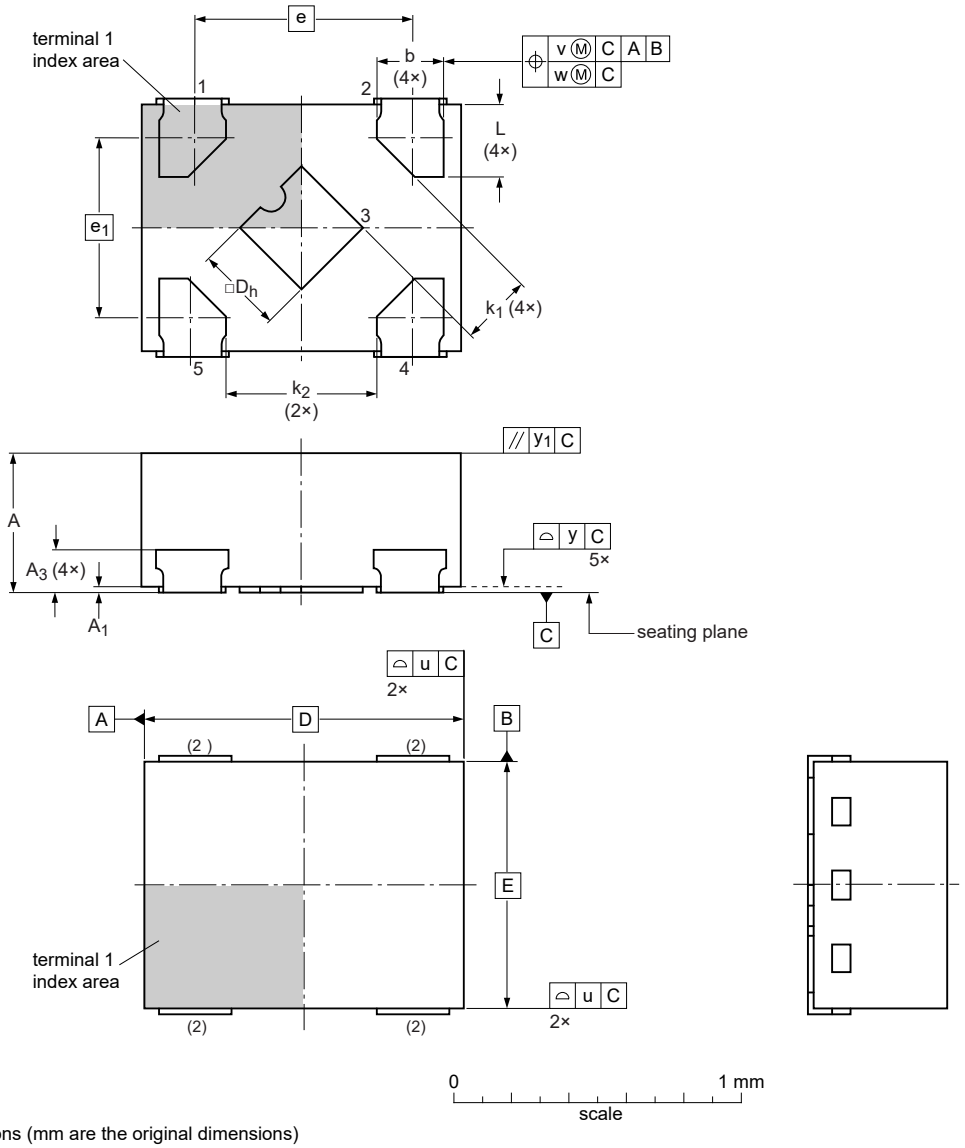
DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	c	D	E	e	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.100 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT753			SC-74A			~~02-04-16~~ 06-03-16

Fig. 8. Package outline SOT753 (SC-74A)

XSON5: Plastic thermal enhanced extremely thin small outline package with side-wettable flanks (SWF); no leads; 5 terminals; body 1.1 × 0.85 × 0.5 mm **SOT8065-1**



Dimensions (mm are the original dimensions)

Unit		A(1)	A1	A3	b	D(1)	Dh	E(1)	e	e1	k1	k2	L	u	v	w	y	y1
mm	max	0.50	0.040	0.135 (typ)	0.28	1.10	0.35	0.85	0.75	0.6	0.2	0.45	0.30	0.05	0.1	0.05	0.05	0.05
	nom	0.47	0.020		0.23		0.30						0.25					
	min	0.44	0.005		0.20		0.27						0.22					

Note:
1. Plastic or metal protrusions per side are not included.
2. Side wettable flanks (SWF), protrusion max. 0.02 mm.

sot8065-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8065-1		MO-340				~~24-07-09~~ 24-08-27

Fig. 9. Package outline SOT8065-1 (XSON5)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CMOS	Complementary Metal Oxide Semiconductor
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT1G125_Q100 v.6	20240919	Product data sheet	-	74AHC_AHCT1G125_Q100 v.5
Modifications:	• Type number 74AHC1G125GZ-Q100 (SOT8065-1/XSON5) added.			
74AHC_AHCT1G125_Q100 v.5	20230915	Product data sheet	-	74AHC_AHCT1G125_Q100 v.4
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard.			
74AHC_AHCT1G125_Q100 v.4	20220111	Product data sheet	-	74AHC_AHCT1G125_Q100 v.3
Modifications:	• Fig. 7: Package outline drawing SOT353-1(TSSOP5) has changed			
74AHC_AHCT1G125_Q100 v.3	20201013	Product data sheet	-	74AHC_AHCT1G125_Q100 v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Section 1 and Section 2 updated. • Table 5: Derating values for P_{tot} total power dissipation updated.			
74AHC_AHCT1G125_Q100 v.2	20121019	Product data sheet	-	74AHC_AHCT1G125_Q100 v.1
Modifications:	• Section 2: ESD protection CDM JESD22-C101E changed to MIL-STD-833.			
74AHC_AHCT1G125_Q100 v.1	20120807	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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