AzureWave Technologies, Inc.

FRDM-IW416-AW-AM510

Wi-Fi Expansion Board for NXP FRDM

Datasheet

Rev. A

DF

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Features

WLAN

- Support 802.11 a/b/g/n
- Dual bands: 2.4 GHz and 5 GHz
- Single stream 802.11n with 20/40 MHz channels for 5G and 20 MHz only for 2.4G
- Up to MCS7 data rates (150 Mbps)
- Support 802.11mc for location
- Dynamic Rapid Channel Switching (DRCS) for simultaneous and power efficient operation in 2.4 GHz and 5 GHz bands
- Interface to coexist with 802.15.4, LTE, or other radios.
- Security: WPA3, WPA2, WPA2 and WPA mix mixed mode, WEP

Bluetooth

- Full Bluetooth 5.2 features
- Long range - 4x coverage
- 2 Mbps data rate - 2x faster
- Improved advertisement capacity- enables more IoT services
- Audio interface: I2S and PCM
- Security: AES

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Revision History

Document NO: R2-2510-DST-05

Version	Revision Date	DCN NO.	Description	Initials	Approved
A	2024/09/13	DCN032367	• Initial Version	JM.Pang	N.C Chen

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AzureWave Technologies, Inc.

Table of Contents

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1. Introduction

1.1 Product Overview

AzureWave Technologies, Inc. introduces the IEEE 802.11a/b/g/n WLAN, BT, combo module – **FRDM-IW416-AW-AM510.** With four advanced radio technologies integrated into a module, FRDM-IW416-AW-AM510 provides the best and most convenient SMT process. The module is targeted to NXP FRDM Development Platform.

By using AW-AM510, the customers can easily integrate the Wi-Fi, BT, by a combo module with the benefits of **high design flexibility, high success rate on SMT process, short development cycle, and quick time-to-market.**

Compliance with the IEEE 802.11a/b/g/n standard, the AW-AM510 uses **DSSS**, **OFDM**, **DBPSK**, **DQPSK**, **CCK** and **QAM** baseband modulation technologies. A high level of integration and full implementation of the power management functions specified in the IEEE 802.11 standard minimize the system power requirements by using AW-AM510.

The FRDM-IW416-AW-AM510 supports standard interface Arduino/FRDM headers **SDIO3.0/UART for WLAN**, **UART for BT**. AW-AM510 is suitable for multiple mobile processors for different applications. With the combo functions and the good performance, the AW-AM510 is the best solution for the consumer electronics and the tablet PC.

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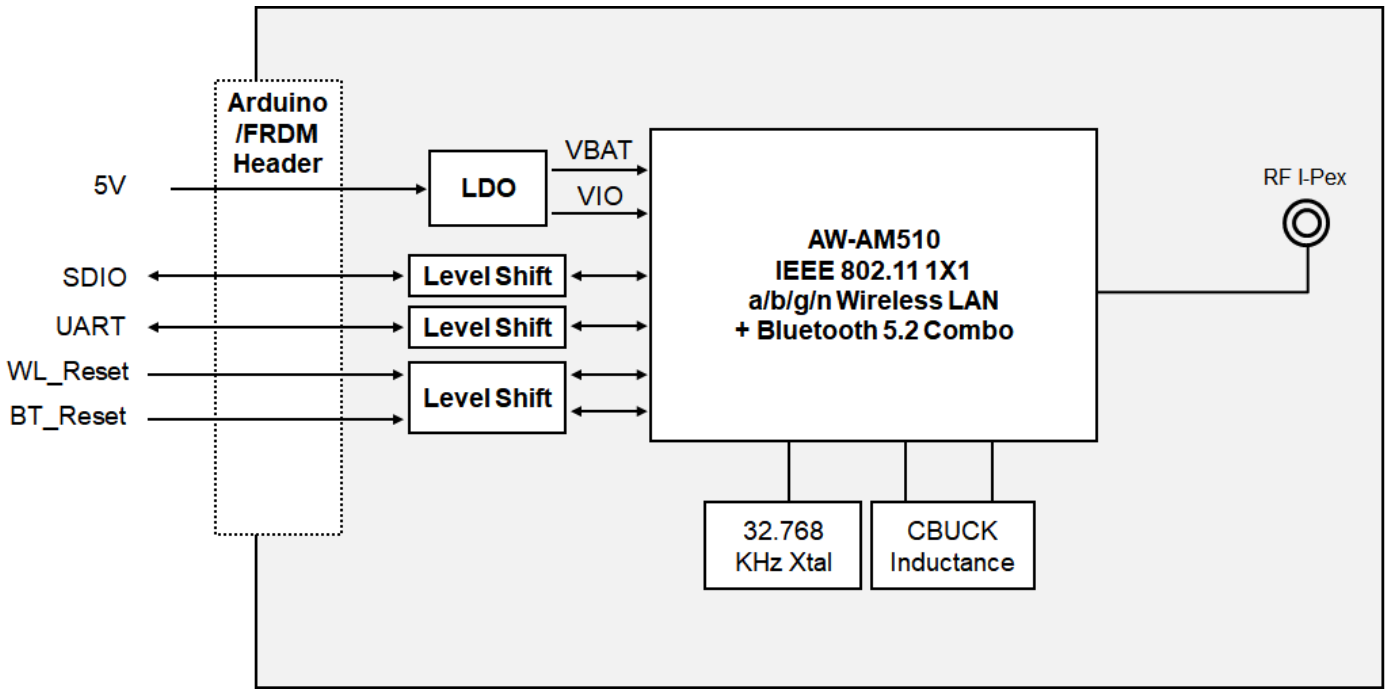
1.2 Block Diagram

A simplified block diagram of the FRDM-IW416-AW-AM510 is depicted in the figure below.



FRDM-IW416-AW-AM510 Block Diagram

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1.3 Specifications Table

1.3.1 General

Features	Description
Product Description	Wi-Fi Expansion Board for NXP FRDM
Major Chipset	NXP IW416 WLCSP (76p)
Host Interface	Wi-Fi + BT ● SDIO + UART
Dimension	63.71 mm x 53.6 mm x 18.78 mm
Form Factor	Arduino/FRDM
Antenna	ANT(Main)：Wi-Fi / Bluetooth → TX/RX
Weight	19.5 g

1.3.2 WLAN

Features	Description
WLAN Standard	IEEE 802.11 a/b/g/n Wi-Fi with Bluetooth 5.2 Combo Module
WLAN VID/PID	NA
WLAN SVID/SPID	NA
Frequency Rage	2.4 GHz ISM Bands 2.412-2.472 GHz 5.15-5.25 GHz (FCC UNII-low band) for US/Canada and Europe 5.25-5.35 GHz (FCC UNII-middle band) for US/Canada and Europe 5.47-5.725 GHz for Europe 5.725-5.825 GHz (FCC UNII-high band) for US/Canada
Modulation	DSSS, OFDM, DBPSK, DQPSK, CCK, 16-QAM, 64-QAM

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<table>
<tr><td>Number of Channels</td><td>2.4GHz:
■ USA, NORTH AMERICA, Canada and Taiwan - 1 ~ 11
■ China, Australia, Most European Countries - 1 ~ 13
■ Japan, 1 ~ 13

5GHz:
■ USA, Canada, Most European Countries - 36,40,44,48,52,56,60,64,100,104,108,112,116,120,124,128,132,136,140,149,153,157,161,165
■ Japan - 36,40,44,48,52,56,60,64,100,104,108,112,116,120,124,128,132,136,140
■ China - 36,40,44,48,52,56,60,64, 149,153,157,161,165</td></tr>
<tr><td>Output Power
(Board Level Limit)*</td><td>2.4G
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>11b (11Mbps)
@EVM<35%</td><td>15.5</td><td>17</td><td>18.5</td><td>dBm</td></tr>
<tr><td>11g (54Mbps)
@EVM≦-27 dB</td><td>14.5</td><td>16</td><td>17.5</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)
@EVM≦-28 dB</td><td>12.5</td><td>14</td><td>15.5</td><td>dBm</td></tr>
</table>
5G
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>11a (54Mbps)
@EVM≦-25 dB</td><td>14</td><td>16</td><td>18</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)
@EVM≦-27 dB</td><td>13</td><td>15</td><td>17</td><td>dBm</td></tr>
<tr><td>11n (HT40 MCS7)
@EVM≦-27 dB</td><td>12</td><td>14</td><td>16</td><td>dBm</td></tr>
</table></td></tr>
</table>

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<table>
<tr><td>Receiver Sensitivity</td><td>
2.4G
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>11b (11Mbps)</td><td>-</td><td>-86</td><td>-83</td><td>dBm</td></tr>
<tr><td>11g (54Mbps)</td><td>-</td><td>-73</td><td>-70</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)</td><td>-</td><td>-69</td><td>-66</td><td>dBm</td></tr>
</table>
5G
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>11a (54Mbps)</td><td>-</td><td>-71</td><td>-68</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)</td><td>-</td><td>-68</td><td>-65</td><td>dBm</td></tr>
<tr><td>11n (HT40 MCS7)</td><td>-</td><td>-66</td><td>-63</td><td>dBm</td></tr>
</table>
</td></tr>
<tr><td>Data Rate</td><td>WLAN:
802.11b : 1, 2, 5.5, 11Mbps
802.11a/g : 6, 9, 12, 18, 24, 36, 48, 54Mbps
802.11n : Maximum data rates up to 72 Mbps (20 MHz channel), 150 Mbps (40 MHz channel)</td></tr>
<tr><td>Security</td><td>■ Wi-Fi: WPA3, WPA2, WPA2 and WPA mixed mode, WEP
■ BT: AES</td></tr>
</table>

* If you have any certification questions about output power please contact FAE directly.

1.3.3 Bluetooth

<table>
<tr><th>Features</th><th>Description</th></tr>
<tr><td>Bluetooth Standard</td><td>Full Bluetooth 5.2 features</td></tr>
<tr><td>Frequency Rage</td><td>2402MHz~2483MHz</td></tr>
<tr><td>Modulation</td><td>Header GFSK
Payload 2M: π/4-DQPSK
Payload 3M: 8DPSK</td></tr>
<tr><td>Output Power</td><td>
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>BDR</td><td>0</td><td>2</td><td>4</td><td>dBm</td></tr>
<tr><td>EDR</td><td>0</td><td>2</td><td>4</td><td>dBm</td></tr>
<tr><td>Low Energy</td><td>0</td><td>2</td><td>4</td><td>dBm</td></tr>
</table>
</td></tr>
</table>

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<table>
<tr><td>Receiver Sensitivity</td><td>BT Sensitivity (BER<0.1%)
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>BDR(DH1)</td><td>-</td><td>-83</td><td>-80</td><td>dBm</td></tr>
<tr><td>EDR(2DH5)</td><td>-</td><td>-88</td><td>-85</td><td>dBm</td></tr>
<tr><td>EDR(3DH5)</td><td>-</td><td>-83</td><td>-80</td><td>dBm</td></tr>
<tr><td>Low Energy</td><td>-</td><td>-96</td><td>-93</td><td>dBm</td></tr>
</table></td></tr>
</table>

1.3.4 Operating Conditions

Features	Description
Operating Conditions	
Voltage	3.3V +-5%
Operating Temperature	0 ℃ to +70 ℃
Operating Humidity	Less than 85% R.H.
Storage Temperature	-40 ℃ to +85 ℃
Storage Humidity	Less than 60% R.H.
ESD Protection	
Human Body Model	±2kV
Changed Device Model	±500V

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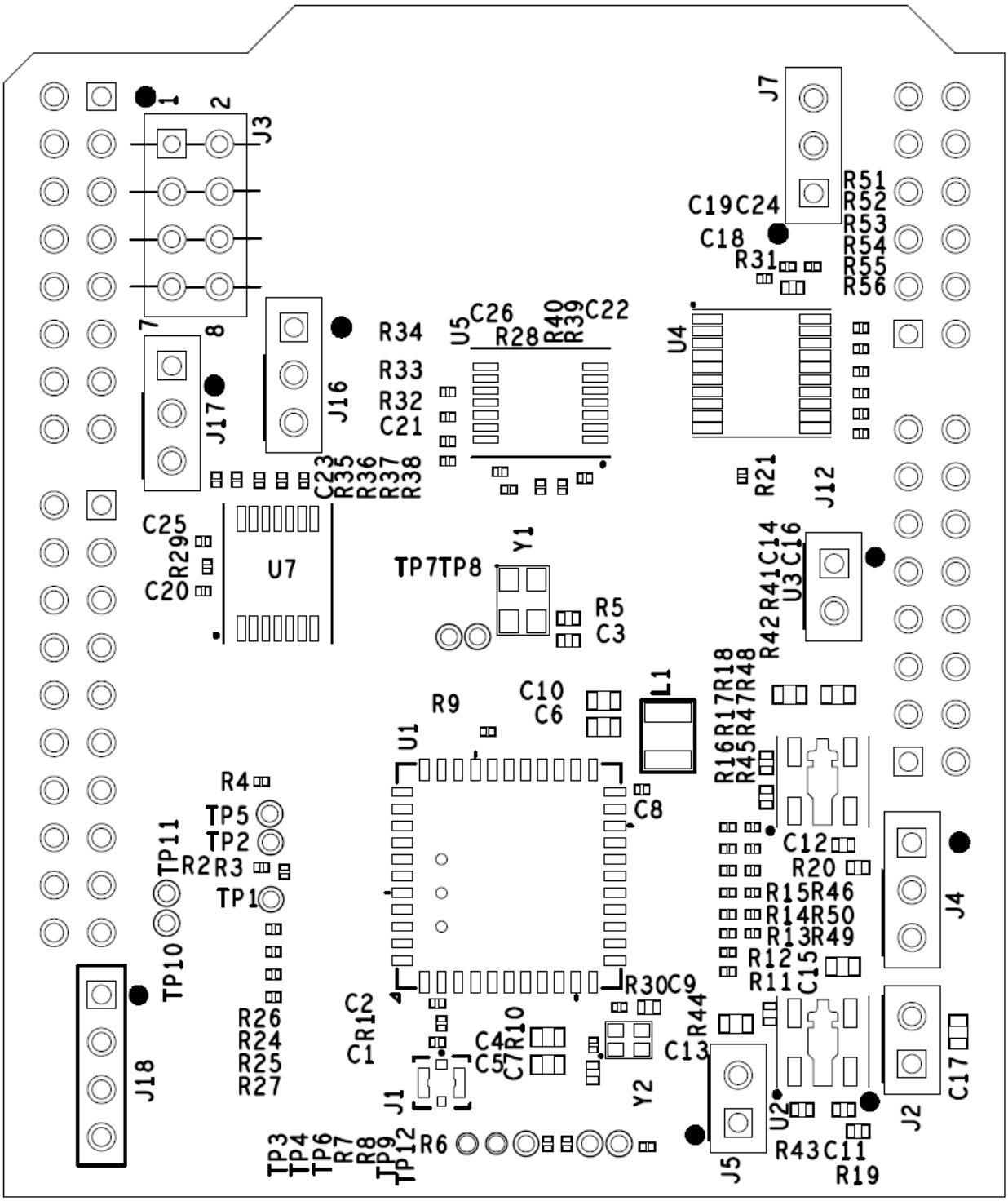
2. Pin Definition

2.1 Pin Map



FRDM-IW416-AW-AM510 Pin Map (Top view)

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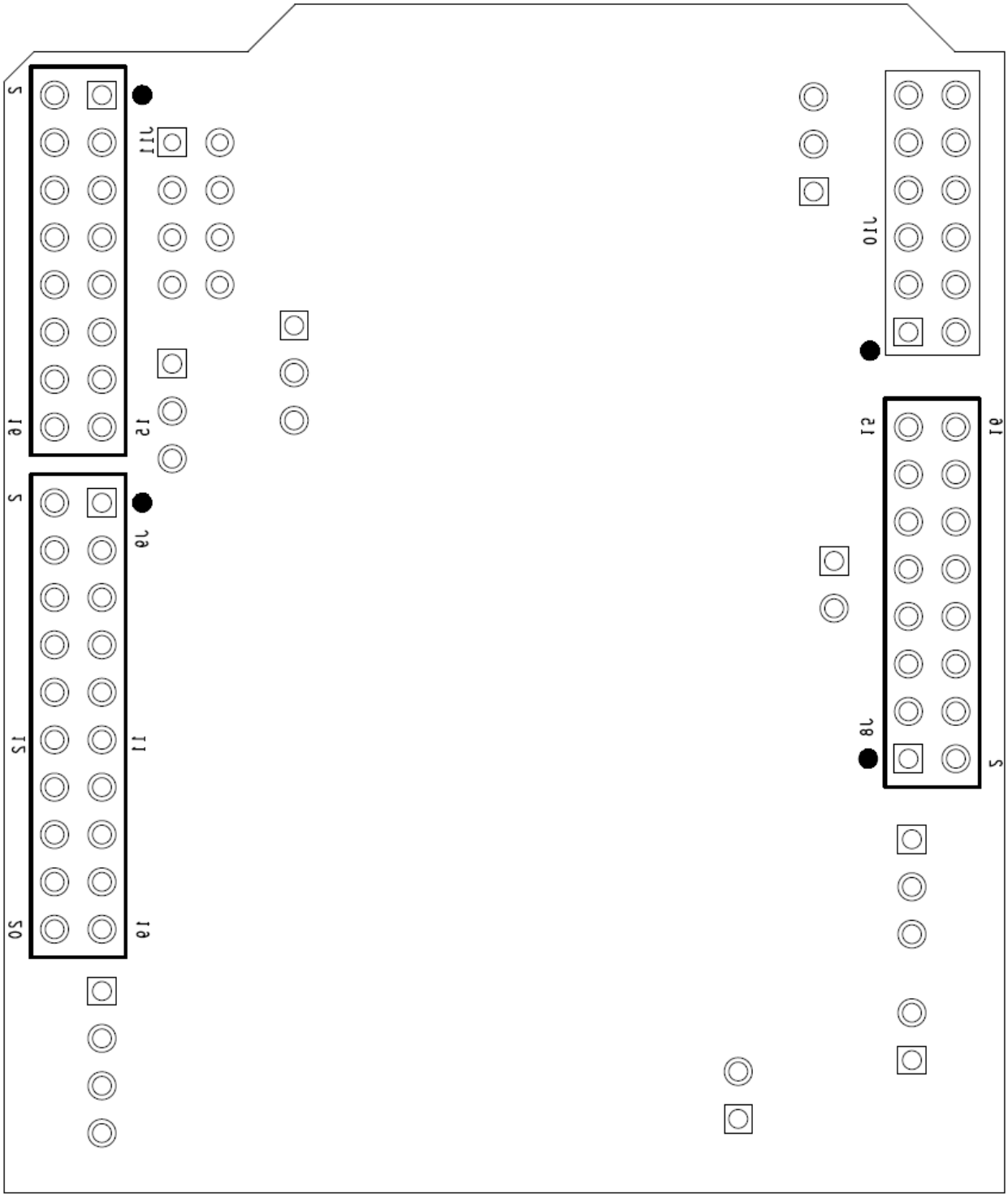

FRDM-IW416-AW-AM510 Pin Map (Bot view)

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2.2 Pin Table

Header	Pin No	Definition	Basic Description	Voltage	Type
J8	1	WL_WAKE_HOST	GPIO Mode: GPIO[1]. WL Host Wake	VDDIO	I/O
J8	5	SDIO_DATA0	SDIO Data line Bit[0]	VDDIO	I/O
J8	7	SDIO_DATA1	SDIO Data line Bit[1]	VDDIO	I/O
J8	9	SDIO_CMD	SDIO Command	VDDIO	I/O
J8	10	VBAT	5V power voltage source input	5V	P
J8	11	SDIO_CLK	SDIO Clock input	VDDIO	I
J8	12	GND	Ground	---	---
J8	13	SDIO_DATA2	SDIO Data line Bit[2]	VDDIO	I/O
J8	14	GND	Ground	---	---
J8	15	SDIO_DATA3	SDIO Data line Bit[3]	VDDIO	I/O
J11	1	UART_RTS_N	UART_RTSn (active low)	VDDIO	O
J11	2	UART_TXD	UART_SOUT	VDDIO	O
J11	3	UART_CTS_N	UART_CTSn(active low)	VDDIO	I
J11	4	UART_RXD	UART_SIN	VDDIO	I
J11	8	BT_WAKE_HOST	GPIO Mode: GPIO[0]. BT Host Wake	VDDIO	O
J11	12	PDn	Full Power-down pin connects to internal PMIC (input) (active low) 0 = full power-down mode 1 = normal mode	VDDIO	I
J18	1	BT_PCM_SYNC	PCM sync signal	VDDIO	I/O
J18	2	BT_PCM_IN	PCM data input	VDDIO	I/O
J18	3	BT_PCM_CLK	PCM Clock	VDDIO	I/O
J18	4	BT_PCM_OUT	PCM Data output	VDDIO	I/O

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3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	DC supply for the 3.3V input	-0.3	5	6	V

3.2 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	DC supply for the 3.3V input	4.3	5	5.5	V

3.3 Digital IO Pin DC Characteristics

3.3.1 1.8V Operation (VDDIO)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{IH}	Input high voltage	0.7*VIO	-	VIO+0.4	V
V_{IL}	Input low voltage	-0.4	-	0.3*VIO	
V_{OH}	Output high voltage	VIO-0.4	-	-	
V_{OL}	Output low voltage	-	-	0.4	
V_{HYS}	Input Hysteresis	100			mV

3.3.2 3.3V Operation (VDDIO)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{IH}	Input high voltage	0.7*VIO	-	VIO+0.4	V
V_{IL}	Input low voltage	-0.4	-	0.3*VIO	
V_{OH}	Output High Voltage	VIO-0.4	-	-	
V_{OL}	Output Low Voltage	-	-	0.4	
V_{HYS}	Input Hysteresis	100			mV

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3.4 Host Interface

3.4.1 SDIO Interface

The FRDM-IW416-AW-AM510 supports a SDIO device interface that conforms to the industry SDIO Full-Speed card specification and allows a host controller using the SDIO bus protocol to access the Wireless SoC device.

The FRDM-IW416-AW-AM510 acts as the device on the SDIO bus. The host unit can access registers of the SDIO interface directly and can access shared memory in the device through the use of BARs and a DMA engine.

- Support SDIO 3.0 Standard.
- On-chip memory used for CIS.
- Supports 4-bit SDIO and 1-bit SDIO transfer modes.
- Special interrupt register for information exchange.
- Allows card to interrupt host.

SDIO Interface Signals

FRDM-IW416-AW-AM510 SDIO Pin Name	Type	Description
SDIO_CLK	I	SDIO 4-bit mode: Clock SDIO 1-bit mode: Clock
SDIO_CMD	I/O	SDIO 4-bit mode: Command line SDIO 1-bit mode: Command line
SDIO_DATA3	I/O	SDIO 4-bit mode: Data line Bit[3] SDIO 1-bit mode: Not used
SDIO_DATA2	I/O	SDIO 4-bit mode: Data line Bit[2] or Read Wait (optional) SDIO 1-bit mode: Read Wait (optional)
SDIO_DATA1	I/O	SDIO 4-bit mode: Data line Bit[1] SDIO 1-bit mode: Interrupt
SDIO_DATA0	I/O	SDIO 4-bit mode: Data line Bit[0] SDIO 1-bit mode: Data line

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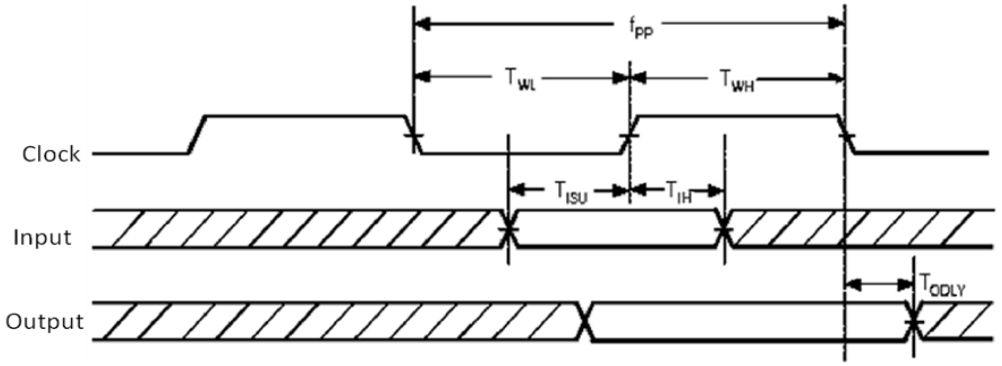
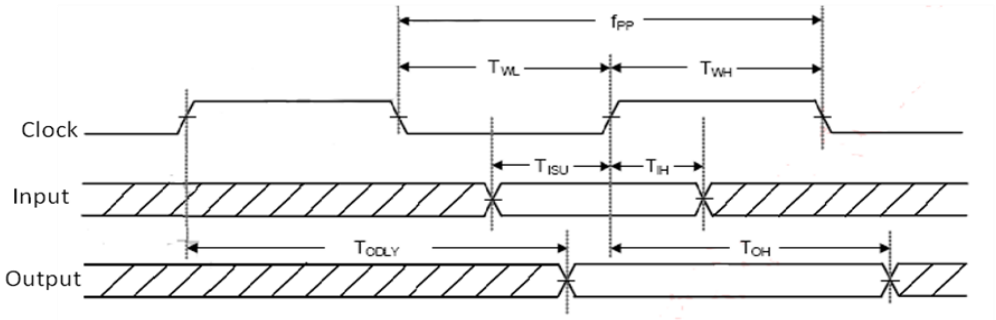
3.4.2 SDIO Protocol Timing

3.4.2.1 Default Speed, High-Speed Modes (3.3V)



SDIO protocol timing Diagram - Default mode. (3.3V)



SDIO protocol timing Diagram - High Speed mode. (3.3V)

Symbol	Parameter	Condition	Min	Typ	Max	Units
fpp	CLK Frequency	Normal	0	--	25	MHz
		High Speed	0	--	50	MHz
T_{WH}	CLK High Time	Normal	10	--	--	ns
		High Speed	7	--	--	ns
T_{WL}	CLK Low Time	Normal	10	--	--	ns
		High Speed	7	--	--	ns
T_{ISU}	Input Setup Time	Normal	5	--	--	ns
		High Speed	6	--	--	ns
T_{IH}	Input Hold Time	Normal	5	--	--	ns
		High Speed	2	--	--	ns
T_{ODLY}	Output Delay Time	Normal	--	--	14	ns
	CL ≦ 40pF (1 card)	High Speed	--	--	14	ns
T_{OH}	Output Hold Time	High Speed	2.5	--	--	ns

SDIO Timing Data – Default Speed / High-Speed modes. (3.3V)

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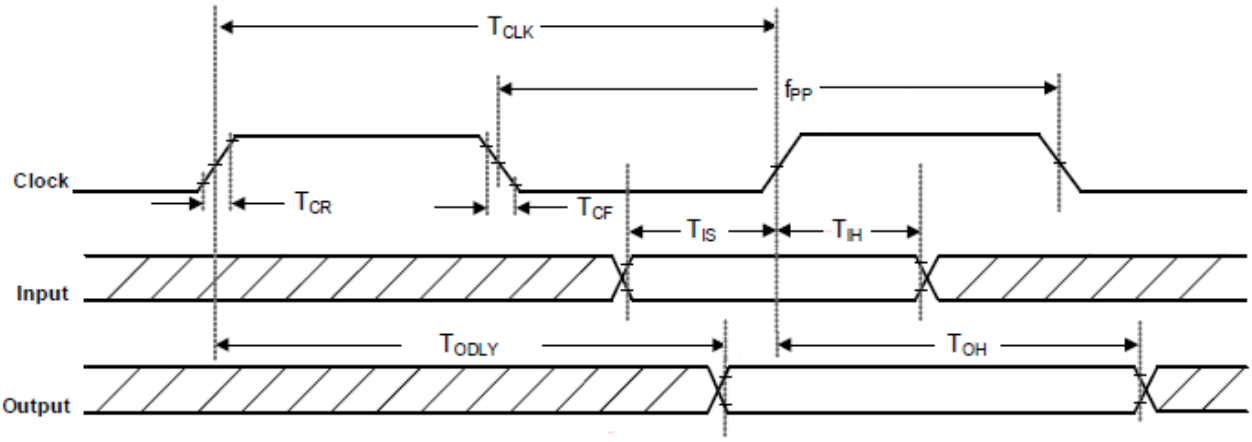
3.4.2.2 SDR12, SDR25, SDR50 Modes (up to 100MHz) (1.8V)



SDIO Protocol Timing Diagram - SDR12, SDR25, SDR50 Modes (up to 100 MHz)(1.8V)

Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{pp}	CLK Frequency	SDR12/25/50	25	-	100	MHz
T_{CLK}	Clock Time	SDR12/25/50	10	-	40	ns
T_{IS}	Input Setup Time	SDR12/25/50	3	-	-	ns
T_{IH}	Input Hold Time	SDR12/25/50	0.8	-	-	ns
T_{CR} ,T_{CF}	Rise time, fail time TCR ,TCF <2ns(max) at 100MHz CCARD =10pF	SDR12/25/50	-	-	0.2*T_{CLK}	ns
T_{ODLY}	Output Delay Time CL ≦ 30pF	SDR12/25/50	-	-	7.5	ns
T_{OH}	Output Hold Time CL =15pF	SDR12/25/50	1.5	-	-	ns

SDIO Timing Data - SDR12/25/50 modes. (1.8V)

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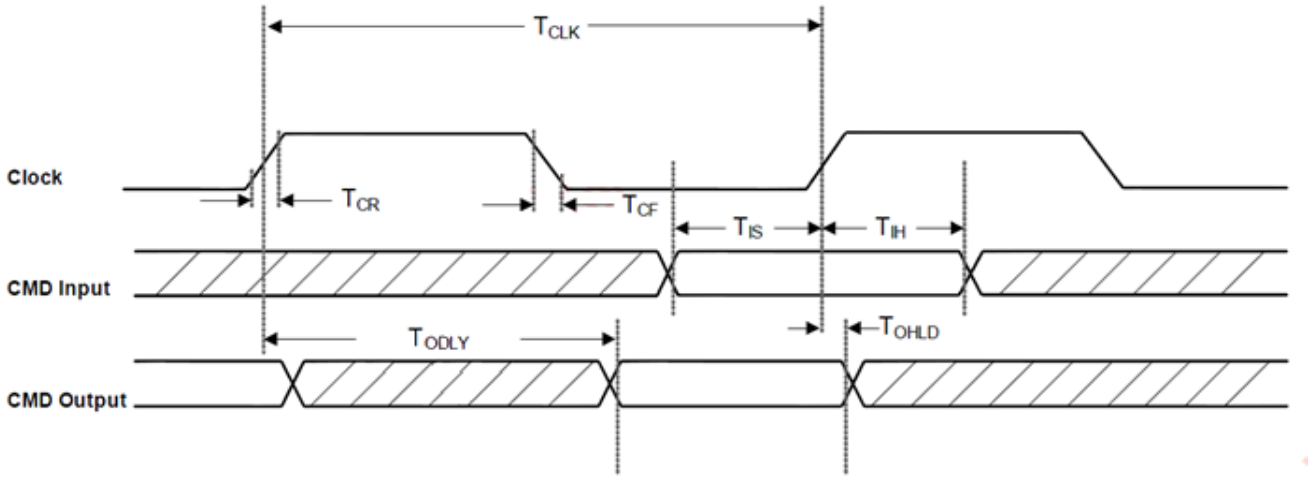
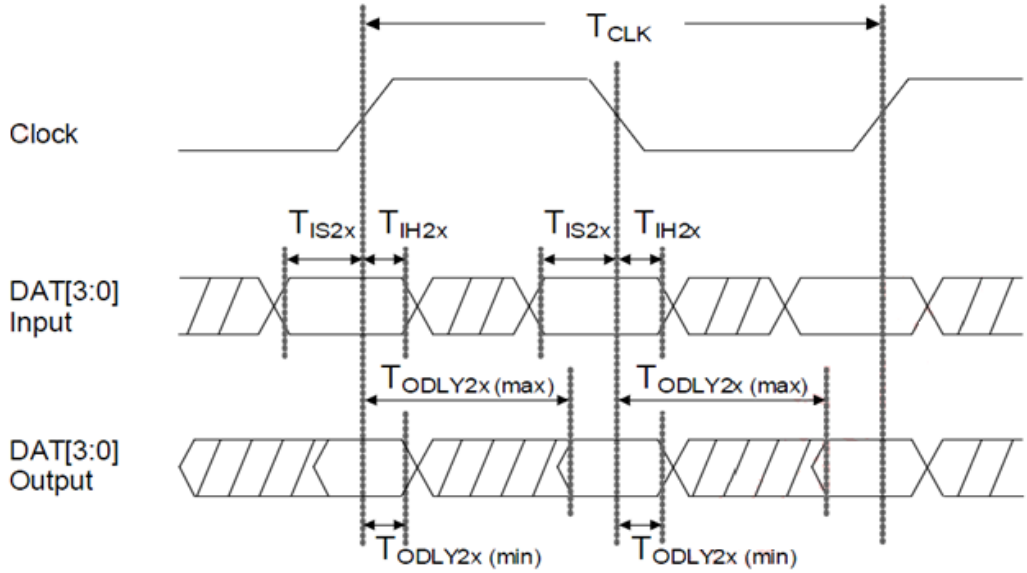
3.4.2.3 DDR50 Mode (50MHz) (1.8V)



SDIO CMD Timing Diagram - DDR50 Mode (50 MHz)



SDIO DAT[3:0] Timing Diagram - DDR50 Mode[1] (50 MHz)

[1] In DDR50 mode, DAT[3:0] lines are sampled on both edges of the clock (not applicable for CMD line).

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Symbol	Parameter	Condition	Min	Typ	Max	Units
Clock						
T_{CLK}	Clock time	DDR50	20	-	-	ns
T_{CR}, T_{CF}	Rise time, fall time	DDR50	-	-	0.2*T_{CLK}	Ns
Clock Duty		DDR50	45	-	55	%
CMD Input						
T_{IS}	Input setup time	DDR50	6	-	-	ns
T_{IH}	Input hold time	DDR50	0.8	-	-	ns
CMD Output						
T_{ODLY}	Output delay time during data transfer mode	DDR50	-	-	13.7	ns
T_{OHLD}	Output hold time	DDR50	1.5	-	-	ns
DAT [3:0] Input						
T_{IS2X}	Input setup time	DDR50	3	-	-	ns
T_{IH2X}	Input hold time	DDR50	0.8	-	-	ns
DAT [3:0] Output						
$T_{ODLY2X(max)}$	Output delay time during data transfer mode	DDR50	-	-	7	ns
$T_{ODLY2X(min)}$	Output hold time	DDR50	1.5	-	-	ns

SDIO Timing Data - DDR50 Mode (50MHz)

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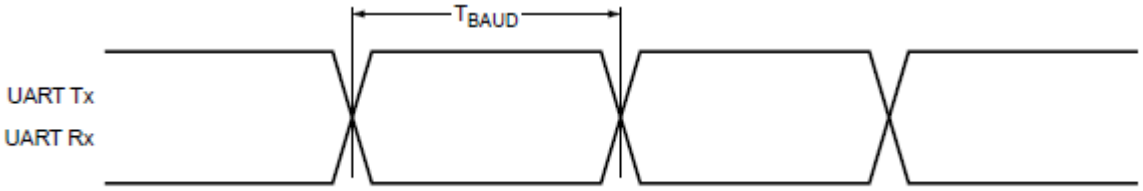
3.4.3.High-Speed UART Interface

The FRDM-IW416-AW-AM510 supports a high-speed Universal Asynchronous Receiver/Transmitter (UART) interface, compliant to the industry standard 16550 specification. High-speed baud rates are supported to provide the physical transport between the device and the host for exchanging Bluetooth data.



Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{BAUD}	Baud rate	26MHz or 40MHz input clock	250	-	-	ns

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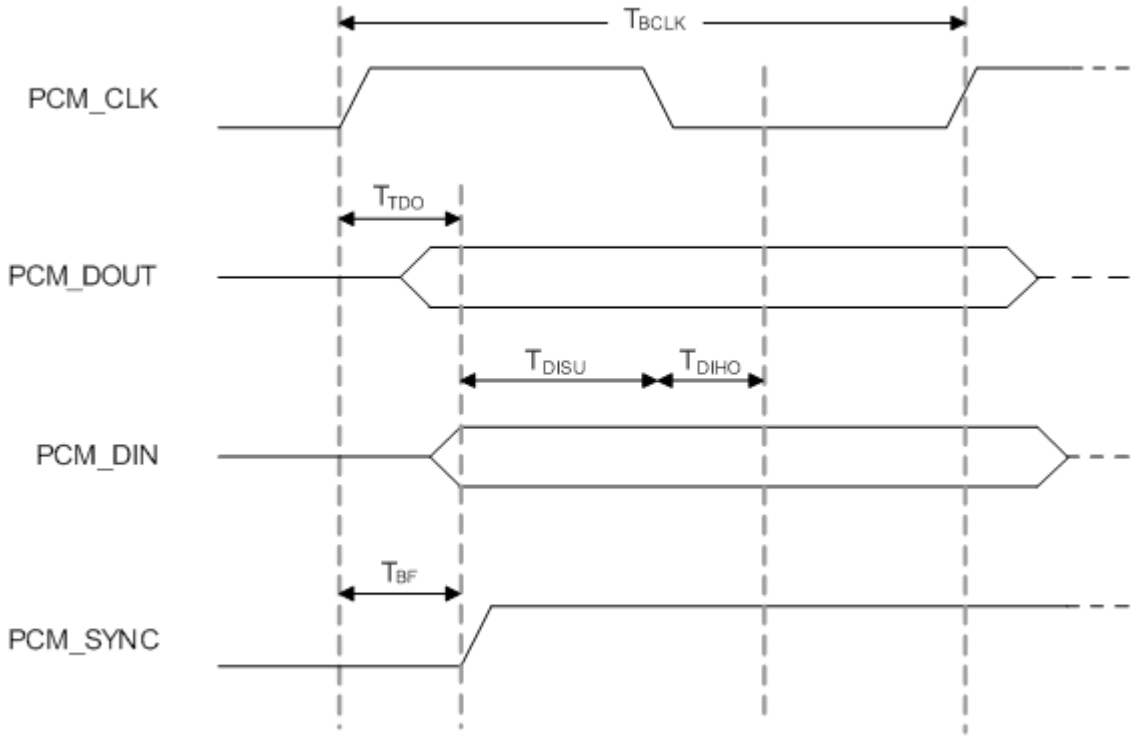
3.4.4 PCM Interface

3.4.4.1 PCM Timing Specification – Master Mode



Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{BCLK}	--	--	--	2/2.048	--	MHz
Duty $Cycle_{BCLK}$	--	--	0.4	0.5	0.6	--
$T_{BCLK\ rise/fall}$	--	--	--	3	--	ns
T_{DO}	--	--	--	--	15	ns
T_{DISU}	--	--	20	--	--	ns
T_{DIHO}	--	--	15	--	--	ns
T_{BF}	--	--	--	--	15	ns

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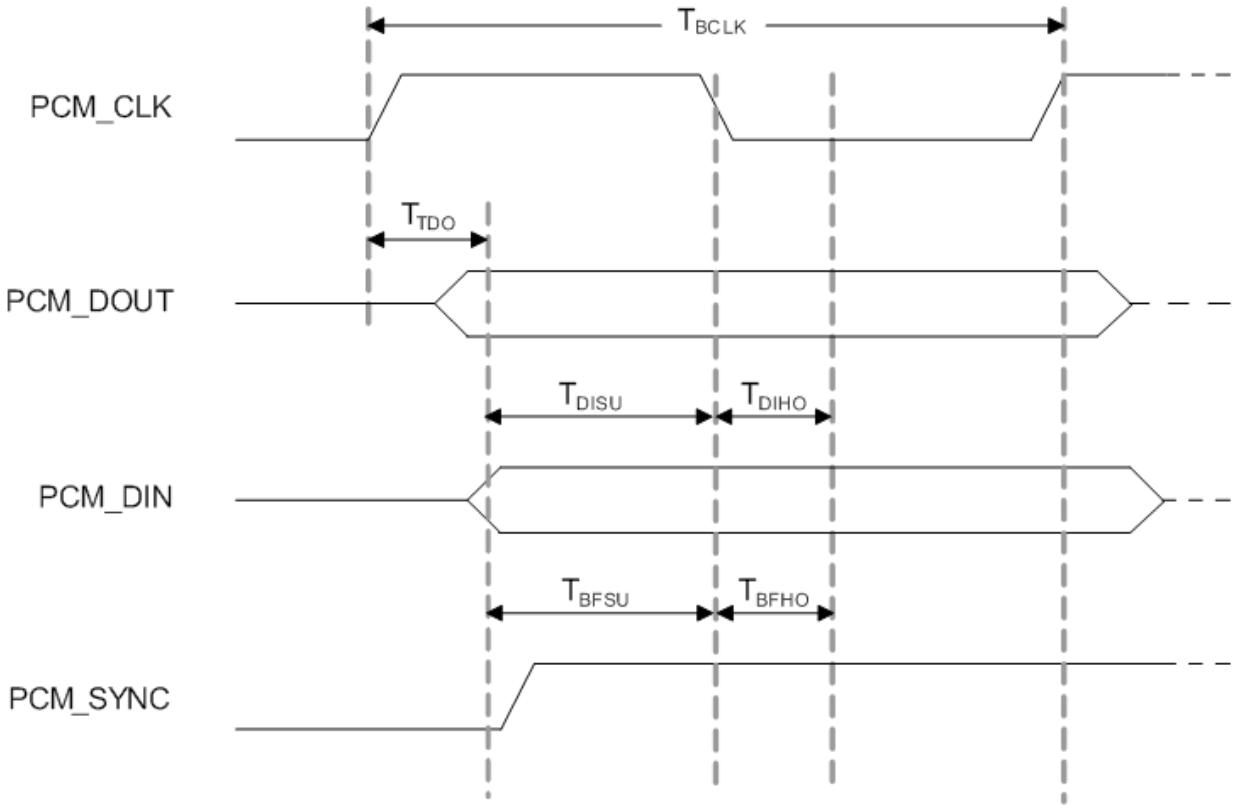
3.4.4.2 PCM Timing Specification – Slave Mode



Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{BCLK}	--	--	--	2/2.048	--	MHz
Duty $Cycle_{BCLK}$	--	--	0.4	0.5	0.6	--
$T_{BCLK\ rise/fall}$	--	--	--	3	--	ns
T_{DO}	--	--	--	--	30	ns
T_{DISU}	--	--	15	--	--	ns
T_{DIHO}	--	--	10	--	--	ns
T_{BFSU}	--	--	15	--	--	ns
T_{BFHO}			10		--	ns

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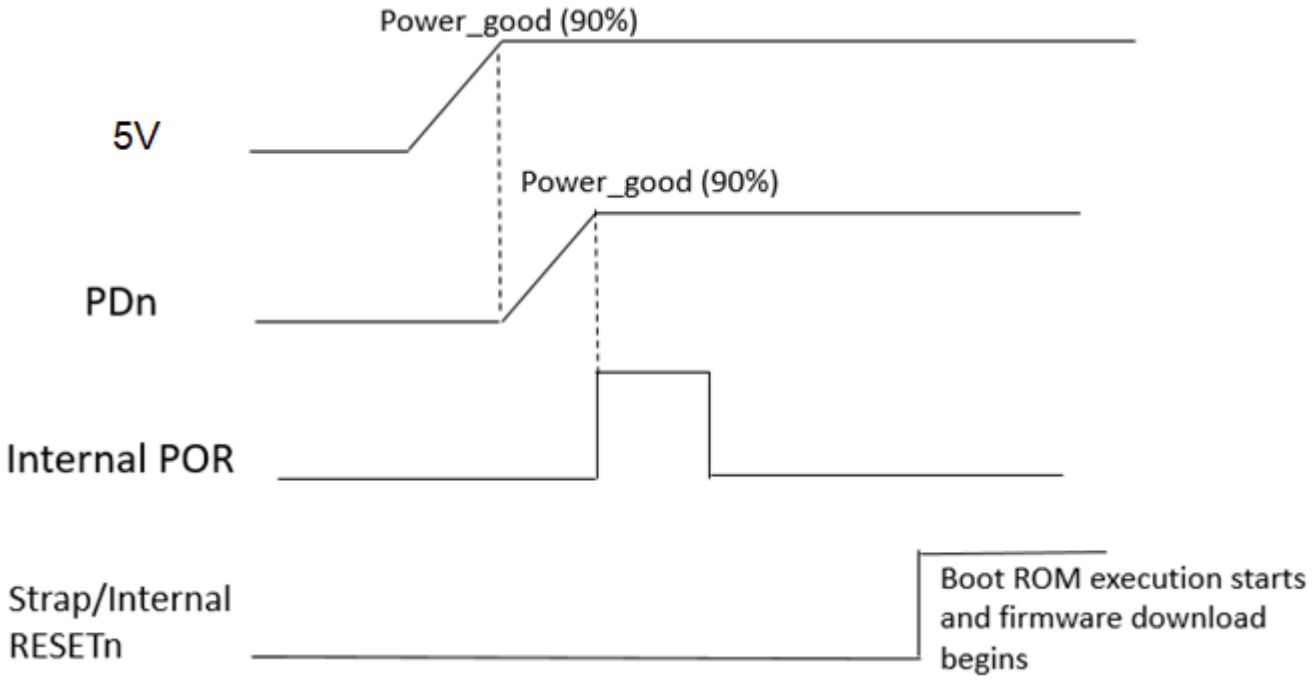
3.5 Timing Sequence

FRDM-IW416-AW-AM510 power up timing sequence.



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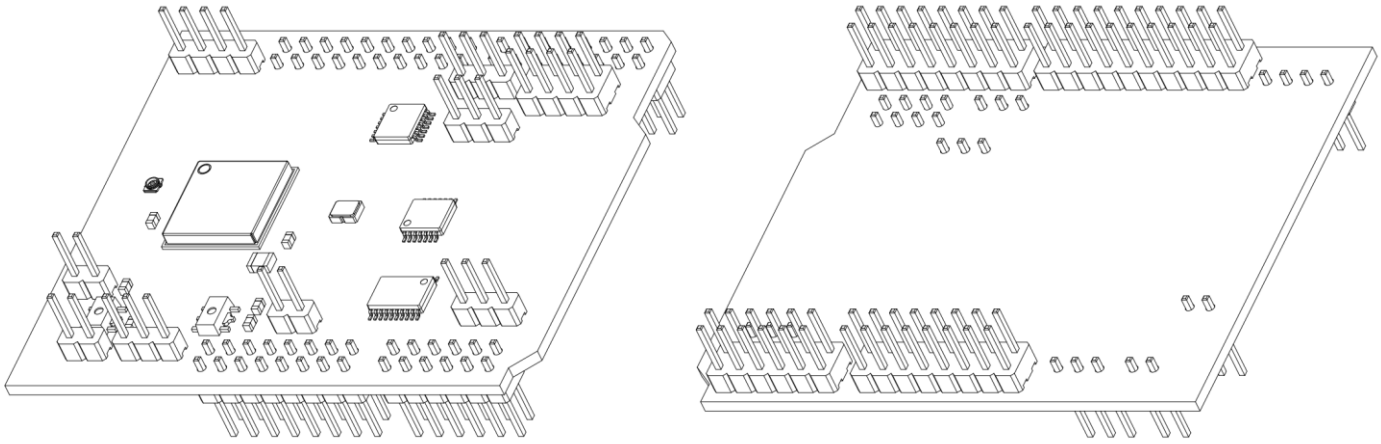
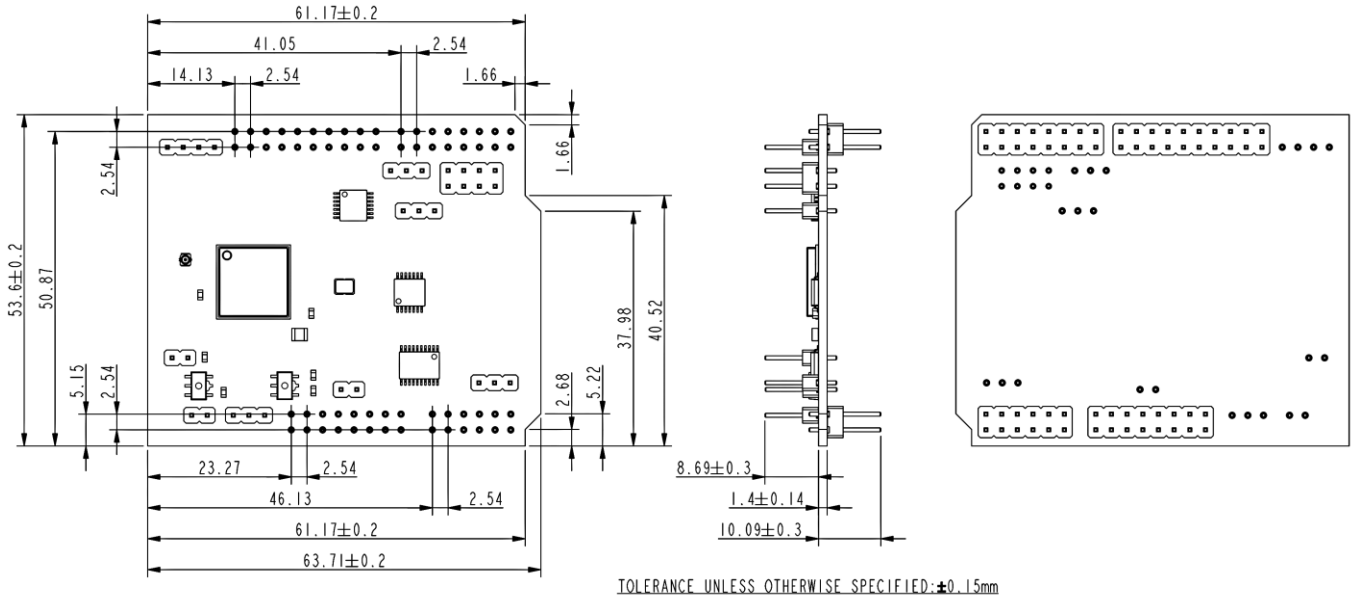
4. Mechanical Information

4.1 Mechanical Drawing





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5. Packing Information

TBD

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