

<b>PCN Number:</b>	20241119009.2	<b>PCN Date:</b>	November 20, 2024
<b>Title:</b>	Qualification of RFAB & MIHO8 Fabs using qualified Process Technologies, Die Revision, Datasheet, and new Assembly/Test site (MLA) & BOM options for select devices		
<b>Customer Contact:</b>	Change Management Team	<b>Dept:</b>	Quality Services
<b>Proposed 1<sup>st</sup> Ship Date:</b>	May 19, 2025	<b>Sample requests accepted until:</b>	December 20, 2024*

**\*Sample requests received after December 20, 2024 will not be supported.**

**Change Type:**

<input checked="" type="checkbox"/>	Assembly Site	<input checked="" type="checkbox"/>	Design	<input type="checkbox"/>	Wafer Bump Material
<input checked="" type="checkbox"/>	Assembly Process	<input checked="" type="checkbox"/>	Data Sheet	<input checked="" type="checkbox"/>	Wafer Bump Process
<input checked="" type="checkbox"/>	Assembly Materials	<input type="checkbox"/>	Part number change	<input checked="" type="checkbox"/>	Wafer Fab Site
<input type="checkbox"/>	Mechanical Specification	<input checked="" type="checkbox"/>	Test Site	<input checked="" type="checkbox"/>	Wafer Fab Material
<input checked="" type="checkbox"/>	Packing/Shipping/Labeling	<input type="checkbox"/>	Test Process	<input checked="" type="checkbox"/>	Wafer Fab Process

**PCN Details**

**Description of Change:**

Texas Instruments is pleased to announce the addition of RFAB & MIHO8 Fabs using the LBC9 & ISOSAX qualified process technologies, Assembly/Test site (MLA) and BOM options for the devices listed below.

Current Fab Site			Additional Fab Site		
Current Fab Site	Process	Wafer Diameter	Additional Fab Site	Process	Wafer Diameter
DL-LIN (2 die)	LBC4	150 mm	RFAB (2 die) MIHO8 (1 die)	LBC9 ISOSAX	300 mm 200 mm

The die were also changed as a result of the process change.

	Current	New
Probe site	No Probe	CD-PR

Construction differences are as follows:

**Group 1 device**

	TAI	MLA
Wire diam/type	1.3mil Au	0.8mil Cu
Mold compound	4209640	4221499

**Group 2 device**

	TAI	MLA
Wire diam/type	0.96mil Au	0.8mil Cu
Mold compound	4209640	4211880

The datasheets will be changing as a result of the above mentioned changes. The datasheet change details can be reviewed in the datasheet revision history. The links to the revised datasheets are available in the table below.



ISO7240CF-Q1, ISO7241C-Q1, ISO7242C-Q1  
SLLSE40B – SEPTEMBER 2010 – REVISED NOVEMBER 2024

Changes from Revision A (September 2011) to Revision B (November 2024)	Page
• Updated reference from capacitive isolation to isolation barrier throughout the document.....	1
• Updated VDE V 0884-11 to DIN VDE 0884-17 throughout the document.....	1
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Updated Thermal Characteristics, Safety Limiting Values, and Thermal Derating Curves to provide more accurate system-level thermal calculations.....	5
• Updated electrical and switching characteristics to match device performance.....	7
• Added the <i>Detailed Description, Overview, Feature Description, Functional Block Diagram, and Device Functional Modes</i> sections.....	19
• Added the <i>Typical Application, Power Supply Recommendations, and Layout</i> sections.....	21



ISO7220A-Q1, ISO7221A-Q1, ISO7221C-Q1  
SLLS965E – JULY 2009 – REVISED NOVEMBER 2024

Changes from Revision D (April 2020) to Revision E (November 2024)	Page
• Updated the content throughout the document to better align with the <a href="#">commercial version of the device</a> .....	1
• Updated reference from capacitive isolation to isolation barrier throughout the document.....	1
• Updated VDE V 0884-11 to DIN VDE 0884-17 throughout the document.....	1
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Updated Thermal Characteristics, Safety Limiting Values, and Thermal Derating Curves to provide more accurate system-level thermal calculations.....	4
• Updated electrical and switching characteristics to match device performance.....	6
• Added the <i>Detailed Description, Overview, Feature Description, Functional Block Diagram, and Device Functional Modes</i> sections.....	16
• Added the <i>Typical Application, Power Supply Recommendations, and Layout</i> sections.....	18



ISO721-Q1, ISO722-Q1  
SLLS918D – JULY 2008 – REVISED NOVEMBER 2024

Changes from Revision C (July 2013) to Revision D (November 2024)	Page
• Updated VDE V 0884-11 to DIN VDE 0884-17 throughout the document.....	1
• Updated reference from capacitive isolation to isolation barrier throughout the document.....	1
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Updated Thermal Characteristics, Safety Limiting Values, and Thermal Derating Curves to provide more accurate system-level thermal calculations.....	4
• Updated electrical and switching characteristics to match device performance.....	6
• Added the <i>Detailed Description, Overview, Feature Description, Functional Block Diagram, and Device Functional Modes</i> sections.....	14
• Added the <i>Typical Application, Power Supply Recommendations, and Layout</i> sections.....	16



ISO7231C-Q1  
SLLSE71A – SEPTEMBER 2011 – REVISED NOVEMBER 2024

Changes from Revision * (September 2011) to Revision A (November 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Updated reference from capacitive isolation to isolation barrier throughout the document.....	1
• Updated VDE V 0884-11 to DIN VDE 0884-17 throughout the document.....	1
• Updated electrical and switching characteristics to match device performance.....	5
• Changed C <sub>1</sub> - Typical value from 1 To: 2.....	6
• Changed <a href="#">Figure 4-1</a> , <a href="#">Figure 4-2</a> , and <a href="#">Figure 4-3</a> .....	10
• Added the <i>Detailed Description, Overview, Feature Description, and Device Functional Modes</i> sections.....	14
• Moved the <i>Functional Diagram</i> section to the <i>Detailed Description</i> section and renamed to "Functional Block Diagram" section.....	14
• Added the <i>Typical Application, Design Requirements, Detailed Design Procedure, and Application Curves</i> sections.....	16
• Changed the <i>Life Expectancy vs Working Voltage</i> section to the <i>Insulation Characteristics Curves</i> section and moved under the <i>Application Curves</i> section.....	17
• Added the <i>Documentation Support and Related Documentation</i> sections.....	19

Product Folder	Current Datasheet Number	New Datasheet Number	Link to full datasheet
ISO724xC-Q1	SLLSE40A	<a href="#">SLLSE40B</a>	<a href="http://www.ti.com/product/ISO7240C-Q1">http://www.ti.com/product/ISO7240C-Q1</a>

ISO722x-Q1	SLLS965D	<b>SLLS965E</b>	<a href="http://www.ti.com/product/ISO7220-Q1">http://www.ti.com/product/ISO7220-Q1</a>
ISO721-Q1, ISO722-Q1	SLLS918C	<b>SLLS918D</b>	<a href="http://www.ti.com/product/ISO722-Q1">http://www.ti.com/product/ISO722-Q1</a>
ISO7231C-Q1	SLLSE71	<b>SLLSE71A</b>	<a href="http://www.ti.com/product/ISO7231C-Q1">http://www.ti.com/product/ISO7231C-Q1</a>

These changes may be reviewed at the datasheet links provided.

Qual details are provided in the Qual Data Section.

**Reason for Change:**

These changes are part of our multiyear plan to transition products from our 150-millimeter factories to newer, more efficient manufacturing processes and technologies, underscoring our commitment to product longevity and supply continuity.

**Anticipated impact on Form, Fit, Function, Quality or Reliability (positive / negative):**

None

**Impact on Environmental Ratings:**

Checked boxes indicate the status of environmental ratings following implementation of this change. If below boxes are checked, there are no changes to the associated environmental ratings.

<b>RoHS</b>	<b>REACH</b>	<b>Green Status</b>	<b>IEC 62474</b>
<input checked="" type="checkbox"/> No Change			

**Changes to product identification resulting from this PCN:**

**Fab Site Information:**

Chip Site	Chip Site Origin Code (20L)	Chip Site Country Code (21L)	Chip Site City
DL-LIN	DLN	USA	Dallas
<b>RFAB</b>	<b>RFB</b>	<b>USA</b>	<b>Richardson</b>
<b>MIH08</b>	<b>MH8</b>	<b>JPN</b>	<b>Ibaraki</b>

**Die Rev:**

<b>Current</b>	<b>New</b>
Die Rev [2P] A, B, C, D	Die Rev [2P] -, A

**Assembly/Test Site Information:**

Assembly Site	Assembly Site Origin (22L)	Assembly Country Code (23L)	Assembly City
TI Taiwan	TAI	TWN	Chung Ho, New Taipei City
<b>MLA</b>	<b>MLA</b>	<b>MYS</b>	<b>Kuala Lumpur</b>
<b>CD-PR</b> (Probe site)	<b>CDP</b>	<b>CHN</b>	<b>Chengdu</b>

Sample product shipping label (not actual product label):

TEXAS INSTRUMENTS

MADE IN: Malaysia  
2DC: 2Q:

MSL 2 /260C/1 YEAR	SEAL DT
MSL 1 /235C/UNLIM	03/29/04

OPT:  
ITEM: 39  
LBL: 5A (L)T0:1750



(1P) SN74LS07NSR  
(Q) 2000 (D) 0336  
(31T) LOT: 3959047MLA  
(4W) TKY (1T) 7523483SI2  
(P)  
(2P) REV: (V) 0033317  
(20L) CSO: SHE (21L) CCO:USA  
(22L) ASO: MLA (23L) ACO: MYS

**Group 1 Product Affected:**

ISO7241CQDWRQ1	ISO7231CQDWRQ1	ISO7240CFQDWRQ1	ISO7242CQDWRQ1
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**Group 2 Product Affected:**

ISO722QDRQ1	ISO7220AQDRQ1	ISO7221CQDRQ1
ISO721QDRQ1	ISO7221AQDRQ1	

For alternate parts with similar or improved performance, please visit the product page on [TI.com](http://TI.com)

TI Information  
Selective Disclosure

Automotive Qualification Summary  
(As per AEC-Q100 Rev. J and JEDEC Guidelines)

ISO RedBull Wave 2 MSL1 Eval Qual at MLA (16-DW ISO7241CQ)  
Approve Date 04-NOVEMBER -2024

Product Attributes

Attributes	Qual Device: ISO7241CQDWRQ1	QBS Process Reference: TCAN1044AEVDRQ1	QBS Package Reference: ISO7240CFQDWRQ1	QBS Package Reference: ISO7241CQDWRQ1	QBS Package Reference: ISO7231CQDWRQ1	QBS Package Reference: ISO7242CQDWRQ1	QBS Package Reference: ISO7241CQDWRQ1
Automotive Grade Level	Grade 1	Grade 0	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1
Operating Temp Range (C)	-40 to 125	-40 to 150	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125
Product Function	Interface	Interface	Interface	Interface	Interface	Interface	Interface
Wafer Fab Supplier	RFAB, MHS, RFAB	RFAB	RFAB, MHS, RFAB	RFAB, MHS, RFAB	RFAB, MHS, RFAB	RFAB, MHS, RFAB	RFAB, MHS, RFAB
Assembly Site	MLA	MLA	MLA	MLA	MLA	MLA	MLA
Package Group	SOIC	SOIC	SOIC	SOIC	SOIC	SOIC	SOIC
Package Designator	DW	D	DW	DW	DW	DW	DW
Pin Count	16	8	16	16	16	16	16

- QBS: Qual By Similarity, also known as Generic Data
- Qual Device ISO7241CQDWRQ1 is qualified at MSL1 260C

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: ISO7241CQDWRQ1	QBS Process Reference: TCAN1044AEVDRQ1	QBS Package Reference: ISO7240CFQDWRQ1	QBS Package Reference: ISO7241CQDWRQ1	QBS Package Reference: ISO7231CQDWRQ1	QBS Package Reference: ISO7242CQDWRQ1	QBS Package Reference: ISO7241CQDWRQ1
Test Group A - Accelerated Environment Stress Tests														
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL1 260C	-	No Fails	No Fails	-	-	-	-	-
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL2 260C	-	-	-	-	No Fails	No Fails	-	No Fails
HAST	A2	JEDEC JESD22-A110	3	77	Biased HAST	130C/85%RH	96 Hours	-	1/77/0	-	1/77/0	-	-	3/231/0

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device:	QBS Process Reference:	QBS Package Reference:				
								ISO7241CQDWRQ1	TCAN1044AEVDRQ1	ISO7240CFQDWRQ1	ISO7241CQDWRQ1	ISO7231CQDWRQ1	ISO7242CQDWRQ1	ISO7241CQDWRQ1
ACU/HAST	A3	JEDEC JESD22-A102/JEDEC JESD22-A118	3	77	Autoclave	121C/15psig	96 Hours	-	1/77/0	-	1/77/0	-	-	-
ACU/HAST	A3	JEDEC JESD22-A102/JEDEC JESD22-A118	3	77	Unbiased HAST	130C/85%RH	96 Hours	3/231/0	-	-	-	-	-	-
TC	A4	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle	-55C/150C	500 Cycles	3/231/0	-	-	1/77/0	-	-	3/231/0
TC-BP	A4	ML-STD883 Method 2011	1	5	Post Temp Cycle Bond Pull	-	-	-	-	-	1/5/0	-	-	-
TC-SAM	A4	-	3	3	Post TC SAM	<50% delamination	-	-	1/12/0	-	-	-	-	-
HTSL	A6	JEDEC JESD22-A103	1	45	High Temperature Storage Life	150C	1000 Hours	-	-	-	1/45/0	-	-	3/135/0
HTSL	A6	JEDEC JESD22-A103	1	45	High Temperature Storage Life	175C	1000 Hours	-	1/45/0	-	-	-	-	-
<b>Test Group B - Accelerated Lifetime Simulation Tests</b>														
HTOL	B1	JEDEC JESD22-A108	3	77	Life Test	150C	1000 Hours	-	3/231/0	-	-	-	-	-
ELFR	B2	AEC Q100-008	3	800	Early Life Failure Rate	150C	48 Hours	-	3/2400/0	-	-	-	-	-
<b>Test Group C - Package Assembly Integrity Tests</b>														
WBS	C1	AEC Q100-001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	-	1/30/0	-	3/90/0	-	-	-
WBP	C2	ML-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	-	1/30/0	-	3/90/0	-	-	-
SD	C3	JEDEC J-STD-002	1	15	PB-Free Solderability	>95% Lead Coverage	-	-	-	-	1/15/0	-	-	-
PD	C4	JEDEC JESD22-B100 and B108	3	10	Physical Dimensions	Cpk>1.67	-	-	-	-	3/30/0	-	-	-
<b>Test Group D - Die Fabrication Reliability Tests</b>														
EM	D1	JESD61	-	-	Electromigration	-	-	Completed Per Process Technology Requirements						
TDD8	D2	JESD35	-	-	Time Dependent Dielectric Breakdown	-	-	Completed Per Process Technology Requirements						
Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device:	QBS Process Reference:	QBS Package Reference:				
								ISO7241CQDWRQ1	TCAN1044AEVDRQ1	ISO7240CFQDWRQ1	ISO7241CQDWRQ1	ISO7231CQDWRQ1	ISO7242CQDWRQ1	ISO7241CQDWRQ1
HCI	D3	JESD60 & 28	-	-	Hot Carrier Injection	-	-	Completed Per Process Technology Requirements						
BTI	D4	-	-	-	Bias Temperature Instability	-	-	Completed Per Process Technology Requirements						
SM	D5	-	-	-	Stress Migration	-	-	Completed Per Process Technology Requirements						
<b>Test Group E - Electrical Verification Tests</b>														
ESD	E2	AEC Q100-002	1	3	ESD HBM	-	12000 Volts	-	1/3/0	-	-	-	-	-
ESD	E2	AEC Q100-002	1	3	ESD HBM	-	2000 Volts	-	-	1/3/0	1/3/0	1/3/0	1/3/0	-
ESD	E2	AEC Q100-002	1	3	ESD HBM	-	4000 Volts	-	1/3/0	-	-	-	-	-
ESD	E3	AEC Q100-011	1	3	ESD CDM	-	1500 Volts	-	1/3/0	-	-	-	-	-
ESD	E3	AEC Q100-011	1	3	ESD CDM	-	500 Volts	-	-	1/3/0	1/3/0	1/3/0	1/3/0	-
LU	E4	AEC Q100-004	1	3	Latch-Up	Per AEC Q100-004	-	-	1/6/0	1/3/0	1/3/0	1/3/0	1/3/0	-
ED	E5	AEC Q100-009	3	30	Electrical Distributions	Cpk>1.67 Room, hot, and cold	-	-	3/90/0	1/30/0	3/90/0	1/30/0	1/30/0	-

**Additional Tests**

- Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable
- The following are equivalent HTOL options based on an activation energy of 0.7eV: 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours
- The following are equivalent HTSL options based on an activation energy of 0.7eV: 150C/1k Hours, and 170C/420 Hours
- The following are equivalent Temp Cycle options per JESD47: -55C/125C/700 Cycles and -55C/150C/500 Cycles

**Ambient Operating Temperature by Automotive Grade Level:**

- Grade 0 (or E): -40C to +150C
- Grade 1 (or Q): -40C to +125C
- Grade 2 (or T): -40C to +105C
- Grade 3 (or I): -40C to +85C

**E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):**

- Room/Hot/Cold: HTOL, ED
- Room/Hot: THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU
- Room: ACU/HAST

Quality and Environmental data is available at TI's external Web site: <http://www.ti.com/>

TI Qualification ID: R-CHG-2406-026

**Automotive Qualification Summary  
(As per AEC and JEDEC Guidelines)**

**Q006 {SOIC} at {MLA}  
Approve Date 04-November-2024**

Attributes	Qual Device:	QBS Package Reference:
	<u>ISO7241CQDWRQ1</u>	<u>ISO7241CQDWRQ1</u>
Automotive Grade Level	Grade 1	Grade 1
Operating Temp Range (C)	-40 to 125	-40 to 125
Product Function	Interface	Interface
Wafer Fab Supplier	RFAB, MH8, RFAB	RFAB, MH8, RFAB
Assembly Site	MLA	MLA
Package Group	SOIC	SOIC
Package Designator	DW	DW
Pin Count	16	16

**Qualification Results**

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: <u>ISO7241CQDWRQ1</u>	QBS Reference: <u>ISO7241CQDWRQ1</u>
<b>Test Group A - Accelerated Environment Stress Tests</b>									
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL1 260C	-	3/0/0	-
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL2 260C	-	-	3/0/0
PC	A1.1	-	3	22	SAM Precon Pre	Review for delamination	-	3/66/0	3/66/0
PC	A1.2	-	3	22	SAM Precon Post	Review for delamination	-	3/66/0	3/66/0
HAST	A2.1	JEDEC JESD22-A110	3	77	Biased HAST	130C/85%RH	96 Hours	-	3/231/0
HAST	A2.1.2	-	3	1	Cross Section, post bHAST, 1X	Post stress cross section	Completed	-	3/3/0
HAST	A2.1.3	-	3	3	Wire Bond Shear, post bHAST, 1X	Post stress	-	-	3/9/0
HAST	A2.1.4	-	3	3	Bond Pull over Stitch, post bHAST, 1X	Post stress	-	-	3/9/0
HAST	A2.1.5	-	3	3	Bond Pull over Ball, post bHAST, 1X	Post stress	-	-	3/9/0
HAST	A2.2	JEDEC JESD22-A110	3	70	Biased HAST	130C/85%RH	192 Hours	-	3/231/0
HAST	A2.2.1	-	3	22	SAM Analysis, post bHAST 2X	Review for delamination	Completed	-	3/66/0
HAST	A2.2.2	-	3	1	Cross Section, post bHAST, 2X	Post stress cross section	Completed	-	3/9/0
HAST	A2.2.3	-	3	3	Wire Bond Shear, post bHAST, 2X	Post stress	-	-	3/9/0
HAST	A2.2.4	-	3	3	Bond Pull over Stitch, post bHAST, 2X	Post stress	-	-	3/9/0
HAST	A2.2.5	-	3	3	Bond Pull over Ball, post bHAST, 2X	Post stress	-	-	3/9/0
TC	A4.1	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	3/231/0	3/231/0

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: ISO7241CQDWRQ1	QBS Reference: ISO7241CQDWRQ1
TC	A4.1.1	-	3	22	SAM Analysis, post TC 1X	Review for delamination	Completed	3/66/0	3/66/0
TC	A4.1.2	-	3	1	Cross Section, post TC, 1X	Post stress cross section	Completed	3/3/0	3/3/0
TC	A4.1.3	-	3	3	Wire Bond Shear, post TC, 1X	Post stress	-	3/9/0	3/9/0
TC	A4.1.4	-	3	3	Bond Pull over Stitch, post TC, 1X	Post stress	-	3/9/0	3/9/0
TC	A4.1.5	-	3	3	Bond Pull over Ball, post TC, 1X	Post stress	-	3/9/0	3/9/0
TC	A4.2	JEDEC JESD22-A104 and Appendix 3	3	70	Temperature Cycle	-65C/150C	1000 Cycles	3/231/0	3/231/0
TC	A4.2.1	-	3	22	SAM Analysis, post TC, 2X	Review for delamination	Completed	3/66/0	3/66/0
TC	A4.2.2	-	3	1	Cross Section, post TC, 2X	Post stress cross section	Completed	3/3/0	3/3/0
TC	A4.2.3	-	3	3	Wire Bond Shear, post TC, 2X	Post stress	-	3/9/0	3/9/0
TC	A4.2.4	-	3	3	Bond Pull over Stitch, post TC, 2X	Post stress	-	3/9/0	3/9/0
TC	A4.2.5	-	3	3	Bond Pull over Ball, post TC, 2X	Post stress	-	3/9/0	3/9/0
HTSL	A6.1	JEDEC JESD22-A103	3	45	High Temperature Storage Life	150C	1000 Hours	-	3/135/0
HTSL	A6.1	JEDEC JESD22-A103	3	45	High Temperature Storage Life	175C	630 Hours	-	-
HTSL	A6.1.1	-	3	1	Cross Section, post HTSL, 1X	Post stress cross section	Completed	-	3/3/0
HTSL	A6.2	JEDEC JESD22-A103	3	44	High Temperature Storage Life	150C	2000 Hours	-	3/135/0
HTSL	A6.2	JEDEC JESD22-A103	3	44	High Temperature Storage Life	175C	1000 Hours	-	-

  

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: ISO7241CQDWRQ1	QBS Reference: ISO7241CQDWRQ1
HTSL	A6.2.1	-	3	1	Cross Section, post HTSL, 2X	Post stress cross section	Completed	-	3/3/0

**Test Group C - Package Assembly Integrity Tests**

WBS	C1	AEC Q100-001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	-	-
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	-	-

- QBS: Qual By Similarity, also known as Generic Data
- Qual Device ISO7241CQDWRQ1 is qualified at MSL1 260C

- Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable
- The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours
- The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours
- The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles

**Ambient Operating Temperature by Automotive Grade Level:**

- Grade 0 (or E): -40C to +150C
- Grade 1 (or Q): -40C to +125C
- Grade 2 (or T): -40C to +105C
- Grade 3 (or I) : -40C to +85C

**E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):**

- Room/Hot/Cold : HTOL, ED
- Room/Hot : THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU
- Room : AC/uHAST

Quality and Environmental data is available at TI's external Web site: <http://www.ti.com/>

TI Qualification ID: R-CHG-2406-026

Automotive Qualification Summary  
(As per AEC-Q100 Rev. J and JEDEC Guidelines)

ISO RedBull Wave 1 Qual at MLA (8-D Automotive)  
Approve Date 04-November-2024

Product Attributes

Attributes	Qual Device: ISO721QDRQ1	Qual Device: ISO7220AQDRQ1	Qual Device: ISO722QDRQ1	Qual Device: ISO7221CQDRQ1	Qual Device: ISO7221AQDRQ1	QBS Package, Package Reference: ISO6721BQDRQ1	QBS Process Reference: SN74HCS74QPWRQ1	QBS Package Reference: AMC22C12QDRQ1
Automotive Grade Level	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1
Operating Temp Range (C)	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125
Product Function	Interface	Interface	Interface	Interface	Interface	Interface	Logic	Signal Chain
Wafer Fab Supplier	RFAB, RFAB, MH8	RFAB, RFAB, MH8	RFAB, RFAB, MH8	RFAB, RFAB, MH8	RFAB, RFAB, MH8	MH8, MH8	RFAB	MH8, DMOS6
Assembly Site	MLA	MLA	MLA	MLA	MLA	MLA	MLA	MLA
Package Group	SOIC	SOIC	SOIC	SOIC	SOIC	SOIC	TSSOP	SOIC
Package Designator	D	D	D	D	D	D	PW	D
Pin Count	8	8	8	8	8	8	14	8

- QBS: Qual By Similarity, also known as Generic Data
- Qual Device ISO721QDRQ1 is qualified at MSL2 260C
- Qual Device ISO7220AQDRQ1 is qualified at MSL2 260C
- Qual Device ISO722QDRQ1 is qualified at MSL2 260C
- Qual Device ISO7221CQDRQ1 is qualified at MSL2 260C
- Qual Device ISO7221AQDRQ1 is qualified at MSL2 260C

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: ISO721QDRQ1	Qual Device: ISO7220AQDRQ1	Qual Device: ISO722QDRQ1	Qual Device: ISO7221CQDRQ1	Qual Device: ISO7221AQDRQ1	QBS Package, Package Reference: ISO6721BQDRQ1	QBS Process Reference: SN74HCS74QPWRQ1	QBS Package Reference: AMC22C12QDRQ1
<b>Test Group A - Accelerated Environment Stress Tests</b>															
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL1 260C	-	-	-	-	3/0/0	-	3/0/0	3/0/0	-
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL2 260C	-	-	-	-	-	-	-	-	3/0/0
HAST	A2	JEDEC JESD22-A110	3	77	Biasd HAST	130C/85%RH	96 Hours	-	-	-	-	-	-	3/231/0	-
ACU/HAST	A3	JEDEC JESD22-A102/JEDEC JESD22-A118	3	77	Autoclave	121C/15psig	96 Hours	-	-	-	1/77/0	-	3/231/0	3/231/0	-
ACU/HAST	A3	JEDEC JESD22-A102/JEDEC JESD22-A118	3	77	Unbiased HAST	130C/85%RH	96 Hours	-	-	-	-	-	-	-	3/231/0
TC	A4	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	-	-	-	1/77/0	-	-	-	-
TC-BP	A4	MIL-STD883 Method 2011	1	5	Post Temp Cycle Bond Pull	-	-	-	-	-	1/5/0	-	-	-	-
TC-SAM	A4	-	3	3	Post TC SAM	<50% delamination	-	-	-	-	1/12/0	-	1/12/0	-	-
HTSL	A6	JEDEC JESD22-A103	1	45	High Temperature Storage Life	175C	500 Hours	-	-	-	-	-	3/135/0	-	-
<b>Test Group B - Accelerated Lifetime Simulation Tests</b>															
HTOL	B1	JEDEC JESD22-A108	3	77	Life Test	125C	1000 Hours	-	-	-	-	-	3/231/0	3/231/0	-
HTOL	B1	JEDEC JESD22-A108	3	77	Life Test	150C	408 Hours	-	-	-	-	-	-	-	3/231/0
ELFR	B2	AEC Q100-008	3	800	Early Life Failure Rate	125C	48 Hours	-	-	-	-	-	-	3/2400/0	-
<b>Test Group C - Package Assembly Integrity Tests</b>															
WBS	C1	AEC Q100-001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	1/30/0	-	-	3/90/0	-	3/228/0	3/90/0	3/90/0
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	1/30/0	-	-	3/90/0	-	3/228/0	3/90/0	3/90/0
SD	C3	JEDEC J-STD-002	1	15	PB Solderability	>95% Lead Coverage	-	-	-	-	-	-	1/15/0	1/15/0	1/15/0
SD	C3	JEDEC J-STD-002	1	15	PB-Free Solderability	>95% Lead Coverage	-	-	-	-	-	-	1/15/0	1/15/0	1/15/0

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: ISO721QDRQ1	Qual Device: ISO7220AQDRQ1	Qual Device: ISO7221QDRQ1	Qual Device: ISO7221CQDRQ1	Qual Device: ISO7221AQDRQ1	QBS Package Reference: ISO6721RQDRQ1	QBS Process Reference: SN74HC874QPWRQ1	QBS Package Reference: AMC22C12QDRQ1
PD	C4	JEDEC JESD22-B100 and B108	3	10	Physical Dimensions	Cpk0.67	-	1/100	-	-	3/300	-	3/300	3/300	3/300
<b>Test Group D - Die Fabrication Reliability Tests</b>															
EM	D1	JESD61	-	-	Electromigration	-	-	Completed Per Process Technology Requirements							
TDD	D2	JESD35	-	-	Time Dependent Dielectric Breakdown	-	-	Completed Per Process Technology Requirements							
HCI	D3	JESD60 & 28	-	-	Hot Carrier Injection	-	-	Completed Per Process Technology Requirements							
BTI	D4	-	-	-	Bias Temperature Instability	-	-	Completed Per Process Technology Requirements							
SM	D5	-	-	-	Stress Migration	-	-	Completed Per Process Technology Requirements							
<b>Test Group E - Electrical Verification Tests</b>															
ESD	E2	AEC Q100-002	1	3	ESD HBM	-	2000 Volts	1/3/0	1/3/0	1/3/0	1/3/0	1/3/0	1/3/0	1/3/0	1/3/0
ESD	E3	AEC Q100-011	1	3	ESD CDM	-	500 Volts	1/3/0	1/3/0	1/3/0	1/3/0	1/3/0	1/3/0	1/3/0	1/3/0
LU	E4	AEC Q100-004	1	3	Latch-Up	Per AEC Q100-004	-	1/3/0	1/3/0	1/3/0	1/3/0	1/3/0	1/6/0	1/6/0	1/6/0
ED	E5	AEC Q100-009	3	30	Electrical Distributions	Cpk0.67 Room, hot, and cold	-	1/30/0	1/30/0	1/30/0	1/30/0	1/30/0	3/90/0	3/90/0	3/90/0
<b>Additional Tests</b>															

- Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable
- The following are equivalent HTOL options based on an activation energy of 0.7eV: 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours
- The following are equivalent HTSL options based on an activation energy of 0.7eV: 150C/1k Hours, and 170C/420 Hours
- The following are equivalent Temp Cycle options per JESD47: -55C/125C/700 Cycles and -65C/150C/500 Cycles

**Ambient Operating Temperature by Automotive Grade Level:**

- Grade 0 (or E): -40C to +150C
- Grade 1 (or Q): -40C to +125C
- Grade 2 (or T): -40C to +105C
- Grade 3 (or I) : -40C to +85C

**E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):**

- Room/Hot/Cold : HTOL, ED
- Room/Hot : THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU
- Room : AC/HAST

Quality and Environmental data is available at TI's external Web site: <http://www.ti.com/>

TI Qualification ID: R-CHG-2304-011

**Automotive Qualification Summary  
(As per AEC and JEDEC Guidelines)**

**Q006 {SOIC} at {MLA}**  
**Approve Date 04-November-2024**

Attributes	Qual Device: ISO721QDRQ1	Qual Device: ISO7220AQDRQ1	Qual Device: ISO722QDRQ1	Qual Device: ISO7221CQDRQ1	Qual Device: ISO7221AQDRQ1	QBS Package, Package Reference: ISO6721BQDRQ1
Automotive Grade Level	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1
Operating Temp Range (C)	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125
Product Function	Interface	Interface	Interface	Interface	Interface	Interface
Wafer Fab Supplier	RFAB, RFAB, MH8	RFAB, RFAB, MH8	RFAB, RFAB, MH8	RFAB, RFAB, MH8	RFAB, RFAB, MH8	MH8, MH8
Assembly Site	MLA	MLA	MLA	MLA	MLA	MLA
Package Group	SOIC	SOIC	SOIC	SOIC	SOIC	SOIC
Package Designator	D	D	D	D	D	D
Pin Count	8	8	8	8	8	8

**Qualification Results**

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: ISO721QDRQ1	Qual Device: ISO7220AQDRQ1	Qual Device: ISO722QDRQ1	Qual Device: ISO7221CQDRQ1	Qual Device: ISO7221AQDRQ1	QBS Reference: ISO6721BQDRQ1
<b>Test Group A - Accelerated Environment Stress Tests</b>													
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL1 260C	-	-	-	-	-	-	3/0/0
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL2 260C	-	-	-	-	-	-	-
PC	A1.1	-	3	22	SAM Precon Pre	Review for delamination	-	-	-	-	-	-	-
PC	A1.2	-	3	22	SAM Precon Post	Review for delamination	-	-	-	-	-	-	2/44/0
HAST	A2.1	JEDEC JESD22-A110	3	77	Biased HAST	130C/85%RH	96 Hours	-	-	-	-	-	-
HAST	A2.1.2	-	3	1	Cross Section, post bHAST, 1X	Post stress cross section	Completed	-	-	-	-	-	2/2/0
HAST	A2.1.3	-	3	3	Wire Bond Shear, post bHAST, 1X	Post stress	-	-	-	-	-	-	-
HAST	A2.1.4	-	3	3	Bond Pull over Stitch, post bHAST, 1X	Post stress	-	-	-	-	-	-	-
HAST	A2.1.5	-	3	3	Bond Pull over Ball, post bHAST, 1X	Post stress	-	-	-	-	-	-	-
HAST	A2.2	JEDEC JESD22-A110	3	70	Biased HAST	130C/85%RH	192 Hours	-	-	-	-	-	3/231/0
HAST	A2.2.1	-	3	22	SAM Analysis, post bHAST 2X	Review for delamination	Completed	-	-	-	-	-	3/66/0
HAST	A2.2.2	-	3	1	Cross Section, post bHAST, 2X	Post stress cross section	Completed	-	-	-	-	-	3/3/0
HAST	A2.2.3	-	3	3	Wire Bond Shear, post bHAST, 2X	Post stress	-	-	-	-	-	-	3/9/0
HAST	A2.2.4	-	3	3	Bond Pull over Stitch, post bHAST, 2X	Post stress	-	-	-	-	-	-	3/9/0

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: ISO721QDRQ1	Qual Device: ISO7220AQDRQ1	Qual Device: ISO722QDRQ1	Qual Device: ISO7221CQDRQ1	Qual Device: ISO7221AQDRQ1	QBS Reference: ISO6721BQDRQ1
HAST	A2.2.5	-	3	3	Bond Pull over Ball, post bHAST, 2X	Post stress	-	-	-	-	-	-	3/9/0
TC	A4.1.1	-	3	22	SAM Analysis, post TC 1X	Review for delamination	Completed	-	-	-	-	-	-
TC	A4.1.2	-	3	1	Cross Section, post TC, 1X	Post stress cross section	Completed	-	-	-	-	-	-
TC	A4.1.3	-	3	3	Wire Bond Shear, post TC, 1X	Post stress	-	-	-	-	-	-	-
TC	A4.1.4	-	3	3	Bond Pull over Stitch, post TC, 1X	Post stress	-	-	-	-	-	-	-
TC	A4.1.5	-	3	3	Bond Pull over Ball, post TC, 1X	Post stress	-	-	-	-	-	-	-
TC	A4.2	JEDEC JESD22-A104 and Appendix 3	3	70	Temperature Cycle	-65C/150C	1000 Cycles	-	-	-	-	-	3/231/0
TC	A4.2.1	-	3	22	SAM Analysis, post TC, 2X	Review for delamination	Completed	-	-	-	-	-	3/66/0
TC	A4.2.2	-	3	1	Cross Section, post TC, 2X	Post stress cross section	Completed	-	-	-	-	-	3/3/0
TC	A4.2.3	-	3	3	Wire Bond Shear, post TC, 2X	Post stress	-	-	-	-	-	-	3/9/0
TC	A4.2.4	-	3	3	Bond Pull over Stitch, post TC, 2X	Post stress	-	-	-	-	-	-	3/9/0
TC	A4.2.5	-	3	3	Bond Pull over Ball, post TC, 2X	Post stress	-	-	-	-	-	-	3/9/0
HTSL	A6.1	JEDEC JESD22-A103	3	45	High Temperature Storage Life	175C	500 Hours	-	-	-	-	-	3/135/0
HTSL	A6.1.1	-	3	1	Cross Section, post HTSL, 1X	Post stress cross section	Completed	-	-	-	-	-	-
HTSL	A6.2	JEDEC JESD22-A103	3	44	High Temperature Storage Life	150C	2000 Hours	-	-	-	-	-	-

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HTSL	A6.2	JEDEC JESD22-A103	3	44	High Temperature Storage Life	175C	1000 Hours	-	-	-	-	-	3/135/0
HTSL	A6.2.1	-	3	1	Cross Section, post HTSL, 2X	Post stress cross section	Completed	-	-	-	-	-	3/3/0
<b>Test Group C - Package Assembly Integrity Tests</b>													
WBS	C1	AEC Q100-001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	1/30/0	-	-	3/90/0	-	3/228/0
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	1/30/0	-	-	3/90/0	-	3/228/0

- QBS: Qual By Similarity, also known as Generic Data
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TI Qualification ID: R-CHG-2304-011

ZVEI ID's: SEM-DE-01, SEM-DE-02, SEM-DE-03, SEM-DS-01, SEM-PW-02, SEM-PW-09, SEM-PW-13, SEM-PA-08, SEM-PA-11, SEM-PA-18, SEM-TF-01

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