LOW POWER HIGH FIDELITY I²S INPUT HEADSET IC

Check for Samples: TLV320DAC3202

FEATURES

- **Ground Referenced Click-Pop Free Class-G Stereo Headset Driver**
- **Capable of Driving 1 VRMS at the Headset Driver Output, Per Channel, in Phase**
- **100-dB(A) Channel SNR With 6.5-mW of Quiescent Power Dissipation**
- **Built In Short-Circuit Protection for Preventing Supply Rails Overload**
- **Supports 8-, 11.025-, 12-, 16-, 24-, 32-, 44.1- and 48-kHz Sample Rates**
- **I²C Interface for Digital Control**
- **Supports 16-, 20-, 24- and 32-Bit Data Width**
- **Supports Standard I²S, PCM, Left and Right Justified Formats**
- **Supports Data Mixing With Gain Options**
- **32-Step Volume Control from 4 to -59 dB**
- **Clocking: Internal Clock Derived from I²S BCLK**
- **Package: WCSP, 0.5 mm Pitch, 2 mm x 2.5 mm**
- **Power Supply: Direct Battery and IO Supply**

APPLICATIONS

- **Smart Phones and Music Phones**
- **Portable Navigation**
- **Personal Media Players**
- **PDAs**
- **Portable Game Consoles**
- **HDD and Flash-Based Portable Audio Players**

DESCRIPTION

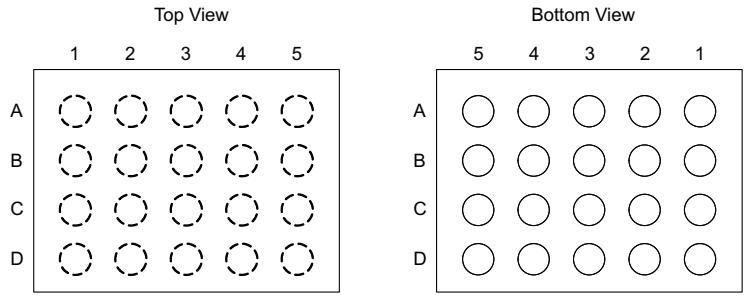
The TLV320DAC3202 is a high fidelity and low power headphone amplifier with integrated DAC and power rails. The small solution size and highly efficient operation maximizes battery life and performance. The digital audio interface supports industry standard formats such as I²S and PCM. Many features of this device such as volume setting, data width and sampling rate are configurable for optimum flexibility and efficiency. The headset power control automatically adjusts the rail voltage based on the input signal to maximize efficiency and performance. The control interface uses an industry standard I²C controller for ease of operation and reduction in device pin count.

Table 1. ORDERING INFORMATION(1)

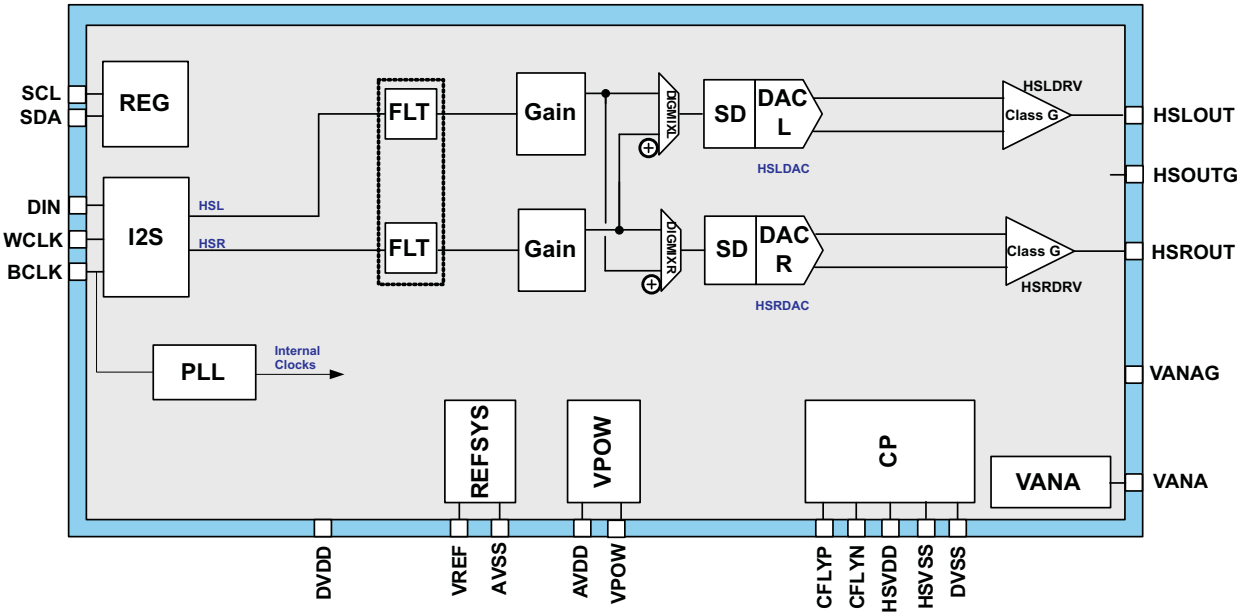
T_A	PACKAGE(2)		ORDERABLE PART NUMBER
–30ºC to 85ºC	YZJ	Tape and reel of 250	TLV320DAC3202CYZJT
		Tape and reel of 3000	TLV320DAC3202CYZJR

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) While this part number includes the YZJ package designator, it does not conform to the standard YZJ footprint. Only the drawings below should be used for system design and not the YZJ drawing available from the TI Packaging website.



FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENTS

Table 2. PIN ASSIGNMENTS (TOP VIEW)

	1	2	3	4	5
A	AVSS	VANAG	VANA	CFLYP	CFLYN
B	VREF	AVDD	VPOW	DVDD	DVSS
C	SDA	SCL	HSOUTG	HSVDD	HSOUTL
D	BCLK	WCLK	DIN	HSOUTR	HSVSS

Table 3. TERMINAL FUNCTIONS

TERMINAL		I/O	VOLTAGE LEVEL (V)	DESCRIPTION
NAME	NO.			
AVSS	A1	Input	0	Analog ground
VANAG	A2	Input	0	Leave floating
VANA	A3	Output	1.55	Analog LDO output
CFLYP	A4	Input/Output	1.95	FLY cap "+" terminal
CFLYN	A5	Input/Output	-1.95	FLY cap "-" terminal
VREF	B1	Output	0.75	Analog reference output
AVDD	B2	Input	VBAT	2.3-V to 4.8-V battery input
VPOW	B3	Output	1.95	VPOW LDO output
DVDD	B4	Input	VIO	1.8-V IO digital supply
DVSS	B5	Input	0	Digital ground
SDA	C1	Input/Output	VIO	I^2C Data
SCL	C2	Input	VIO	I^2C CLK in
HSOUTG	C3	Input	0	Headset feedback ground
HSVDD	C4	Input/Output	1.95	Headset positive supply
HSOUTL	C5	Output	+/-1.5	Headset output left
BCLK	D1	Input	VIO	I^2S bit clock
WCLK	D2	Input	VIO	I^2S word clock
DIN	D3	Input	VIO	I^2S downlink data

Table 3. TERMINAL FUNCTIONS (continued)

TERMINAL		I/O	VOLTAGE LEVEL (V)	DESCRIPTION
NAME	NO.			
HSOUTR	D4	Output	±1.5	Headset output right
HSVSS	D5	Input/Output	-1.95	Headset negative supply

ABSOLUTE MAXIMUM RATINGS(1)

All voltages values are with respect to GND. Over operating free-air temperature range (unless otherwise noted).

			VALUE	UNIT
AVDD (V_{BAT})	DC		-0.3 to 5	V
	AC(2)		-0.3 to 5.5	
DVDD (V_{IO})	DC		-0.3 to 2.1	V
	AC(2)		-0.3 to 2.2	
T_A	Operating free air temperature		-40 to 85	°C
T_J	Maximum junction temperature		125	°C
T_{stg}	Storage temperature		-65 to 150	°C
	Lead temperature		115	°C
	ESD rating (all pins)	Human Body Model	-2000 to 2000	V
		Charged Device Model	-500 to 500	

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) For spike duration of 1 ms, 10,000 times over 7 years (lifetime).

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_A	Operating free air temperature	-30		85	°C
T_{stg}	Storage temperature	-55		150	°C

ELECTRICAL CHARACTERISTICS

AVDD = 3.7 V, DVDD = 1.8 V, T_A = 25°C, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AVDD (V_{BAT})		Functional only	2.3		4.8	V
		Parametric performance	2.3		4.8	
DVDD (V_{IO})			1.65	1.8	1.95	V
V_{IH}, digital(1)			0.65 x V_{IO}			V
V_{IL}, digital(1)					0.35 x V_{IO}	V
	HSOUTL/R Voltage	Enabled	-1.5		1.5	V
		Disabled, HiZ			1.8	
	Power consumption from all supplies with internal PLL (SNR = 100 dBA)	No load		6.5		mW
		0.1 mW/channel, 1 kHz, 32 Ω		9.7		

(1) CHIP_EN = 1, HSLEN = 1, HSREN = 1, active I^2S, idle channel, amplifiers muted

ELECTRICAL CHARACTERISTICS (continued)

AVDD = 3.7 V, DVDD = 1.8 V, T_A = 25°C, unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Shutdown current	AVDD, GND mode(2)				2	µA
		DVDD, GND mode(2)				2	
		AVDD, HiZ mode(3)				1	
		DVDD, HiZ mode(3)				1	
	Startup time	From CHIP_EN assertion to Florin reaching Standby state (clock and power supplies available)			15.5		ms
	Wake up time	From HSL/R_EN assertion to Florin reaching Active state, during which the system is completely powered up with headset drivers enabled			3		ms
AUDIO PATH ELECTRICAL PERFORMANCE							
	Maximum amplitude at ball	0-dB PCM, 1 kHz, THD = 1%, 32-Ω load, 4-dB gain			1.05		Vrms
	Amplitude across load	32-Ω load		0.7			Vrms
		16-Ω load		0.45	0.5		
	Dynamic range	1 kHz, -60 dBFs, A-weighted		97	100		dB (A)
THD+N		1 kHz, 16-Ω load in series with 10 Ω (R_{EMI})	P_{OUT} = 20 mW		68		dB
			P_{OUT} = 12 mW	70	74		
			P_{OUT} = 4 mW		72		
	Frequency response	20 Hz to 20 kHz		-0.25		0.25	dB
	Channel separation	1 kHz, full scale input(4)		90	95		dB
PSRR		217 Hz, 500-mVpp ripple on AVDD		80	90		dB
	Pop noise specification(5)	Maximum DC value after power up				0.5	mV
RECEIVE CHANNEL DIGITAL FILTER PERFORMANCE, F_s = 44.1 kHz or 48 kHz							
	HPF -3 dB corner				0.8		Hz
	LPF pass band corner frequency	-10 dBF_s		5		0.42 F_s	Hz
	LPF pass band ripple			-0.25		0.25	dB
	LPF -3 dB corner				0.48 F_s		Hz
	LPF interpolation multiplier				8		
	LPF magnitude response	< 0.16 F_s		-0.05		0.05	dB
	LPF stop band corner frequency			0.6 F_s			Hz
	LPF stop band attenuation	< 2 F_s		70			dB
	Absolute delay	Filter only, at 1 kHz, without HPF Excludes interface + compute latency		11/ F_s			s
AUDIO INTERFACE TIMING PARAMETERS							
T_{bclk}	Audio clock period	Variable BCLK			1/BCLK		ns
T_{bclkh}	BCLK high duration			0.35 x BCLK period			ns
T_{bclkl}	BCLK low duration			0.35 x BCLK period			ns
T_{dv}	Data hold time following BCLK falling edge					20	ns

(2) CHIP_EN = 0, HIZ_L = 0, HIZ_R = 0
(3) CHIP_EN = 0, HIZ_L = 1, HIZ_R = 1
(4) The maximum board resistance should be less than 250 mΩ between the HSOUTL/HSOUTR pins and the HSOUTG pin.
(5) Maximum slew rate (ΔV/Δt) < 5 V/s after A-weighting

ELECTRICAL CHARACTERISTICS (continued)

AVDD = 3.7 V, DVDD = 1.8 V, T_A = 25°C, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{FS}	Sample clock setup time following BCLK falling edge				10	ns
T_{ds}	Data set time before BCLK rising edge		0.2 x BCLK period			ns
T_{dh}	Data hold time after BCLK rising edge		0.2 x BCLK period			ns
T_{wclks}	Short frame sync pulse width			1/BCLK		ns

TYPICAL PERFORMANCE CHARACTERISITICS

DAC TO HEADSET FFT
AT -3 dBFS WITH 32-Ω HEADSET

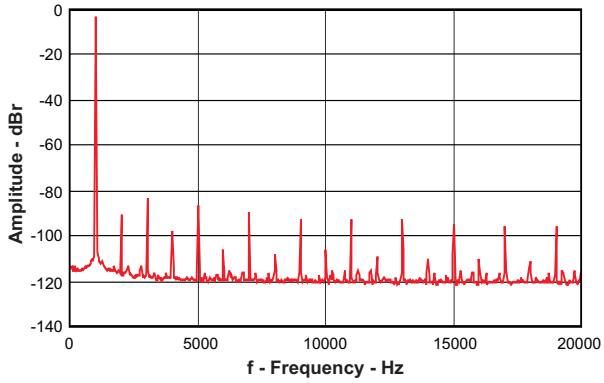


Figure 1.

DAC TO HEADSET FFT
AT -3 dBFS WITH 16-Ω HEADSET

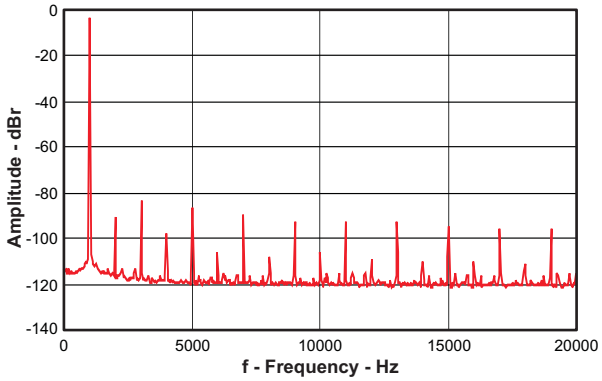


Figure 2.

CLICK AND POP PERFORMANCE
WITH 32-Ω HEADSET

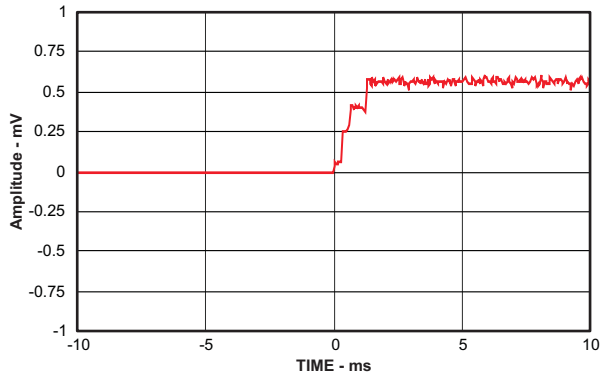


Figure 3.

CLICK AND POP PERFORMANCE
WITH 16-Ω HEADSET

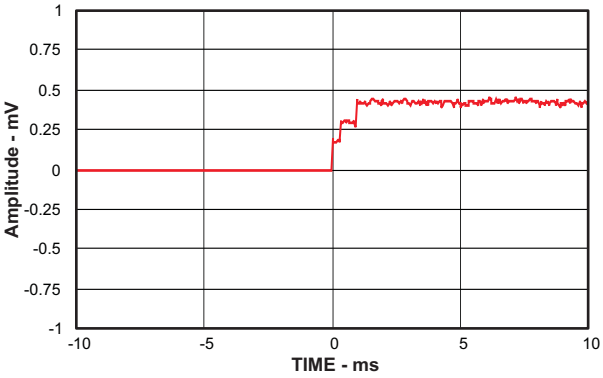


Figure 4.

TOTAL HARMONIC DISTORTION + NOISE
vs
HEADPHONE OUTPUT POWER
WITH 32-Ω HEADSET

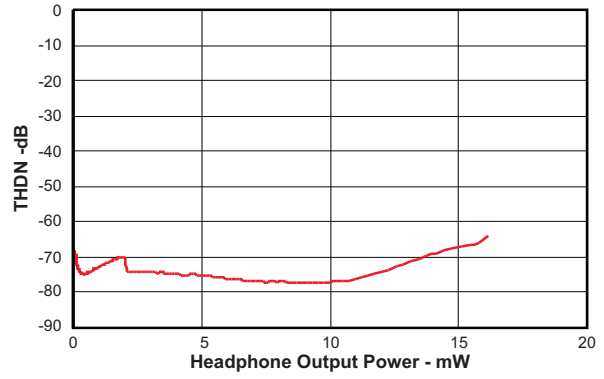


Figure 5.

TOTAL HARMONIC DISTORTION + NOISE
vs
HEADPHONE OUTPUT POWER
WITH 16-Ω HEADSET

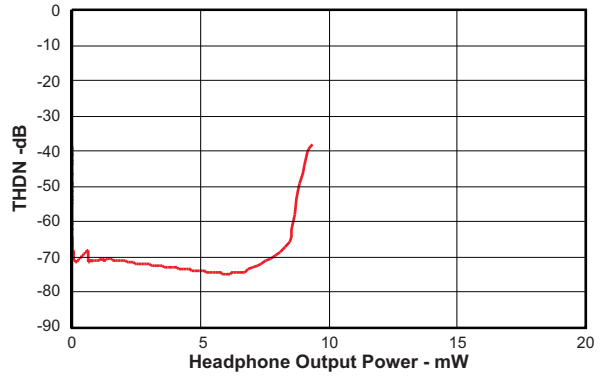


Figure 6.

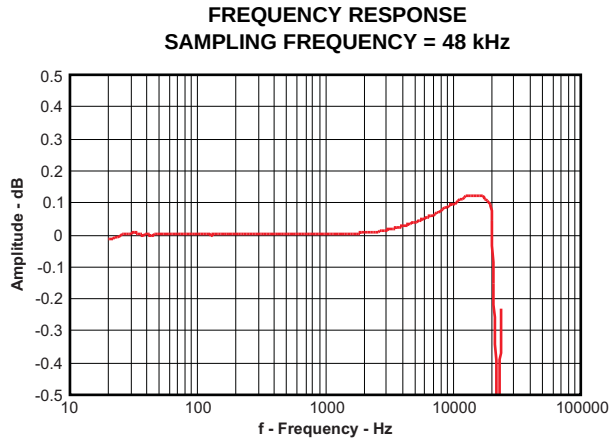


Figure 7.

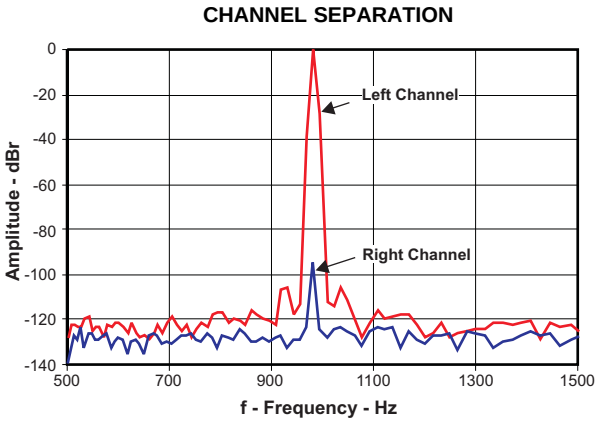


Figure 8.

DIGITAL INTERFACE

Audio Interface

The audio interface for data communication with application processor or modem supports multiple formats such as I^2S, left justified, right justified or the short frame sync PCM formats. The default interface format is I^2S at 48-kHz sampling rate and 16-bit data size. The clock input selection module within PLL block also supports multiple input frequency options. The input clock must be in standard square wave format; hence a clock squarer is not necessary. The following tables shows the details of audio interface configuration through I^2C register controls.

Table 4. Audio Interface Format Configuration Register

INTF_MODE (1:0)		INTERFACE FORMAT TYPE
0	0	Standard I^2S
0	1	Left justified I^2S
1	0	Right justified I^2S
1	1	Short PCM

Table 5. Audio Interface BCLK to WCLK Ratio Setting Register

INTF_FRAME_SIZE (2:0)			INTF_SIZE (1:0)		INTERFACE FRAME SIZE, BCLK/WCLK
0	0	0	0	0	2 x 16 x F_S
0	0	1	0	1	2 x 20 x F_S
0	1	0	1	0	2 x 24 x F_S
0	1	1	1	1	2 x 32 x F_S
1	0	0	0	0	4 x 16 x F_S
1	0	1	0	1	4 x 20 x F_S
1	1	0	1	0	4 x 24 x F_S
1	1	1	1	1	4 x 32 x F_S

Table 6. Audio Sampling Rate Setting Register

CLK_MODE(3:0)				INTERFACE SAMPLING RATE, WCLK (kHz)
0	0	0	0	8
0	0	0	1	11.025
0	0	1	0	12
0	0	1	1	NA
0	1	0	0	16
0	1	0	1	22.05
0	1	1	0	24
0	1	1	1	NA
1	0	0	0	32
1	0	0	1	44.1
1	0	1	0	48
1	0	1	1	NA
1	1	0	0	NA

Table 7. Detailed Configuration of Interface Including PLL Setup Registers

BCLK/WCLK	DATA SIZE	F_S (WCLK)	F_S x DATA	BCLK/PLL INPUT
32	16	48.000	1536	1536
40	20	48.000	1920	1920
48	24	48.000	2304	2304
64	32	48.000	3072	3072

Table 7. Detailed Configuration of Interface Including PLL Setup Registers (continued)

BCLK/WCLK	DATA SIZE	F_S (WCLK)	F_S x DATA	BCLK/PLL INPUT
32	16	44.100	1411.2	1411.2
40	20	44.100	1764	1764
48	24	44.100	2116.8	2116.8
64	32	44.100	2822.4	2822.4
64	16	8.000	256	512
64	16	11.025	352.8	705.6
64	16	12.000	384	768
64	16	16.000	512	1024
64	16	22.050	705.6	1411.2
64	16	24.000	768	1536
64	16	32.000	1024	2048
64	16	44.100	1411.2	2822.4
64	16	48.000	1536	3072
80	20	8.000	320	640
80	20	11.025	441	882
80	20	12.000	480	960
80	20	16.000	640	1280
80	20	22.050	882	1764
80	20	24.000	960	1920
80	20	32.000	1280	2560
80	20	44.100	1764	3528
80	20	48.000	1920	3840
96	24	8.000	384	768
96	24	11.025	529.2	1058.4
96	24	12.000	576	1152
96	24	16.000	768	1536
96	24	22.050	1058.4	2116.8
96	24	24.000	1152	2304
96	24	32.000	1536	3072
96	24	44.100	2116.8	4233.6
96	24	48.000	2304	4608
128	32	8.000	512	1024
128	32	11.025	705.6	1411.2
128	32	12.000	768	1536
128	32	16.000	1024	2048
128	32	22.050	1411.2	2822.4
128	32	24.000	1536	3072
128	32	32.000	2048	4096
128	32	44.100	2822.4	5644.8
128	32	48.000	3072	6144

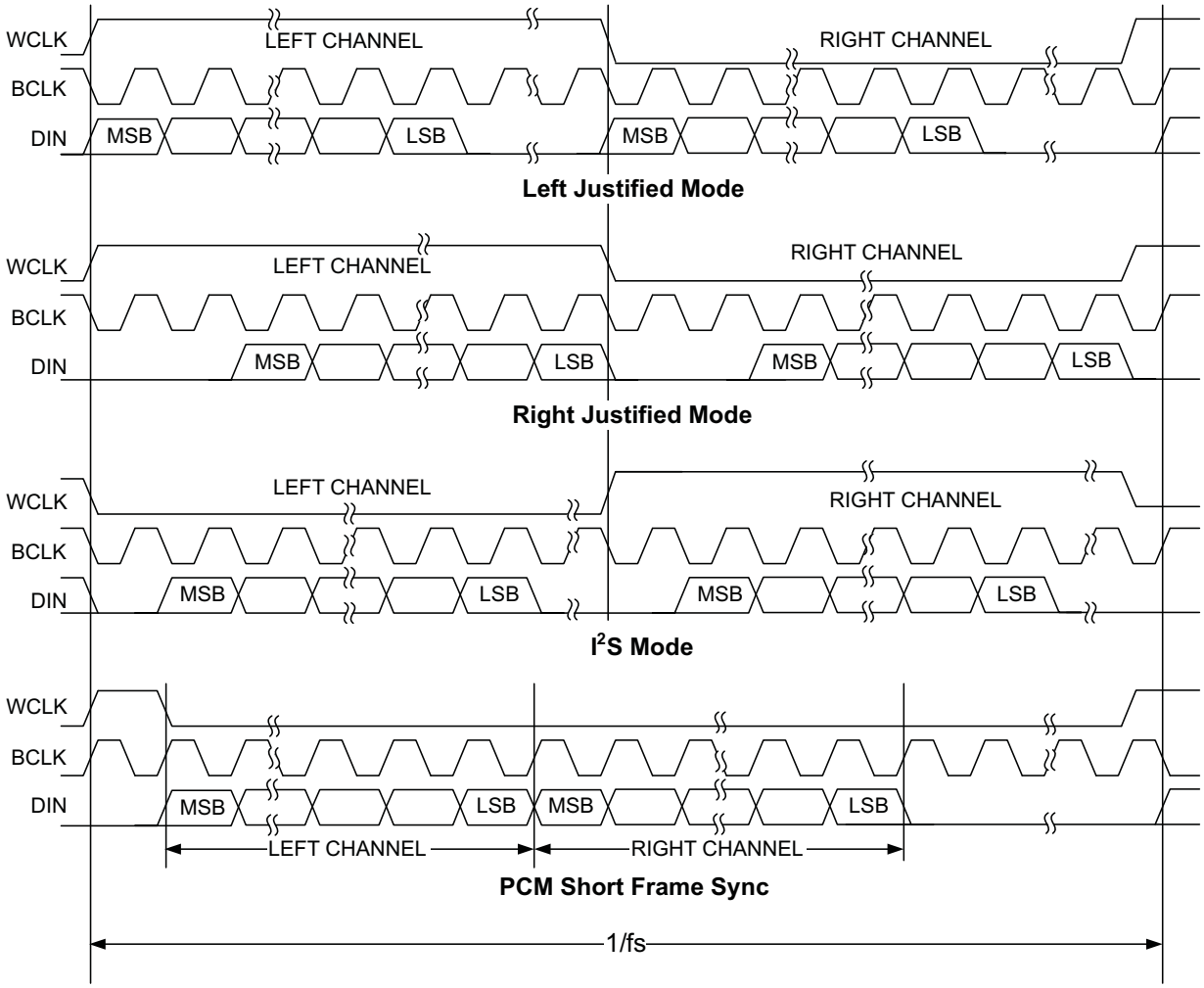


Figure 9. Interface Format Supporting Four Different Options

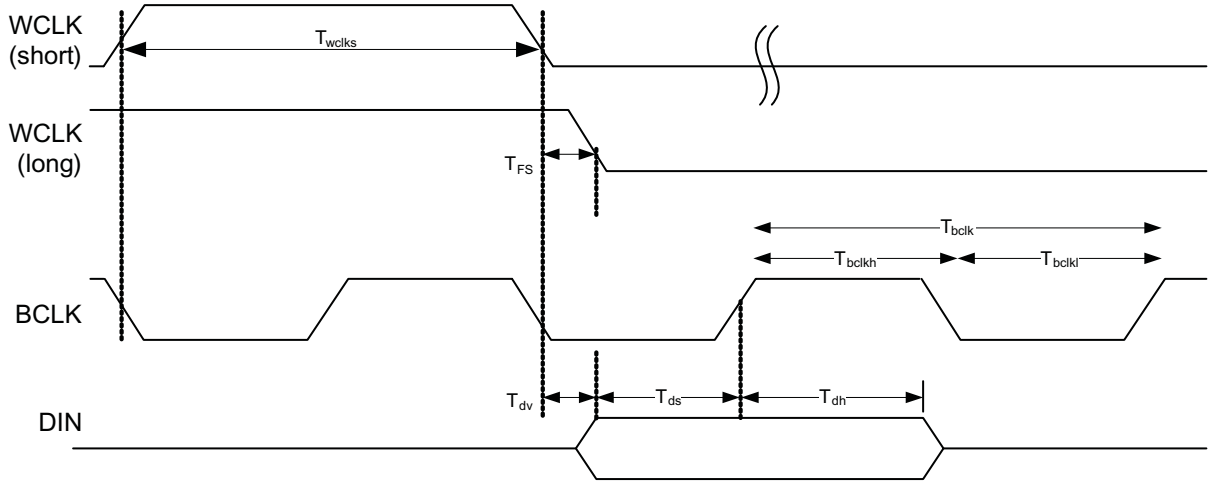


Figure 10. Interface Timing for I²S (Long) or PCM (Short) WCLK Options

AUDIO

Channel Performance

The receive channel of TLV320DAC3202 converts the digital signal to analog for the headset amplifier through a highly efficient low-power DAC. The signal in stereo I^2S format with configurable data size drives the Class G amplifier after the conversion. The channel gain is implemented in two segments in digital and analog domains. In digital domain the gain steps have finer resolution whereas in the analog domain the amplifier gain steps are defined at 2-dB resolution. The detail of volume control is shown in the register map description. The mixing feature allows the left and right channels to be combined in digital domain prior to conversion and then routed to either channel. The audio signal can be disabled either by soft mute feature in the digital domain or by disabling the output amplifier.

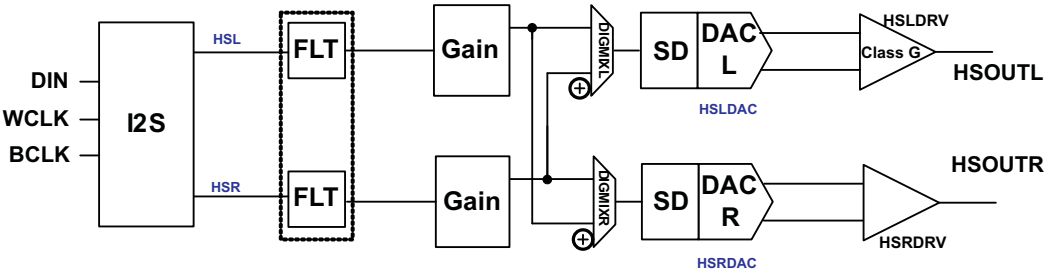


Figure 11. Audio Path Diagram

Volume Control

The volume control module is implemented with combination of digital and analog gain settings for optimum performance. The total gain range is from 4 dB to -59 dB with variable steps. The gain for the amplifiers is from 4 dB to -12 dB in 2-dB steps.

Table 8. Volume Control Register Decoding

REGISTER VALUE	GAIN (dB)	GAIN_ANALOG (dB)	GAIN_DIGITAL (dB)
31	4	4	0
30	3	4	-1
29	2	2	0
28	1	2	-1
27	0	0	0
26	-1	0	-1
25	-2	-2	0
24	-3	-2	-1
23	-4	-4	0
22	-5	-4	-1
21	-6	-6	0
20	-7	-6	-1
19	-8	-8	0
18	-9	-8	-1
17	-10	-10	0
16	-11	-10	-1
15	-13	-12	-1
14	-15	-12	-3
13	-17	-12	-5
12	-19	-12	-7
11	-21	-12	-9

Table 8. Volume Control Register Decoding (continued)

REGISTER VALUE	GAIN (dB)	GAIN_ANALOG (dB)	GAIN_DIGITAL (dB)
10	-23	-12	-11
9	-25	-12	-13
8	-27	-12	-15
7	-31	-12	-19
6	-35	-12	-23
5	-39	-12	-27
4	-43	-12	-31
3	-47	-12	-35
2	-51	-12	-39
1	-55	-12	-43
0	-59	-12	-47

SYSTEM AND CONTROL

Power-Up Sequence

The power up sequence of the IC is initiated by asserting the CHIP_EN bit to logic '1'. It is expected that V_{BAT} and V_{IO} are powered up prior to assertion of this bit. The HSL/R amplifiers are then enabled by writing to their perspective control bits in register address 0x01. The I^2S clock must be present prior to power up sequence and maintain its activity during active mode. The figure below shows the typical power up sequence of the IC. The IC power up state machine updates I^2C register bits corresponding to enabled modules. I^2C register control can subsequently be used to turn OFF unused circuits.

The power down sequence is initiated by de-asserting the CHIP_EN bit in CODEC_EN register. It is expected that the CHIP_EN bit is de-asserted prior to turning OFF the V_{IO} supply.

The HS driver power on/off sequence is designed to be click-pop free.

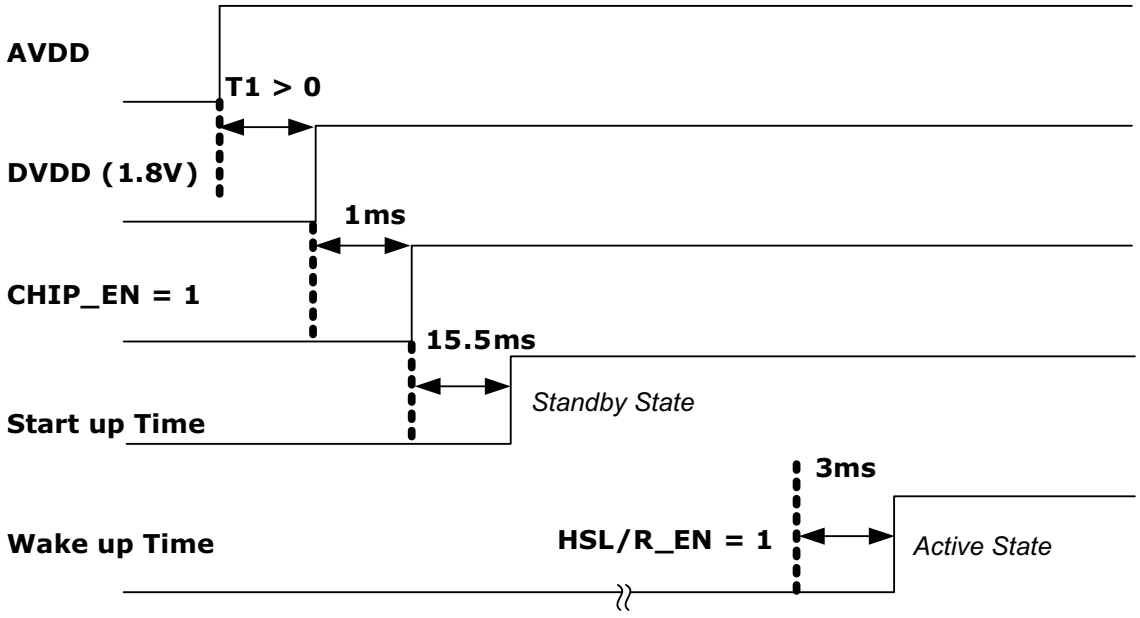


Figure 12. Power-Up Sequence Timing

Dual Supply Charge Pump

The charge pump on TLV320DAC3202 has dual-supply capability module with automatic selection which can be either from V_{BAT} or V_{IO} depending on the input signal range and load current that is detected. Charge pump generates both the positive and negative rails for low and high headset rails. For typical listening range where the signal level is low, the supply is expected to be from V_{IO} and headset rail is 0.9 V. For higher signal levels where higher current drains from V_{IO} are not possible, the IC uses an automatic input voltage and load current threshold based algorithm to switch ON the V_{POW} regulator and use V_{POW}, which is powered from V_{BAT}. It is designed to power the left and right headset drivers up to rated full scale output.

The threshold point to transition between the low and high power range can be programmed through I^2C interface. There are two threshold points controlled by register bits, one for each of left and right channels. The threshold monitor mechanisms for each channel can be independently enabled and programmed. The load current threshold settings can be 10.5 mA, 11.5 mA, 12.5 mA (default) or 13.5 mA per channel.

Output Impedance

In order to share the output connector between audio and other signals such as video output, a high impedance option is implemented that can be enabled through I^2C controller. In this mode the output impedance is increased while the signal is muted. As shown in below table the output impedance is large enough to avoid an unwanted attenuation of other signal connected to the jack contact.

Table 9. Output Impedance in Various Mode Settings

CHIP_EN	HiZ	HS_EN	IMPEDANCE	MODE
0	0	0	150 Ω	Shut down
0	0	1	150 Ω	Shut down
0	1	0	8.5 Ω at 40 kHz	HiZ
			600 Ω at 6 MHz	
			400 Ω at 13 MHz	
0	1	1	-	Invalid
1	0	0	150 Ω	Active, HS off
1	0	1	-	Active
1	1	0	-	Invalid
1	1	1	-	Invalid

I^2C INTERFACE

The control interface for programming the registers on TLV320DAC3202 is done using a standard I^2C interface with the IC operating in slave mode. The 2 modes of operation as defined in Ref [1,2] are (a) Standard-mode up to 100 kbit/s, and (b) Fast-mode up to 400 kbit/s. The IC defaults to fast-mode. A 7-bit slave addressing is used. The device I^2C slave address is fixed to 0011010X, with 00110100 for master write cycle (TLV320DAC3202 reads) and 00110101 for master read cycle (TLV320DAC3202 writes). For data and clock lines, pull up resistors are required and are expected to be provided as defined in section 7 of Ref [1].

References

[1] UM10204: I^2C-Bus Specification and user manual Rev. 03 – 19 June 2007

[2] The I^2C-BUS SPECIFICATION VER 2.1 January 2000

[3] I^2S Bus specification, Phillips Semiconductors, June 1996

Register Map

Table 10. Register Map Designation for I²C Interface

ADDRESS	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	INITIAL VALUE	ACCESS (R, W, WR)
0x00											
0x01	EN	HSL_EN	HSR_EN	-	-	-	-	THERMAL	CHIP_EN	0x00	R
0x02	VOL_CTRL	HSL_MUTE	HSR_MUTE	VOLCTRL(4:0)					-	0xC0	WR
0x03	HIZ_CTRL	-	-	SPARE	SPARE	-	-	HIZ_L	HIZ_R	0x00	WR
0x04	ASICREV	ASICID(3:0)				VERSION(3:0)				0x00	R
0x05	I2CID	I2CID(7:0)								0x34	R
0x06	HS_LP2HP _SW1	HS_LP_MODE	HS_BYPASS _CUR_SW	-	-	HSL_CUR_THRD(1:0)		HSR_CUR_THRD(1:0)		0x00	WR
0x07	CODEC_EN	HSL_DRV_EN	HSR_DRV_EN	CP_EN	PLL_EN	REF_EN	-	DACL_EN	DACR_EN	0x00	W
0x08	CODEC_CTRL	HSL_FIR_EN	HSR_FIR_EN	HSL_RAMP _DIS	HSR_RAMP _DIS	HSL_MIX_CTRL(1:0)		HSR_MIX_CTRL(1:0)		0x00	WR
0x09	INTF	INTF_MODE(1:0)		INTF_DATA_SIZE(1:0)		-	INTF_FRAME_SIZE(2:0)			0x00	WR
0x0A	FIR	CLK_MODE(3:0)				-	-	INTERPOLATION(1:0)		0xA3	WR
0x0B	CP	CP_OPEN	CP_HPMODE	CP_ENCLAMP	CP_FET_SIZE(2:0)			-	-	0x00	WR
0x0C	REF	-	-	REF_CM_HIGH_SWING(1:0)		REF_CUR(3:0)				0x00	WR
0x0D	DAC	DAC_INV_CLK	OFFSET _CORR_EN	-	-	DACR_SWING	DACL_SWING	DACR_LP	DACL_LP	0x00	WR
0x0E	HS_LP2HP _SW2	HP_LOW _IBIAS	HS_BYPASS _SHTDN	HS_SW_OVER_SPEED(1:0)		HS_AMP_SW_OVER(1:0)		HS_HIGHAMP_SW_OVER(1:0)		0x80	WR
0x11	PM_EN	REFSYS_EN	-	SPARE_W	VANA_EN	-	VPOW_EN	-	-	0x00	W
0x12	PM_LDO	-	-	VPOW_OUT(1:0)		-	-	VANA_OUT(1:0)		0x00	WR
0x18	UNLOCK_PM	-	-	-	-	-	-	-	UNLOCK_PM	0x00	WR
0x19	PM_TEST1	TEST_REFSYS _SET_BG	EEPROM _BYPASS	SPARE	TEST_VANA _HIZ	-	TEST_VPOW _HIZ	EEPROM _PROGRAM	DIEID _PROGRAM	0X00	WR
0x1A	HS_TEST	SPARE	SPARE	TEST_HSL _TM1	TEST_HSL _OCDIS	TEST_DC2DAC	TEST_ISUM _DETECT	TEST_HSR _TM1	TEST_HSR _OCDIS	0x00	WR
0x1B	CODEC_TEST1	CODEC_TEST_MUX(3:0)				TEST_BYP_FIR	TEST_CP_CLK(2:0)			0x00	WR
0x1C	CODEC_TEST2	TEST_BYP _MOD	TEST_BYP _RANDOMIZER	TEST_PLL_ OVERRIDE_EN	PLL_PRE_DIV_OVR(4:0)					0x00	WR
0x1D	CODEC_TEST3	SPARE	PLL_FB_LOOP_OVR(6:0)							0x00	WR
0x1E	CODEC_TEST4	CP_TEST(1:0)		PLL_TEST_MODE_L(5:0)						0x30	WR
0x1F	CODEC_TEST5	PLL_TEST_MODE_H(7:0)								0x00	WR

PCB DEVELOPMENT

The following table explains the PCB recommendations. In addition, it is recommended to split the ground plane into analog and digital segment for clean and noisy signals. They should be connected only in a single point to avoid ground loop.

Table 11. PCB Recommendations

BALL NAME	DESCRIPTION	LAYOUT RECOMMENDATIONS
AVSS	Analog ground	
VANAG	Connected to VANA via capacitor	Connect to output capacitor with < 10 mΩ.
VANA	Analog LDO output	Connect to output capacitor with < 10 mΩ.
DVDD	IO/Digital supply	Minimize the resistance path with adequate decoupling very close to the ball.
CFLYP	FLY capacitor "+" terminal	Connect to positive side of output capacitor with < 10 mΩ.
VREF	Analog reference output	Connect to AVSS via output capacitor. The capacitor trace on the AVSS side of the capacitor should not be connected to GND plane directly but at the AVSS pin. See application diagram.
AVDD	2.3-V to 4.8-V battery input	Minimize the resistance path with adequate decoupling very close to the ball.
VPOW	CP LDO output	Minimize the resistance path with adequate decoupling very close to the ball.
DVSS	Digital ground	Connect to separate GND plane for noisy signals, i.e. PLL and interfaces. Connect the two planes in a single point to avoid GND loop.
CFLYN	FLY capacitor "-" terminal	Connect to negative side of output capacitor with < 10 mΩ.
SDA	I^2C data	Keep this away from clean quite signal paths over the digital GND plane.
SCL	I^2C CLK in	Keep this away from clean quite signal paths over the digital GND plane.
HSOUTG	HS feedback ground	Trace impedance must be very small, < 60 mΩ. This is important for cross talk reduction. Connection to GND plane must be at IC ball.
HSVDD	HS positive supply	Decouple this path to DVSS with trace impedance of < 20 mΩ.
HSOUTL	HS output left	Must be routed in differential pair with GNDHS to the connector. Match the impedances and as small as possible.
DIN	I^2S downlink data	Keep this trace away from quite GND/signal traces.
WCLK	I^2S word clock	Keep this trace away from quite GND/signal traces.
BCLK	I^2S bit clock	Keep this trace away from quite GND/signal traces.
HROUTR	HS output right	Must be routed in differential pair with GNDHS to the connector. Match the impedances and as small as possible.
HSVSS	HS negative supply	Decouple this path to DVSS with trace impedance of < 20 mΩ.

TYPICAL CIRCUIT CONFIGURATION

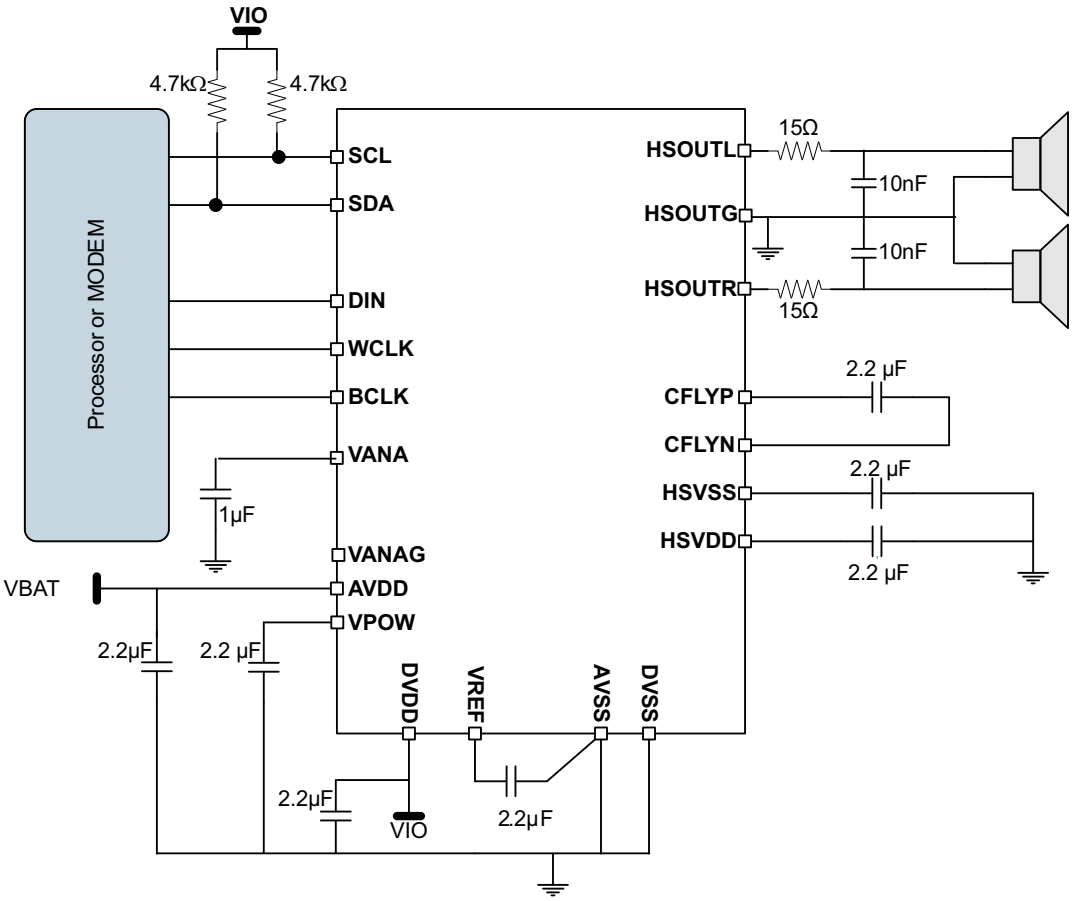


Figure 13. Typical Circuit

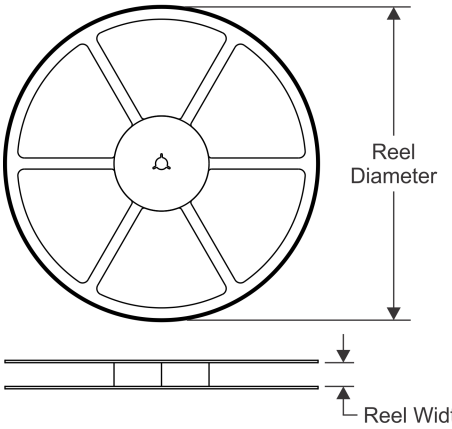
Table 12. External Component List(1)

PIN NAME	DESCRIPTION
AVDD	2.2 µF, 6.3-V tolerance
VPOW	2.2 µF, 6.3-V tolerance
VREF	2.2 µF, 6.3-V tolerance
VANA	1 µF, 6.3-V tolerance
HSVDD	2.2 µF, 6.3-V tolerance
HSVSS	2.2 µF, 6.3-V tolerance
CFLYP/N	2.2 µF, 6.3-V tolerance
DVDD	2.2 µF, 6.3-V tolerance

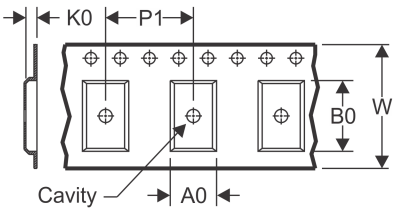
(1) The headset amplifiers output power and distortion are characterized using the nominal capacitance for the supply, ground, output loads, and the charge pump fly cap as shown in the above application diagram. To meet the stated performance with discrete component variations, it is recommended that the external components be chosen to account for manufacturing tolerance, voltage and temperature de-rating.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

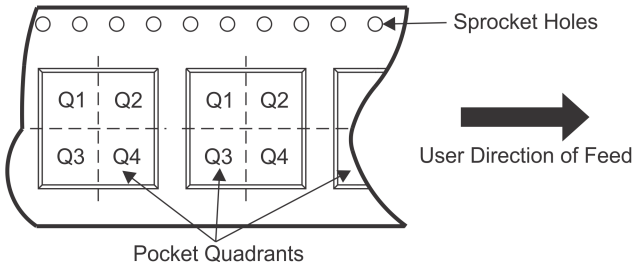


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

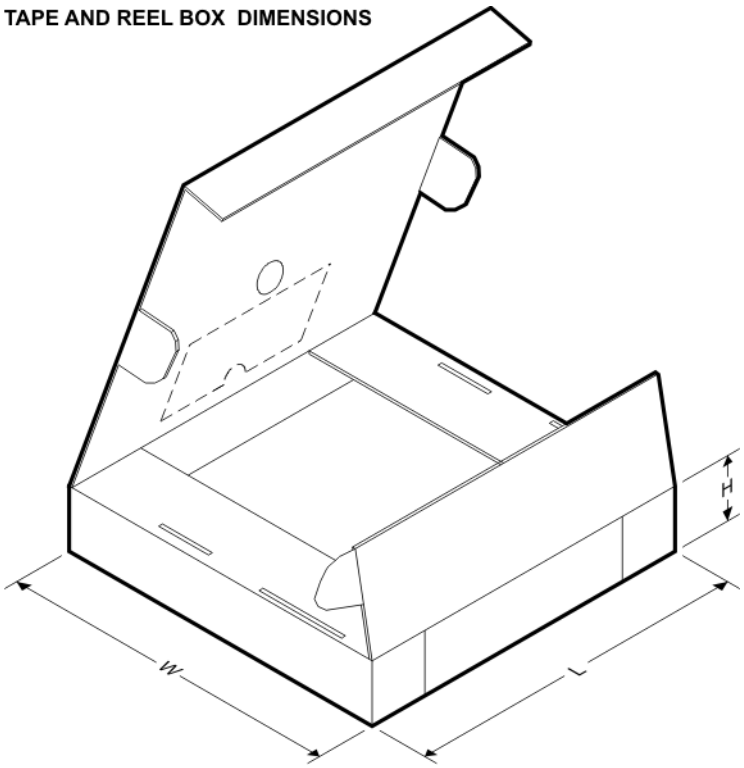
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV320DAC3202CYZJR	DSBGA	YZJ	20	3000	180.0	8.4	2.09	2.59	0.78	4.0	8.0	Q2

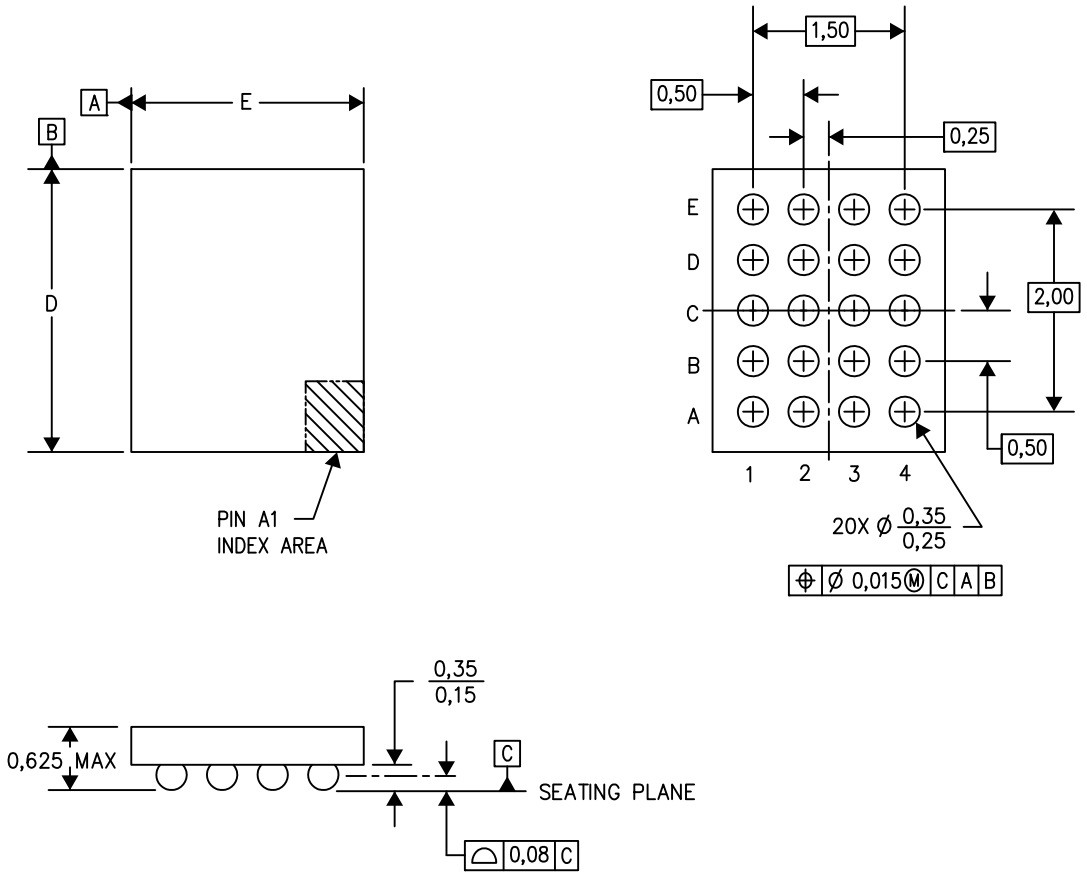
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV320DAC3202CYZJR	DSBGA	YZJ	20	3000	182.0	182.0	20.0

YZJ (R–XBGA–N20) DIE–SIZE BALL GRID ARRAY



4205061/E 07/13

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

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