8-bit serial-in/serial or parallel-out shift register with output latches; 3-state

Description：

74HC595 is a high-speed silicon gate CMOS device with pins compatible with low-power Schottky TTL circuits (LSTTL). It complies with JEDEC standard No.7A. It consists of eight serial shift registers with storage registers and three state outputs. The shift register and storage register have separate clocks. Data in shift clock SH_ When the rising edge of CP arrives, shift transmission is performed, while the storage clock ST_
When the rising edge of CP arrives, it is transferred from the shift register to the storage register. If two clocks are connected together, the data on the shift register is always one clock pulse ahead of the storage register. The shift register has a serial input (DS) and a cascaded serial output (Q7 '), as well as an asynchronous reset (effective at low levels).

The storage register has an eight bit parallel bus driver output with a three state output. When the output enable end (OE) is at low level, the output end is normal output. Conversely, when OE is at high level, the output is in high resistance off state.

Features：

-Eight bit serial input

-Eight bit serial or parallel output

-Shift output frequency ESD protection function at 100MHz (typical value)

-A storage register with a three state output and a shift register with direct zeroing

Application：

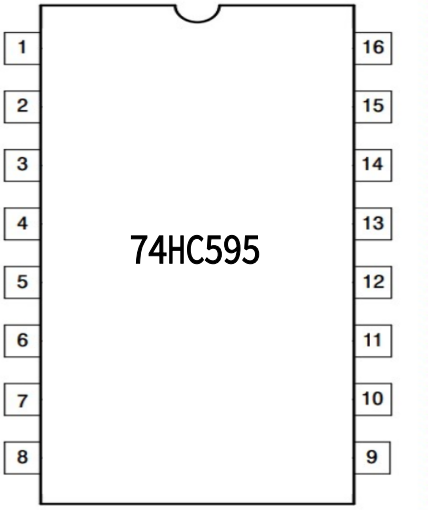
-serial parallel conversion

-Remote control memory retention device

Absolute Maximum Ratings

parameter	symbol	Test conditions	min	max	unit
supply voltage	Vcc		-0.5	7	V
Input diode current	IIK	VI<-0.5V or VI>Vcc+0.5V	-	±20	mA
Output diode current	loK	Vo<-0.5V or Vo>Vcc+0.5V	-	±20	mA
Output pouring current or pulling current	lo	-0.5V<Vo<Vcc+0.5V	-		
		Q' standard output	-	±25	mA
		Q0~Q7 bus drive output	-	±35	mA
Vcc, GND current	Icc, IGND		-	±70	mA
storage temperature	Tstg		-65	150	℃
consumption	Ptot	Tamb=-40 to 125℃	-	500	mW

Pin Assignment：



DIP/SOP16

pin no.	symbol	function description
1	Q1	Parallel output terminal
2	Q2	Parallel output terminal
3	Q3	Parallel output terminal
4	Q4	Parallel output terminal
5	Q5	Parallel output terminal
6	Q6	Parallel output terminal
7	Q7	Parallel output terminal
8	GND	grounding(0V)
9	Q7'	Serial output terminal
10	$\overline{MR}$	Main reset (effective at low level)
11	SH_CP	Shift register clock input
12	ST_CP	Memory register clock input terminal
13	$\overline{OE}$	Output enabling terminal(effective at low level)
14	DS	Serial input terminal
15	Q0	Parallel output terminal
16	Vcc	power supply

menubar

input					output		function
SH_CP	ST_CP	$\overline{OE}$	$\overline{MR}$	DS	Q7'	Qn	
×	×	L	L	×	L	n.c	MR only resets the shift register when the power level is low
×	↑	L	L	×	L	L	Shift register transfers null values to storage registers
×	×	H	L	×	L	Z	Clear the shift register to zero; Parallel output in
↑	×	L	H	H	Q6'	n.c	The logic high level is transmitted from the input to the shift register of segment 0; The data of all shift registers is sequentially transmitted under the action of the shift clock
×	↑	L	H	×	n.C,	Qn'	All shift register data is transmitted to the corresponding storage registers under the action of the storage clock
↑	↑	L	H	×	Q6'	Qn'	The shift register is sequentially passed back; Simultaneously shifting the register to transfer the previous state to the corresponding storage register and output

Note: H=high level L=low level ↓ falling edge ↑ rising edge
Z=high resistance closed state n.c.=no change
X=irrelevant quantity

function diagram

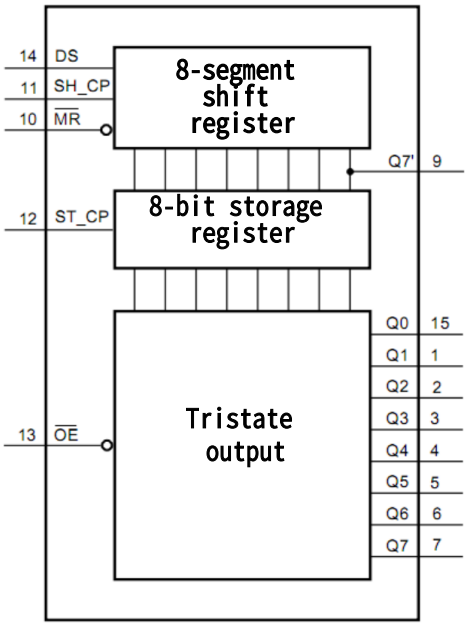


Figure 3 Functional Diagram

logic diagram

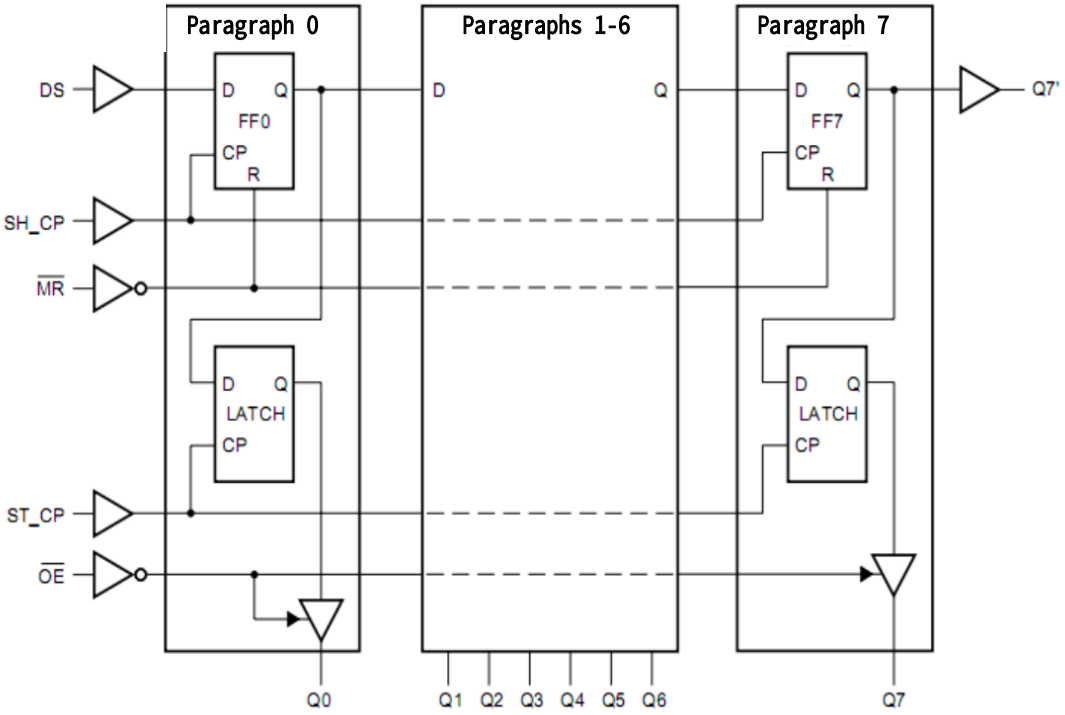


Figure 4 Logic Diagram

Timing Diagram

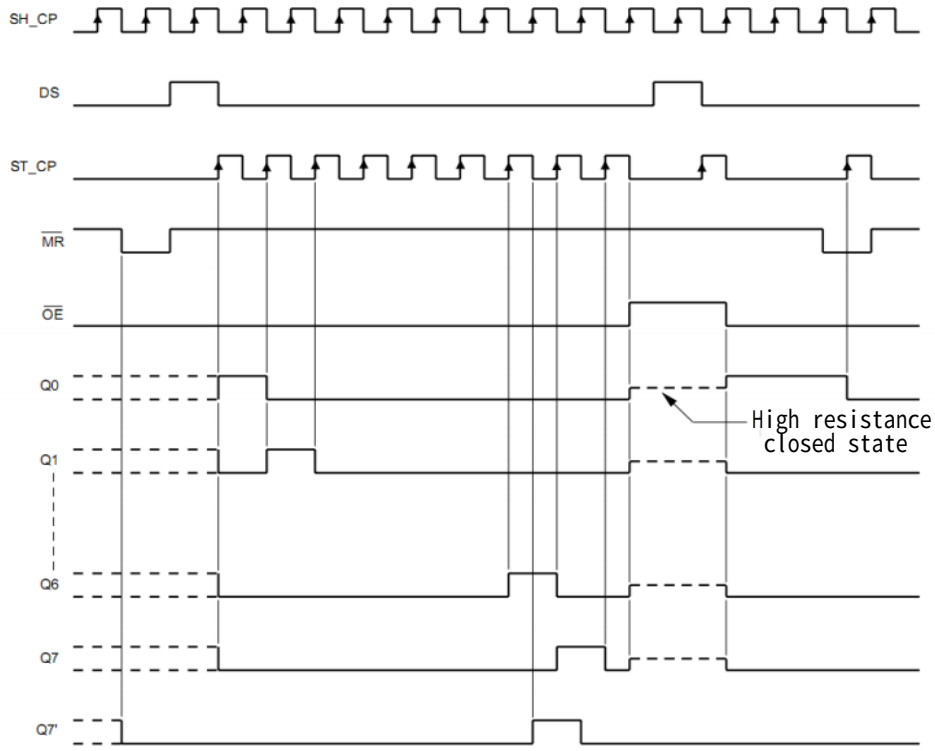


Figure 5 Timing Chart

DC parameters (ambient temperature: -40~+125 °C; all typical values are tested at 25 °C)

parameter	symbol	Test conditions		min	typ	max	unit
		condition	Vcc(V)				
High Level Input Voltage	VIH		2	1.5	1.2	-	V
			4.5	3.15	2.4	-	V
			6	4.2	3.2	-	V
low level input voltage	VIL		2	-	0.8	0.5	V
			4.5	-	2.1	1.35	V
			6	-	2.8	1.8	V
high level output voltage	VOH	VI=VIH or VIL					
		All outputs Io=-20uA	2	1.9	2	-	V
			4.5	4.4	4.5	-	V
			6	5.9	6	-	V
		Q7' Standard output terminal Io=-4.0mA	4.5	3.84	4.32	-	V
		Io=-5.2mA	6	5.34	5.81	-	V
		Qn bus drive output Io=-6.0mA	4.5	3.84	4.32	-	V
		Io=-7.8mA	6	5.34	5.81	-	V
Low Level Output Voltage	VOL	VI=VIH or VIL					
		All outputs Io=-20uA	2	-	0	0.1	
			4.5	-	0	0.1	
			6	-	0	0.1	V
		output terminal Io=-4.0mA	4.5	-	0.15	0.33	
		Io=-5.2mA	6	-	0.16	0.33	V
		output Io=-6.0mA	4.5	-	0.16	0.33	
		Io=-7.8mA	6	-	0.16	0.33	V
Input peak current	IL	VI=Vcc or GND	6	-	-	±1	uA
Three state output high resistance current	Ioz	VI=VIH or VIL Vo=Vcc or GND	6	-	-	±5	uA
Static power supply current	Icc	VI=Vcc or GND Io=0	6	-	-	80	uA

ambient temperature:-40 ~+125 ℃

parameter	symbol	Test conditions		min	typ	max	unit
		condition	Vcc(V)				
High Level Input Voltage	VIH		2	1.5	-	-	V
			4.5	3.15	-	-	V
			6	4.2	-	-	V
low level input voltage	VIL		2	-	-	0.5	V
			4.5	-	-	1.35	V
			6	-	-	1.8	V
high level output voltage	VOH	VI=VIH or VIL					
		ALL outputs Io=-20uA	2	1.9	-	-	V
			4.5	4.4	-	-	V
			6	5.9	-	-	V
		Q7'Standard output terminal Io=-4.0mA	4.5	3.7	-	-	V
		Io=-5.2mA	6	5.2	-	-	V
		Qn bus drive output Io=-6.0mA	4.5	3.7	-	-	V
		Io=-7.8mA	6	5.2	-	-	V
Low Level Output Voltage	VOL	VI=VIH or VIL					
		ALL outputs Io=-20uA	4.5	-	-	0.1	V
		Q7'Standard output terminal Io=-4.0mA	4.5	-	-	0.4	V
		Qn bus drive output Io=-6.0mA	4.5	-	-	0.4	V
Input peak current	ILI	VI=Vcc or GND	5.5	-	-	±1	uA
Three state output high resistance current	Ioz	VI=VIH or VIL Vo=Vcc or GND	5.5	-	-	±10	uA
Static power supply current	Icc	VI=Vcc or GND Io=0	5.5	-	-	160	uA

AC parameters (GND=0V; tr-tf-6ns ; CL=50Pf)

ambient temperature：25℃

parameter	symbol	Test conditions		min	typ	max	unit
		wave form	Vcc(V)				
Transmission delay time from SH_CP to Q7'	tPHL/tPLH	See Figure 6	2	-	52	160	ns
			4.5	-	19	32	ns
			6	-	15	27	ns
ST_CP to Qn transmission delay time		See Figure 7	2	-	55	175	ns
			4.5	-	20	35	ns
			6	-	16	30	ns
Transmission delay time from MR to Q7'	tPHL	See Figure 9	2	-	47	175	ns
			4.5	-	17	35	ns
			6	-	14	30	ns
OE causes Qn terminal to transition from high resistance state to enable output time	tPZH/tPZL	See Figure 10	2	-	47	30	ns
			4.5	-	17	150	ns
			6	-	14	30	ns
OE enables the Qn terminal to output from enable to high resistance state time	tPHZ/tPLZ	See Figure 10	2	-	41	26	ns
			4.5	-	15	150	ns
			6	-	12	30	ns
Shift clock pulse width (high or low level)	tW	See Figure 6	2	75	17	26	ns
			4.5	15	6	-	ns
			6	13	5	-	ns
Store clock pulse width (high or low level)		See Figure 7	2	75	11	-	ns
			4.5	15	4	-	ns
			6	13	3	-	ns
Main reset pulse width (low level)		See Figure 9	2	75	17	-	ns
			4.5	15	6	-	ns
			6	13	5	-	ns
Establishment time from DS to SH_CP	tsu	See Figure 8	2	50	11	-	ns
			4.5	10	4	-	ns
			6	9	3	-	ns
Establishment time from SH_CP to ST_CP		See Figure 7	2	75	22	-	ns
			4.5	15	8	-	ns
			6	13	7	-	ns
DS to SH_CP retention time	th	See Figure 8	2	3	-6	-	ns
			4.5	3	-2	-	ns
			6	3	-2	-	ns
MR enables SH CP reset time	trem	See Figure 9	2	50	-19	-	ns
			4.5	10	-7	-	ns
			6	9	-6	-	ns
Minimum clock pulse width of SH_CP or ST_CP	fmax	See Figure 6,7	2	9	30	-	MHZ
			4.5	30	91	-	MHZ
			6	35	108	-	MHZ

ambient temperature：-40℃~85℃

parameter	symbol	Test conditions		min	typ	max	unit
		wave form	Vcc(V)				
Transmission delay time from SH_CP to Q7'	tPHL/tPLH	See Figure 6	2	-	-	200	ns
			4.5	-	-	40	ns
			6	-	-	34	ns
ST_ CP to Qn transmission delay time		See Figure 7	2	-	-	220	ns
			4.5	-	-	44	ns
			6	-	-	37	ns
Transmission delay time from MR to Q7'	tPHL	See Figure 9	2	-	-	220	ns
			4.5	-	-	44	ns
			6	-	-	37	ns
OE causes Qn terminal to transition from high resistance state to enable	tPZH/tPZL	See Figure 10	2	-	-	190	ns
			4.5	-	-	38	ns
			6	-	-	33	ns
OE enables the Qn terminal to output from enable to high resistance	tPHZ/tPLZ	See Figure 10	2	-	-	190	ns
			4.5	-	-	38	ns
			6	-	-	33	ns
Shift clock pulse width (high or low level)	tW	See Figure 6	2	95	-	-	ns
			4.5	19	-	-	ns
			6	16	-	-	ns
Store clock pulse width (high or low level)		See Figure 7	2	95	-	-	ns
			4.5	19	-	-	ns
			6	16	-	-	ns
Main reset pulse width (low level)		See Figure 9	2	95	-	-	ns
			4.5	19	-	-	ns
			6	16	-	-	ns
Establishment time from DS to SH_ CP	tsu	See Figure 8	2	65	-	-	ns
			4.5	13	-	-	ns
			6	11	-	-	ns
Establishment time from SH_ CP to ST_ CP		See Figure 7	2	95	-	-	ns
			4.5	19	-	-	ns
			6	16	-	-	ns
DS to SH_ CP retention time	th	See Figure 8	2	3	-	-	ns
			4.5	3	-	-	ns
			6	3	-	-	ns
MR enables SH_ CP reset time	trem	See Figure 9	2	65	-	-	ns
			4.5	13	-	-	ns
			6	11	-	-	ns
Minimum clock pulse width of SH_ CP or ST_ CP	fmax	See Figure 6,7	2	4.8	-	-	MHZ
			4.5	24	-	-	MHZ
			6	28	-	-	MHZ

ambient temperature：-40℃~125℃

parameter	symbol	Test conditions		min	typ	max	unit
		wave form	Vcc(V)				
Transmission delay time from SH_ CP to Q7'	tPHL/tPLH	See Figure 6	2	-	-	240	ns
			4.5	-	-	48	ns
			6	-	-	41	ns
ST_ CP to Qn transmission delay time		See Figure 7	2	-	-	265	ns
			45	-	-	53	ns
			6	-	-	45	ns
Transmission delay time from MR to Q7'	tPHL	See Figure 9	2	-	-	265	ns
			4.5	-	-	53	ns
			6	-	-	45	ns
OE causes Qn terminal to transition from high resistance state to enable	tPZH/tPZL	See Figure 10	2	-	-	225	ns
			4.5	-	-	45	ns
			6	-	-	35	ns
OE enables the Qn terminal to output from enable to high resistance	tPHZ/tPLZ	See Figure 10	2	-	-	225	ns
			4.5	-	-	45	ns
			6	-	-	35	ns
Shift clock pulse width (high or low level)	tW	See Figure 6	2	110	-	-	ns
			4.5	22	-	-	ns
			6	19	-	-	ns
Store clock pulse width (high or low level)		See Figure 7	2	110	-	-	ns
			4.5	22	-	-	ns
			6	19	-	-	ns
Main reset pulse width (low level)		See Figure 9	2	110	-	-	ns
			4.5	22	-	-	ns
			6	19	-	-	ns
Establishment time from DS to SH_ CP	tsu	See Figure 8	2	75	-	-	ns
			4.5	15	-	-	ns
			6	13	-	-	ns
Establishment time from SH_ CP to ST_ CP		See Figure 7	2	110	-	-	ns
			4.5	22	-	-	ns
			6	19	-	-	ns
DS to SH_ CP retention time	th	See Figure 8	2	3	-	-	ns
			4.5	3	-	-	ns
			6	3	-	-	ns
MR enables SH_ CP reset time	trem	See Figure 9	2	75	-	-	ns
			4.5	15	-	-	ns
			6	13	-	-	ns
Minimum clock pulse width of SH_ CP or ST _ CP	fmax	See Figure 6,7	2	4	-	-	MHZ
			4.5	20	-	-	MHZ
			6	24	-	-	MHZ

AC waveform

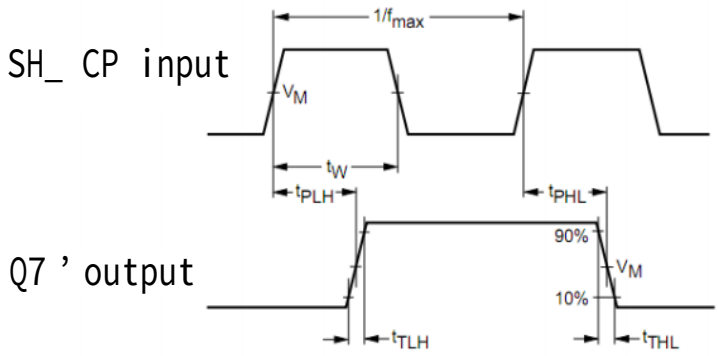


Figure 6: The above figure shows the transmission delay time, shift clock pulse width, and maximum shift clock frequency
from shift clock (SH_CP) to output (Q7 ')

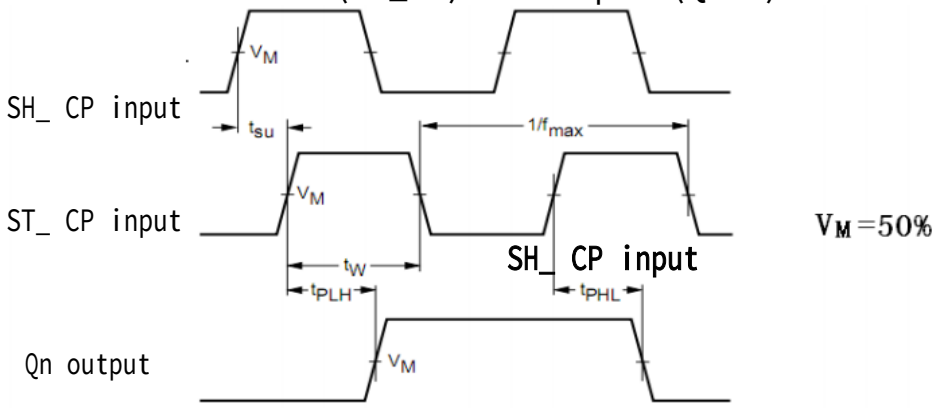


Figure 7: The above figure shows the transmission delay time from storage clock (ST_CP) to output (Qn), storage clock pulse width, and establishment time from shift clock to storage clock

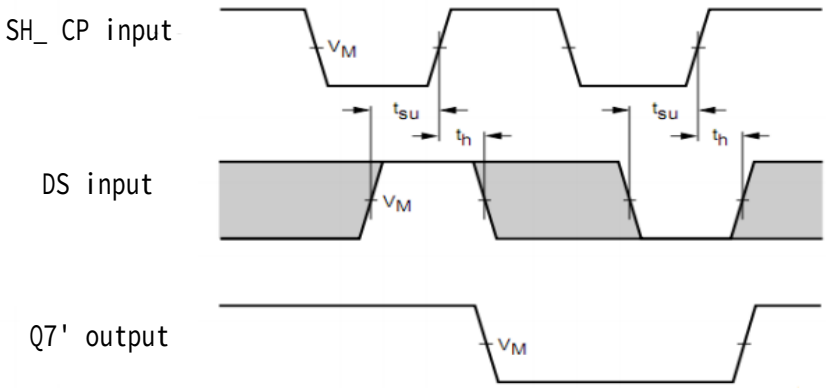


Figure 8: The above figure shows the establishment and retention time of DS input
Note: The shaded portion indicates that the input signal has no effect on the output at this time

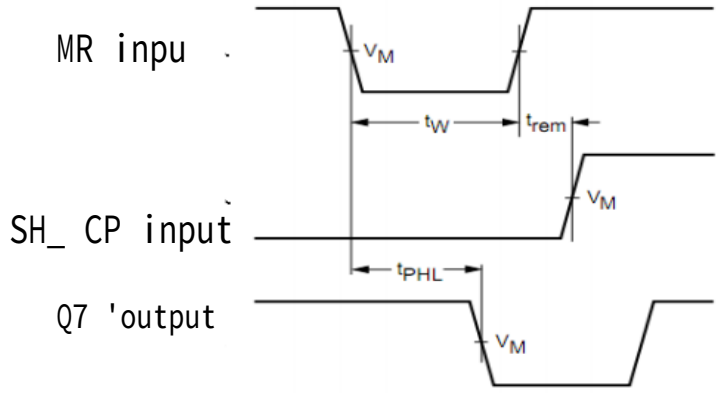
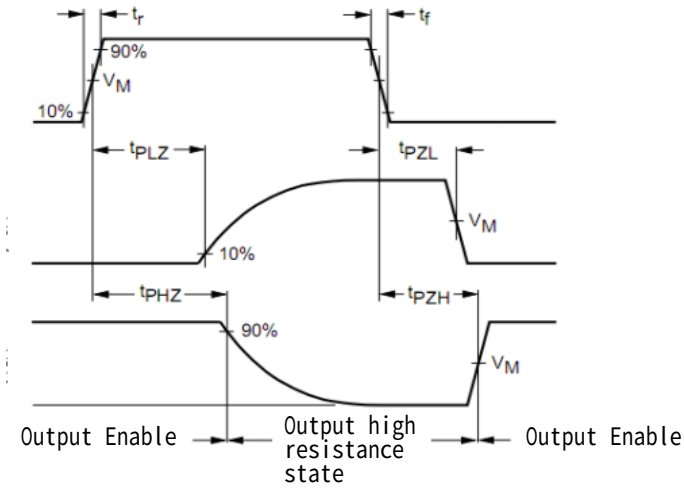


Figure 9: The above figure shows the pulse width of the main reset (MR), the transmission delay time from the main reset to the output (Q7 '), and the reset time from the main reset to the shift clock (SH_CP)

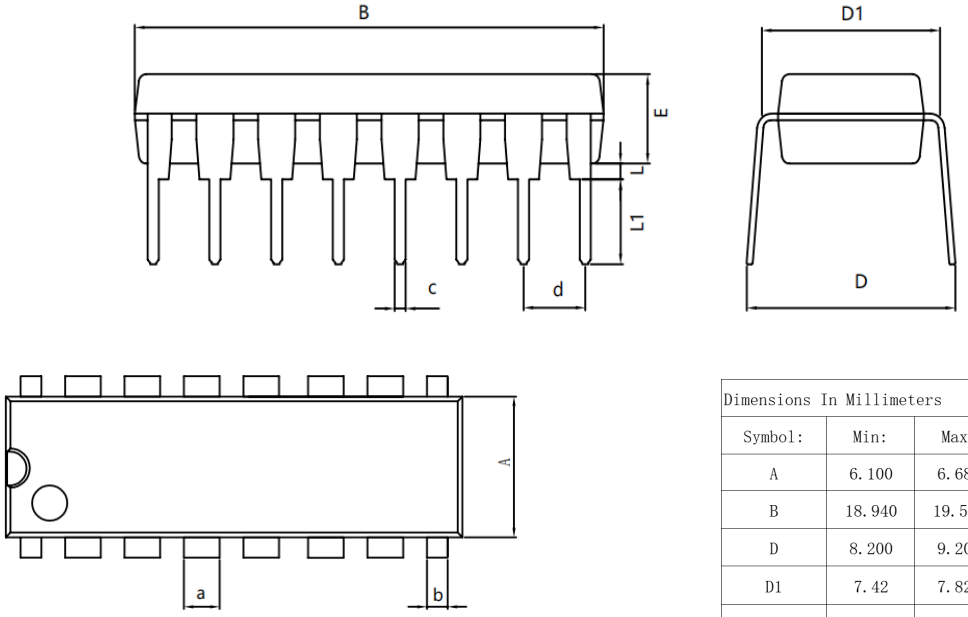


Qn output:
From low level to high resistance state, from high resistance state to low level Qn output:
From high level to high resistance state, from high resistance state to high level

Figure 10: The above figure shows the variation time of the three state output with the output enable end

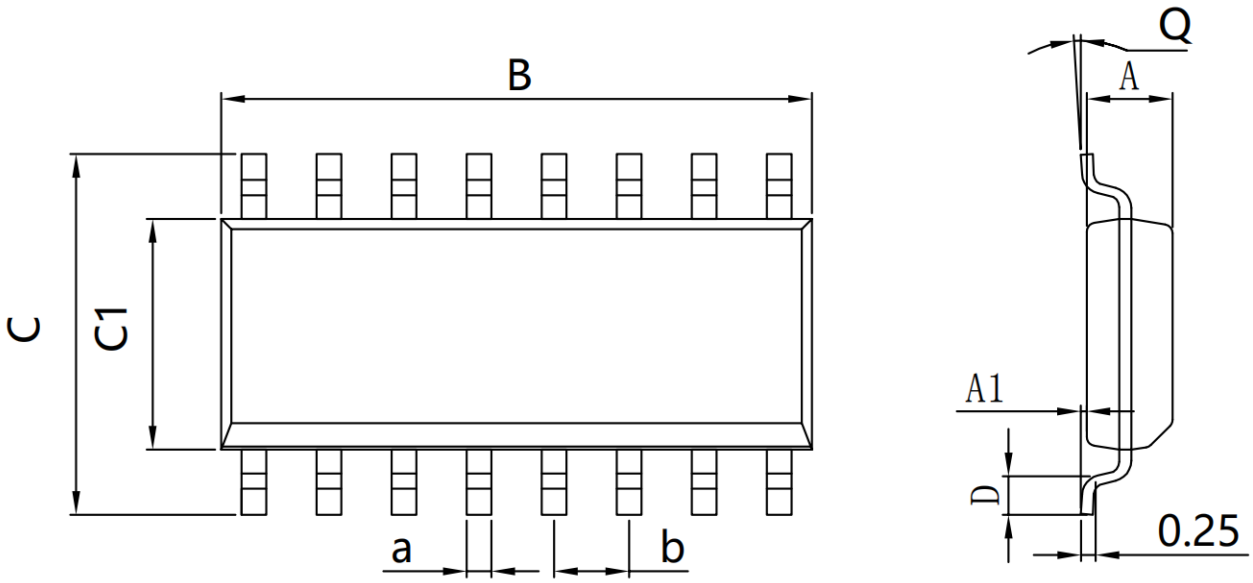
Pin Assignment：

DIP16



Dimensions In Millimeters					
Symbol:	Min:	Max:	Symbol:	Min:	Max:
A	6.100	6.680	L	0.500	0.800
B	18.940	19.560	a	1.524 TYP	
D	8.200	9.200	b	0.889 TYP	
D1	7.42	7.820	C	0.457 TYP	
E	3.100	3.550	d	2.540 TYP	
L	0.500	0.800			

SOP16



Dimensions In Millimeters					
Symbol:	Min:	Max:	Symbol:	Min:	Max:
A	1.225	1.570	D	0.400	0.950
A1	0.100	0.250	Q	0°	8°
B	9.800	10.00	a	0.420 TYP	
C	5.800	6.250	b	1.270 TYP	
C1	3.800	4.000			