

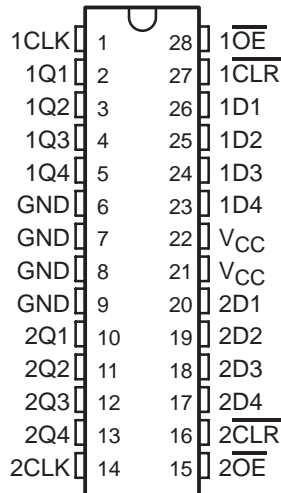
# 74AC11874

## DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOP WITH 3-STATE OUTPUTS

SCAS236 – MARCH 1990 – REVISED APRIL 1993

- **3-State Buffer-Type Outputs Drive Bus Lines Directly**
- **Asynchronous Clear**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin  $V_{CC}$  and GND Configurations Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1- $\mu$ m Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

DW OR NT PACKAGE  
(TOP VIEW)



### description

This dual 4-bit D-type edge-triggered flip-flop features 3-state outputs designed specifically for bus driving. This makes these devices particularly suitable for implementing buffer registers, I/O ports, and working registers.

The flip-flops enter data on the low-to-high transition of the clock. The 74AC11874 has clear ( $\overline{1CLR}$  and  $\overline{2CLR}$ ) inputs and noninverting outputs. Taking  $\overline{CLR}$  low causes the four Q outputs to go low independently of the clock.

The 74AC11874 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE  
(each 4-bit flip-flop)

INPUTS				OUTPUT
$\overline{OE}$	$\overline{CLR}$	CLK	D	Q
L	L	X	X	L
L	H	$\uparrow$	H	H
L	H	$\uparrow$	L	L
L	H	L	X	$Q_0$
H	X	X	X	Z

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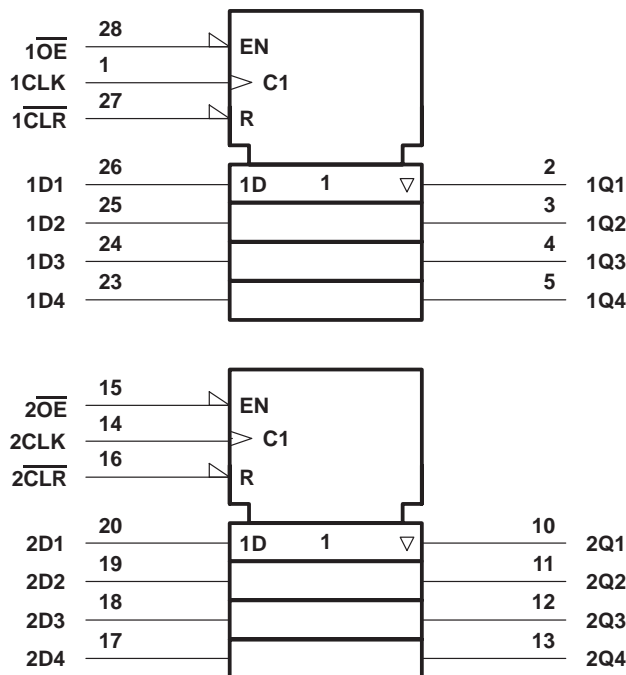


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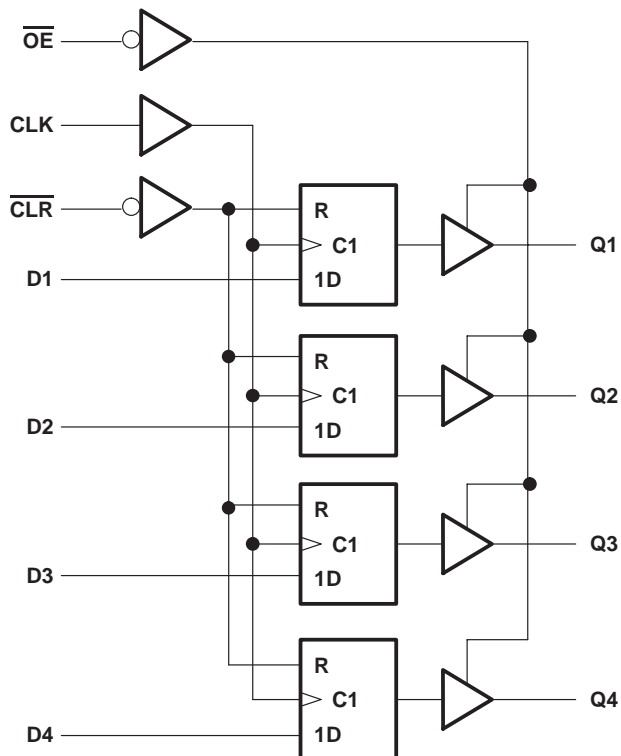
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## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram, each quad flip-flop (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) .....	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	$\pm 50$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND pins .....	$\pm 200$ mA
Storage temperature range .....	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

**74AC11874**  
**DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOP**  
**WITH 3-STATE OUTPUTS**

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**recommended operating conditions**

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	3	5	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 3\text{ V}$	2.1		V
		$V_{CC} = 4.5\text{ V}$	3.15		
		$V_{CC} = 5.5\text{ V}$	3.85		
$V_{IL}$	Low-level input voltage	$V_{CC} = 3\text{ V}$	0.9		V
		$V_{CC} = 4.5\text{ V}$	1.35		
		$V_{CC} = 5.5\text{ V}$	1.65		
$V_I$	Input voltage	0	$V_{CC}$		V
$V_O$	Output voltage	0	$V_{CC}$		V
$I_{OH}$	High-level output current	$V_{CC} = 3\text{ V}$	-4		mA
		$V_{CC} = 4.5\text{ V}$	-24		
		$V_{CC} = 5.5\text{ V}$	-24		
$I_{OL}$	Low-level output current	$V_{CC} = 3\text{ V}$	12		mA
		$V_{CC} = 4.5\text{ V}$	24		
		$V_{CC} = 5.5\text{ V}$	24		
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10		ns/V
$T_A$	Operating free-air temperature	-40	85		°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$V_{OH}$	$I_{OH} = -50\ \mu\text{A}$	3 V	2.9		2.9		V	
		4.5 V	4.4		4.4			
		5.5 V	5.4		5.4			
	$I_{OH} = -4\ \text{mA}$	3 V	2.58		2.48			
		4.5 V	3.94		3.8			
		5.5 V	4.94		4.8			
$I_{OH} = -75\ \text{mA}^\dagger$	5.5 V			3.85				
$V_{OL}$	$I_{OL} = 50\ \mu\text{A}$	3 V			0.1		V	
		4.5 V			0.1			
		5.5 V			0.1			
	$I_{OL} = 12\ \text{mA}$	3 V			0.36			
		4.5 V			0.36			
		5.5 V			0.36			
$I_{OL} = 75\ \text{mA}^\dagger$	5.5 V			1.65				
$I_I$	$V_I = V_{CC}$ or GND	5.5 V			$\pm 0.1$		$\mu\text{A}$	
$I_{OZ}$	$V_O = V_{CC}$ or GND	5.5 V			$\pm 0.5$		$\mu\text{A}$	
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			8		$\mu\text{A}$	
$C_i$	$V_I = V_{CC}$ or GND	5 V	4.5				pF	
$C_o$	$V_O = V_{CC}$ or GND	5 V	13.5				pF	

$^\dagger$  Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.



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timing requirements over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
		MIN	MAX			
$f_{\text{clock}}$	Clock frequency	0	60	0	60	MHz
$t_w$	Pulse duration	$\overline{\text{CLR}}$ low	4	4		ns
		CLK high or low	8.3	8.3		
$t_{\text{su}}$	Setup time before $\text{CLK}\uparrow$	Data	3	3		ns
		$\overline{\text{CLR}}$ inactive	1.5	1.5		
$t_h$	Hold time after $\text{CLK}\uparrow$	Data	1	1		ns

timing requirements over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
		MIN	MAX			
$f_{\text{clock}}$	Clock frequency	0	125	0	125	MHz
$t_w$	Pulse duration	$\overline{\text{CLR}}$ low	4	4		ns
		CLK high or low	4	4		
$t_{\text{su}}$	Setup time before $\text{CLK}\uparrow$	Data	2	2		ns
		$\overline{\text{CLR}}$ inactive	1.5	1.5		
$t_h$	Hold time after $\text{CLK}\uparrow$	Data	1	1		ns

switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$f_{\text{max}}$			60			60		MHz
$t_{\text{PLH}}$	CLK	Q	2.9	7.3	11	2.9	12.5	ns
$t_{\text{PHL}}$			3.7	8.8	13.1	3.7	14.6	
$t_{\text{PHL}}$	$\overline{\text{CLR}}$	Q	3.9	9.3	14	3.9	15.7	ns
$t_{\text{PZH}}$	$\overline{\text{OE}}$	Q	2.1	5.6	8.7	2.1	9.8	ns
$t_{\text{PZL}}$			3.1	8.4	13.1	3.1	14.9	
$t_{\text{PHZ}}$	$\overline{\text{OE}}$	Q	4	6.2	8.2	4	8.7	ns
$t_{\text{PLZ}}$			3.9	6.3	8.5	3.9	9	

switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$f_{\text{max}}$			125			125		MHz
$t_{\text{PLH}}$	CLK	Q	2.3	5.2	7.4	2.3	8.3	ns
$t_{\text{PHL}}$			2.9	6.1	8.6	2.9	9.6	
$t_{\text{PHL}}$	$\overline{\text{CLR}}$	Q	2.9	6.3	8.9	2.9	10	ns
$t_{\text{PZH}}$	$\overline{\text{OE}}$	Q	1.5	4	5.9	1.5	6.6	ns
$t_{\text{PZL}}$			2.3	5.4	7.8	2.3	8.8	
$t_{\text{PHZ}}$	$\overline{\text{OE}}$	Q	3.8	5.7	7.3	3.8	7.7	ns
$t_{\text{PLZ}}$			3.7	5.5	7.1	3.7	7.5	



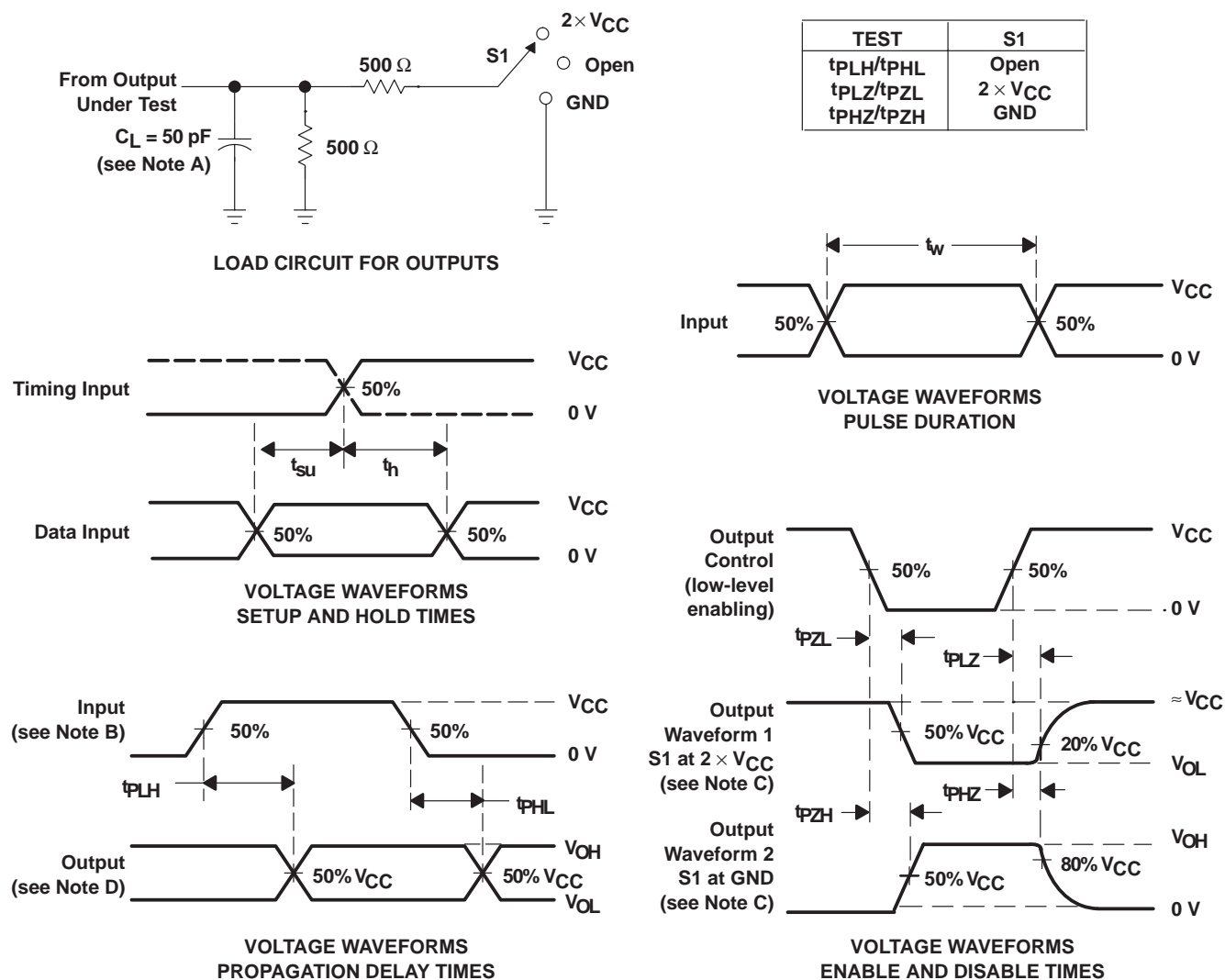
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operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance per flip-flop	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	31	pF
			13	

## PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .  
For testing pulse duration:  $t_r = t_f = 1\text{ to }3\text{ ns}$ . Pulse polarity can be either high-to-low-to-high or low-to-high-to-low.

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.  
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
74AC11874DW	OBSOLETE	SOIC	DW	28		TBD	Call TI	Call TI
74AC11874NT	OBSOLETE	PDIP	NT	28		TBD	Call TI	Call TI
74AC11874NT	OBSOLETE	PDIP	NT	28		TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

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**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

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<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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