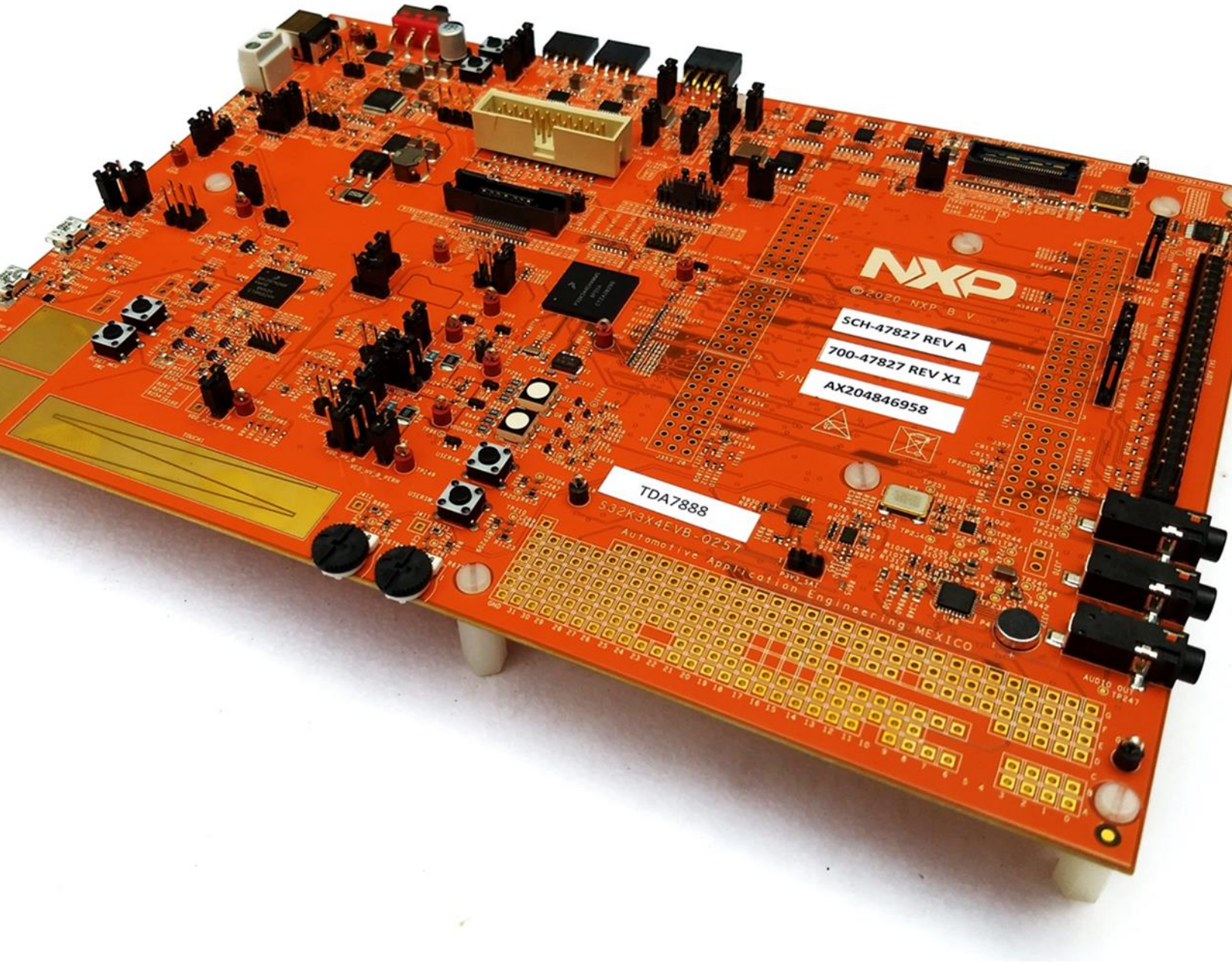
S32K3X4EVB-Q257
S32K3X4EVBQ257ND

Customer Evaluation Board for S32K3x4 MCUs
Hardware User Manual



1 Table of contents

2 Definitions, Acronyms, and Abbreviations

The following list defines the abbreviations used in this document.

CD	Compact Disk
CMOS	Complementary Metal Oxide Semiconductor
CPLD	Custom Programmed Logic Devices
CPU	Central Processing Unit
CSI	Camera Sensor Imaging
CSPI	Serial Peripheral Interface
DDR	Double Data Rate
DIP	Dual In-line Package
EEPROM	Electrically Erasable Programmable Read Only Memory
EPROM	Erasable Programmable Read Only Memory
GPIO	General Purpose Input/output
GPO	General Purpose Output
I2C	Inter-Integrated Circuit
ICE	In-Circuit Emulator
I/O	Input/output
JTAG	Joint Test Access Group
LAN	Local Area Network
LCD	Liquid Crystal Display
LED	Light Emitting Diode
MB	Megabyte
MCU	Microcontroller Unit
MMC	Multi-Media Card
MCP	Multi-chip product
MS	Memory Stick
NVRAM	Non-volatile Random-Access Memory
PC	Personal Computer
PCB	Printed Circuit Board
PHY	Physical interface
POR	Power on Reset
PSRAM	Pseudo Random Access Memory
PWR	Power
PWM	Pulse Width Modulation
QVGA	Graphics Adapter
RAM	Random Access Memory
SD	SanDisk (Smart Media)
SDRAM	Synchronous Dynamic Random-Access Memory
SI	System International (international system of units and measures)
SIMM	Single In-Line Memory Module
SPST	Single Pole Single Throw
TFT	Thin Film Transistor
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus.
HW	Hardware.
POP	Populate – Component placed
DNP	Do not populate – Component removed

3 Block Diagram

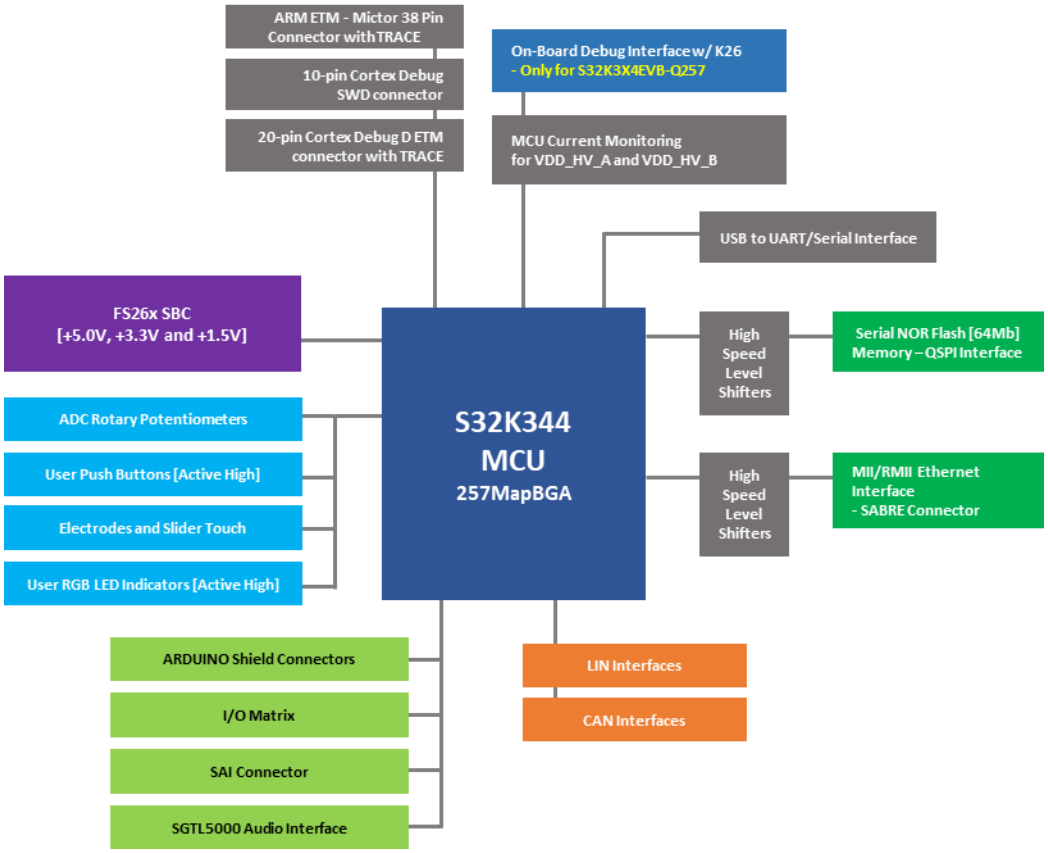


Figure 1. S32K3X4EVB-Q257 | S32K3X4EVBQ257ND – Block diagram

4 Features

IMPORTANT

- Verify and download the last version of this document in http://www.nxp.com
- Before the S32K344 Customer Evaluation board is used or power is applied, please fully read this user manual. An incorrect configuration in the board may cause a damage irreparable on the component, MCU or EVB. Power must be removed from the EVB prior to:
  - Removing or placing some component or measurement
  - Re-configuring the board jumpers

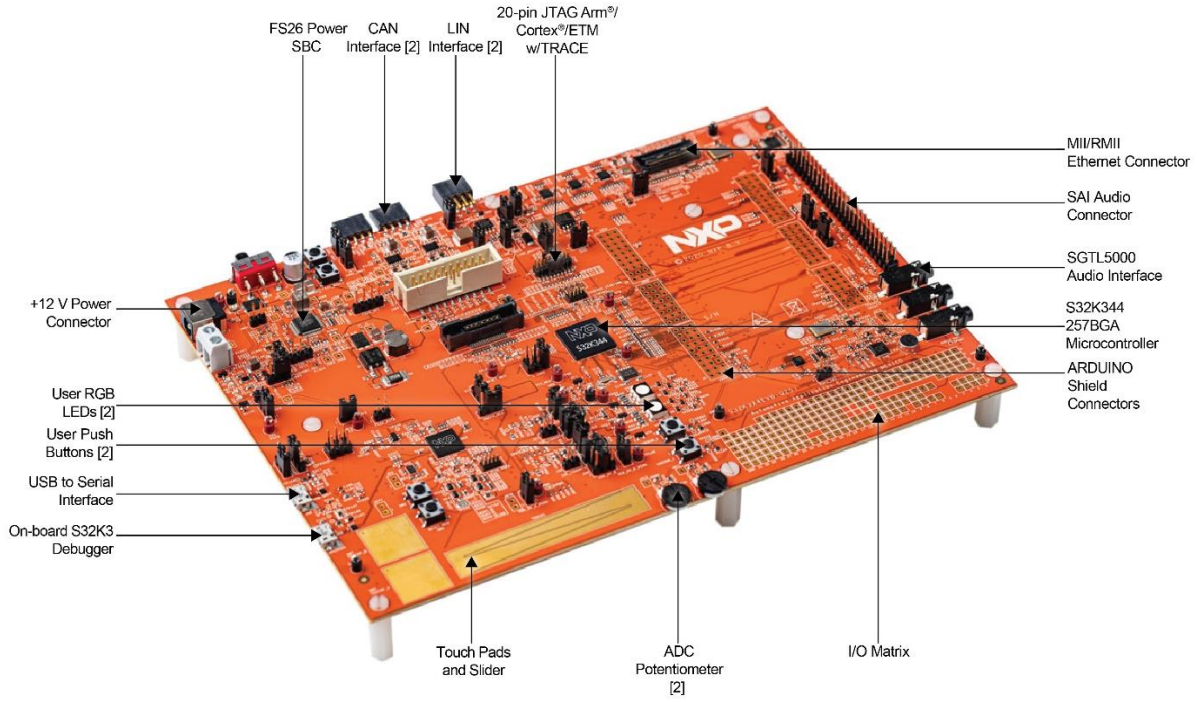


Figure 2. S32K3X4EVB-Q257 – Features

5 Default Configuration

Table 1. S32K3X4EVB-Q257 - Default Configuration

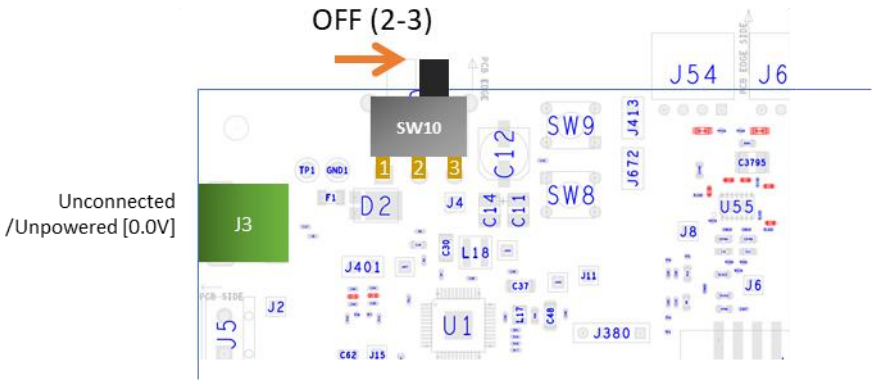
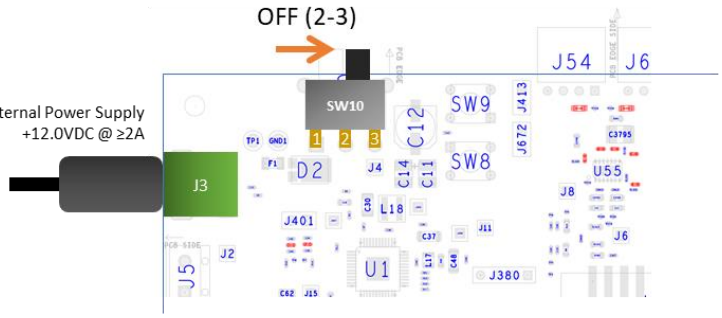
Interface	S32K3X4 EVB-Q257	S32K3X4 EVBQ257 ND	Reference / Signal	Configuration	Description/Comment
MCU Power Supply	●	●	VDD_HV_A_MCU	+5.0V	The VDDA_HV_A domain is connected to +5.0V– Switching Power Supply
	●	●	VDD_HV_B_MCU	+3.3V	The VDDA_HV_B domain is connected to +3.3V– Switching Power Supply
	●	●	VDD_REFH_MCU	[VDD_HV_A]	The VDD_REFH domain is connected to VDD_HV_A_MCU
	●	●	V15_MCU	External NPN Transistor	The V15_MCU domain is routed to the external NPN Ballast Transistor
Ethernet	●	●	J63	MII/RMII Enabled	Ethernet MII signals are routed to ENET SABRE connector.

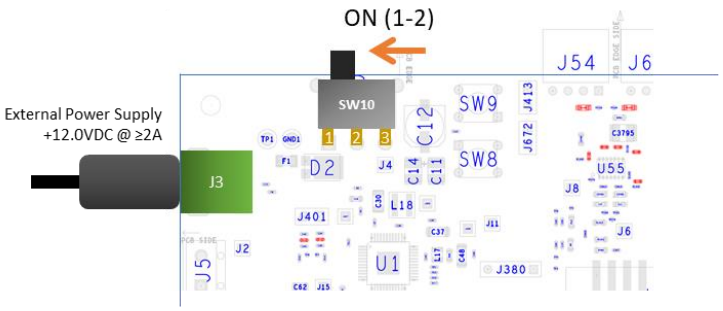
Interface	S32K3X4 EVB-Q257	S32K3X4 EVBQ257 ND	Reference / Signal	Configuration	Description/Comment
QSPI-A Memory	●	●		Enabled	The MCU signals to the QSPI-A Memory Interface are enabled
Open SDA	●			PTA15	PTA15/LPUART6_RX is routed to OpenSDA for serial interface
				PTA16	PTA16/LPUART6_TX is routed to OpenSDA for serial interface
USB to Serial Interface	●	●		PTC26	PTC26/LPUART3_RX is routed to the USB2UART Interface
				PTC27	PTC27/LPUART3_TX is routed to the USB2UART Interface
CAN Interface	TJA1153	TJA1043	/CAN0	PTA6	CAN0_RX is routed to CAN Phy0
				PTA7	CAN0_TX is routed to CAN Phy0
				PTC23	CAN0_ERRN is routed to PTC23 for CAN Phy0
				PTC21	CAN0_EN is routed to PTC21 for CAN Phy0
				PTC20	CAN0_STB is routed to PTC20 for CAN Phy0
			/CAN1	PTE14	CAN4_RX is routed to PTE14 to CAN Phy1
				PTE3	CAN4_TX is routed to PTE3 to CAN Phy1
				PTE8	CAN1_ERRN is routed to PTE8 for CAN Phy1
				PTD15	CAN1_EN is routed to PTD15 for CAN Phy1
				PTD13	CAN1_STB is routed to PTD13 for CAN Phy1
LIN Interface	●	●	LIN1	PTB9	LPUART9_RX is routed to LIN Phy0
				PTB10	LPUART9_TX is routed to LIN Phy0
			LIN2	PTB28	LPUART5_RX is routed to LIN Phy1
				PTB27	LPUART5_TX is routed to LIN Phy1
User Push Buttons	●	●	SW4	PTB26	Active Low, before PTA0
	●	●	SW5	PTB19	Active Low, before PTA1
User LEDs	●	●	D32	PTA29	Red
				PTA30	Green
				PTA31	Blue
	●	●	D33	PTB18	Red
				PTB25	Green
				PTE12	Blue
ADC Potentio-meters	●	●	R672	PTA11	ADCPOT0 [R672] is routed to PTA11 - ADC1_S10
	●	●	R679	PTA17	ADCPOT1 [R679] is routed to PTA17 - ADC2_S19

6 S32K3X4EVB-Q257 and S32K3X4EVBQ257ND - Startup

Follow these steps to connect and power on the board

1. Carefully unpack the S32K3X4EVB-Q257 and observe ESD preventive measures while handling the K3 development board.
2. Connect necessary cables between host PC and EVB board prior to applying power to the EVB.
3. The power-ON sequence for the EVB must be as follows:

a)	- The power switch -SW10 must be in OFF position before to the EVB be connected to an external power supply. 
b)	- Once the power switch -SW10 is in OFF position, then the EVB can be connected to an external power supply. 

c)	- Now the power switch -SW10 can be changed to ON- position. 

4. When power is applied to the EVB, three orange LED's adjacent to the voltage regulators show the presence of the supply voltages as follows:
   - LED D34 Indicates that the 12.0V is connected to the EVB correctly.
   - LED D35 Indicates that the 5.0V linear regulator is enabled and working correctly.
   - LED D36 Indicates that the +3.3Vlinear regulator is enabled and working correctly.

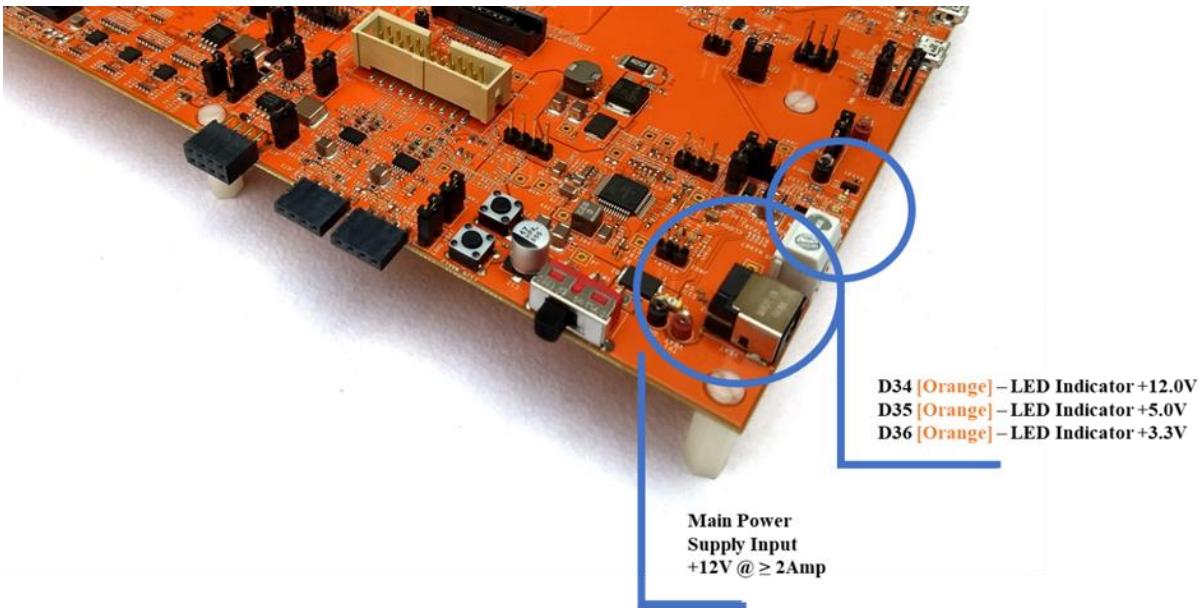


Figure 3. S32K3X4EVB-Q257 | S32K3X4EVBQ257ND – Power supply Input and LED power indicators

If no LED's are illuminated when power is applied to the EVB and the regulators are correctly enabled using the appropriate jumpers, it is possible that either power supply is not connected properly, or the voltage level is lower that the specified [+12.0V to ≥2Amps].

Note that the fuse will not protect against one of the EVB regulators being shorted. If this happens, damage is likely to occur to the EVB and / or components.

5. The board is ready to use now.

7 Power supply

The EVB requires an external power supply voltage of between to +12V/≥2A. This allows the EVB to be easily used in a vehicle if required. The 12v input is on the EVB is used to supply a FS26/SBC – U1, the power management IC controller provides +5.0V, +3.3V and +1.5V, for the different power configurations of VDD_HV_A, VDD_HV_B, V15 and other interfaces.

7.1 S32K3X4EVB-Q257 - Main Power Supply

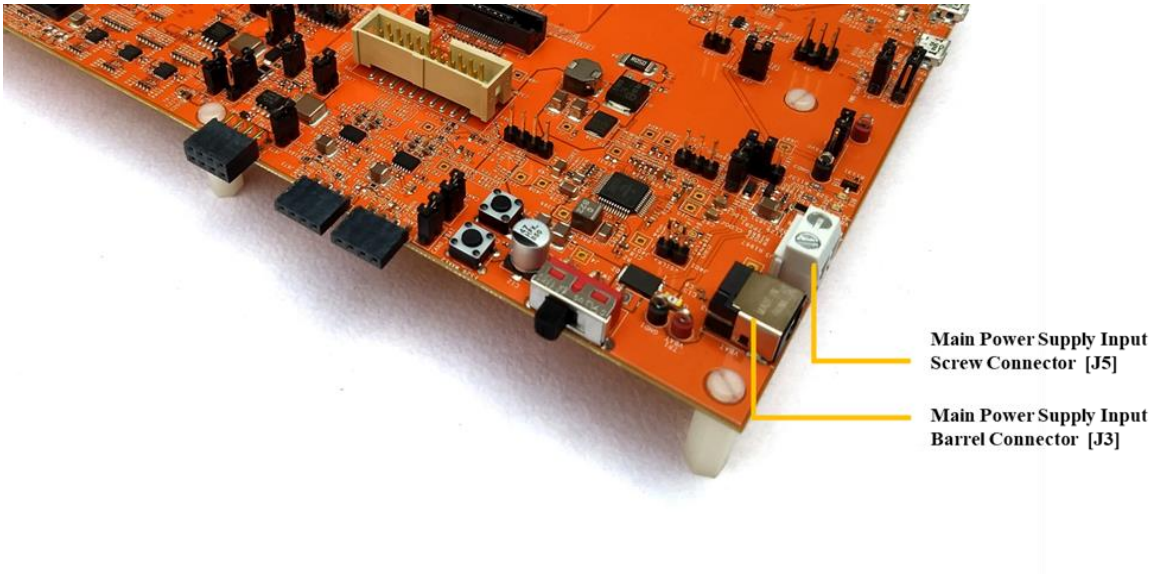
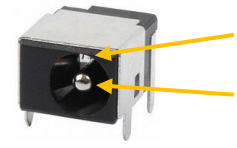
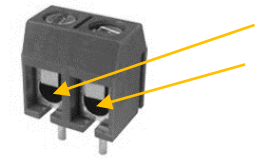


Figure 4. S32K3X4EVB-Q257 | S32K3X4EVBQ257ND – Main power supply input

Table 2. Main power supply connectors

Connector	Description
 Ground V+ (+12Volts).	**2.1mm Barrel Connector – J3** This connector should be used to connect the supplied wall-plug mains adapter. Note – if a replacement or alternative adapter is used, care must be taken to ensure the 2.1mm plug uses the correct polarization as shown
 Ground V+ (12Volts).	**2-Way Screw Type Connector – J5** This can be used to connect a bare wire lead to the EVB, typically from a laboratory power supply. The polarization of the connectors is clearly marked on the EVB. Care must be taken to ensure correct connection.

7.2 S32K3X4EVB-Q257 – FS26/Modes Operation

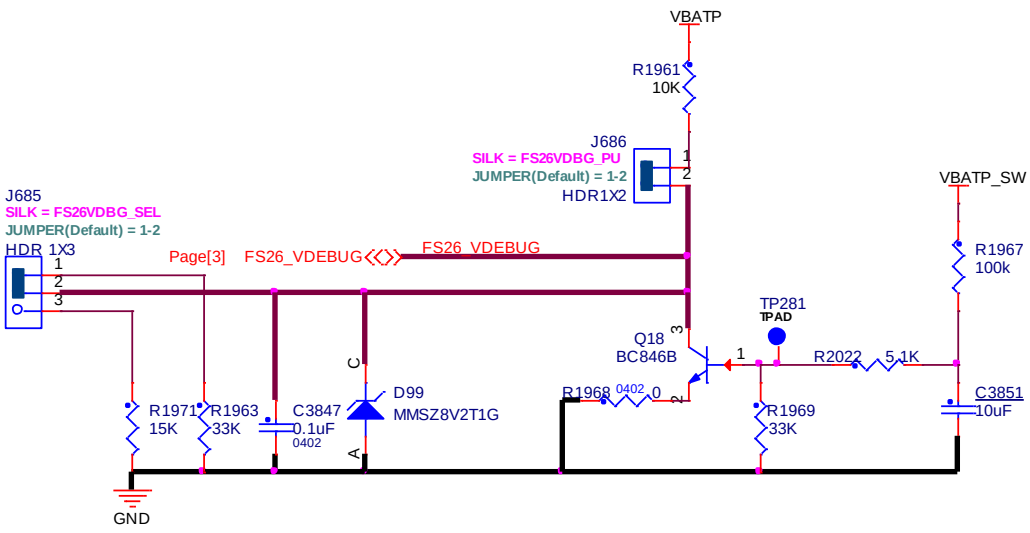
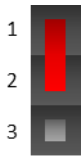
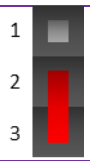
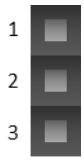


Figure 5. S32K3X4EVB-Q257 | S32K3X4EVBQ257ND – FS26/Modes Operation

Table 3. S32K3X4EVB-Q257 – FS26/Modes Operation

Reference	Jumper Position			Description	Comments
Flash Mode [Default configuration]	J686	1-2		The R1961 resistor to VBATP (VBAT protected +12.0V) is routed as pull-up to the VDEBUG Pin. This is a common pull-up resistor for the 2 voltage divider configurations, with R1971 or R1963.	
	J685	1-2		The R1963 is selected for the divider voltage, +8.0V is applied on VDEBUG pin to set the FS26-SBC on MCU Flash Mode. In this mode device power up sequence starts with debug mode enabled and can be used during customer production process to flash MCU without need of WD refresh. After ~80ms once the SW10 is in ON-.position the VDEBUG pin will be switching to a low voltage (GND) due to the RC delay circuitry and Q18	
Debug Mode	J686	1-2		The R1961 resistor to VBATP (VBAT protected +12.0V) is routed as pull-up to the VDEBUG Pin. This is a common pull-up resistor for the 2 voltage divider configurations, with R1971 or R1963.	
	J685	2-3		The R1963 is selected for the divider voltage, +5.0V is applied on VDEBUG pin to set the FS26-SBC on Debug Mode, voltage must be removed from debug pin in order to start power up sequence. In this mode Watchdog refresh is not needed. After	

Reference	Jumper Position			Description	Comments
				~80ms once the SW10 is in ON-.position the VDEBUG pin will be switching to a low voltage (GND) due to the RC delay circuitry and Q18.	
Normal Mode	J686	OPEN		In this mode the FS26 can enter Normal mode by configuring the init fs window and sending properly serviced watchdog refresh by SPI. Please review the FS26 documentation.	
	J685	OPEN			
All change of jumpers must be done once the EVB is unpowered from J3 and J5 as MANDATORY					

7.3 S32K3X4EVB-Q257 – +5.0 Volts Power Supply

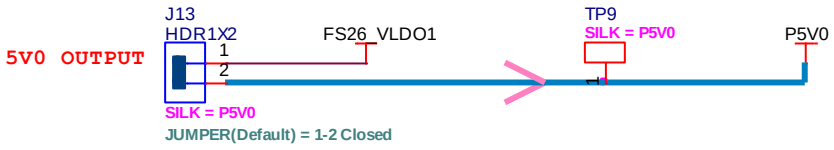
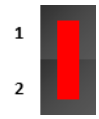


Figure 6. S32K3X4EVB-Q257 | S32K3X4EVBQ257ND – General jumper for the P5V0 (+5.0V) reference

Table 4. S32K3X4EVB-Q257 – +5.0 Volts Power Supply

Reference	Jumper Position		Description	Comments
J13	1-2		The +5.0V output of the FS26x SBC [FS26_VLDO1] is routed to the main P5V0 domain (+5.0V for all board).	Default closed
	OPEN		P5V0 domain (+5.0V for all board) is isolated/disconnected from the FS26x	

7.4 S32K3X4EVB-Q257 – +3.3 Volts Power Supply

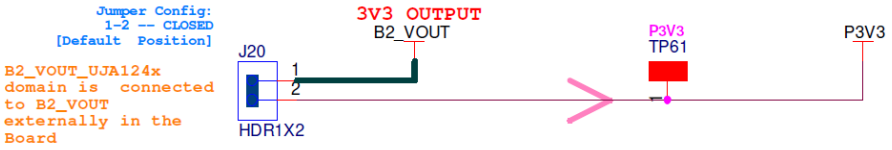
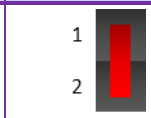
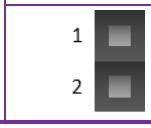


Figure 7. S32K3X4EVB-Q257 | S32K3X4EVBQ257ND – General jumper for the P3V3 (+3.3V) reference

Table 5. S32K3X4EVB-Q257 – +.3.3 Volts Power Supply

Reference	Jumper Position		Description	Comments
J20		1-2	The +3.3V Switching power supply is routed to the main P3V3 domain (+3.3V for all board).	Default closed
		OPEN	The +3.3V output of the FS26x SBC is isolated to the main P3V3 domain (+3.3V for all board).	

7.5 S32K3X4EVB-Q257 – VDD_HV_A

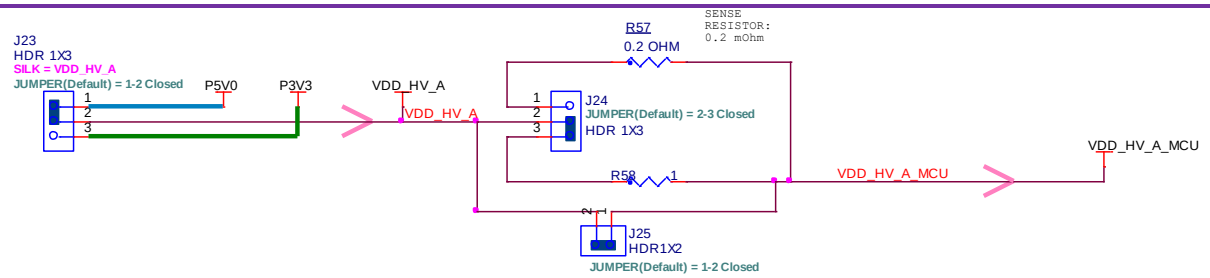
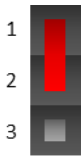
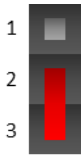
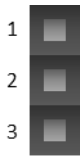
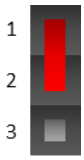
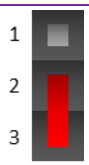
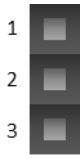


Figure 8. S32K3X4EVB-Q257 | S32K3X4EVBQ257ND – VDD_HV_A power supply

Table 6. S32K3X4EVB-Q257 – VDD_HV_A

Reference	Jumper Position		Description	Comments
J23		1-2	P5V0 (+5.0V Switching Power Supply) is selected for the VDD_HV_A_MCU reference	Default closed
		2-3	P3V3_DC_SW (+3.3V Switching Power Supply) is selected for the VDD_HV_A_MCU reference	
		OPEN	VDD_HV_A domain is isolated and unpowered	
J24		1-2	The shunt resistor R57 [0.2 Ohms] is selected for current measurement proposals on the VDD_HV_A_MCU reference	
		2-3	The shunt resistor R58 [1 Ohms] is selected for current measurement proposals on the VDD_HV_A_MCU reference	Default closed
		OPEN	The shunt resistors R57 and R58 are disabled for current measurement proposals on the VDD_HV_A_MCU reference	
J25		1-2	VDD_HV_A is routed to VDD_HV_A_MCU reference. A jumper on this position disables the shunt resistors R57 and R58 are disabled for current measurement proposals.	Default closed
		OPEN	This jumper allows a differential measurement to the shunt resistor in series for the VDD_HV_A_MCU domain.	

7.5.1 S32K3X4EVB-Q257 – VDD_HV_B

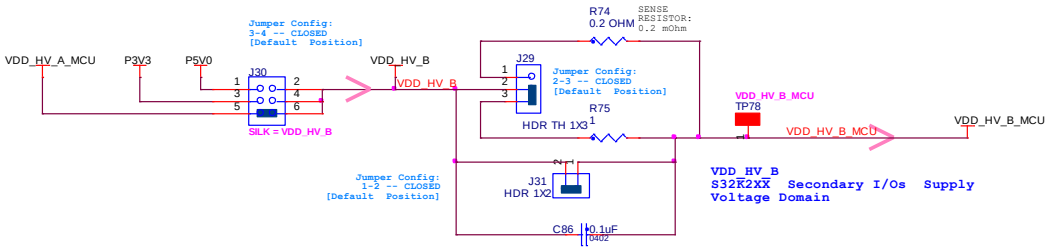
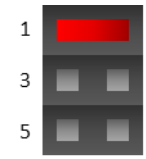
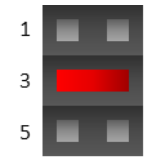
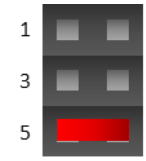
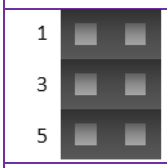
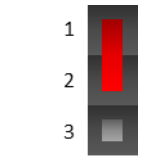
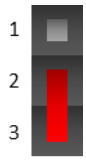
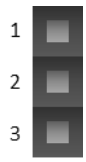


Figure 9. S32K3X4EVB-Q257 | S32K3X4EVBQ257ND – Main power supply

Table 7. S32K3X4EVB-Q257 – VDD_HV_B

Reference	Jumper Position		Description	Comments
J30		1-2	P5V0 (+5.0V Switching Power Supply) is selected for the VDD_HV_B_MCU reference	
		3-4	P3V3_DC_SW (+3.3V Switching Power Supply) is selected for the VDD_HV_B_MCU reference	
		5-6	VDD_HV_A_MCU is routed to VDD_HV_B_MCU reference	Default closed
		OPEN	VDD_HV_B domain is isolated and unpowered	
	CAUTION - 2 or more connections/jumpers in this header selector is NOT ALLOWED			
J29		1-2	The shunt resistor R74 [0.2 Ohms] is selected for current measurement proposals on the VDD_HV_B_MCU reference	

		2-3	The shunt resistor R75 [1 Ohms] is selected for current measurement proposals on the VDD_HV_B_MCU reference	Default closed
		OPEN	The shunt resistors R74 and R75 are disabled for current measurement proposals on the VDD_HV_B_MCU reference	
J31		1-2	VDD_HV_B is routed to VDD_HV_B_MCU reference. A jumper on this position disables the shunt resistors R74 and R75 are disabled for current measurement proposals.	Default closed
		OPEN	This jumper allows a differential measurement to the shunt resistor in series for the VDD_HV_B_MCU domain.	

7.5.2 S32K3X4EVB-Q257 – VREFH

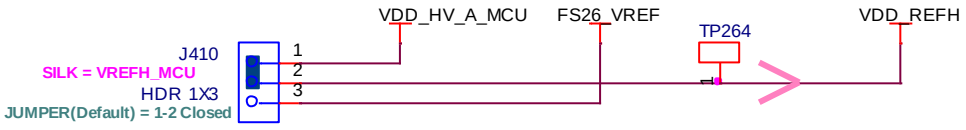
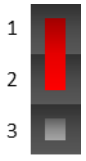
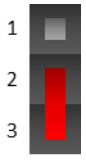
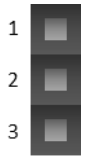


Figure 10. S32K3X4EVB-Q257 | S32K3X4EVBQ257ND – VREFH power supply

Table 8. S32K3X4EVB-Q257 – VREFH

Reference	Jumper Position		Description	Comments
J410		1-2	The VREFH_MCU reference is routed to the VDD_HV_A_MCU domain.	Default closed
		2-3	The VREFH_MCU reference is routed to the FS26_VREF output domain [+5.0V].	VREH_MCU should not be connected to a higher voltage than VDD_HV_A, therefore J410[1-2] can be placed only when J23[1-2]
		OPEN	The VREFH_MCU is floated/unpowered	

7.5.3 S32K3X4EVB-Q257 – V15

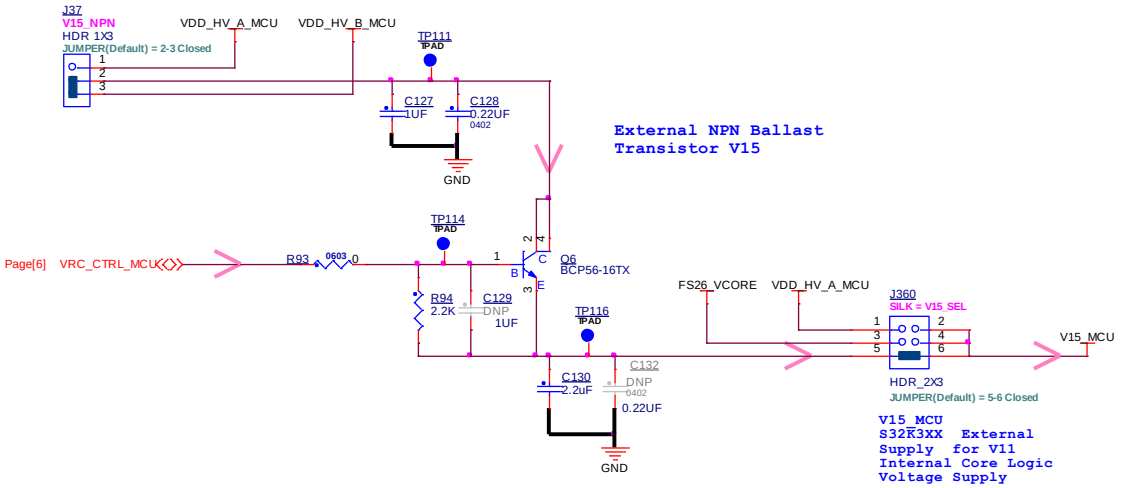
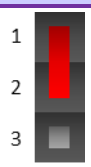
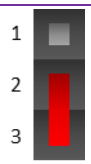
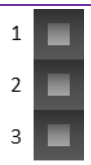
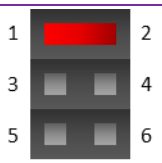
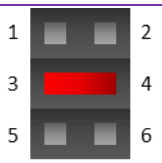
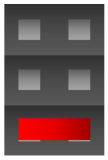
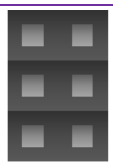


Figure 11. S32K3X4EVB-Q257 – V15 power supply

Table 9. S32K3X4EVB-Q257 – V15 Domain

Reference	Jumper Position		Description	Comments
J37		1-2	The VDD_HV_A domain is routed to the collector terminal in order to supply the NPN external Ballast transistor for the V15_MCU domain.	
		2-3	The VDD_HV_B domain is routed to the collector terminal in order to supply the NPN external Ballast transistor for the V15_MCU domain.	Default closed
		OPEN	The VDD_HV_A and VDD_HV_B domains are isolated to supply the NPN external Ballast transistor for V15.	
J360		1-2	The VDD_HV_A domain is directly routed the V15_MCU domain.	
		2-3	The FS26_VCORE domain [+1.5V] is directly routed the V15_MCU domain.	

		5-6	The NPN external Ballast transistor is selected to supply the V15_MCU domain.	Default closed
		OPEN	The V15_MCU domain is disconnected and isolated from the local external supplies.	

8 Programming and Debug Interface

8.1 RESET Switch and LED indicator

The RESET switch [SW2] provides for manual application of the RESET input signal. The S32K3 MCU will drive the RESET signal to reset the EVB board peripherals. The RESET LED indicator [D22] will be ON for the duration of the RESET signal. This operation indicates the S32K344 MCU is in the Reset state.

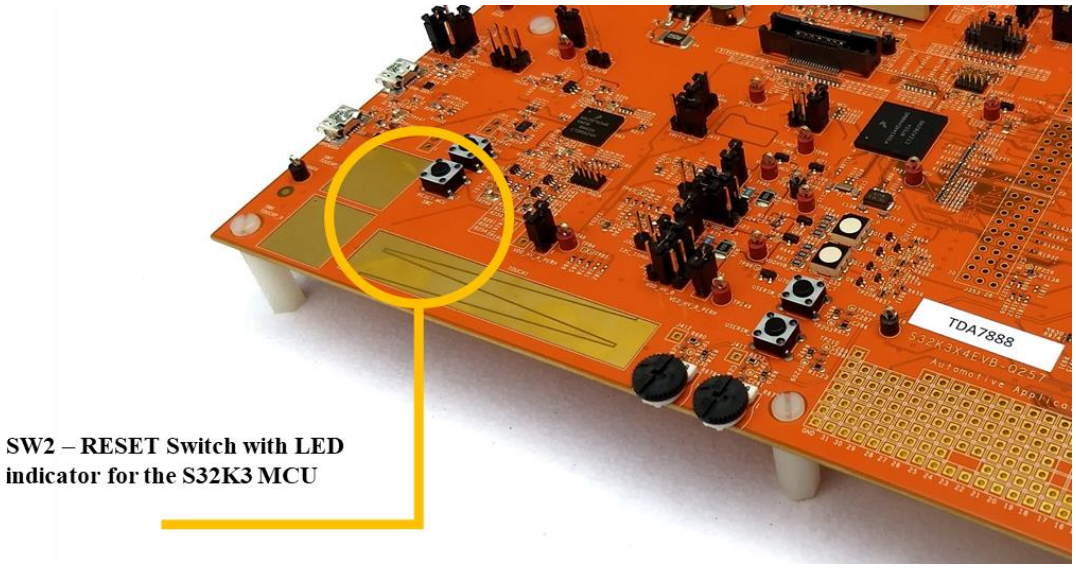


Figure 12. S32K3X4EVB-Q257 | S32K3X4EVBQ257ND – RESET Switch

8.2 On-board S32K3 Debugger

The S32K3X4EVB-Q257 [only] incorporates an On-Board Debugger embedded well as JTAG connectors. It bridges serial and debug communications between a USB host and an embedded target processor.

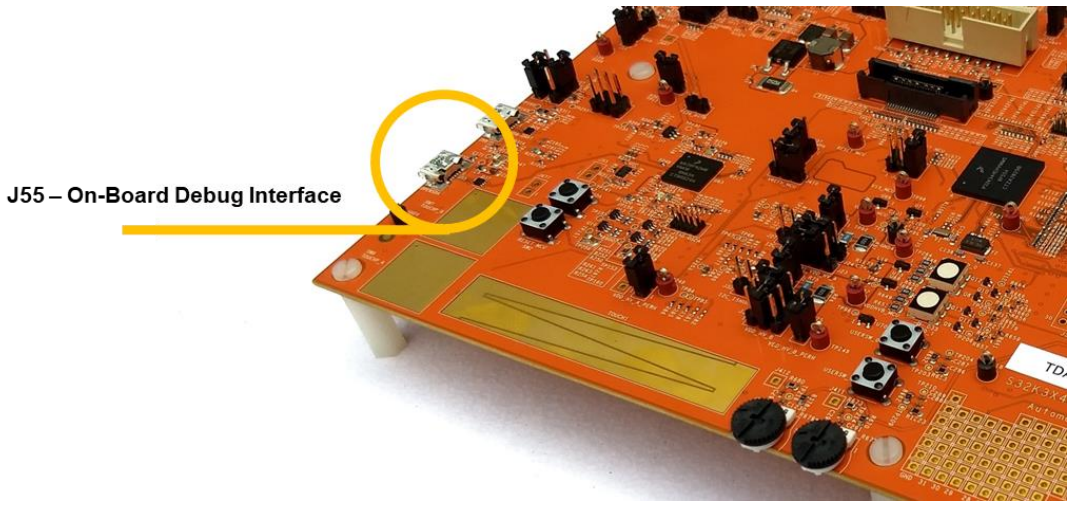


Figure 13. S32K3X4EVB-Q257 | S32K3X4EVBQ257ND – On-board S32K3 Debugger

Table 10. Programming and Debug Connectors

<table>
<tr><th colspan="2">Connector</th><th>S32K3X4EVB-Q257
S32K3X4EVBQ257ND</th><th>Description</th></tr>
<tr><td>20-Pin Cortex Debug + ETM Connector</td><td>  </td><td>J50</td><td>This small 20-pin (0.05") connector provides access to SWD, SWV, JTAG, and ETM (4-bit) signals available on a Cortex-M3/M4/M7 device.
A 20-pin header (Samtec FTSH-110-01) is specified with dimensions:
0.50" x 0.188" (12.70 mm x 4.78 mm).
NOTE - JTAG – TRACE Signals
Due that the MCU ports used for the trace signals also are shared with other interfaces. It is important to isolate these signals/interfaces for the J4-Cortex Debug D ETM connector.
<table>
<tr><th>SIGNAL NAME</th><th>MCU PORT</th><th>COMMENT</th></tr>
<tr><td>TRACE_CLK</td><td>PTB9</td><td></td></tr>
<tr><td>TRACE_D0</td><td>PTB8</td><td></td></tr>
<tr><td>TRACE_D1</td><td>PTE2</td><td></td></tr>
<tr><td>TRACE_D2</td><td>PTA14</td><td></td></tr>
<tr><td>TRACE_D3</td><td>PTA13</td><td></td></tr>
</table></td></tr>
<tr><td>10-Pin Cortex Debug Connector</td><td>  </td><td>J52</td><td>The Cortex Debug Connector provides support for Serial Wire and JTAG interface modes in a very small, low cost 10-pin (0.05") connector. This new style connector provides access to all SWD, SWV, and JTAG signals available on a Cortex-Mx device.
A 10-pin header (Samtec FTSH-105-01) is specified with these dimensions:
0.25" x 0.188" (6.35 mm x 4.78 mm).</td></tr>
</table>

38-Pin ARM ETM Mictor Connector		**P1**	The Mictor (Matched Impedance Connector) has been the standard way to connect a trace probe to an ARM target. It supports up to 32-bit ETM trace and is really intended for use with very high-speed ARM processors such as Cortex-R4 and Cortex-A9. Cortex-M7 supports 16-bit data trace using the Mictor connector. This is only available with DS-5 using a DSTREAM debug and trace unit.
20-Pin ARM Standard JTAG Connector		**J365**	The ARM standard JTAG connector has been used for many years in systems with ARM processors. It supports the JTAG interface for accessing ARM7 and ARM9 based devices. For Cortex-Mx devices, it supports Serial Wire and JTAG interfaces for accessing all SWD, SWV, and JTAG signals available on a Cortex-Mx device. The header (e.g. a Samtec: TST-110-01-L-D) is a 20-Pin, 0.10" (2.54 mm) pitch connector with these dimensions: 1.3" x 0.365" (33 mm x 9.27mm).

9 USB to Serial Interface

The EVB incorporates an interface providing a serial connectivity via a direct USB connection between the PC and the EVB. The circuit contains an FTDI FT2232D USB to Serial interface which should automatically install the drivers for 2 additional COM ports on your PC. Note that only one of these is used so you will need to try both. For more information on the USB drivers and general fault finding, consult the FTDI website at http://www.ftdichip.com/

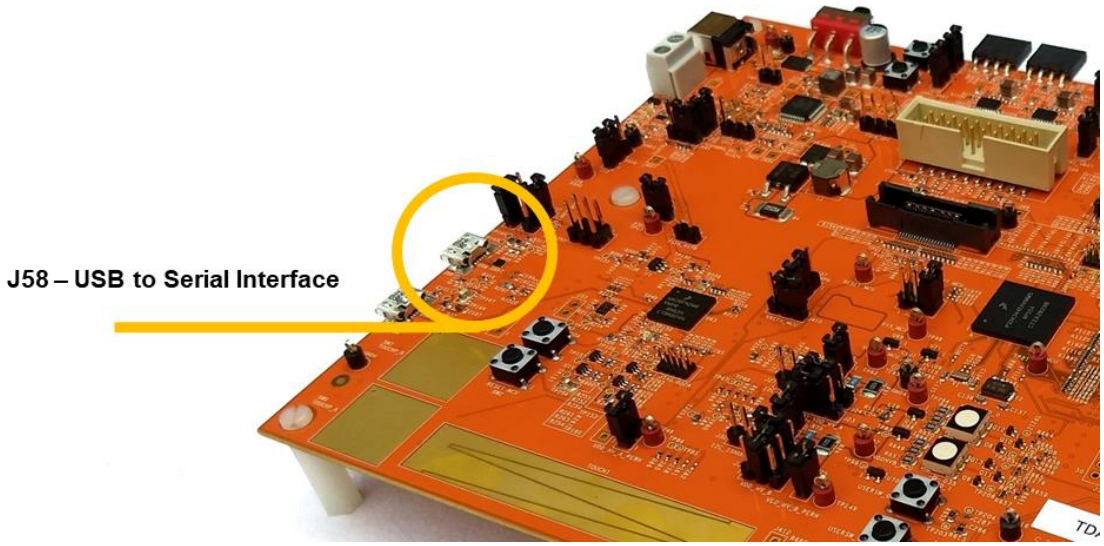


Figure 14. S32K3X4EVB-Q257 | S32K3X4EVBQ257ND – USB to Serial Interface

The PTC27 MCU port (LPUART13_TX) and PTC26 MCU port (LPUART13_RX) signals are routed to the FTDI transceiver via zero ohms resistors allowing the transceiver to be isolated from the MCU pin if desired. The default configuration is with the zero ohms resistors, routing the TX and RX signals from the MCU to the FTDI transceiver.

Table 11. USB to serial interface - Control Jumpers

	Signal /Module	MCU Port	Reference	Description	Comment
1	LPUART13_RX	PTC26	R303	LPUART13_RX signal is routed to FTDI interface	Default configuración
	LPUART13_TX	PTC27	R309	LPUART13_TX signal is routed to FTDI interface	Default configuración
2	LPUART6_RX	PTA15	R302	LPUART6_RX signal is routed to FTDI interface	
	LPUART6_TX	PTA16	R308	LPUART6_TX signal is routed to FTDI interface	

1. If the user want use or change to LPUART6 RX/TX, then:
   - R303 and R309 must be removed.
   - R302-0603-0ohms and R308-0603-0ohms must be populated
2. If the user wants to use other LPUARTx RX/TX module of the MCU, the user can have access to the USB to serial interface by the J677 header. For this use case R302, R303, R308 and R309 must be removed.
   - For a LPUARTx RX/TX module under the domain voltage VDD_HV_A, the R293 must be populated and R294 must be removed.
   - For a LPUARTx RX/TX module under the domain voltage VDD_HV_B, the R294 must be populated and R293 must be removed.

The USB to Serial UART interface in the EVB has two options to configure.

- USB Bus powered configuration.
- USB Self powered Configuration.

USB Bus Powered Configuration (*Default Configuration*).

The USB Bus Powered device gets its power from the USB bus. Basic rules for USB Bus power devices are as follows:

- On plug-in, the device must draw no more than 100mA
- On USB Suspend the device must draw no more than 500µA.
- A High-Power USB Bus Powered Device (one that draws more than 100mA) should use the PWREN# pin to keep the current below 100mA on plug-in and 500µA on USB suspend.
- A device that consumes more than 100mA cannot be plugged into a USB Bus Powered Hub.
- No device can draw more that 500mA from the USB Bus.

USB Self Powered Configuration.

A USB Self Powered configuration gets its power from its own POWER SUPPLY and does not draw current from the USB bus. The basic rules for USB Self power devices are as follows.

- A Self-Powered device should not force current down the USB bus when the USB Host or Hub Controller is powered down.
- A Self Powered Device can take as much current as it likes during normal operation and USB suspend as it has its own POWER SUPPLY.
- A Self Powered Device can be used with any USB Host and both Bus and Self Powered USB Hubs.

10 LIN Interface

The EVB incorporates two LIN interfaces connected the S32K344 MCU. Using an NXP LIN transceivers the TJA1021T/20/C, supporting both master and slave mode (jumper selectable). The output from the LIN transceivers is connected to J675.

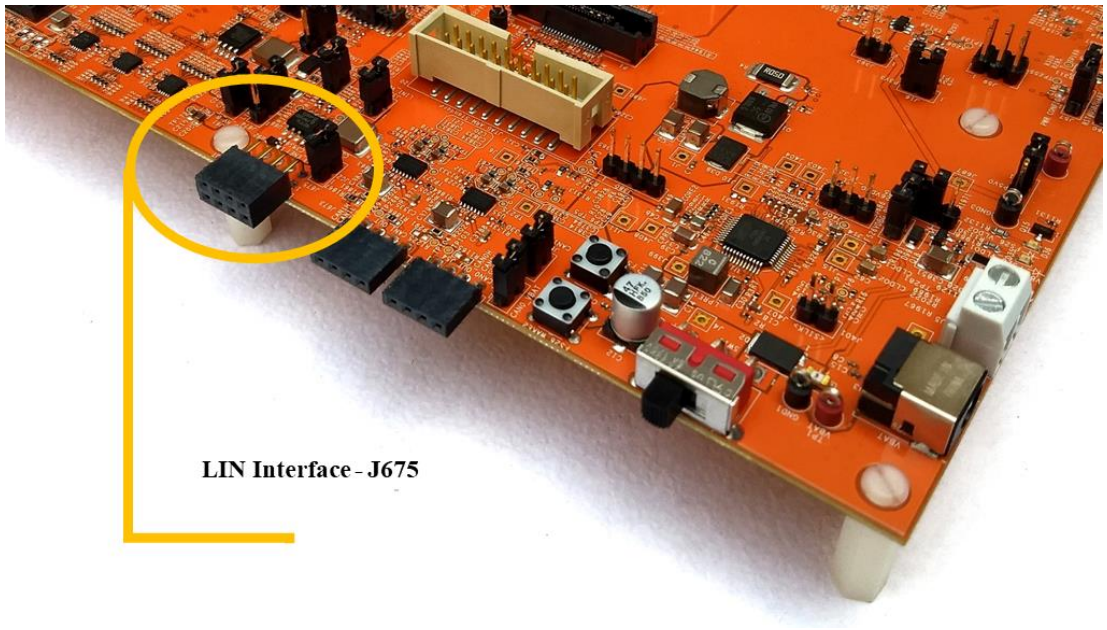
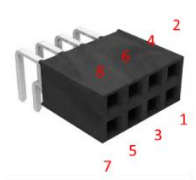


Figure 15. S32K3X4EVB-Q257 | S32K3X4EVBQ257ND – V15 power supply

The pinout of these headers is shown below and is also detailed on the PCB silkscreen.

Table 12. LIN Connector

Connector	Reference	Pin Number	Signal/Connection
	J675	1	GND
		2	GND
		3	NC
		4	NC
		5	VBAT
		6	VBAT
		7	LIN2_OUT
		8	LIN1_OUT

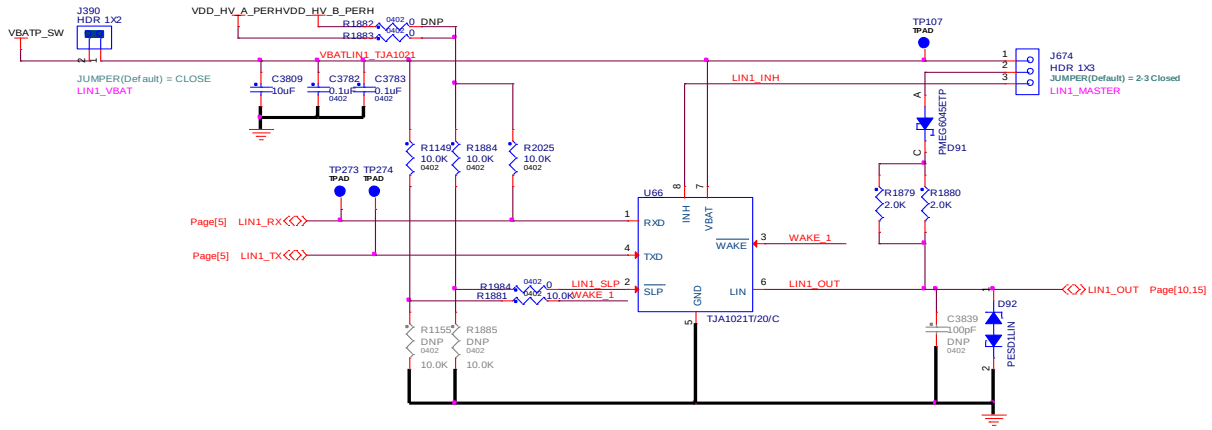


Figure 16. S32K3X4EVB-Q257 | S32K3X4EVBQ257ND – LIN Physical Layer1 TJA1021HG: Quad LIN 2.2A/SAE J2602 transceiver

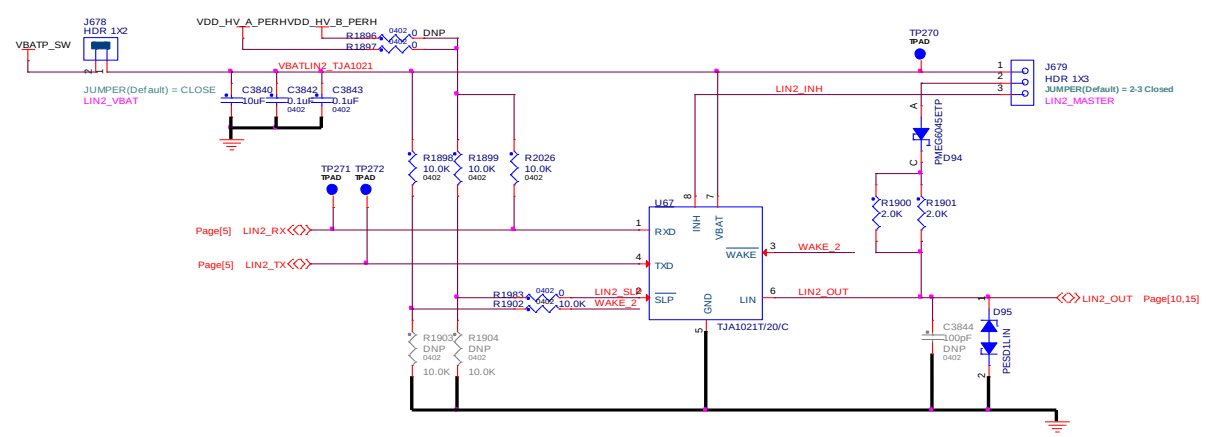


Figure 17. S32K3X4EVB-Q257 | S32K3X4EVBQ257ND – LIN Physical Layer2 TJA1021HG: Quad LIN 2.2A/SAE J2602 transceiver

Table 13. LIN Interface – MCU Connections

LIN Interface	Signal Name	MCU Port	Comment/Description
TJA1021 /LIN1	LIN1_RX	PTB9	LPUART9_RX is routed to LIN Phy1
	LIN1_TX	PTB10	LPUART9 is routed to LIN Phy1
TJA1021 /LIN2	LIN2_RX	PTB28	LPUART5_RX is routed to PTE14 to LIN Phy2
	LIN2_TX	PTB27	LPUART5_TX is routed to PTE3 to LIN Phy2

11 CAN Interface

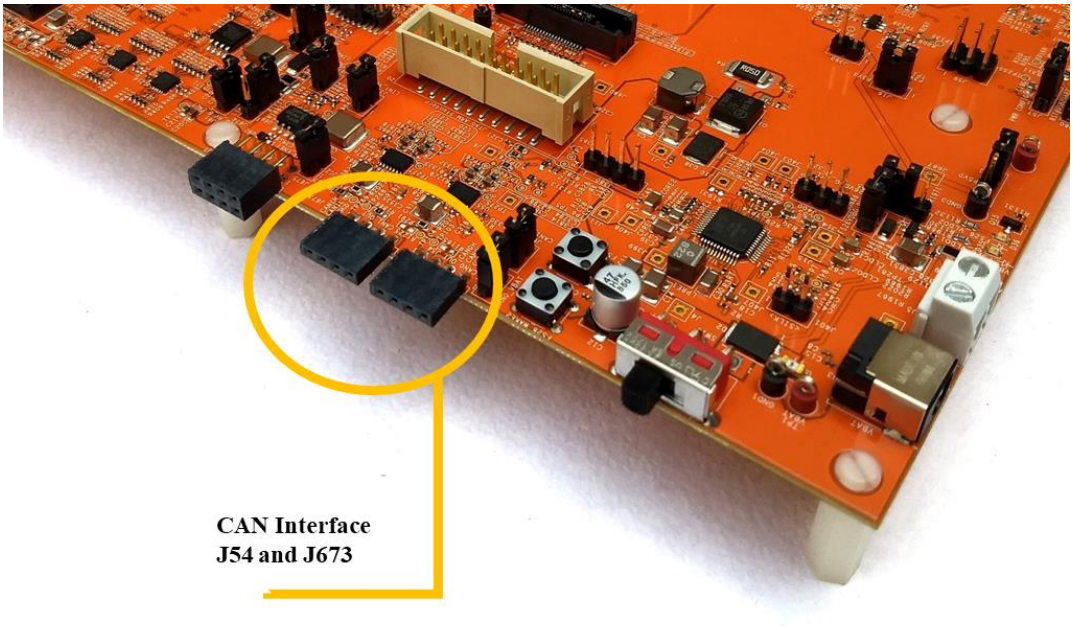


Figure 18. S32K3X4EVB-Q257 | S32K3X4EVBQ257ND – CAN Interface

Table 14. CAN Interface - Connectors

Connector	Reference	Circuit/ Interface	Pin Number	Signal/Connection
	J54	CAN0	1	CANH0
			2	CANL0
			3	GND
			4	NC
	J673	CAN1	1	CANH1
			2	CANL1
			3	GND
			4	NC

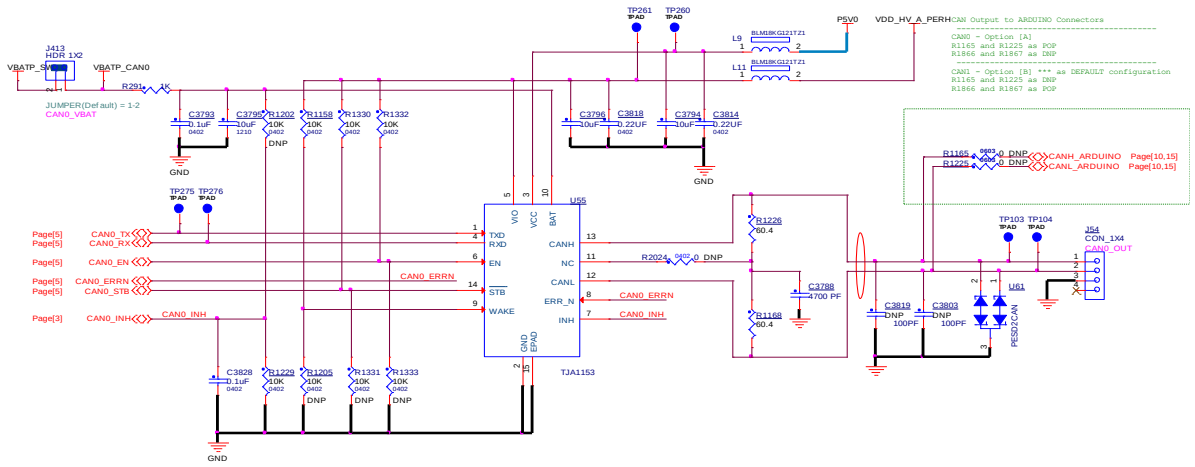


Figure 19. S32K3X4EVB-Q257 | S32K3X4EVBQ257ND – CAN Physical Layer0 - TJA1153 Secure HS-CAN Transceiver

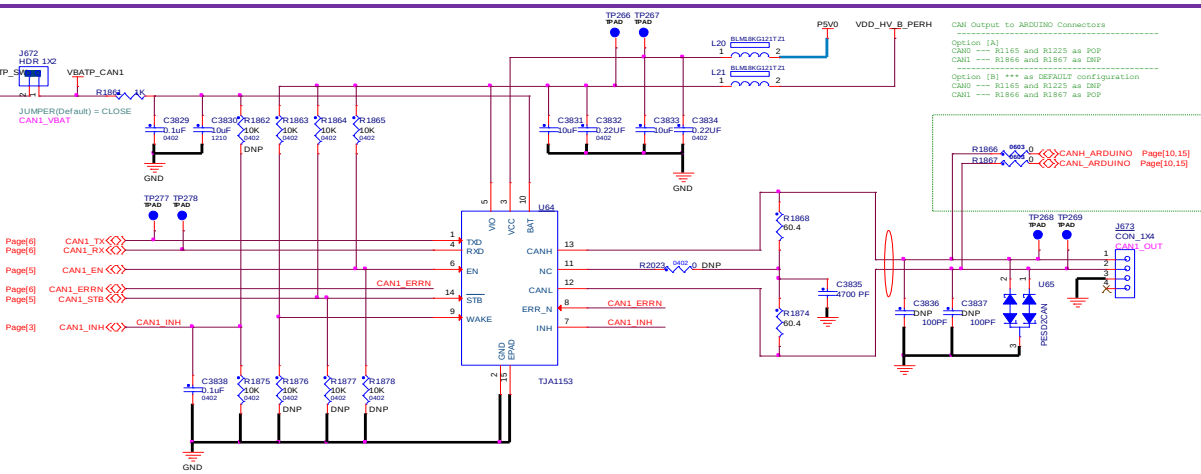


Figure 20. S32K3X4EVB-Q257 | S32K3X4EVBQ257ND – CAN Physical Layer1 - TJA1153 Secure HS-CAN Transceiver

Table 15. CAN Interface – MCU Connections

CAN Interface	Signal Name	MCU Port	Comment/Description
TJA1153 /CAN0	CAN0_RX	PTA6	[CAN0_RX Module] is routed to CAN Phy0
	CAN0_TX	PTA7	[CAN0_TX Module] is routed to CAN Phy0
	CAN0_ERRN	PTC23	PTC23 is routed to CAN Phy0 as CAN0_ERRN
	CAN0_EN	PTC21	PTC21 is routed to CAN Phy0 as CAN0_EN
	CAN0_STB	PTC20	PTC20 is routed to CAN Phy0 as CAN0_STB
TJA1153 /CAN1	CAN1_RX	PTE14	[CAN4_RX Module] is routed to PTE14 to CAN Phy1
	CAN1_TX	PTE3	[CAN4_TX Module] is routed to PTE3 to CAN Phy1
	CAN1_ERRN	PTE8	PTE8 is routed to CAN Phy1 as CAN1_ERRN

CAN Interface	Signal Name	MCU Port	Comment/Description
	CAN1_EN	PTD15	PTD15 is routed to CAN Phy1 as CAN1_EN
	CAN1_STB	PTD13	PTD13 is routed to CAN Phy1 as CAN1_STB

12 Ethernet Interface

The S32K3 EVB incorporates a complete Ethernet interface providing a MII and/or RMII connectivity and LPSPI, I2Cx, GPIOs [3] as digital signals and +3.3V and +12.0V (+5.0V as optional) to the ethernet connector.

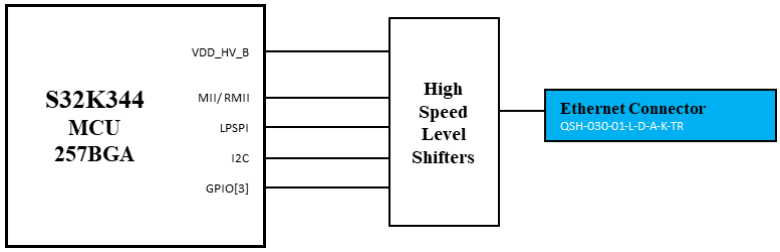


Figure 21. S32K3X4EVB-Q257 | S32K3X4EVBQ257ND – CAN Physical Layer1 - TJA1153 Secure HS-CAN Transceiver

Ethernet Connector - The *EVB* has a High-Speed Connector that is compatible with some external boards:

- ADTJA1101-RMII
- ETHPHY100BASET

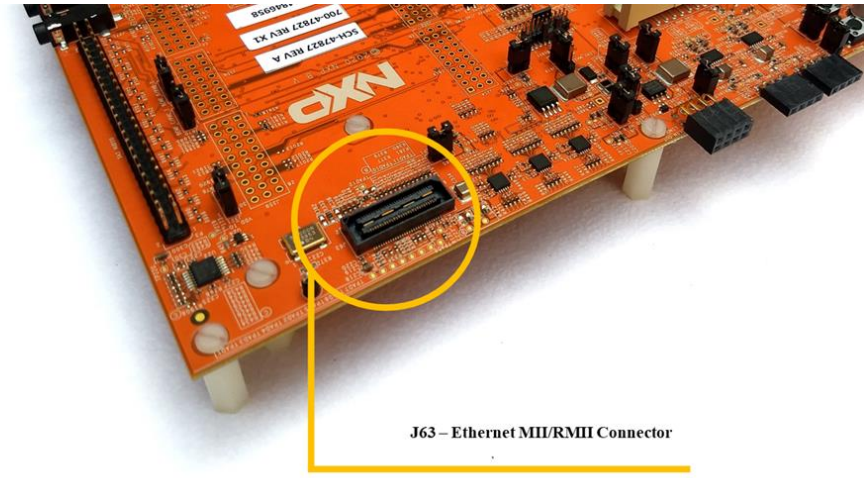


Figure 22. S32K3X4EVB-Q257 – Ethernet RMII/MII and SABRE Connector

13 Ethernet MII/RMII Connector – Pinout

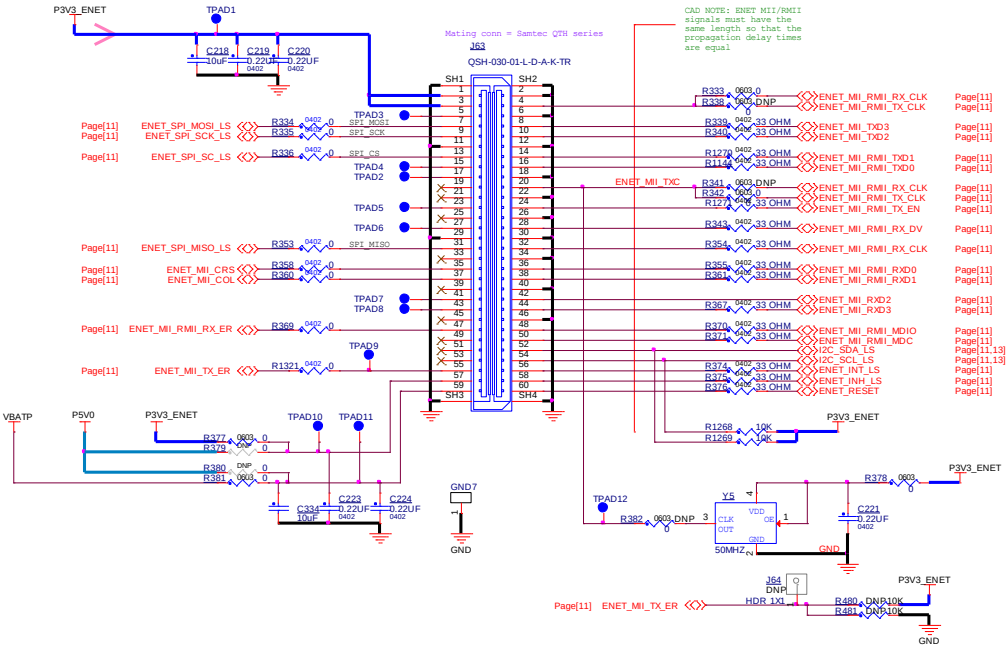


Figure 23. S32K3X4EVB-Q257 | S32K3X4EVBQ257ND – Ethernet MII/RMII Connector

Table 16. Ethernet MII/RMII Configuration

MODULE /FUNCTION	SIGNAL	MCU PORT	DESCRIPTION /COMMENT
MII/RMII	ENET_MII_RMII_RXD0	PTD9	All ports routed to the Ethernet MII/RMII signal are not connected to other interface in the EVB
	ENET_MII_RMII_RXD1	PTD8	
	ENET_MII_RXD2	PTC15	
	ENET_MII_RXD3	PTC14	
	ENET_MII_RMII_RX_CLK	PTC1	
	ENET_MII_RMII_RX_ER	PTC16	
	ENET_MII_RMII_RX_DV	PTC17	
	ENET_MII_RMII_TXD0	PTB5	
	ENET_MII_RMII_TXD1	PTB4	
	ENET_MII_TXD2	PTD6	
	ENET_MII_TXD3	PTD5	
	ENET_MII_RMII_TX_CLK	PTC0	
	ENET_MII_RMII_TX_EN	PTE9	
	ENET_MII_RMII_MDC	PTD17	
	ENET_MII_RMII_MDIO	PTD16	
	ENET_MII_COL	PTB23	
	ENET_MII_CRS	PTB22	

GPIOs	ENET_INH_LS	PTA26	
	ENET_INT_LS	PTA27	
	ENET_RESET	PTE5	As optional GPIO for a RESET on the ethernet connector is the PTE21, for this option, R439/0-Ohms must be placed.
LPSPIx	ENET_SPI_MISO_LS	PTC9	
	ENET_SPI_MOSI_LS	PTB1	
	ENET_SPI_SC_LS	PTC8	
	ENET_SPI_SCK_LS	PTB8	
I2C	I2C_SDA_LS	PTC6	
	I2C_SCL_LS	PTC7	
PWR	VBATP	+12V	P5V0 [+5.0V] can be routed to the Ethernet connector as optional power supply reference instead the VBATP reference. For this option, R380/0-Ohms must be placed and R381 must be removed.
	P3V3_ENET	+3.3V	P5V0 [+5.0V] can be routed to the Ethernet connector as optional power supply reference instead the P3V3_ENET reference. For this option, R380/0-Ohms must be placed and R381 must be removed.

Table 17. Ethernet Interface - Jumpers

	Reference	**Position**	**Description/Comment**
Ethernet Interface	**J32**	1-2	P3V3 domain is used to supply the Ethernet Interface
		OPEN	The Ethernet Interface is disabled
	J61	1-2	VDD_HV_B_PERH is routed to VDD_HV_B_ENET
		OPEN	The level Shifters for the Ethernet Interface are disabled

14 QSPI-A Configuration

The S32K3 EVB incorporates a MX25L6433F is 64Mb bits Serial NOR Flash memory, which is connected to the QSPIA Module of the S32K344 MCU.

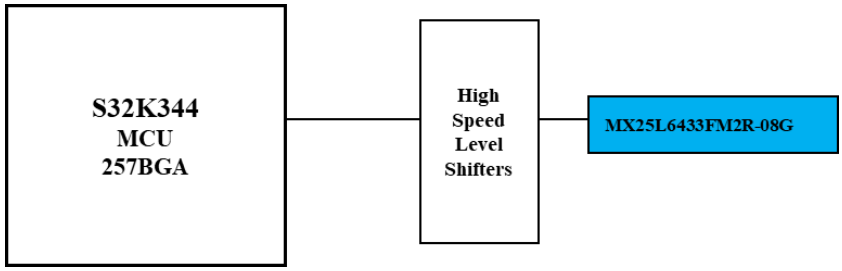


Figure 24. S32K3X4EVB-Q257 – CAN Physical Layer1 - TJA1153 Secure HS-CAN Transceiver

Table 18. QSPIA Memory Interface - Jumpers

	Reference	Position	Description/Comment
QSPI Interface	**J65**	1-2	P3V3 domain is used to supply the QSPIA Memory interface
		OPEN	The QSPIA Memory interface is disabled
	J402	1-2	VDD_HV_B_PERH is routed to VDD_HV_B_QSPI
		OPEN	The level Shifters for QSPIA Memory interface are disabled

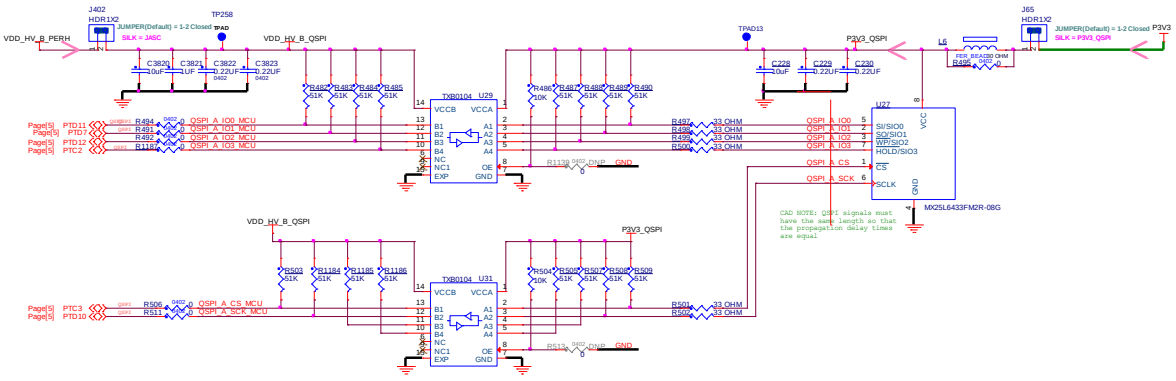


Figure 25. S32K3X4EVB-Q257 | S32K3X4EVBQ257ND – QSPIA Memory Interface

The table below details the signals configuration for the QSPI-A.

Module /Function	Signal	MCU PORT	DESCRIPTION /COMMENT
QSPIA	QSPI_A_IO0_MCU	PTD11	All MCU ports routed to the QSPIA Memory Interface are not connected to other interface in the EVB.
	QSPI_A_IO1_MCU	PTD7	
	QSPI_A_IO2_MCU	PTD12	
	QSPI_A_IO3_MCU	PTC2	
	QSPI_A_SCK_MCU	PTD10	
	QSPI_A_CS_MCU	PTC3	

15 User Peripherals

15.1 GPIO Matrix

A subset of available GPIO pins (available pins being those not already routed to the Ethernet connector and the QSPIA-Memory Interface) are available at the GPIO matrix as detailed below. The matrix provides an easy to follow, intuitive, space-saving grid of 0.1” header through-hole pads. Users can solder wires, fit headers, or simply insert a scope probe into the respective pad.

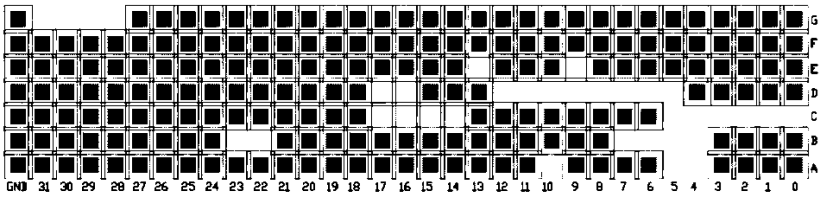


Figure 26. S32K3X4EVB-Q257 | S32K3X4EVBQ257ND – GPIO Matrix

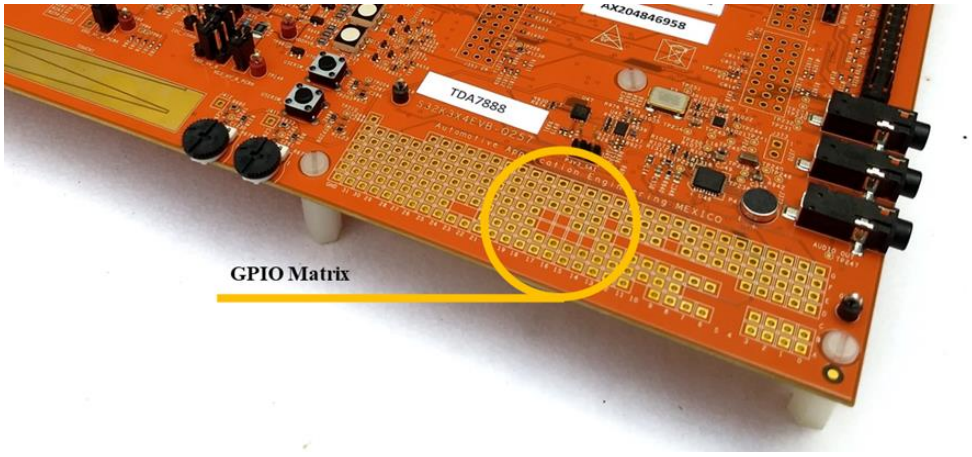


Figure 27. S32K3X4EVB-Q257 | S32K3X4EVBQ257ND – GPIO Matrix

15.2 User LED Indicators

There are 2 active high user RGB LED's are connected by NPN transistors to the MCU ports. The USERLEDs are connected as follows:

Table 19. User LED Indicators

Reference	Signal Name	MCU Port Default	Color	Comment
D32	RGBLED0_RED	PTA29	Red	Active High
	RGBLED0_GREEN	PTA30	Green	Active High
	RGBLED0_BLUE	PTA31	Blue	Active High
D33	RGBLED1_RED	PTB18	Red	Active High
	RGBLED1_GREEN	PTB25	Green	Active High
	RGBLED1_BLUE	PTE12	Blue	Active High
		PTB24		Disabled

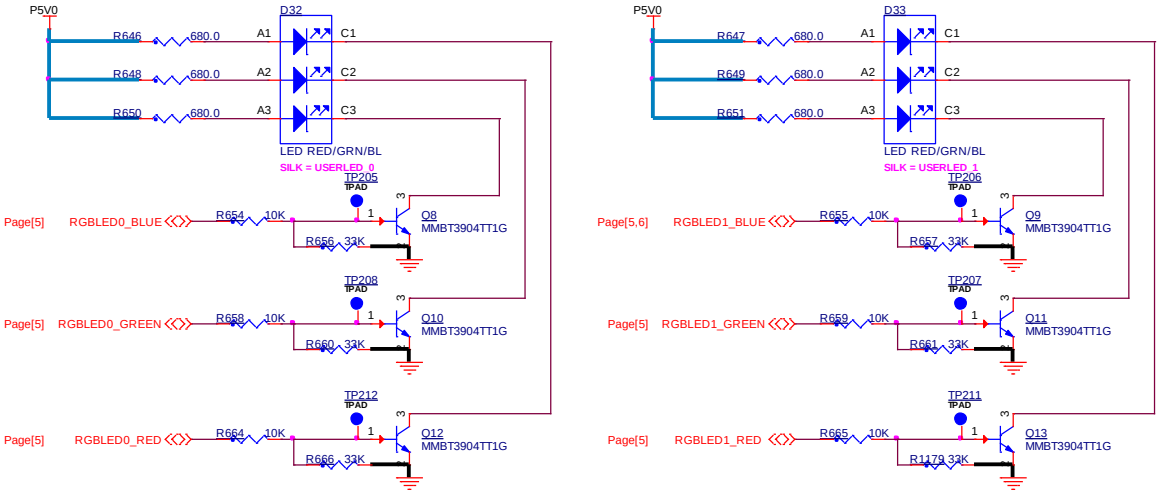


Figure 28. S32K3X4EVB-Q257 | S32K3X4EVBQ257ND – User LED indicators

15.3 User Pushbuttons

There are 2 push-buttons active to high (pulled low, driven to VDD_HV_A and VDD_HV_B), the push button switches (SW4 and SW5) connected to MCU ports. The switches are connected as follows:

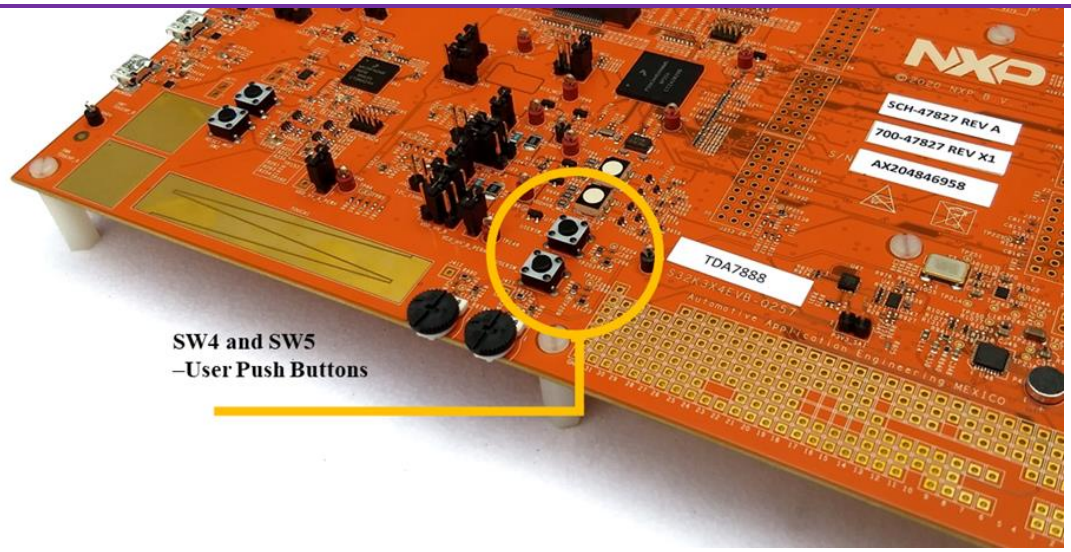


Figure 29. S32K3X4EVB-Q257 | S32K3X4EVBQ257ND – User Pushbuttons

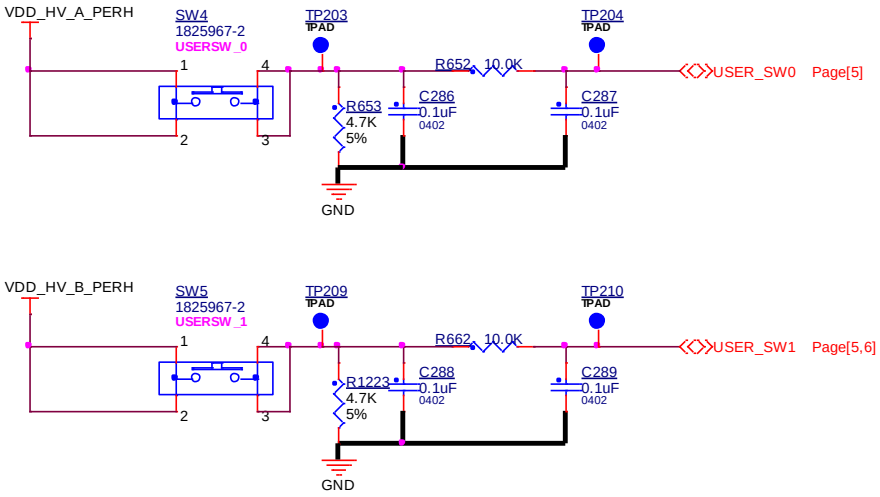


Figure 30. S32K3X4EVB-Q257 | S32K3X4EVBQ257ND – User Pushbuttons

Table 20. User Pushbuttons

Reference	Function	MCU Port	Comments
SW4	USER_SW0	PTB26	Active to HIGH
SW5	USER_SW1	PTB19	Enabled as DEFAULT
		PTF31	Disabled
		PTC18	Disabled

1. There are zero-ohm resistors on the direct connections between each **USER_SWx** and the MCU pins. These can be removed if required to isolate or change the User Switch from the default MCU pin.

15.4 ADC Rotary Potentiometers

The EVB incorporates a couple of ADC Rotary Potentiometer [which routes a voltage between 0v to VD_HV_A] directly connected to ADC Precise Input Chanel of the S32K3XX Microcontroller.

Table 21. ADC Potentiometers

Reference	Function	MCU Port	Comments
R672	ADC_POT0	PTA11	Enabled as DEFAULT
		PTA9	Disabled
R679	ADC_POT1	PTA17	Enabled as DEFAULT

NOTE

1. There are zero-ohm resistors on the direct connections between each USERSW and the MCU pins. These can be removed if required to isolate or change the User Switch from the default MCU pin.

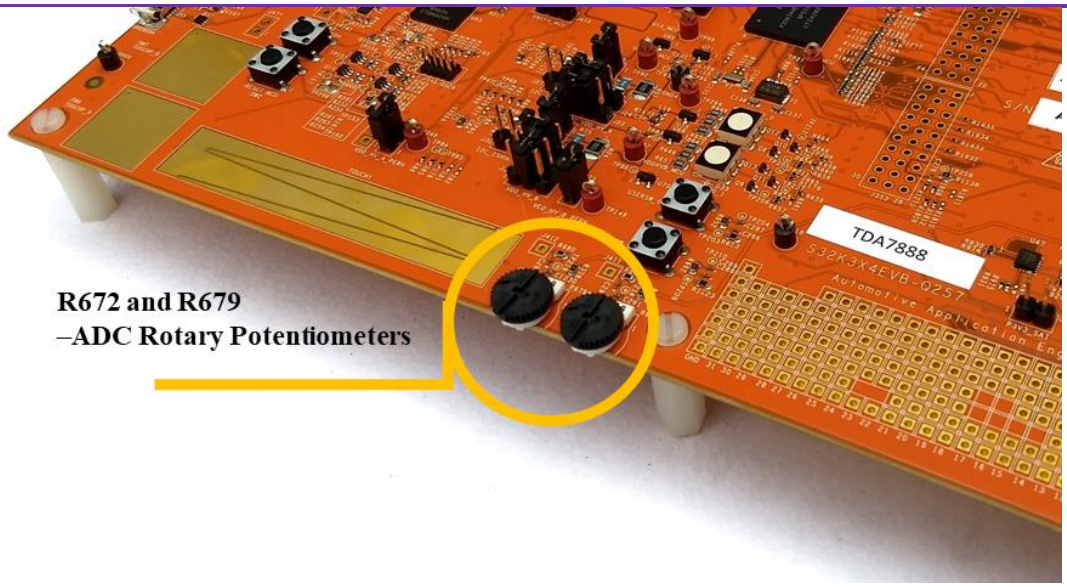


Figure 31. S32K3X4EVB-Q257 | S32K3X4EVBQ257ND – ADC Rotary Potentiometers

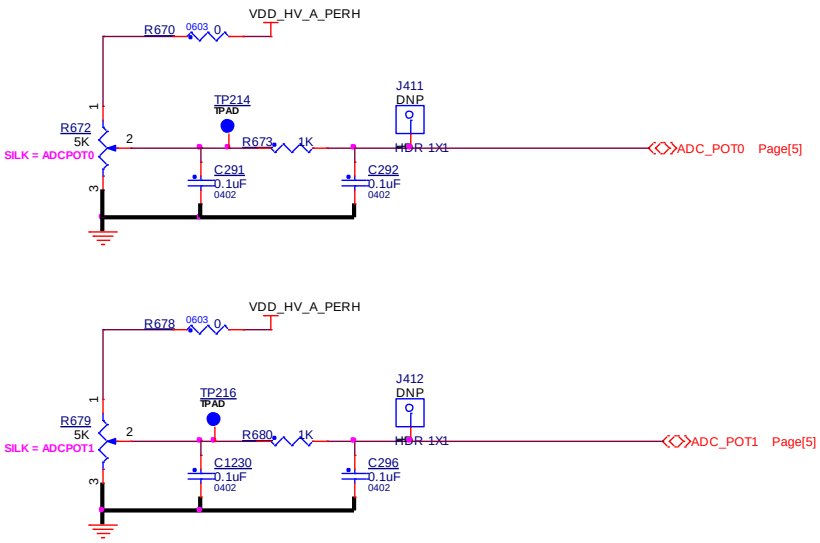


Figure 32. S32K3X4EVB-Q257 | S32K3X4EVBQ257ND – ADC Rotary Potentiometers

16 Default Jumpers

Table 22. Default Jumper Configuration

Interface	Reference	Position	Description / Comments
FS26x SBC Power Supply	**J13**	1-2	FS26_VLDO1 [+5.0V] is routed to P5V0 domain
	J16	1-2	FS26_VLDO2 [+3.3V] is routed to P3V3 domain
	J686	1-2	Flash Mode – configuration in the FS26
	J685	1-2	
USB to UART Interface	**J57**	1-2	P5V0_USBSER domain is routed to P5V0 for the USB Self Powered Configuration
	J60	2-3	The Reset# pin is routed to the divider resistor for the USB Self Powered Configuration
Ethernet Interface	**J61**	1-2	VDD_HV_B reference is routed for the VDD_HV_B_ENET reference
	J62	1-2	P3V3 domain is routed to P3V3_ENET
QSPI Interface	**J65**	1-2	P3V3 domain is used to supply the QSPIA interface
	J402	1-2	VDD_HV_B_PERH is routed to VDD_HV_B_QSPI
S32K3XX MCU Power Supply	**J23**	1-2	P5V0 (+5.0V from the FS26) is selected for the VDD_HV_A_MCU reference.
	J24	2-3	The shunt resistor R58 [1 Ohms] is selected for current measurement on the VDD_HV_A_MCU reference.
	J25	1-2	VDD_HV_A is routed to VDD_HV_A_MCU reference. A jumper on this position disables the shunt resistors R57 and R58 are disabled for current measurement proposals.
	J30	3-4	P3V3 (+3.3V from the FS26) is selected for the VDD_HV_B_MCU reference.
	J29	2-3	The shunt resistor R75 [1 Ohms] is selected for current measurement on the VDD_HV_B_MCU reference.

	J31	1-2	VDD_HV_B is routed to VDD_HV_B_MCU reference. A jumper on this position disables the shunt resistors R74 and R75 are disabled for current measurement proposals.
	J37	2-3	The VDD_HV_B domain is routed to the collector terminal in order to supply the NPN external Ballast transistor for V15_MCU domain
	J360	5-6	The NPN external Ballast transistor is selected to supply the V15_MCU domain.
	J375	1-2	VDD_HV_B is routed to VDD_HV_B_PERH
	J374	1-2	VDD_HV_A is routed to VDD_HV_A_PERH
	J410	1-2	VDD_HV_A_MCU is routed to VDD_REFH
User Peripherals	**J670**	1-2	PTE0 is routed to the ARDUINO shield connectors
	J671	2-3	PTA9 is routed to the ARDUINO shield connectors
	J321	1-2	VDD_HV_A_PERH is routed to VDD_IO
LIN Interface	**J390**	1-2	LIN1 Physical layer – LIN1 is enabled
	J674	3-4	INH function is routed to LIN1 pullup circuitry for Master configuration
	J678	1-2	LIN2 Physical layer – LIN2 is enabled
	J679	3-4	INH function is routed to LIN2 pullup circuitry for Master configuration
CAN Interface	**J413**	1-2	CAN0 Physical Layer is enabled. VBATP_SW is routed/turning-ON the TJA1153 -U55
	J672	1-2	CAN1 Physical Layer is enabled. VBATP_SW is routed/turning-ON the TJA1153 -U64

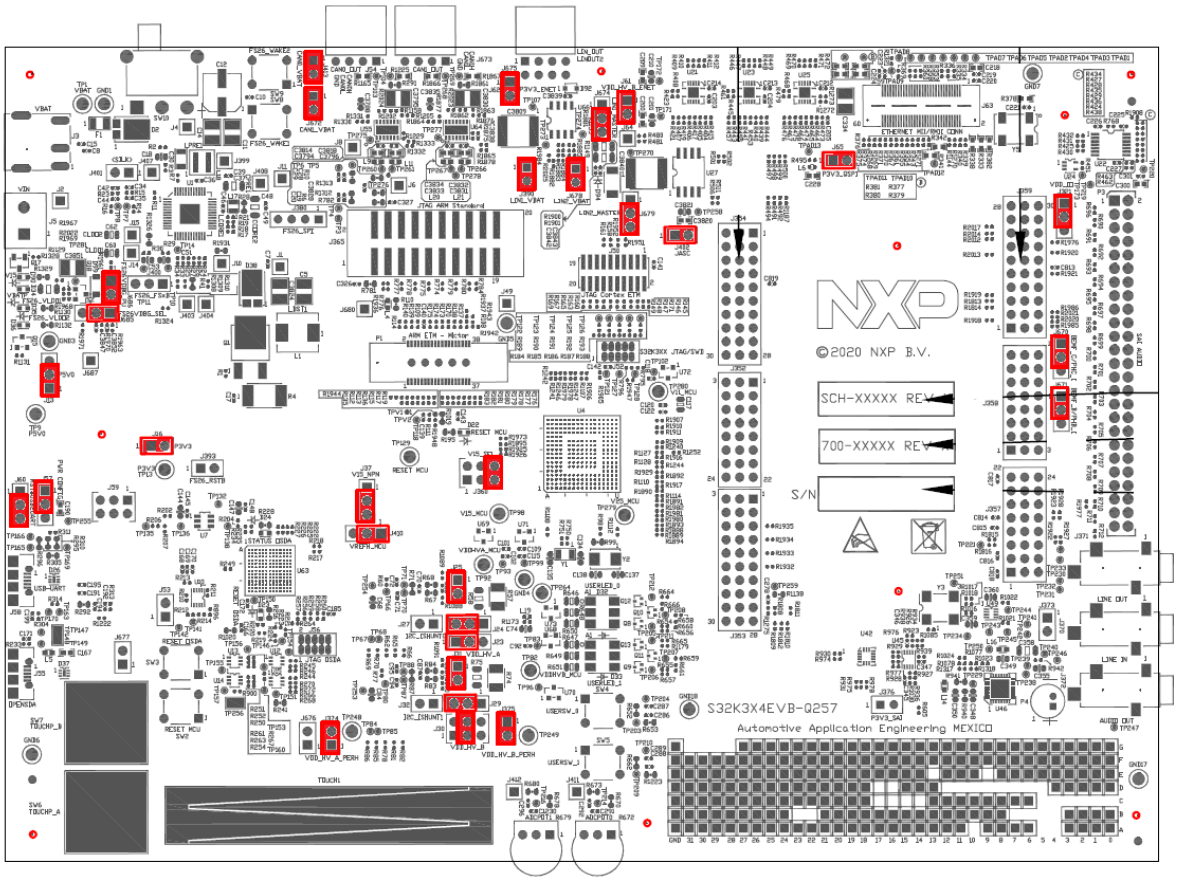


Figure 33. S32K3X4EVB-Q257 | S32K3X4EVBQ257ND – Default jumpers' configuration

17 Revision history

Table 23. Revision history

Document Revision	Date	Board Name	Schematic/ Board Number	Schematic/ Board Revision	Changes	Author
A	08/2021	S32K3X4EVB-Q257	47827	A	Infernal DRAFT	Jesús Sánchez
B	09/2021	S32K3X4EVB-Q257	47827	A	Release version	
		S32K3X4EVBQ257ND	53189	A		

18 Legal Information

18.1 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

18.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Suitability for use in automotive applications — This NXP Semiconductors product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — While NXP Semiconductors has implemented advanced security features, all products may be subject to unidentified vulnerabilities. Customers are responsible for the design and operation of their applications and products to reduce the effect of these vulnerabilities on customer's applications and products, and NXP Semiconductors accepts no liability for any vulnerability that is discovered. Customers should implement appropriate design and operating safeguards to minimize the risks associated with their applications and products.

18.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.