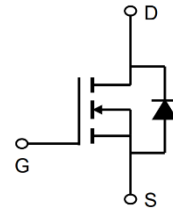


**Description**

The AP10N65F/P is silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.



**General Features**

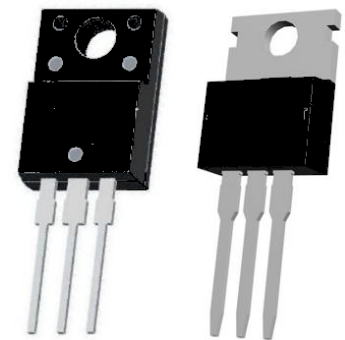
$V_{DS} = 650V$   $I_D = 10A$

$R_{DS(ON)} < 0.9\Omega$  @  $V_{GS}=10V$  (Type:  $0.75\Omega$ )

**Application**

Uninterruptible Power Supply(UPS)

Power Factor Correction (PFC)



**Absolute Maximum Ratings ( $T_C=25^\circ C$  unless otherwise noted)**

Symbol	Parameter	Value		Unit
		TO-220F	TO-220	
VDSS	Drain-Source Voltage ( $V_{GS} = 0V$ )	650		V
ID	Continuous Drain Current	10		A
IDM	Pulsed Drain Current (note1)	58		A
VGS	Gate-Source Voltage	$\pm 30$		V
EAS	Single Pulse Avalanche Energy (note2)	426		mJ
IAR	Avalanche Current (note1)	9		A
EAR	Repetitive Avalanche Energy note1)	41		mJ
PD	Power Dissipation ( $T_C = 25^\circ C$ )	32.1		W
TJ, Tstg	Operating Junction and Storage Temperature Range	-55~+150		$^\circ C$
RthJC	Thermal Resistance, Junction-to-Case	4.46		$^\circ C/W$
RthJA	Thermal Resistance, Junction-to-Ambient	46.7		$^\circ C/W$

**650V N-Channel Enhancement Mode MOSFET**

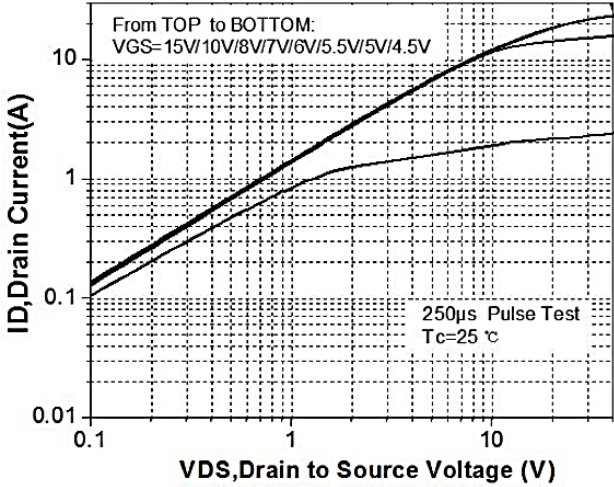
**Electrical Characteristics (T<sub>J</sub>=25°C, unless otherwise noted)**

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V(BR)DSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	650	685	--	V
IDSS	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 650V, V <sub>GS</sub> = 0V, T <sub>J</sub> =25°C	--	--	1	μA
IGSS	Gate-Source Leakage	V <sub>GS</sub> = ±30V	--	--	±100	nA
VGS(th)	Gate-Source Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	2.0	--	4.0	V
RDS(on)	Drain-Source On-Resistance (Note3)	V <sub>GS</sub> = 10V, I <sub>D</sub> = 3.5A	--	0.75	0.9	Ω
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 25V, f = 1.0MHz	--	1037	--	pF
C <sub>oss</sub>	Output Capacitance		--	138	--	
C <sub>rss</sub>	Reverse Transfer Capacitance		--	5.3	--	
Q <sub>g</sub>	Total Gate Charge	V <sub>DD</sub> =520V, I <sub>D</sub> = 9A, V <sub>GS</sub> = 10V	--	19	--	nC
Q <sub>gs</sub>	Gate-Source Charge		--	7.3	--	
Q <sub>gd</sub>	Gate-Drain Charge		--	8.5	--	
td(on)	Turn-on Delay Time	V <sub>DD</sub> =325V, I <sub>D</sub> = 7A, R <sub>G</sub> = 25Ω	--	18	--	ns
t <sub>r</sub>	Turn-on Rise Time		--	30	--	
td(off)	Turn-off Delay Time		--	61	--	
t <sub>f</sub>	Turn-off Fall Time		--	36	--	
I <sub>S</sub>	Continuous Body Diode Current	T <sub>C</sub> = 25 °C	--	--	9.0	A
I <sub>SM</sub>	Pulsed Diode Forward Current		--	--	36	A
V <sub>SD</sub>	Body Diode Voltage	T <sub>J</sub> = 25°C, I <sub>SD</sub> = 7A, V <sub>GS</sub> = 0V	--	--	1.2	V
trr	Reverse Recovery Time	V <sub>GS</sub> = 0V, I <sub>S</sub> = 7A, di <sub>F</sub> /dt = 100A/μs	--	431	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge		--	2.6	--	μC

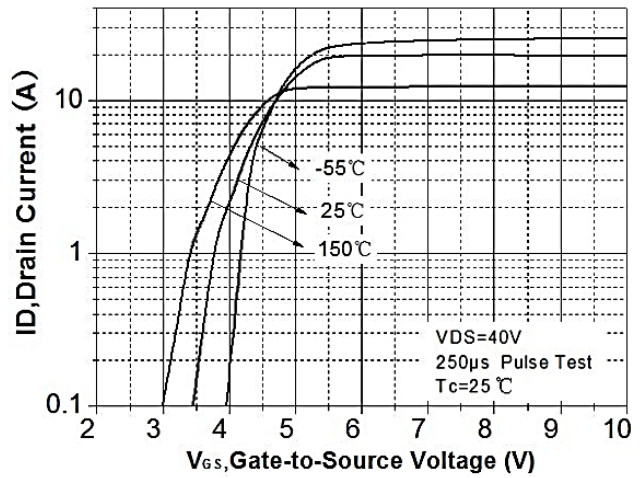
**Note :**

- 1、 The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.
- 2、 The EAS data shows Max. rating . I<sub>AS</sub> = 9.0A, V<sub>DD</sub> = 50V, R<sub>G</sub> = 25 Ω, Starting T<sub>J</sub> = 25 °C
- 3、 The test condition is Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 1%
- 4、 The power dissipation is limited by 150°C junction temperature
- 5、 The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

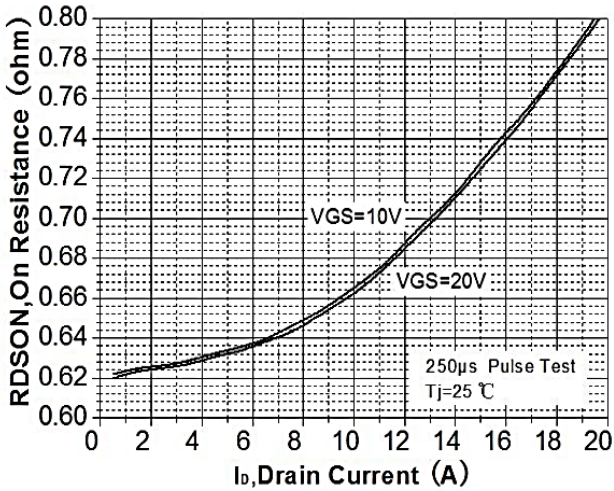
**Typical Characteristics**



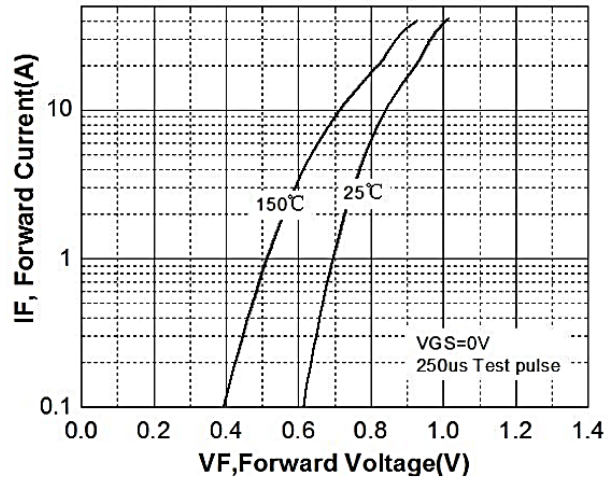
**Figure 1. On-Region Characteristics**



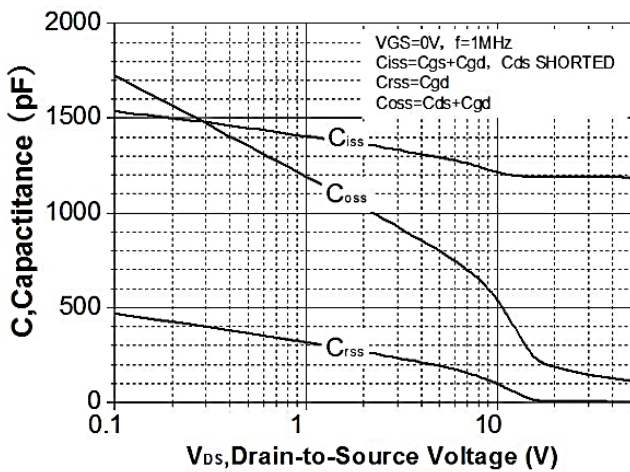
**Figure 2. Transfer Characteristics**



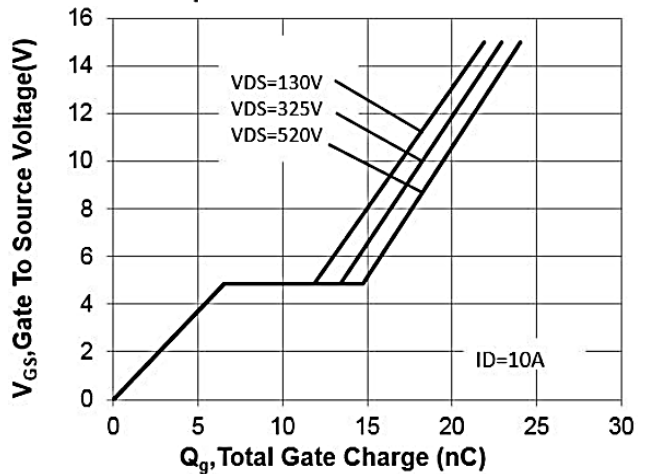
**Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage**



**Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature**



**Figure 5. Capacitance Characteristics**



**Figure 6. Gate Charge Characteristics**

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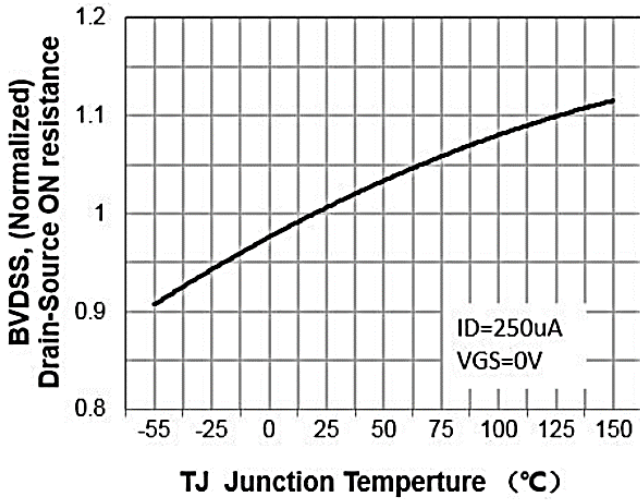


Figure 7. Breakdown Voltage Variation vs Temperature

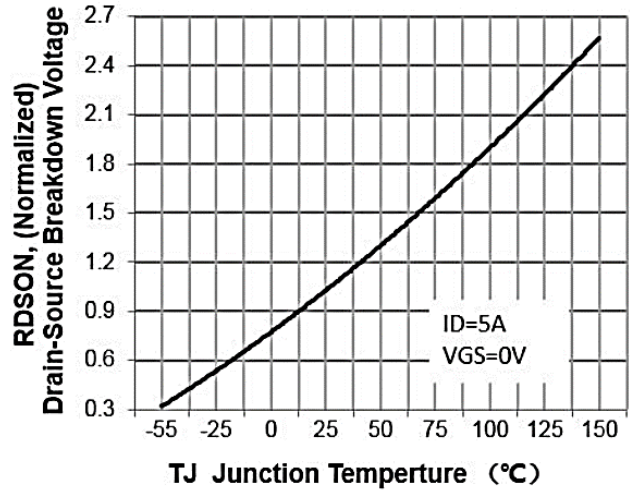


Figure 8. On-Resistance Variation vs Temperature

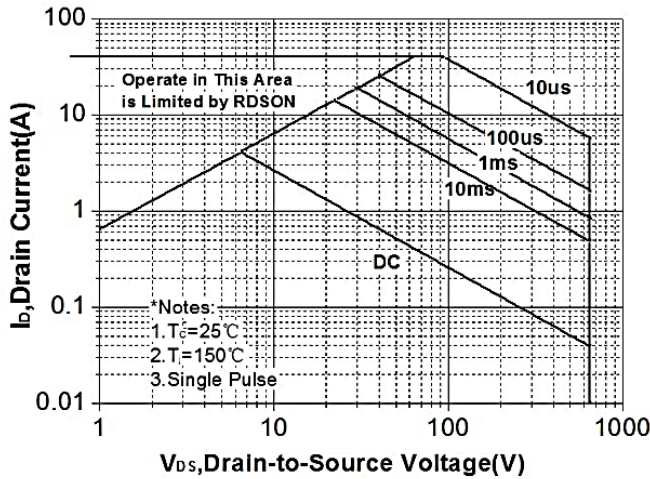


Figure 9. Maximum Safe Operating Area

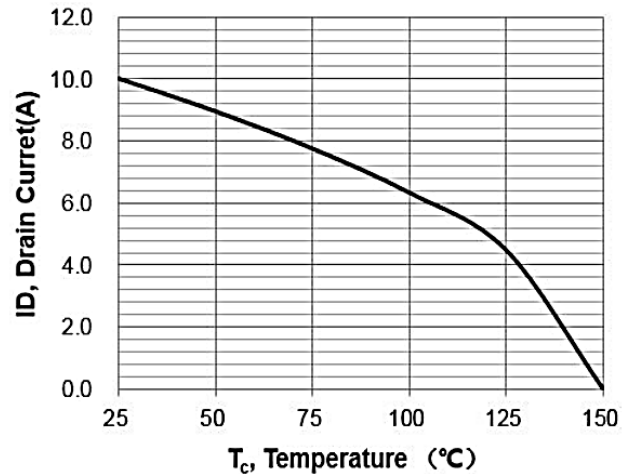


Figure 10. Maximum Drain Current vs Case Temperature

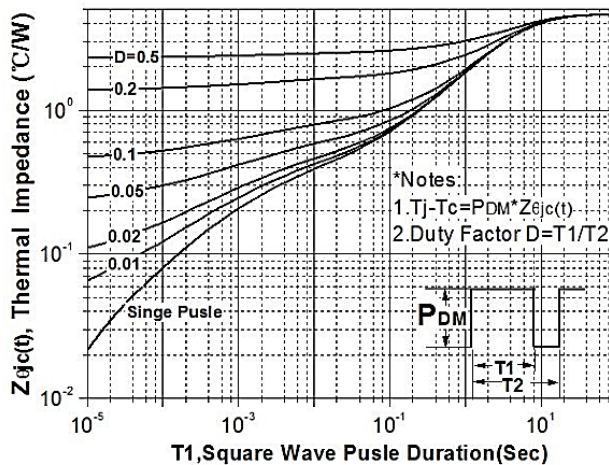


Figure 11. Transient Thermal Response Curve

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