

TC7WBL3305CFK, TC7WBL3306CFK

1. Functional Description

- Low-Voltage, Low-Capacitance Dual Bus Switch

2. General

The TC7WBL3305CFK and TC7WBL3306CFK are Low Voltage/Low Capacitance CMOS 2bit Bus Switches. The low ON-resistance of the switch allows connections to be made with minimal propagation delay time.

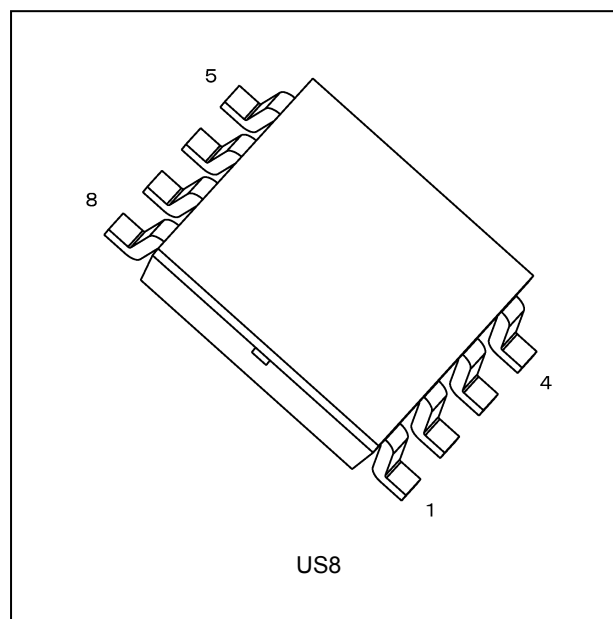
The TC7WBL3306CFK requires the output enable (\overline{OE}) input to be set high to place the output into the high impedance state, whereas the TC7WBL3305CFK requires the output enable (OE) input to be set low to place the output into the high impedance.

All inputs are equipped with protection circuits against static discharge.

3. Features

- (1) Operating voltage: $V_{CC} = 1.65$ to 3.6 V
- (2) ON capacitance: $C_{I/O} = 7$ pF Switch On (typ.) @ $V_{CC} = 3.0$ V
- (3) ON resistance: $R_{ON} = 6.0$ Ω (typ.) @ $V_{CC} = 3.0$ V, $V_{IS} = 0$ V
- (4) ESD performance: Machine model $\geq \pm 200$ V
Human body model $\geq \pm 2000$ V
- (5) Power-down protection for inputs (OE and \overline{OE} , I/O)
- (6) Package: US8

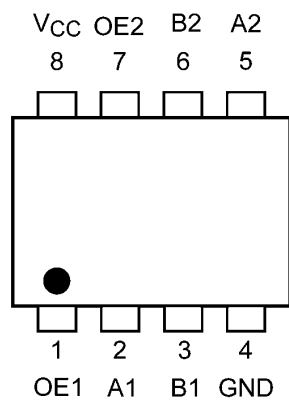
4. Packaging



Start of commercial production
2009-03

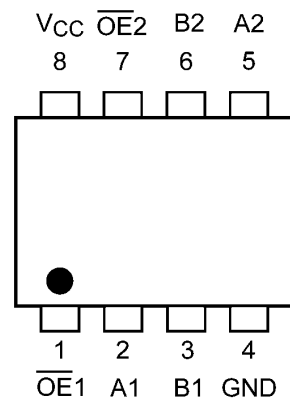
5. Pin Assignment

TC7WBL3305CFK



(Top view)

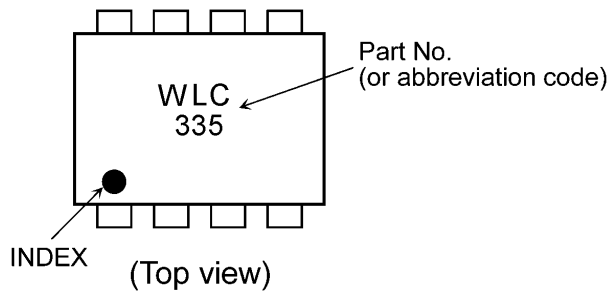
TC7WBL3306CFK



(Top view)

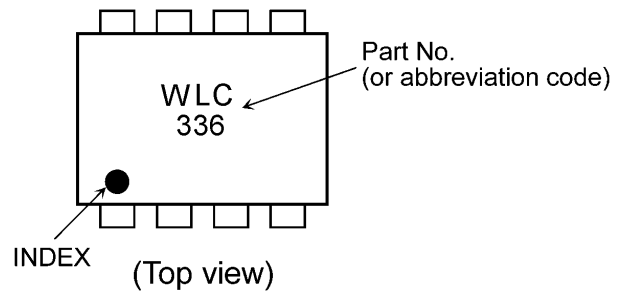
6. Marking

TC7WBL3305CFK



(Top view)

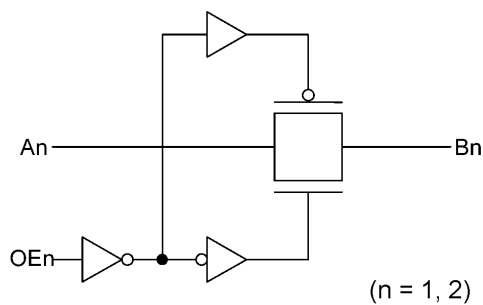
TC7WBL3306CFK



(Top view)

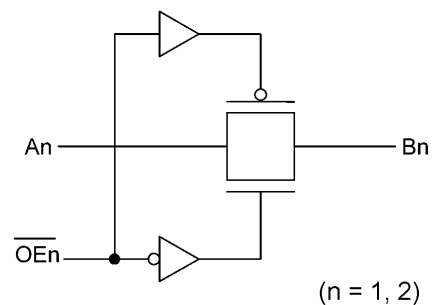
7. Block Diagram

TC7WBL3305CFK



(n = 1, 2)

TC7WBL3306CFK



(n = 1, 2)

8. Truth Table

| Inputs OE (TC7WBL3305CFK) | Inputs \overline{OE} (TC7WBL3306CFK) | Function |
|------------------------------|---|-----------------|
| H | L | A port = B port |
| L | H | Disconnect |

9. Absolute Maximum Ratings (Note)

| Characteristics | Symbol | Test Condition | Rating | Unit |
|--------------------------------------|------------------|---------------------------------------|------------------------|--------------------|
| Supply voltage | V_{CC} | | -0.5 to 4.6 | V |
| Input voltage (OE, \overline{OE}) | V_{IN} | | -0.5 to 4.6 | V |
| Switch I/O voltage | V_S | $V_{CC} = 0\text{ V}$ or Switch = Off | -0.5 to 4.6 | V |
| | | Switch = On | -0.5 to $V_{CC} + 0.5$ | |
| Clamp diode current | I_{IK} | | -50 | mA |
| Switch I/O current | I_S | | 50 | mA |
| Power dissipation | P_D | | 200 | mW |
| V_{CC} /ground current | I_{CC}/I_{GND} | | ± 100 | mA |
| Storage temperature | T_{stg} | | -65 to 150 | $^{\circ}\text{C}$ |

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

10. Operating Ranges (Note)

| Characteristics | Symbol | Test Condition | Rating | Unit |
|--------------------------------------|-----------|---------------------------------------|---------------|--------------------|
| Supply voltage | V_{CC} | | 1.65 to 3.6 | V |
| Input voltage (OE, \overline{OE}) | V_{IN} | | 0 to 3.6 | V |
| Switch I/O voltage | V_S | $V_{CC} = 0\text{ V}$ or Switch = Off | 0 to 3.6 | V |
| | | Switch = On | 0 to V_{CC} | |
| Operating temperature | T_{opr} | | -40 to 85 | $^{\circ}\text{C}$ |
| Input rise time | dt/dv | | 0 to 10 | ns/V |

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused control inputs must be tied to either V_{CC} or GND.

11. Electrical Characteristics

11.1. DC Characteristics (Unless otherwise specified, $T_a = -40$ to 85 °C)

| Characteristics | Symbol | Note | Test Condition | V_{CC} (V) | Min | Typ. | Max | Unit |
|---|-----------|-----------------------|--|--------------|---------------------|------|---------------------|----------|
| High-level input voltage (OE, \overline{OE}) | V_{IH} | | — | 1.65 to 3.6 | $0.7 \times V_{CC}$ | — | — | V |
| Low-level input voltage (OE, \overline{OE}) | V_{IL} | | — | 1.65 to 3.6 | — | — | $0.3 \times V_{CC}$ | V |
| Input leakage current (OE, \overline{OE}) | I_{IN} | | $V_{IN} = 0$ to 3.6 V | 1.65 to 3.6 | — | — | ± 1.0 | μA |
| Power-OFF leakage current | I_{OFF} | | OE, \overline{OE} , A, B = 0 to 3.6 V | 0 | — | — | 10 | μA |
| Switch OFF-state leakage current | I_{SZ} | | A, B = 0 V to V_{CC} , OE = GND (TC7WBL3305CFK), OE = V_{CC} (TC7WBL3306CFK) | 1.65 to 3.6 | — | — | ± 1.0 | μA |
| ON-resistance | R_{ON} | (Note 1), (Note 2) | $V_{IS} = 0$ V, $I_{IS} = 30$ mA | 3.0 | — | 6.0 | 10.5 | Ω |
| | | | $V_{IS} = 3.0$ V, $I_{IS} = 30$ mA | 3.0 | — | 11 | 17 | |
| | | | $V_{IS} = 2.4$ V, $I_{IS} = 15$ mA | 3.0 | — | 12 | 19 | |
| | | | $V_{IS} = 0$ V, $I_{IS} = 24$ mA | 2.3 | — | 6.5 | 12 | |
| | | | $V_{IS} = 2.3$ V, $I_{IS} = 24$ mA | 2.3 | — | 13 | 21 | |
| | | | $V_{IS} = 2.0$ V, $I_{IS} = 15$ mA | 2.3 | — | 15 | 22 | |
| | | | $V_{IS} = 0$ V, $I_{IS} = 4$ mA | 1.65 | — | 8 | 14 | |
| | | | $V_{IS} = 1.65$ V, $I_{IS} = 4$ mA | 1.65 | — | 18 | 27 | |
| Quiescent supply current | I_{CC} | | $V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0$ A | 3.6 | — | — | 10 | μA |

Note 1: All typical values are at $T_a = 25$ °C.

Note 2: Measured by the voltage drop between A and B pins at the indicated current through the switch. On-resistance is determined by the lower of the voltages on the two (A or B) pins.

11.2. AC Characteristics (Unless otherwise specified, $T_a = -40$ to 85 °C)

| Characteristics | Symbol | Test Condition | V_{CC} (V) | Min | Max | Unit |
|---------------------|--------------------|--|----------------|-----|-----|------|
| Output enable time | t_{PZL}, t_{PZH} | See Fig. 11.2.1, 11.2.2, Table 11.2.1 | 3.3 ± 0.3 | — | 6 | ns |
| | | | 2.5 ± 0.2 | — | 7 | |
| | | | 1.8 ± 0.15 | — | 10 | |
| Output disable time | t_{PLZ}, t_{PHZ} | See Fig. 11.2.1, 11.2.2, Table 11.2.1 | 3.3 ± 0.3 | — | 6 | ns |
| | | | 2.5 ± 0.2 | — | 7 | |
| | | | 1.8 ± 0.15 | — | 10 | |

11.3. Capacitive Characteristics (Note) (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$)

| Characteristics | Symbol | Test Condition | V_{CC} (V) | Typ. | Unit |
|---------------------------------|-----------|---|--------------|------|------|
| Input capacitance | C_{IN} | $V_{IN} = 0\text{ V}$ | 3.0 | 4 | pF |
| Switch terminal OFF-capacitance | $C_{I/O}$ | $\overline{OE} = \text{GND}$ (TC7WBL3305CFK), $\overline{OE} = V_{CC}$ (TC7WBL3306CFK), $V_{IS} = 0\text{ V}$ | 3.0 | 3.5 | pF |
| Switch terminal ON-capacitance | $C_{I/O}$ | $\overline{OE} = V_{CC}$ (TC7WBL3305CFK), $\overline{OE} = \text{GND}$ (TC7WBL3306CFK), $V_{IS} = 0\text{ V}$ | 3.0 | 7 | pF |

Note: Parameter guaranteed by design.

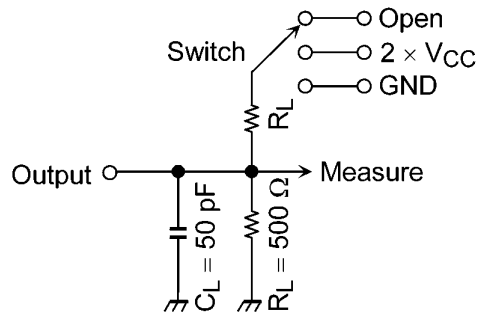


Fig. 11.2.1 AC Test Circuit

Table 11.2.1 Parameter for AC Test Circuit

| Parameter | Switch |
|-----------------------|-------------------|
| t_{PLZ} , t_{PZL} | $2 \times V_{CC}$ |
| t_{PHZ} , t_{PZH} | GND |

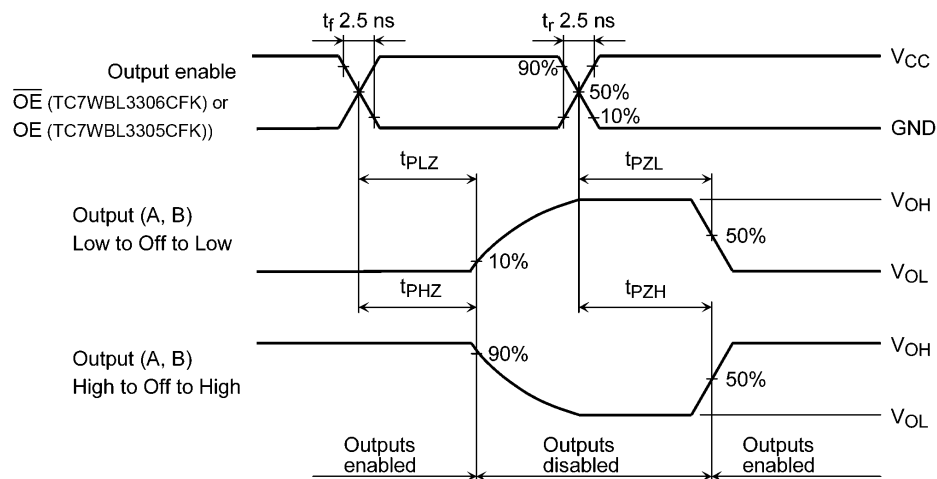


Fig. 11.2.2 AC Waveform t_{PLZ} , t_{PHZ} , t_{PZL} , t_{PZH}

12. Rise and Fall Time (t_r/t_f)

The $t_{r(out)}$ and $t_{f(out)}$ values of the output signals are affected by the CR time constant of the input, which consists of the switch terminal capacitance ($C_{I/O}$) and the on-resistance (R_{ON}) of the input.

In practice, the $t_{r(out)}$ and $t_{f(out)}$ values are also affected by the circuit's capacitance and resistance components other than those of the TC7WBL3305CFK, TC7WBL3306CFK.

The $t_{r(out)}/t_{f(out)}$ values can be approximated as follows. (Figure 12.1, Table 12.1 shows the test circuit.)

$$t_{r(out)}/t_{f(out)} \text{ (approx)} = - (C_{I/O} + C_L) \cdot (R_{DRIVE} + R_{ON}) \cdot \ln ((V_{OH} - V_{OL}) - V_M) / (V_{OH} - V_{OL})$$

Where, R_{DRIVE} is the output impedance of the previous-stage circuit.

Calculation example:

$$t_{r(out)} \text{ (approx)} = - (7 + 15) \text{ E} - 12 \cdot (120 + 6) \cdot \ln (((3.0 - 0) - 1.5) / (3.0 - 0)) \approx 1.9 \text{ ns}$$

Calculation conditions:

$V_{CC} = 3.0 \text{ V}$, $C_L = 15 \text{ pF}$, $R_{DRIVE} = 120 \Omega$ (output impedance of the previous IC), $V_M = 1.5 \text{ V}$ ($V_{CC}/2$)

Output of the previous IC = digital (i.e., high-level voltage = V_{CC} , low-level voltage = GND)

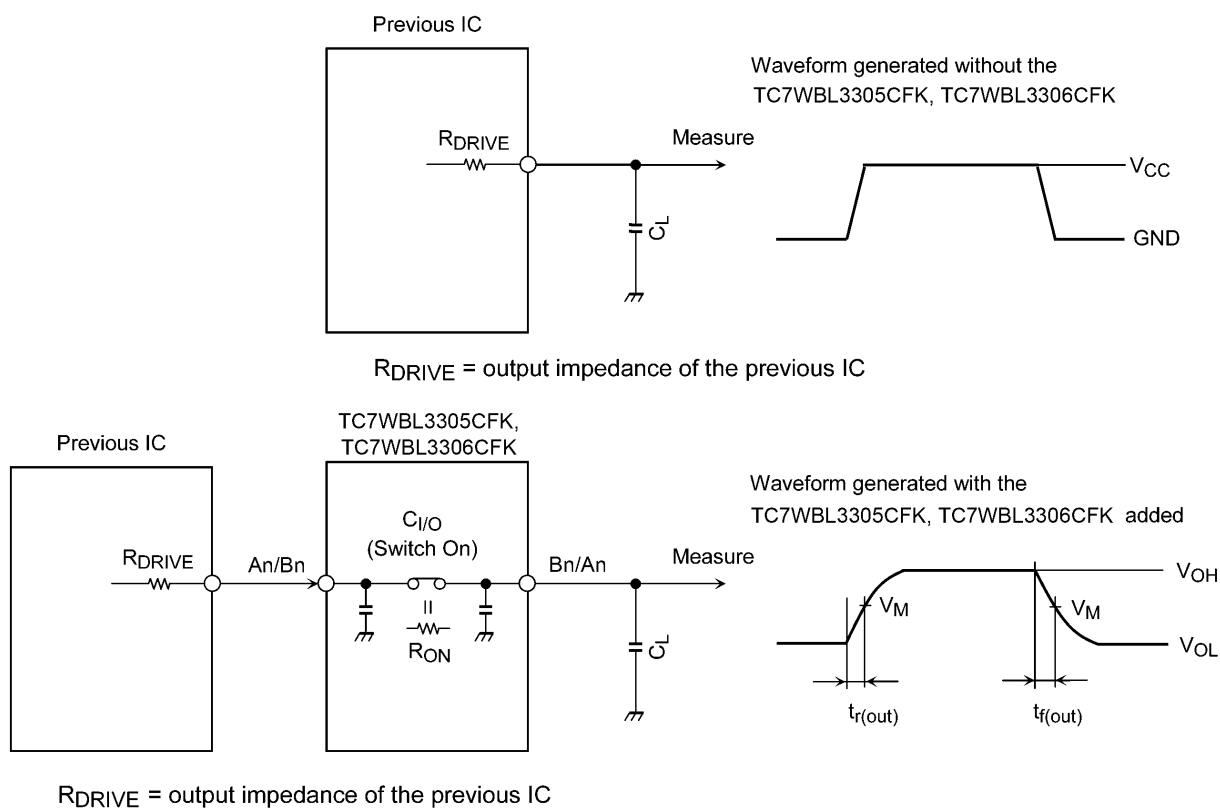


Fig. 12.1 Calculation Circuit

Table 12.1 Calculation Circuit

| Characteristics | $V_{CC} = 3.3 \pm 0.3 \text{ V}$ | $V_{CC} = 2.5 \pm 0.2 \text{ V}$ | $V_{CC} = 1.8 \pm 0.15 \text{ V}$ |
|-----------------|----------------------------------|----------------------------------|-----------------------------------|
| V_M | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ |

13. Characteristics Curves (Note)

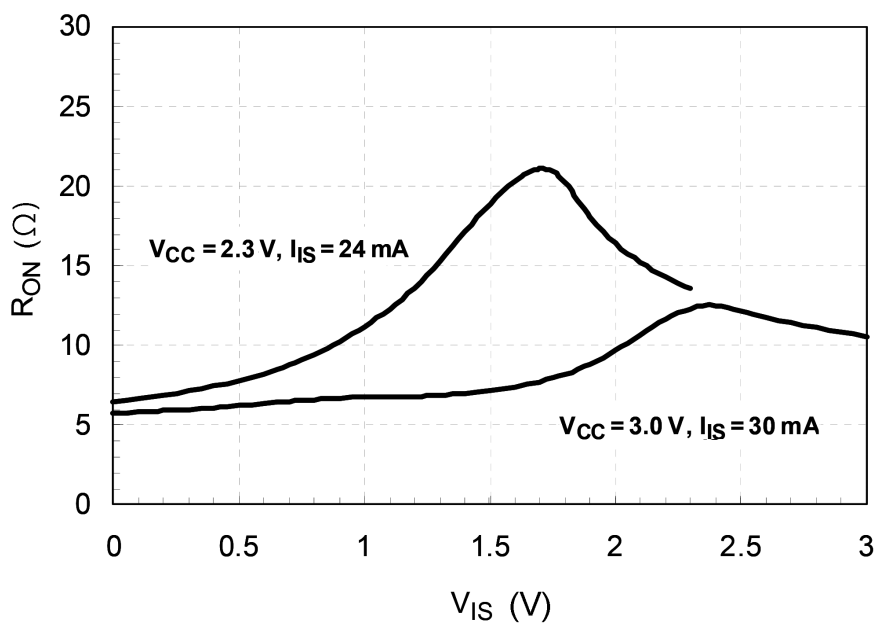
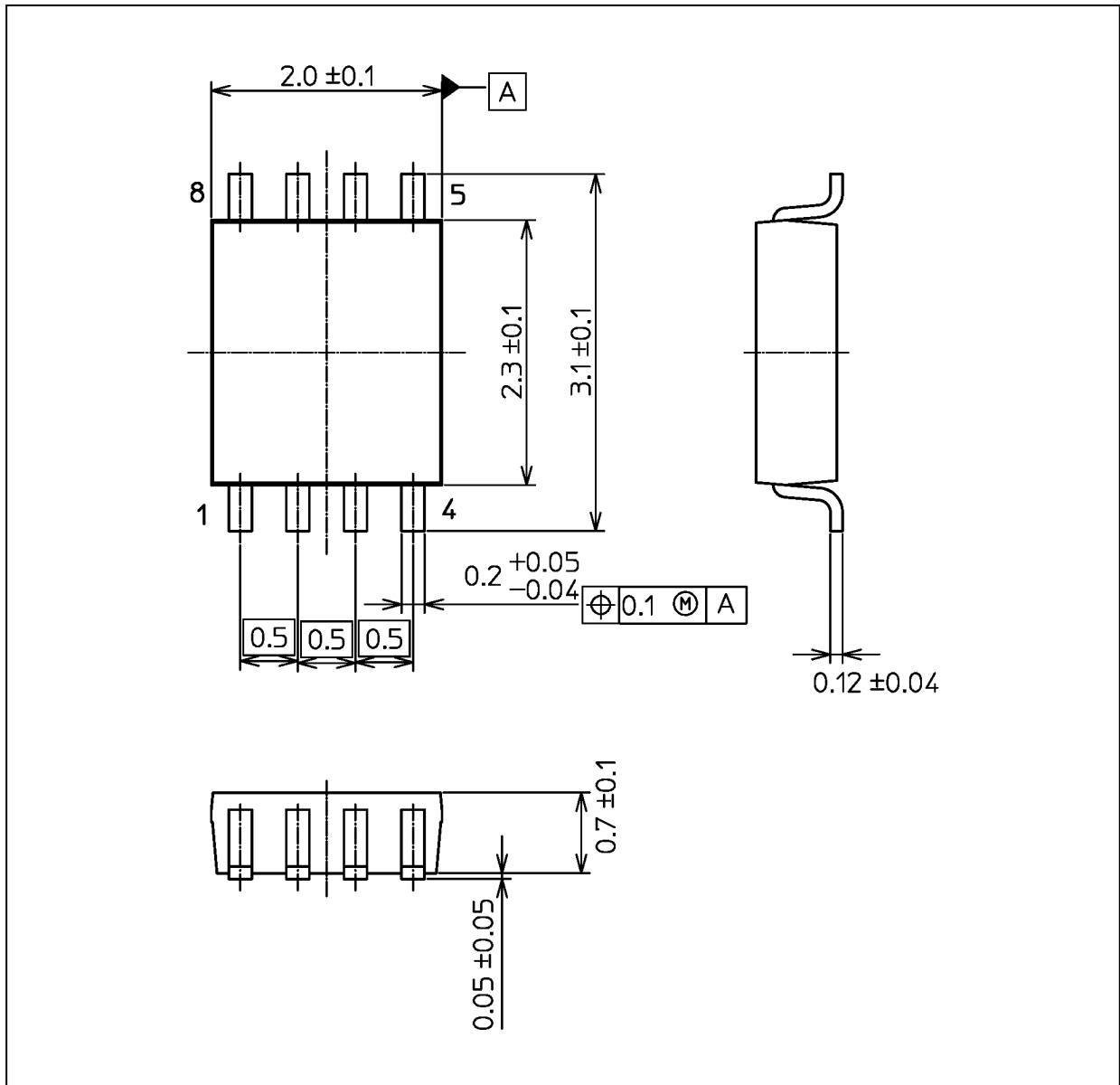


Fig. 13.1 $R_{ON} - V_{IS}$ ($T_a = 25\text{ }^\circ\text{C}$)

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

Package Dimensions

Unit: mm



Weight: 0.01 g (typ.)

| Package Name(s) |
|-----------------|
| JEDEC: SOT-765 |
| Nickname: US8 |

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