NXP Semiconductors
User Guide

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S32G-VNP-EVB3 User Guide

by: NXP Semiconductors

1. Introduction

S32G is a high-performance vehicle network processor that combines controller area network (CAN), local interconnect network (LIN), and FlexRay networking with high data-rate Ethernet networking. It also combines a functional safe-core infrastructure with MPU cores, and includes high level security features.

A platform for software development on S32G is available from NXP, named the S32G Vehicle Network Processor Evaluation Board (S32G-VNP-EVB3). This hardware supports the most common S32G use cases primarily by enabling the communication interfaces to allow users to rapidly prototype software using the features of S32G-VNP-EVB3.

This user guide provides detailed reference for usage of the S32G-VNP-EVB3. This includes detailed board configuration including connectors, jumpers, LED indicators and S32G on-board programming.

Contents

2. S32G-VNP-EVB3 Hardware Kit Contents

The following table lists the items included in the S32G-VNP-EVB3 hardware kit.

Table 1. **Items included in hardware kit**

Item	Description	Quantity
S32GRV-PLATEVB	Platform board	1
S32G-PROCEVB3-S	Processor board	1
Power Supply	12 V,6.67 A AC-DC power supply,	1
Universal Adaptor	HW accessory	1
Connector Adapter	2.5 mm to 2.1 mm adapter	1
Power Cord	3-pin female to 3-pin male cable	1
Ethernet Cable	Shielded CAT6A blue ethernet cable	1
Micro USB Cable	USB A to micro USB B cable	1
Micro SD card	32 GB micro SD card	1
IC vacuum tool	IC picker	1
Heat Sink for PMIC	Heatsink 14mm*14mm, 10mm height with adhesive tape, black	1
Heat Sink for AQR113	Heatsink with thermal tape, customized for AQR113C	1
Fan	To be used with heat sink for S32G3x[1]	1

[1] S32G-PROCEVB3-S provides fan as an add-on accessory. It should be specifically used when working with S32G3x silicon in stressed conditions. The fan can be turned off or not used when working with S32G2x or when working with S32G3x under typical lab conditions (i.e., when the overall consumption on 0.8V rail can be limited to within 4.5 Watts). Instructions to assemble heat sink with fan are available in "S32G-PROCEVB3-S – Silicon mounting guide".

3. S32G-VNP-EVB3 Details

S32G-VNP-EVB3 is a combination of two boards

- S32G-PROCEVB3-S – the processor board
- S32GRV-PLATEVB – the platform board

3.1 Power connections from PMIC to S32G

Refer to section “Power Connections” in device Hardware Design Guidelines for power supply connections from PMIC VR5510 to S32G.

3.2 Power connections for S32G-VNP-EVB3

When the S32G-PROCEVB3-S is stacked over S32GRV-PLATEVB, **jumper J96 on S32G-PROCEVB3-S should be kept in 1-2 position** and only S32GRV-PLATEVB needs to be powered. Connect power supply to 12 V power jack P3 on S32GRV-PLATEVB.

S32G-PROCEVB3-S can be powered independently and can also work standalone. For S32G-PROCEVB3-S to work standalone, **jumper J96 on S32G-PROCEVB3-S should be kept at position 2-3**. Connect power supply to 12 V power jack P1 on S32G-PROCEVB3-S.

Refer to the following image for the position of J96 on S32G-PROCEVB3-S.

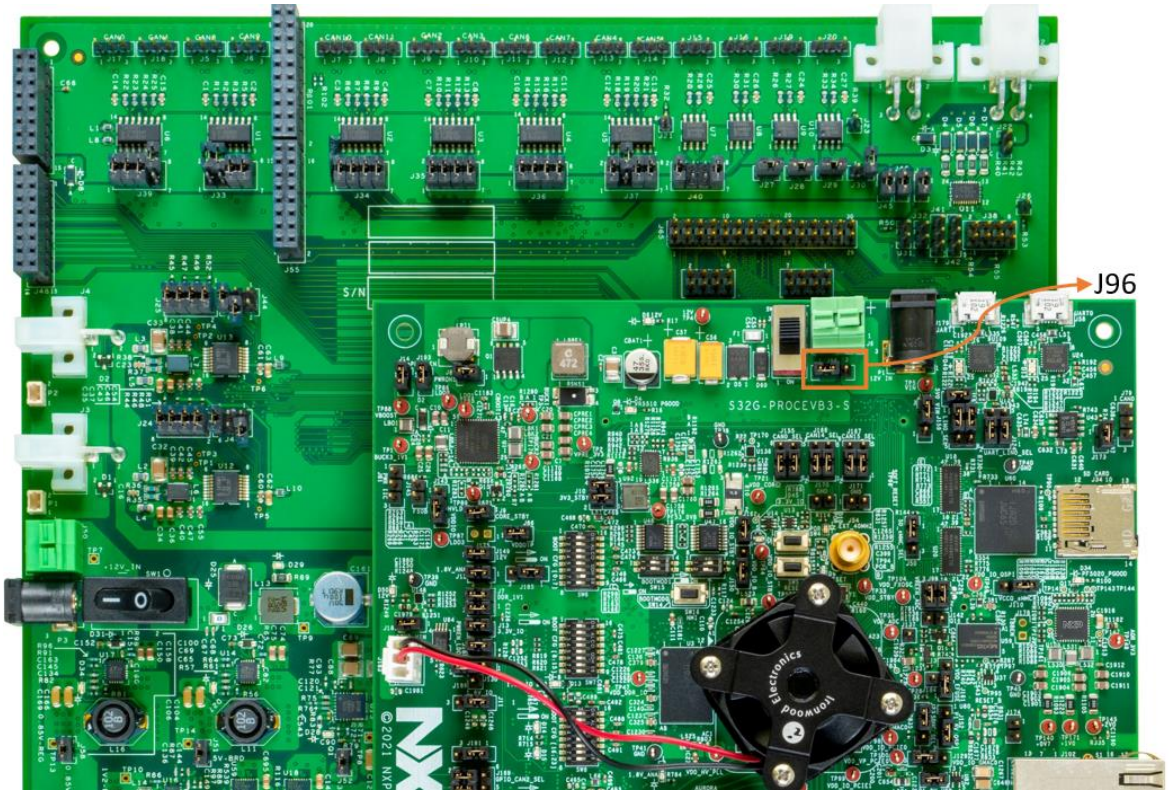

Figure 1. **S32G-VNP-EVB3 with J96 highlighted**

The following image shows the polarity of Barrel Connector.

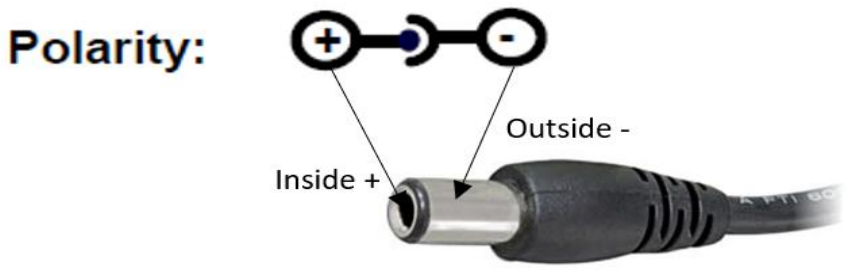

Figure 2. **Barrel connector polarity**

3.3 Part numbers of memories and PHY on S32G-VNP-EVB3

The main components used on S32G-PROCEVB3-S boards are as listed in the following table.

Table 2. **Component part number on S32G-PROCEVB3-S**

Function	Description	Part number
Power solution	NXP PMIC + PF53	PVR5510AMDALES + PPF53BDAMMA1ES
DRAM	32 Gbit LPDDR4	MT53D1024M32D4DT-053
QSPI	512Mbit NOR Flash	MX25UW51245GXDR00
SDHC	Micro SD card slot	SD/MMC SKT
eMMC	eMMC memory	MTFC32GAPALBH-AAT
Ethernet PHY	RGMII PHY	KSZ9031RNXVB-VAO
Serial RCON	EEPROM	AT24C01C-XPD-T
CAN	CAN PHY	TJA1051T/3,118
Ethernet SERDES	SGMII PHY	AQR113C-B0-C
UART	UART2USB	FT232RQ
USB UPLPI	USB ULPI PHY	USB83340AM
AURORA	Connector	ASP-130367-01

3.4 Peripheral addressing table of S32G-VNP-EVB3

3.4.1 MDC/MDIO address table

The following table describes the MDC/MDIO address for peripherals on S32G-VNP-EVB3.

Table 3. **MDC/MDIO address for peripherals**

MDC/MDIO	Location	Reference Destination	PHY	Address
PFE_MAC0/ GMAC0	S32GRV-PLATEVB	U57	TJA1102	0x6,0x7
	S32G-PROCEVB3-S	U51	AQR113C	0x4
	S32GRV-PLATEVB	U53, U54	KSZ9031RNXCA	0x2,0x3
	S32GRV-PLATEVB	J100	Side Band connector	Add on board
PFE_MAC1	S32GRV-PLATEVB	U43	KSZ9031RNXCA	0x5
	S32GRV-PLATEVB	U51	AQR107	0x1
	S32G-PROCEVB3-S	U53	KSZ9031RNXCA	0x4
PFE_MAC2	S32GRV-PLATEVB	J93	Add on board connector	Add on board

3.4.2 I2C address table

The following table describes the I2C address on S32G-VNP-EVB3.

Table 4. **I2C address Peripherals**

I2C	Location	Reference Destination	Device	Address
I2C_0	S32G-PROCEVB3-S	U64	AT24C01B	0xA0
I2C_1	S32GRV-PLATEVB	J99	X16 PCIe connector	Add on board
	S32GRV-PLATEVB	J93	ENET add on board	Add on board
I2C_2	S32G-PROCEVB3-S	U65	AT24C01B	0xA1
	S32GRV-PLATEVB	J56	Arduino connector	Add on board
I2C_3	S32G-PROCEVB3-S	U50	x1 PCIe connector	Add on board
	S32GRV-PLATEVB	J56	Arduino connector	Add on board
I2C_4	S32G-PROCEVB3-S	U1	PMIC (VR5510)	0x20
	S32G-PROCEVB3-S	U92	PF53	0x40
	S32GRV-	J49	Arduino	Add on board

I2C	Location	Reference Destination	Device	Address
	PLATEVB		connector	

3.5 S32G-PROCEVB3-S overview

The following figure shows an image of S32G-PROCEVB3-S with key areas highlighted.

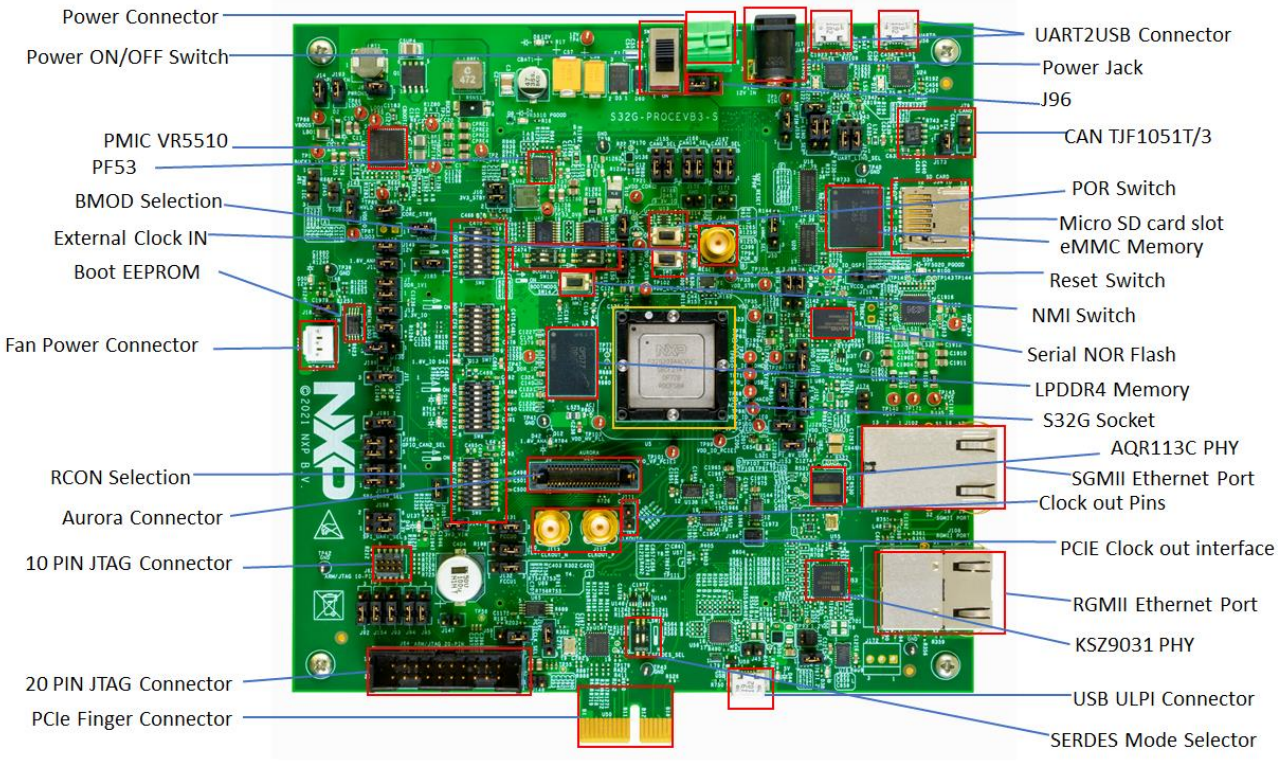

Figure 3. **S32G-PROCEVB3-S key areas**

NOTE

For high resolution image of S32G-PROCEVB3-S refer to attachments.

3.5.1 Boot mode

BootROM is responsible for booting customer applications. BootROM supports Serial Boot, Boot from RCON and Boot from Fuses. SW14 and SW15 controls the boot mode for S32G and can be configured as shown in the following table.

Table 4. Boot mode configuration

Boot Mode	SW14[1:2]		SW15[1:2]	
Boot from RCON (S32G-VNP-EVB3 is set to SD boot mode by default)	ON	OFF	OFF	OFF
Boot from Serial	OFF	OFF	ON	OFF

For more details refer to AN12422.

3.5.2 Connectors and Switches

The following table describes the S32G-PROCEVB3-S connectors and switches.

Table 5. **S32G-PROCEVB3-S connectors and switches**

Connector	Description	Connector Type/Function	Typical Connection
P1	12 V power jack	DC power jack	Connects to 12 V power supply
SW10	Power ON switch	Enable/disable board power	ON (1-2) position allows the board to be powered
J64	JTAG	20-pin ARM JTAG header	Debug Interface
J62	JTAG	10-pin ARM JTAG header	Debug Interface
J26	Aurora Port	40-pin Aurora port connector	Debug Interface
J58	Micro USB port	UART to USB port (UART0)	Connects to host PC
J179	Micro USB port	UART to USB port (UART1)	Connects to host PC
J102	RJ45 Ethernet	Ethernet SGMII PHY port	Connect to host PC or Ethernet network
J108	RJ45 Ethernet	Ethernet RGMII PHY port	Connect to host PC or Ethernet network
J34	Micro SD Card Slot	Slot to insert micro SD containing boot image	N/A
SW6	RCON Switch	Boot CFG[0:7]	Connects to BOOT_RCON0 - BOOT_RCON7 lines respectively
SW7	RCON Switch	Boot CFG[8:15]	Connects to BOOT_RCON8- BOOT_RCON15 lines respectively
SW8	RCON Switch	Boot CFG[16:23]	Connects to BOOT_RCON16 - BOOT_RCON23 lines respectively
SW9	RCON Switch	Boot CFG[24:31]	Connects to BOOT_RCON24 - BOOT_RCON31 lines respectively
SW14	BOOTMOD Switch	BOOTMOD0	Connects to Boot Mode 0 line
SW15	BOOTMOD Switch	BOOTMOD1	Connects to Boot Mode 1 line
SW16	S32G NMI	Triggers NMI	Connects to S32G NMI line
SW5	S32G Reset	Resets S32G	Connects to S32G Reset line
SW4	S32G POR	Applies POR to S32G	Connects to S32G POR line
J54	SMA connector	External clock input interface	Connects external clock source to S32G-VNP-EVB3

Connector	Description	Connector Type/Function	Typical Connection
J112	SMA connector	PCIE clock out interface	Clock out interface for external observation and usage
J113	SMA connector	PCIE clock out interface	Clock out interface for external observation and usage
J57	Single pin header	Clock out interface	Clock out interface for external observation and usage
J111	Single pin header	Clock out interface	Clock out interface for external observation and usage
J79	Connector	CAN connector	Used for CAN_H and CAN_L connections
J81	3-pin Connector	3-pin connector to program VR5510 via I2C	Connects to I2C signals to program VR5510
SW17	SERDES switch	2-pin SERDES switch	Selects SGMII or PCIe functionality
J183	Fan PWR Connector	3-pin Fan PWR connector	Connector for Fan

3.5.3 Jumpers

The following table shows the jumper settings for the S32G-PROCEVB3-S.

Table 6. **S32G-PROCEVB3-S jumpers**

Jumper	Size	Name/function	Position
J96	1x3	Selects 12 V power source	1-2: Takes input from 12 V supply connected to S32GRVB-PLATEVB (default) 2-3: Takes input from 12 V supply connected to S32G-PROCEVB3-S
J85	1x2	PWRON1 (disables the complete system power)	1-2: Enables power to board (default) 2-3: Disables power to board
J143	1x3	Source Selection for VDDIO voltage	1-2: Connects VPRE_3V3 from VR5510 to VDDIO voltage (default) 2-3: Connects LDO3_3V3 from VR5510 to VDDIO voltage
J86	1x2	VDDOTP	Off: To put PMIC in normal mode On: To put PMIC in debug mode (default)
J153	1x2	P1_8V_IO_USB (USB IO voltage)	Off: Disconnects P1_8V_ANA to P1_8V_IO_USB On: Connects P1_8V_ANA to P1_8V_IO_USB (default)
J162	1x2	P3_3V_STBY_MCU (VDD_IO_STBY voltage)	Off: Disconnects P3_3V_STBY_BRD to P3_3V_STBY_MCU On: Connects P3_3V_STBY_BRD to P3_3V_STBY_MCU (default)
J152	1x3	Source Selection for	1-2: Connects P1_8V_ANA to

Jumper	Size	Name/function	Position
		P1_8V_IO_QSPI (1.8V QSPI IO voltage)	P1_8V_IO_QSPI 2-3: Connects P1_8V_IO to P1_8V_IO_QSPI (default)
J98	2x2	Enables VREFH_ADC and VDD_ADC voltages	1-2: Connects P1_8V_ANA to VREFH_ADC_P (default) 3-4: Connects P1_8V_ANA to VDD_ADC (default)
J161, J184	1x3, 1x1	Source Selection for VDD_EFUSE	J161 - 1-2: Connects P1_8V_ANA to VDD_EFUSE(default) J161 - 2-3: Grounds VDD_EFUSE J184 - 1 to J161 - 2: Connects IO controlled supply to VDD_EFUSE
J129	1x3	Source Selection for VDD_IO_GMAC0 (GMAC0 IO voltage)	1-2: Connects P1_8V_ANA to VDD_IO_GMAC0 2-3: Connects P3_3V_IO3P3 to VDD_IO_GMAC0 (default)
J150	1x3	Source Selection for VDD_IO_B	1-2: Connects P3_3V_STBY_BRD to VDD_IO_B 2-3: Connects P3_3V_IO3P3 to VDD_IO_B (default)
J23	1x3	Source Selection for VDD_IO_SDHC	1-2: Selects 3.3 V for VDD_IO_SDHC (default) 2-3: Selects 1.8 V for VDD_IO_SDHC
J104	1x2	RGMII PHY Interrupt	Off: Disconnects RGMII PHY interrupt line from GPIO31 On: Connects RGMII PHY interrupt line to GPIO31 (default)
J101	1x2	SGMII PHY Interrupt	Off: Disconnects AQR113C PHY interrupt line from GPIO31 On: Connects AQR113C PHY interrupt line to GPIO31 (default)
J92	1x3	JTAG_nSRST	1-2: Enables J_nSRST for JTAG (default) 2-3: Enables JTAG_RESET for SWD (Serial wire debug)
J93	1x3	JTAG_TDO	1-2: Enables J_TDO for JTAG (default) 2-3: Enables TDO for SWD (Serial wire debug)
J94	1x3	JTAG_TCK	1-2: Enables J_TCK for JTAG (default) 2-3: Enables TCK for SWD (Serial wire debug)
J95	1x3	JTAG_TMS	1-2: Enables TMS For JTAG (default) 2-3: Enables TMS for SWD (Serial wire debug)
J154	1x3	JTAG_TDI	1-2: Enables TDO for JTAG (default) 2-3: Enables TDI for SWD (Serial wire

Jumper	Size	Name/function	Position
			debug)
J59	1X3	JCOMP	1-2: Pulls up the value of JCOMP to 3.3 V, required for connecting 10-pin Lauterbach cable to JTAG header 2-3: Grounds JCOMP (default)
J60	1x3	TEST	1-2: Pulls up the value of TEST to 3.3 V 2-3: Grounds TEST (default)
J131	1x3	FCCU_ERR0 (Fault collection and control unit)	1-2: Connects FCCU_EER0 to test point 2-3: Connects FCCU_EER0 to VR5510 (default)
J132	1x3	FCCU_ERR1 (Fault collection and control unit)	1-2: Connects FCCU_EER1 to test point 2-3: Connects FCCU_EER1 to VR5510 (default)
J50	1x3	Select pin for SD or eMMC	1-2: Enables SD (default) 2-3: Enables eMMC
J110	1x3	Source selection for VDD_eMMC	1-2: Connects P1_8V_ANA to VDD_eMMC 2-3: Connects +3V3 to VDD_eMMC (default)
J144	1x3	ADC selection jumper	1-2: Connects analog voltage from VR5510 to ADC_CH_11 2-3: Connects a GPIO to ADC_CH_11 (default)
J155	1x2	Termination Resistor for CAN	Off: Disables termination resistor for CAN On: Enables termination resistor for CAN (default)
J124	3x2	Selects the UART signal for UART2USB	1-3: Connects PC_09 (CC LIN 0 TX) to UART2USB (default) 2-4: Connects PC_10 (CC LIN 0 RX) to UART2USB (default) 3-5: Connects PK_15 (LLCE/CC LIN 0 Tx) to UART2USB 4-6: Connects PL_00 (LLCE/CC LIN 0 Rx) for UART2USB
J159	3x2	Selects source of LIN 0 routed to S3GRV PLATEVB	1-3: Connects PK_15 (LLCE/CC LIN 0 Tx) to LIN0_TX (default) 2-4: Selects PL_00 (LLCE/CC LIN 0 RX) to LIN0_RX (default) 3-5: Selects PC_09 (CC LIN 0 TX) to LIN0_TX 4-6: Selects PC_10 (CC LIN 0 RX) to LIN0_RX
J155	3x2	Selects the path to route CAN 0	1-3: Routes CAN 0_RX on S32G-PROCEVB3-S (default) 2-4: Routes CAN 0_TX on S32G-

Jumper	Size	Name/function	Position
			PROCEVB3-S (default) 3-5: Routes CAN 0_TX on S3GRV PLATEVB 4-6: Routes CAN 0_TX on S3GRV PLATEVB
J166	3x2	Jumper to select between CC CAN2 and LLCE CAN14_RX	1-3: Selects CC CAN 2 RX (default) 2-4: Selects CC CAN 2 TX (default) 3-5: Selects LLCE CAN 14 RX 4-6: Selects LLCE CAN 14 TX
J167	3x2	Jumper to select between CC CAN2 and LLCE CAN14_RX	1-3: Selects CC CAN 3 RX (default) 2-4: Selects CC CAN 3 TX (default) 3-5: Selects LLCE CAN 15 RX 4-6: Selects LLCE CAN 15 TX
J158	3x2	Jumper to select between UART and SPI	1-3: Connects SPI SIN to PC_10 2-4: Connects SPI SCK to PC_09 3-5: Connects UART RX to PC_10(default) 4-6: Connects UART TX to PC_09 (default)
J168	3x2	Jumper to select between FlexCAN 3 and SPI	1-3: Connects FlexCAN 3 RX to PB_10 (default) 2-4: Connects FlexCAN 3 TX to PB_09 (default) 3-5: Connects SPI CS to PB_10 4-6: Connects SOUT to PB_09
J169	3x2	Jumper to select between FlexCAN 2 and GPIO	1-3: Connects FlexCAN 2 RX to PB_12 (default) 2-4: Connects FlexCAN 2 TX to PB_11 (default) 3-5: Connects GPIO28 to PB_12 4-6: Connects GPIO27 to PB_11
J130,J186	1x3, 1x1	Jumper to select between I2C0 _SDA and UART1_RXD	J130 - 1-2: Connects PB_10 to GPIO16_CS J130 - 2-3: Connects PB_10 to I2C0_SDA (default) J130 - 2 to J186 - 1: Connects PB_10 to UART1_RXD
J185	1x3	Jumper to select between DSPI0_SCK and UART1_TXD	1-2: Connects PA_13 to DSPI0_SCK (default) 2-3: Connects PA_13 to UART1_TXD
J145	1x2	VR5510 fault indicator	Off: Disconnects fail safe output signal from VR5510 to S32G (default) On: Connects fail safe output signal from VR5510 to S32G
J45	1x2	Selection pin between USB HOST	Off: USB behaves as USB DEVICE

Jumper	Size	Name/function	Position
		and USB DEVICE	(default) On: USB behaves as USB HOST
J147	1x2	To enable 12V_PCIE_X1	Off: Disconnects 12 V to 12V_PCIE_X1 (default) On: Connects 12 V to 12V PCIE_X1
J148	1x2	To enable 3.3V_PCIE_X1	Off: Disconnects 3.3 V to 3.3V_PCIE_X1 (default) On: Connects 3.3 V to 3.3V_PCIE_X1
J191	1x2	Jumper to select EFUSE_EN and GPIO23	1-2: Connects GPIO23 to PB_07 (default) 2-3: Connects EFUSE_EN to PB_07
J194	3x2	Jumper to select RGMII connectivity with AQR	1-3 2-4: Connects RGMII_A MDC/MDIO to AQR on Serdes 1 Lane 0 (default)
			3-5 4-6: Connects RGMII_C MDC/MDIO to AQR on Serdes 0 Lane 0
J195	3x2	Jumper to select RGMII connectivity with AQR	1-3 2-4: Connects RGMII_C MDC/MDIO to AQR on Serdes 1 Lane 1 (default)
			3-5 4-6: Connects RGMII_A MDC/MDIO to AQR on Serdes 0 Lane 1
J193	1x2	Jumper to enable PF53	Off: Disables PF53 On: Enables PF53 (default)
J189	1x2	12V0_VIN (12V voltage)	Off: Disconnects P12V_BRD to 12V0_VIN On: Connects P12V_BRD to 12V0_VIN (default)
J187	1x2	5V0_VIN (5V voltage)	Off: Disconnects Ps5V_BRD to 5V0_VIN On: Connects P5V_BRD to 5V0_VIN (default)
J141	1x2	P3_3V (3V3 voltage)	Off: Disconnects P3_3V_STBY_BRD to P3_3V On: Connects P3_3V_STBY_BRD to P3_3V (default)
J188	1x2	Jumper to enable PWREN_LDO3 (Load switch enable)	Off: Disconnects LDO3_3V3 to PWREN_LDO3 On: Connects LDO3_3V3 to PWREN_LDO3 (default)
J192	1x3	Connects to PCIE clock generator	1-2: Configures the output as(default): OUT0: 100 MHz OUT1: 100 MHz OUT2: 25 MHz OUT3: 26 MHz OUT4: 125 MHz OUT5: 100 MHz 2-3: Configures the output as: OUT0: 100 MHz OUT1: 100 MHz

Jumper	Size	Name/function	Position
			OUT2: 25 MHz OUT3: 26 MHz OUT4: 100 MHz OUT5: 100 MHz

3.5.4 PMIC select jumpers

The following table shows the jumper available on S32G-PROCEVB3-S at the PMIC output. These jumpers can be used to isolate the supplies or measure current across these supplies.:

Table 7. **S32G-PROCEVB3-S PMIC jumpers**

Jumper	Size	Name/function	Position
J9	1x2	Source Selection for P0_8V_STBY voltage (0.8 V Core standby voltage)	Off: Disconnects HVLDO_0V8 from VR5510 to P0_8V_STBY On: Connects HVLDO_0V8 from VR5510 to P0_8 V_STBY (default)
J7	2x2	Source Selection for P1_1V (1.1 V DDR voltage)	Off: Disconnects BUCK3_1V1 from VR5510 to P1_1V On: Connects BUCK3_1V1 from VR5510 to P1_1V (default)
J10	2x3	Source Selection for P3_3V_STBY_BRD voltage (3.3 V Standby voltage)	Off: Disconnects VPRE_3V3 from VR5510 to P3_3V_STBY_BRD voltage On: Connects VPRE_3V3 from VR5510 to P3_3V_STBY_BRD voltage (default)
J11	1x3	Source Selection for P1_8V_IO voltage (1.8 V IO voltage)	1-2: Connects BUCK1 from VR5510 to P1_8V_IO voltage (default) 2-3: Connects LDO2_1V8 from VR5510 to P1_8V_IO voltage
J12	1x2	Source Selection for P1_8V_ANA voltage (1.8 V Analog voltage)	Off: Disconnects LDO1_1V8 from VR5510 to P1_8V_ANA voltage On: Connects LDO1_1V8 from VR5510 to P1_8V_ANA voltage (default)
J13	1x2	Source Selection for P3_3V_IO3P3 voltage (3.3 V IO voltage)	Off: Disconnects LDO3_3V3 from VR5510 to P3_3V_IO3P3 voltage On: Connects LDO3_3V3 from VR5510 to P3_3V_IO3P3 voltage (default)
J149	1x2	Source Selection for 12 V voltage	Off: Disconnects P12V from VR5510 to 12 V voltage On: Connects P12V from VR5510 to 12 V voltage (default)
J14	1x2	Source Selection for 5 V voltage	Off: Connects VBOOST_5V from VR5510 to 12 V voltage On: Connects VBOOST_5V from VR5510 to 12 V voltage (default)

3.5.4.1 LED indicators

The table below describes the S32G-PROCEVB3-S LEDs:

Table 8. **S32G-PROCEVB3-S LEDs**

LED	Color	Name	Description
D4	Green	VR5510 PGOOD Indicator	Indicates that power sent from VR5510 are within expected range
D34	Green	PF53 PGOOD Indicator	Indicates that power sent from PF53 are within expected range
D38	Green	1.2V Power Supply Indicator	1.2 V power present
D42	Green	1.8V Analog Power Supply Indicator	1.8 V Analog power present
D43	Green	1.8V IO Power Supply Indicator	1.8 V IO power present
D44	Green	5V Power Supply Indicator	5 V power present
D45	Green	3.3V IO Power Supply Indicator	3.3 V IO power present
D46	Green	3.3V Power Supply Indicator	3.3 V power present
D6, D50	Green	12V Power Supply Indicator	12 V power present
D10	Red	POR Indicator	When either PGOOD signal from SoC is not good or when POR button is pressed
D9	Blue	Reset	Reset on reset button
D13	Red	UART to USB Rx Indicator	Activity present on Rx line of UART0 to USB
	Green	UART to USB Tx Indicator	Activity present on Tx line of UART0 to USB
D49	Red	UART to USB Rx Indicator	Activity present on Rx line of UART1 to USB
	Green	UART to USB Tx Indicator	Activity present on Tx line of UART1 to USB
D14	Green	General purpose LED	General purpose
D15	Green	General purpose LED	General purpose

3.6 S32GRV-PLATEVB-S Overview

The S32G-PROCEVB3-S is stacked over the S32GRV-PLATEVB as shown below:

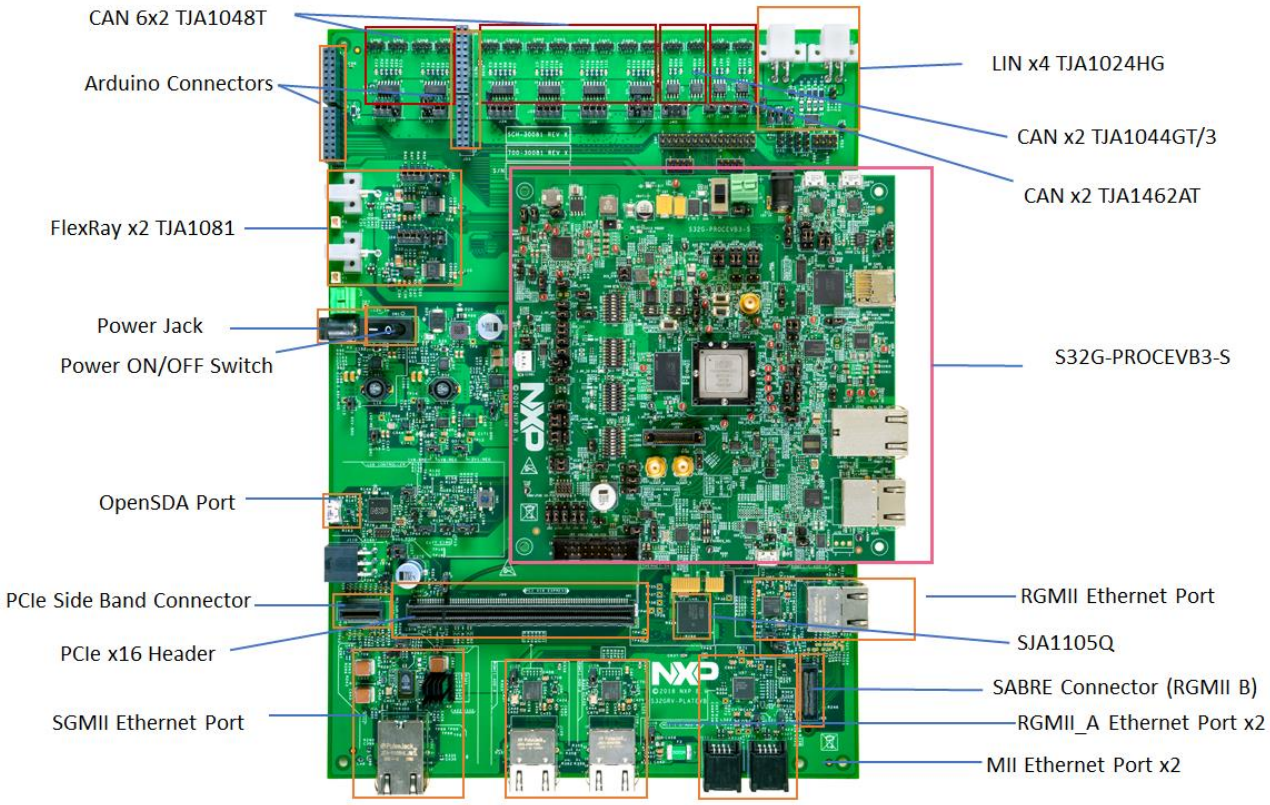

Figure 4. **S32G-PROCEVB3-S and S32GRV-PLATEVB in stacked mode**

NOTE

For high resolution image of S32G-PROCEVB3-S and S32GRV-PLATEVB in stacked mode refer to attachments.

3.6.1 S32G-PROCEVB3-S Connections to the S32GRV-PLATEVB

The connections from S32G-PROCEVB3-S to the S32GRV-PLATEVB can be referred from the schematics as shown below:

S32G-PROCEVB3-S <-> S32GRV-PLATEVB

1. J1<->J80 connection

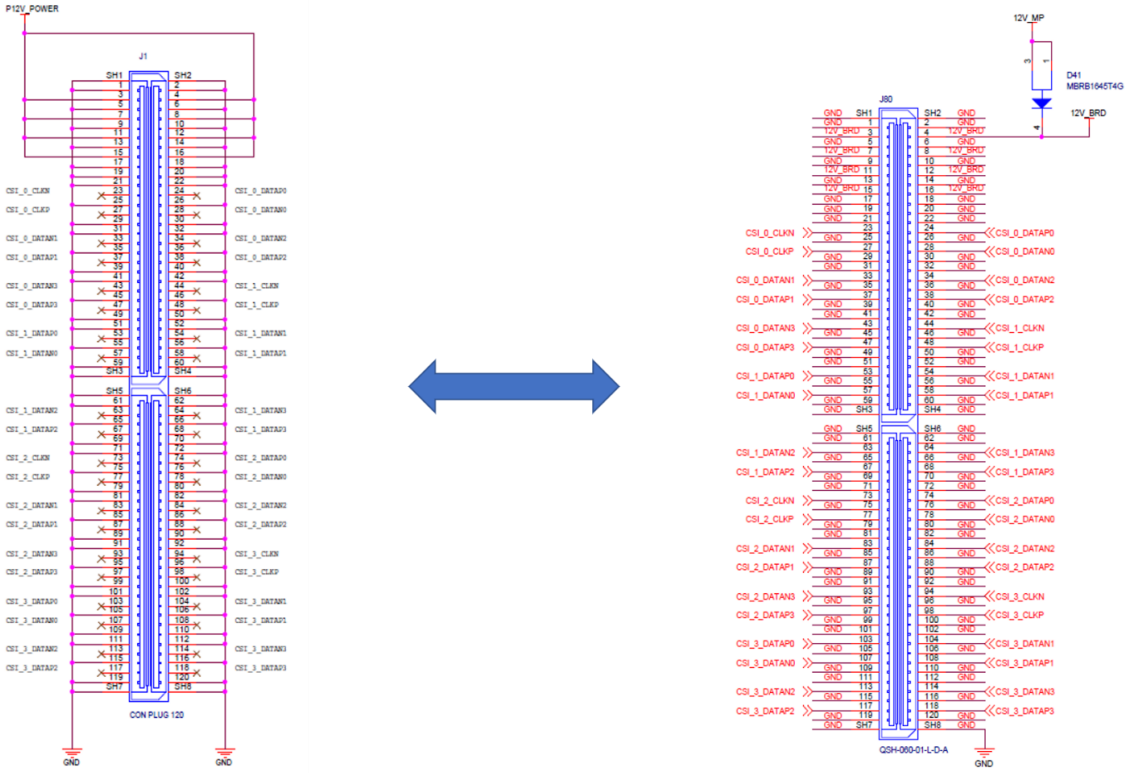

Figure 5. **J1<->J80 connection**

1. J2<->J66 connection

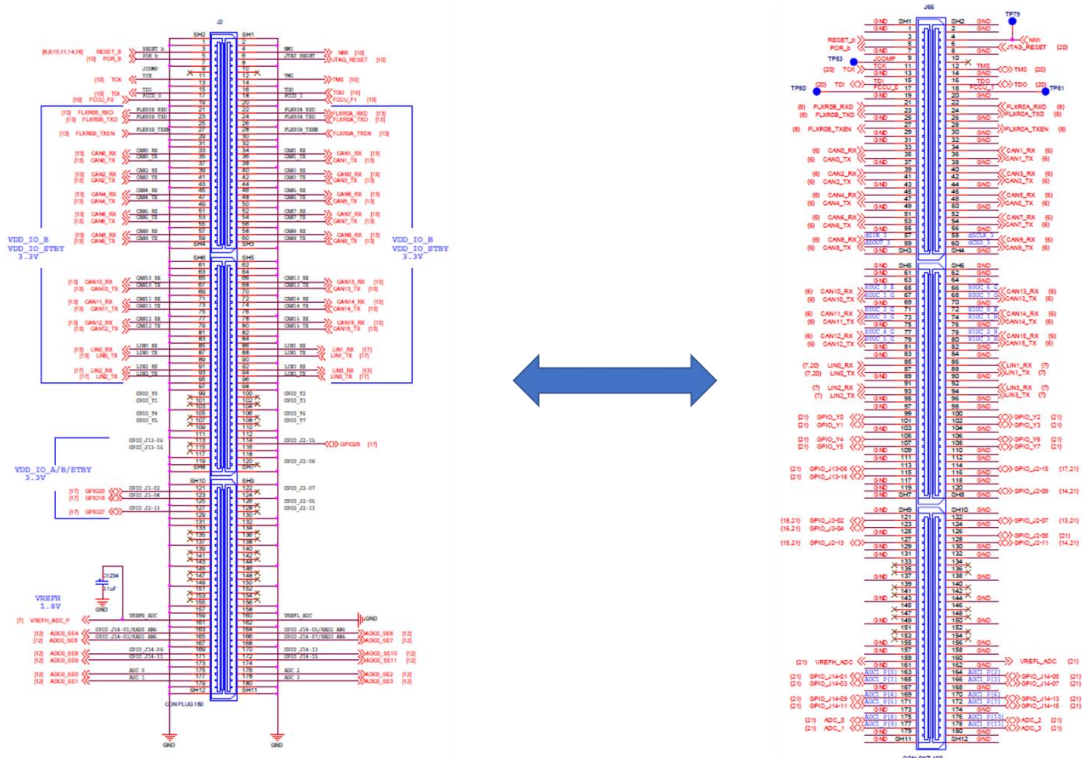

Figure 6. **J2<->J66 connection**

1. J3<->J81 connection

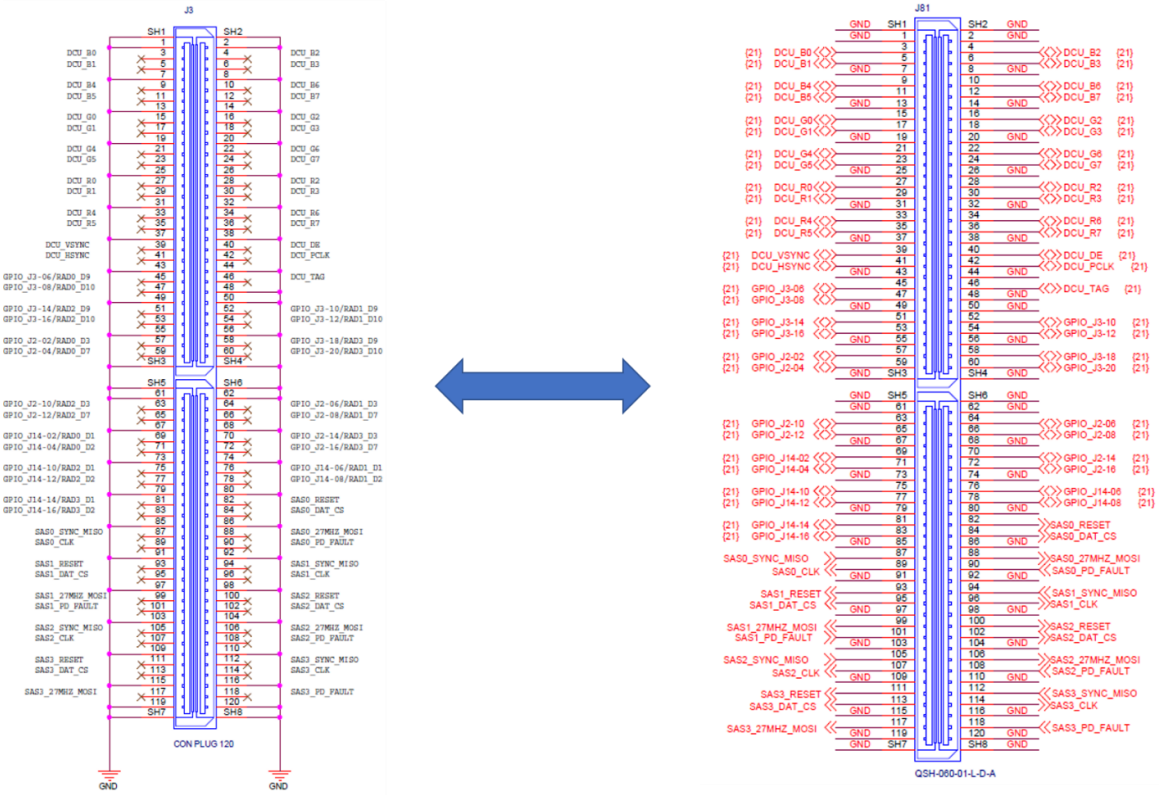

Figure 7. **J3<->J81 connection**

1. J4<->J87 connection

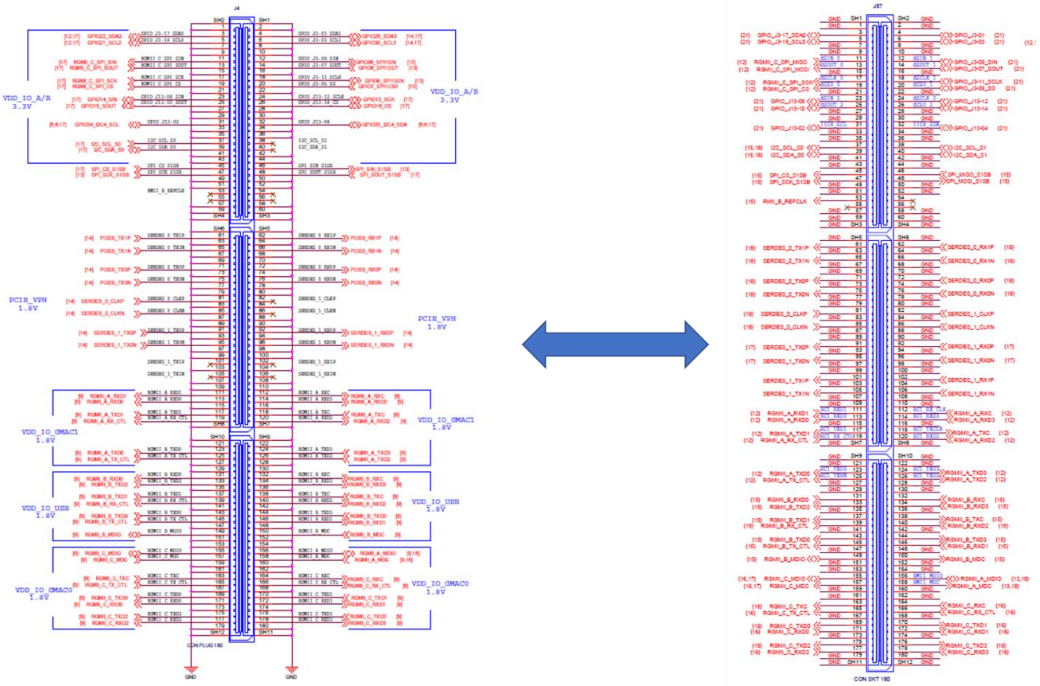

Figure 8. **J4<->J87 connection**

3.6.2 Connectors and Switches

The following table describes the S32GRV-PLATEVB connectors and switches:

Table 9. **S32GRV-PLATEVB connector and switches**

Connector	Description	Connector Type/Function	Typical Connection
P3	12 V power jack	DC power jack	Connects to 12 V power supply
SW1	Power ON switch	Position of SW1 should be 1-2 to power up the board	
J64	OpenSDA port	Micro USB port	Connects to host PC
J111	OABR Ethernet	Ethernet MII OABR PHY port[2]	Connect to host PC/Ethernet network
J112	OABR Ethernet	Ethernet MII OABR PHY port[2]	Connect to host PC/Ethernet network
J108	OABR Ethernet	Ethernet MII OABR PHY port[2]	Connect to host PC/Ethernet network
J109	OABR Ethernet	Ethernet MII OABR PHY port[2]	Connect to host PC/Ethernet network
J93	SABRE Connector	RGMII Sabre Connector	Connect to host PC/Ethernet network
J85	RJ45 Ethernet	Ethernet RGMII PHY port	Connect to host PC/Ethernet network
J102	RJ45 Ethernet	Ethernet SGMII PHY port	Connect to host PC/Ethernet network
J1	CON Plug	LIN Connector	-open-
J2	CON Plug	LIN Connector	-open-
J3	CON Plug	FlexRAY B Connector	-open-
J4	CON Plug	FlexRAY A Connector	-open-
J110	CON Plug	PCIe external power connector	-open-
J68	JTAG connector	OpenSDA interface JTAG Connector	Debug Interface
J55	connector	Arduino Connector	-open-
J56	connector	Arduino Connector	-open-
J48	connector	Arduino Connector	-open-
J49	connector	Arduino Connector	-open-
J61	connector	ADC connector	Voltage source
J114	Aquantia Connector	3-pin Aquantia connector	Connects to Aquantia Probe to program Aquantia firmware

[2] Via SJA1105Q automotive Ethernet switch

3.6.3 Jumpers

The following table shows the jumper settings for the S32GRV-PLATEVB.

Table 10. **S32GRV-PLATEVB jumpers**

Jumper	Size	Name/function	Position
J51	1x2	To enable 5V_BRD	Off: Disables 5V_BRD On: Enables 5V_BRD (default)
J52	1x2	To enable 3V3_BRD	Off: Disables 3V3_BRD On: Enables 3V3_BRD (default)
J53	1x2	To enable 1V2_BRD	Off: Disables 1V2_BRD On: Enables 1V2_BRD (default)
J57	1x2	To enable 2V1_BRD	Off: Disables 2V1_BRD On: Enables 2V1_BRD (default)
J58	1x2	To enable 0V85_BRD	Off: Disables 0V85_BRD On: Enables 0V85_BRD (default)
J113	1x2	To enable 1V8_BRD	Off: Disables 1V8_BRD On: Enables 1V8_BRD (default)
J33	4x2	To enable CAN 8, CAN 9	1-2: Enables CAN8_RX (default) 3-4: Enables CAN8_TX (default) 5-6: Enables CAN8_RX (default) 7-8: Enables CAN9_TX (default)
J34	4x2	To enable CAN 10, CAN 11	1-2: Enables CAN10_RX (default) 3-4: Enables CAN10_TX (default) 5-6: Enables CAN11_RX (default) 7-8: Enables CAN11_TX (default)
J35	4x2	To enable CAN 2, CAN 3	1-2: Enables CAN2_RX (default) 3-4: Enables CAN2_TX (default) 5-6: Enables CAN3_RX (default) 7-8: Enables CAN3_TX (default)
J36	4x2	To enable CAN 6, CAN 7	1-2: Enables CAN6_RX (default) 3-4: Enables CAN6_TX (default) 5-6: Enables CAN7_RX (default) 7-8: Enables CAN7_TX (default)
J37	4x2	To enable CAN 4, CAN 5	1-2: Enables CAN4_RX (default) 3-4: Enables CAN4_TX (default) 5-6: Enables CAN5_RX (default) 7-8: Enables CAN5_TX (default)
J39	4x2	To enable CAN 0, CAN 1	1-2: Enables CAN0_RX (default) 3-4: Enables CAN0_TX (default) 5-6: Enables CAN1_RX (default) 7-8: Enables CAN1_TX (default)
J40	4x2	To enable CAN 12, CAN 13	1-2: Enables CAN12_RX (default) 3-4: Enables CAN12_TX (default) 5-6: Enables CAN13_RX (default) 7-8: Enables CAN13_TX (default)
J27	1x2	To enable CAN 14 Tx	Off: Disables CAN14_TX

Jumper	Size	Name/function	Position
			On: Enables CAN14_TX (default)
J28	1x2	To enable CAN 14 Rx	Off: Disables CAN14_RX On: Enables CAN14_RX (default)
J29	1x2	To enable CAN 15 Tx	Off: Disables CAN15_TX On: Enables CAN15_TX (default)
J30	1x2	To enable CAN 15 Rx	Off: Disables CAN15_RX On: Enables CAN15_RX (default)
J38	4x2	To enable LIN2 and LIN3	1-2: Enables LIN2_RX (default) 3-4: Enables LIN2_TX (default) 5-6: Enables LIN3_RX (default) 7-8: Enables LIN3_TX (default)
J41	1x3	Selection pin between LIN1 PHY Rx and ARDUINO J2-01	1-2: Enables LIN1 RX (default) 2-3: Enables ARDUINO J2-01
J42	1x3	Selection pin between LIN1 PHY Tx and ARDUINO J2-03	1-2: Enables LIN1 TX (default) 2-3: Enables ARDUINO J2-03
J31	1x2	To enable LIN0_Rx	Off: Disables LIN0_RX (default) On: Enables LIN0_RX
J32	1x2	To enable LIN0_Tx	Off: Disables LIN0_TX (default) On: Enables LIN0_TX
J22	1x2	To enable 12V_LIN	Off: Disables 12V_LIN On: Enables 12V_LIN (default)
J24	4x2	To enable FLXR0B	1-2: Enables FLXR0B-BGE (default) 3-4: Enables FLXR0B-STBN (default) 5-6: Enables FLXR0B-EN (default) 7-8: Enables FLXR0B-WAKE (default)
J25	4x2	To enable FLXR0B	1-2: Enables FLXR0A-BGE (default) 3-4: Enables FLXR0A-STBN (default) 5-6: Enables FLXR0A-EN (default) 7-8: Enables FLXR0A-WAKE (default)
J43	3X2	To enable FLXR0B	1-2: Enables FLXR0B-JTXD (default) 3-4: Enables FLXR0B-JTXEN (default) 5-6: Enables FLXR0B-JRXD (default)
J44	3X2	To enable FLXR0A	1-2: Enables FLXR0A-JTXD (default) 3-4: Enables FLXR0A-JTXEN (default) 5-6: Enables FLXR0A-JRXD (default)
J103	1x2	To enable TJ1102 INT	Off: Disables TJ1102 INT On: Enables TJ1102 INT (default)
J104	1x2	To enable GE PHY1 INT	Off: Disables GE PHY1 INT On: Enables GE PHY1 INT (default)
J105	1x2	To enable GE PHY2 INT	Off: Disables GE PHY2 INT On: Enables GE PHY2 INT (default)
J106	1x2	To enable 12V_ENET	Off: Disables 12V_ENET On: Enables 12V_ENET (default)
J98	1x2	To enable 3V3_ECARD	Off: Disables 3V3_ECARD On: Enables 3V3_ECARD (default)

Jumper	Size	Name/function	Position
J91	1x2	To enable ECARD INT	Off: Disables ECARD INT On: Enables ECARD INT (default)
J90	1x2	To enable GE PHY3 INT	Off: Disables GE PHY3 INT On: Enables GE PHY3 INT (default)
J101	1x2	To enable XGT INT	Off: Disables XGT INT On: Enables XGT INT (default)
J107	3x2	To enable 12V_PCIE	1-3 2-4 Enables 12V_PCIE from 12V_MP (default) 3-5 4-6 Enables 12V_PCIE from 12V_EXT
J95	1x2	To enable ENETSB INT	Off: Disables ENETSB INT (default) On: Enables ENETSB INT
J96	1x2	To enable VIO_ENETSB	Off: Disables VIO_ENETSB (default) On: Enables VIO_ENETSB
J94	1x2	To enable 3V3_PCIE	Off: Disables 3V3_PCIE On: Enables 3V3_PCIE (default)
J67	1x3	SDA_RESET	1-2: Enables SDA RESET (default) 2-3: Enables button when OpenSDA is not powered
J70	1x3	Selection pin between TDI and SWD	1-2: Enables SWD 2-3: Enables TDI (default)
J62	1x2	To enable SDA UART RX	Off: Disables SDA UART RX (default) On: Enables SDA UART RX
J63	1x2	To enable SDA UART TX	Off: Disables SDA UART TX (default) On: Enables SDA UART TX
J59	1x2	To enable VDDIO_SDA	Off: Disables VDDIO_SDA On: Enables VDDIO_SDA (default)
J45	1x2	To enable 12V_ARDUINO	Off: Disables 12V_ARDUINO On: Enables 12V_ARDUINO (default)
J47	1x2	To enable 3V3_ARDUINO	Off: Disables 3V3_ARDUINO On: Enables 3V3_ARDUINO (default)
J46	1x2	To enable 5V_ARDUINO	Off: Disables 5V_ARDUINO On: Enables 5V_ARDUINO (default)
J115	1x2	To enable 1V8_RGMII3_DVDD of U43	Off: Disables 1V8_RGMII3_DVDD On: Enables 1V8_RGMII3_DVDD (default)
J116	1x2	To enable 1V2_RGMII3_VDDL of U43	Off: Disables 1V2_RGMII3_VDDL On: Enables 1V2_RGMII3_VDDL (default)
J117	1x2	To enable 3V3_RGMII3_AVDD of U43	Off: Disables 3V3_RGMII3_AVDD On: Enables 3V3_RGMII3_AVDD (default)

3.6.4 LED indicators

The following table describes the S32GRV-PLATEVB LEDs.

Table 11. **S32GRV-PLATEVB LEDs**

LED	Color	Name	Description
D27	Green	5 V power supply indicator	5 V power present
D28	Green	3.3 V power supply indicator	3.3 V power present
D29	Green	12 V power supply indicator	12 V power present
D30	Green	1.2 V power supply indicator	1.2 V power present
D34	Green	0.85 V power supply indicator	0.85 V power present
D37	Green	2.1 V power supply indicator	2.1 V power present
D516	Green	1.8 V power supply indicator	1.8 V power present
D39	Orange	Open SDA activity Indicator	Activity is present
D40	Red	Open SDA reset indicator	OpenSDA in reset

3.5 Viewing console logs over UART

Connect a micro USB cable from host PC to J58 on S32G-PROCEVB3-S for viewing console logs over UART0 and J179 for console logs over UART1.

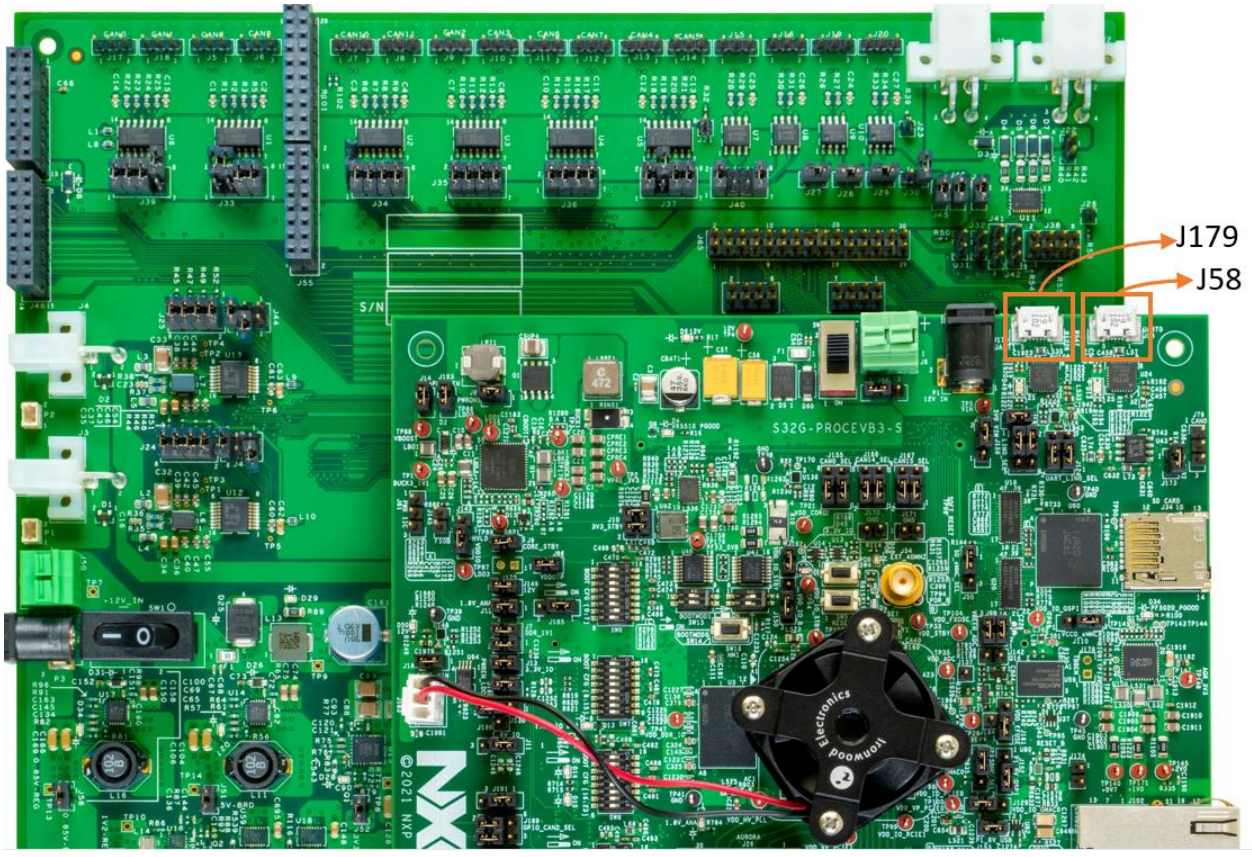

Figure 9. **Viewing console logs**

4. Debugger Connections

This section shows the hardware connection setup required to connect the debugger to S32G-PROCEVB3-S.

4.1 Lauterbach

Lauterbach's PowerDebug USB allows to debug and control the system on the S32G-VNP-EVB3 using T32 software.

To attach the 20-pin Lauterbach cable on S32G-PROCEVB3-S, follow the below steps:

1. Attach power supply to Lauterbach.
2. Connect the cable from Lauterbach to PC.
3. Connect the 20-pin cable to the JTAG header J64 on S32G-PROCEVB3-S.

Figure 10. **Connecting 20-pin Lauterbach cable on S32G-PROCEVB3-S**

4.2 S32 debug probe

Attached is the complete image of the S32 debug probe with included accessories (Ethernet cable is shown but not included in the kit).

Figure 11. **S32G debug probe package**

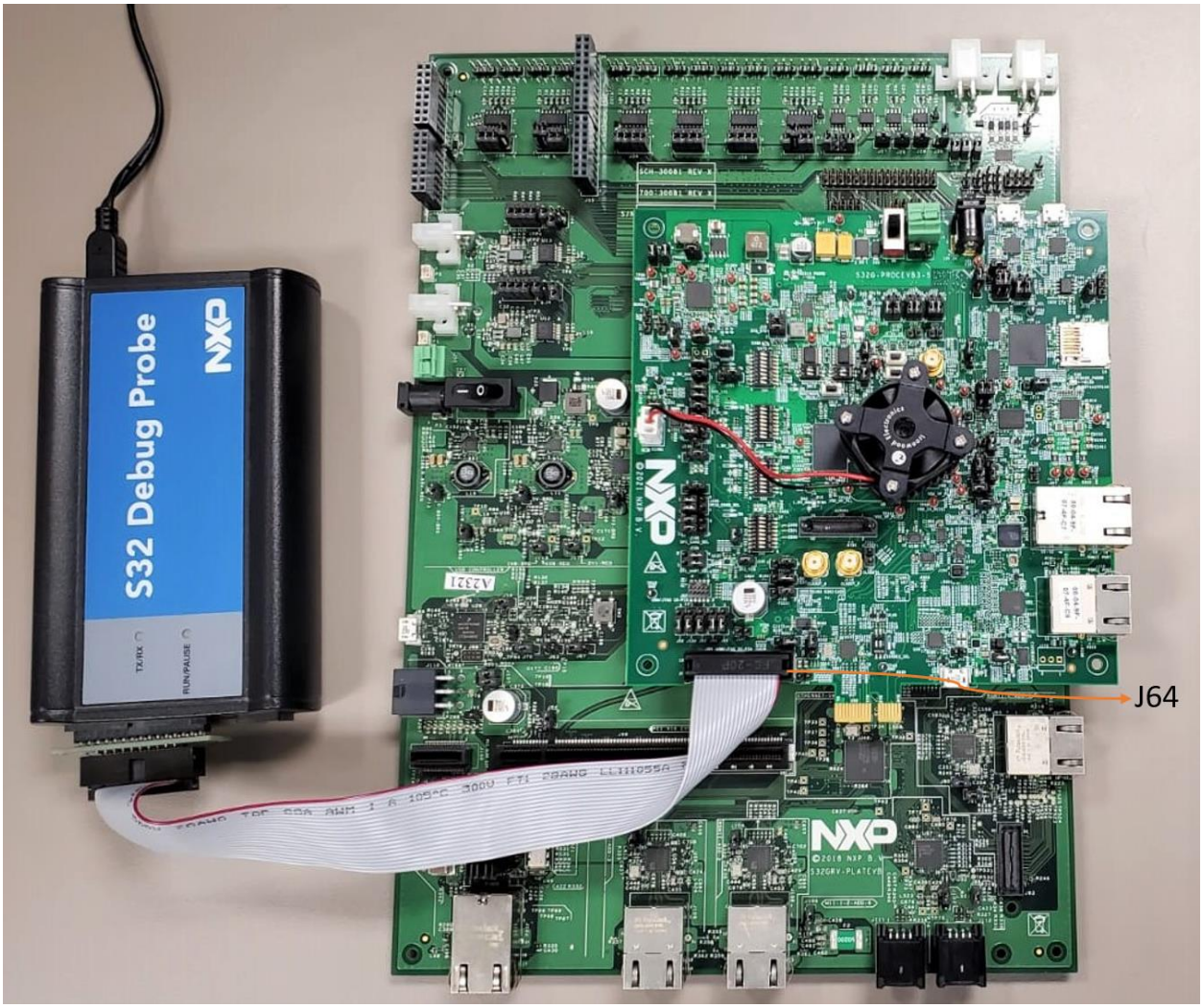

Figure 12. **Connecting S32 Debug probe on S32G-VNP-EVB3**

Following are the details of the S32 Debug Probe:

- Debug probe: S32DBGPROBE
- Debug cable: ARM® 20-pin probe tip and ribbon cable (included in S32DBGPROBE kit)

To attach the ARM 20-pin probe tip and ribbon cable to S32G-PROCEVB3-S, follow the below steps:

1. S32 Debug Probe can be connected directly via USB or anywhere via Ethernet
    a. For USB setup, attach supplied USB cable to PC and S32 Debug Probe
    b. For Ethernet setup, attach supplied power cable to S32 Debug Probe and Ethernet cable to network port and S32 Debug Probe. See S32_Debug_Probe_User_Guide.pdf for details on obtaining the network address of the S32 Debug Probe.
2. Connect the ARM 20-pin probe tip and ribbon cable together.
3. Connect the ARM 20-pin probe tip to the S32 Debug Probe.
4. Connect the ribbon cable to the JTAG header J64 on S32G-PROCEVB3-S.

For more information on the S32 Debug Probe, see ‘S32_Debug_Probe_User_Guide.pdf’ contained within the S32 Design Studio installation (..\S32DS\tools\S32Debugger\Debugger\Docs).

For more information on the S32 Debugger, see the section on ‘Debugging’ in ‘S32DS_User_Guide.pdf’ contained within the S32 Design Studio installation (..\S32DS\help\pdf).

4.3 Aurora based debugger

Lauterbach’s PowerTrace along with PowerDebug Pro Ethernet allows to capture the real-time trace in addition to debugging and controlling the system on the S32G-VNP-EVB3 using T32 software.

The aurora based debugger can be connected on S32G-PROCEVB3-S as below :

1. Connect Deutronic DC power supply to Lauterbach.
2. Connect the cable from Lauterbach to PC.
3. Connect the 20-pin JTAG cable to JTAG header J64 on S32G-PROCEVB3-S.
4. Connect the 40-pin Aurora Trace probe(ATP) to Aurora header J26 on S32G-PROCEVB3-S.

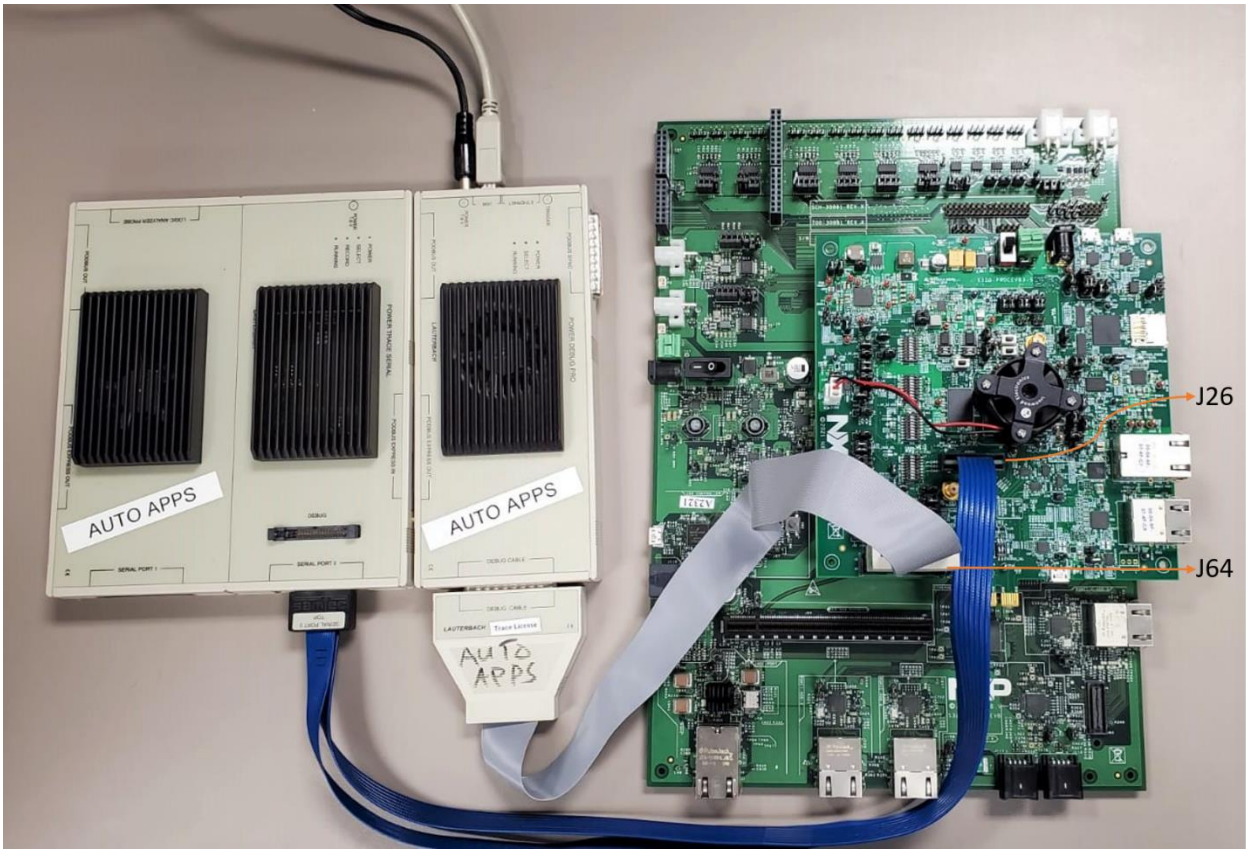

Figure 13. **Aurora Port setup 1 with ATP and JTAG cable connected on S32G-VNP-EVB3**

Aurora port also supports JTAG debug capabilities which can be used by doing below hardware modification on S32G-PROCEVB3-S:

- Populate a 0Ω resistor at R724 to connect J_TCK to AUR_TCK

- Populate a 0Ω resistor at R725 to connect J_TMS to AUR_TMS
- Populate a 0Ω resistor at R726 to connect J_COMP to AUR_COMP
- Populate a 0Ω resistor at R727 to connect J_TDI to AUR_TDI
- Populate a 0Ω resistor at R728 to connect J_TDO to AUR_TDO
- Populate a 0Ω resistor at R729 to connect J_nSRST to AUR_nSRST

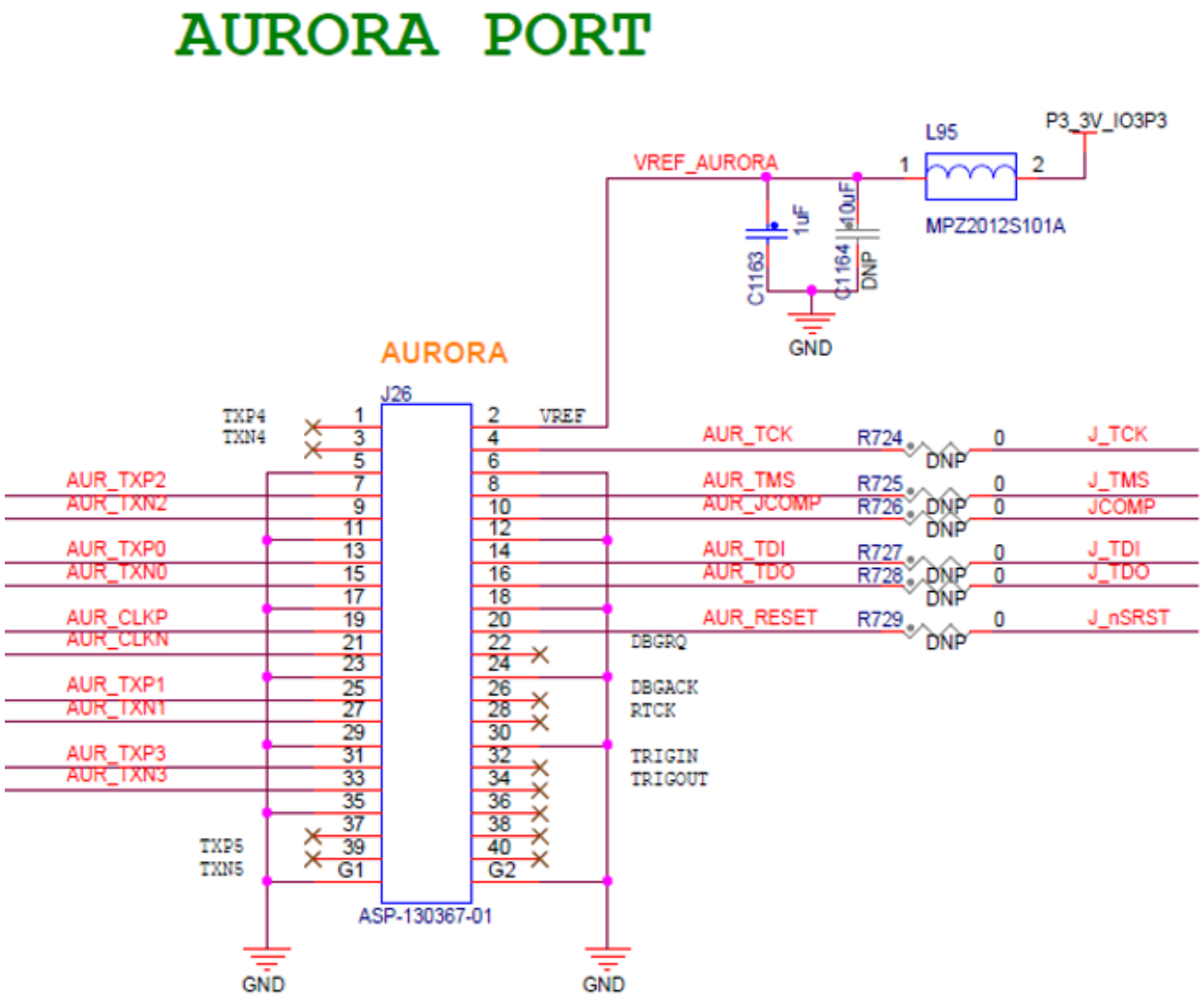

Figure 14. **Schematics snapshot of Aurora Port**

To use JTAG debug capability of Aurora port, connect the debugger on S32G-PROCEVB3-S as below:

1. Connect Deutronic DC power supply to Lauterbach.
2. Connect the cable from Lauterbach to PC.
3. Connect the 20-pin JTAG cable to the JTAG header Aurora based debugger.
4. Connect the 40-pin Aurora Trace probe(ATP) to the Aurora header J26 on S32G-PROCEVB3-S.

Figure 15. **Aurora Port setup 1 with only ATP cable connected to S32G-VNP-EVB3**

5. S32G-VNP-EVB3 Software

All NXP releases for S32G are supported on S32G-VNP-EVB3. Refer the product page for more details on SW releases.

6. Interfaces Block Diagram

The block diagram for various interfaces are shown in below subsections where blue boxes represent the interfaces present on S32G-PROCEVB3-S and yellow boxes represent the interfaces present on S32G-PLATEVB.

6.1 CAN interface

The following figure shows the CAN signals on S32G-VNP-EVB3.

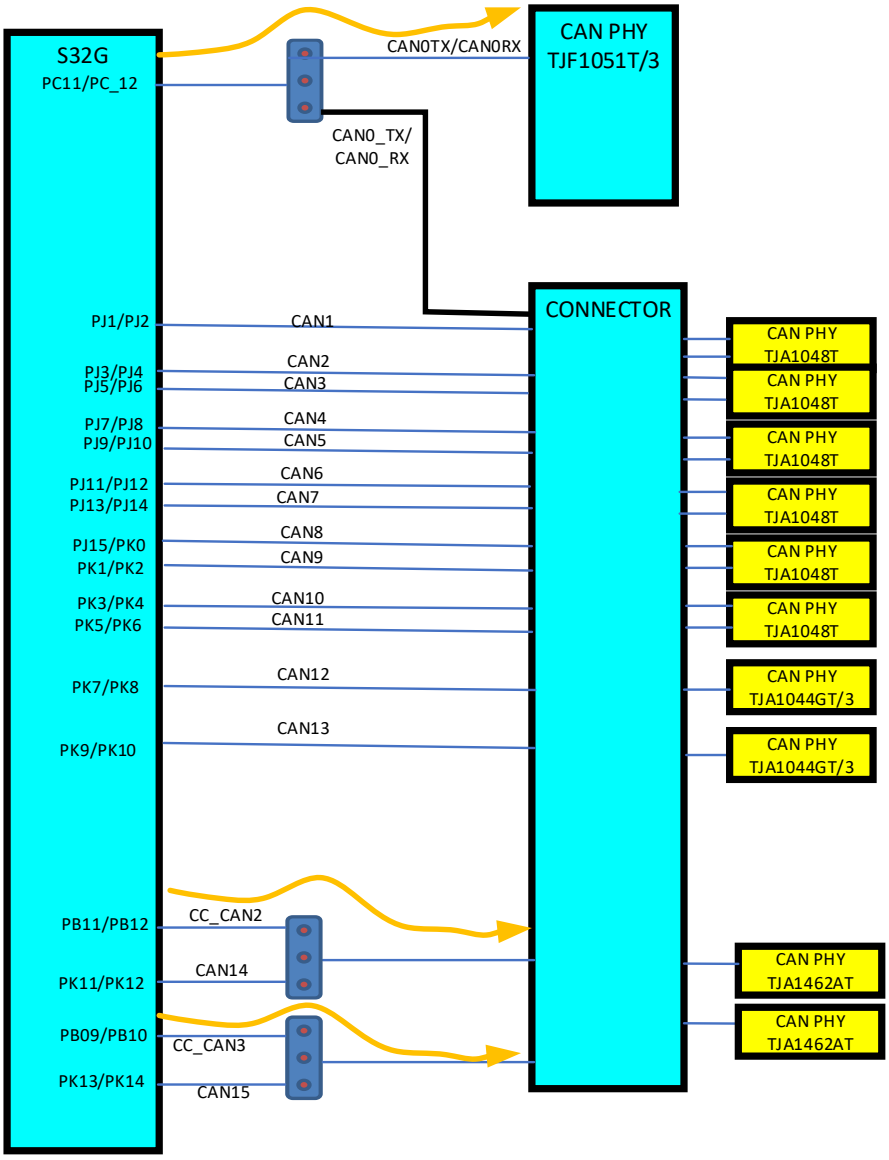

Figure 16. **CAN interfacing with S32G-VNP-EVB3**

6.2 LIN interface

The following diagram shows the LIN/UART2USB signals on S32G-VNP-EVB3.

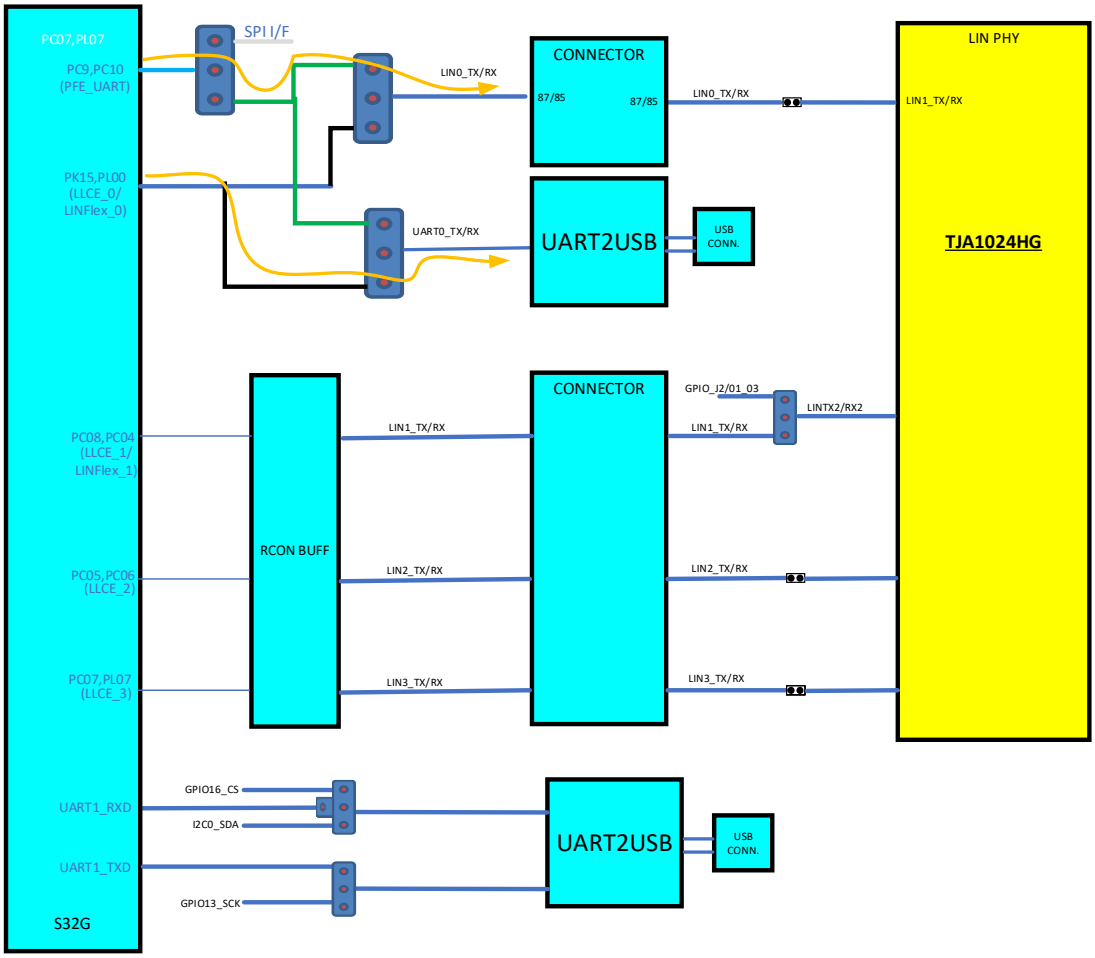

Figure 17. **LIN interfacing with S32G-VNP-EVB3**

6.3 FlexRay interface

The following figure shows the FlexRay signals on S32G-VNP-EVB3.

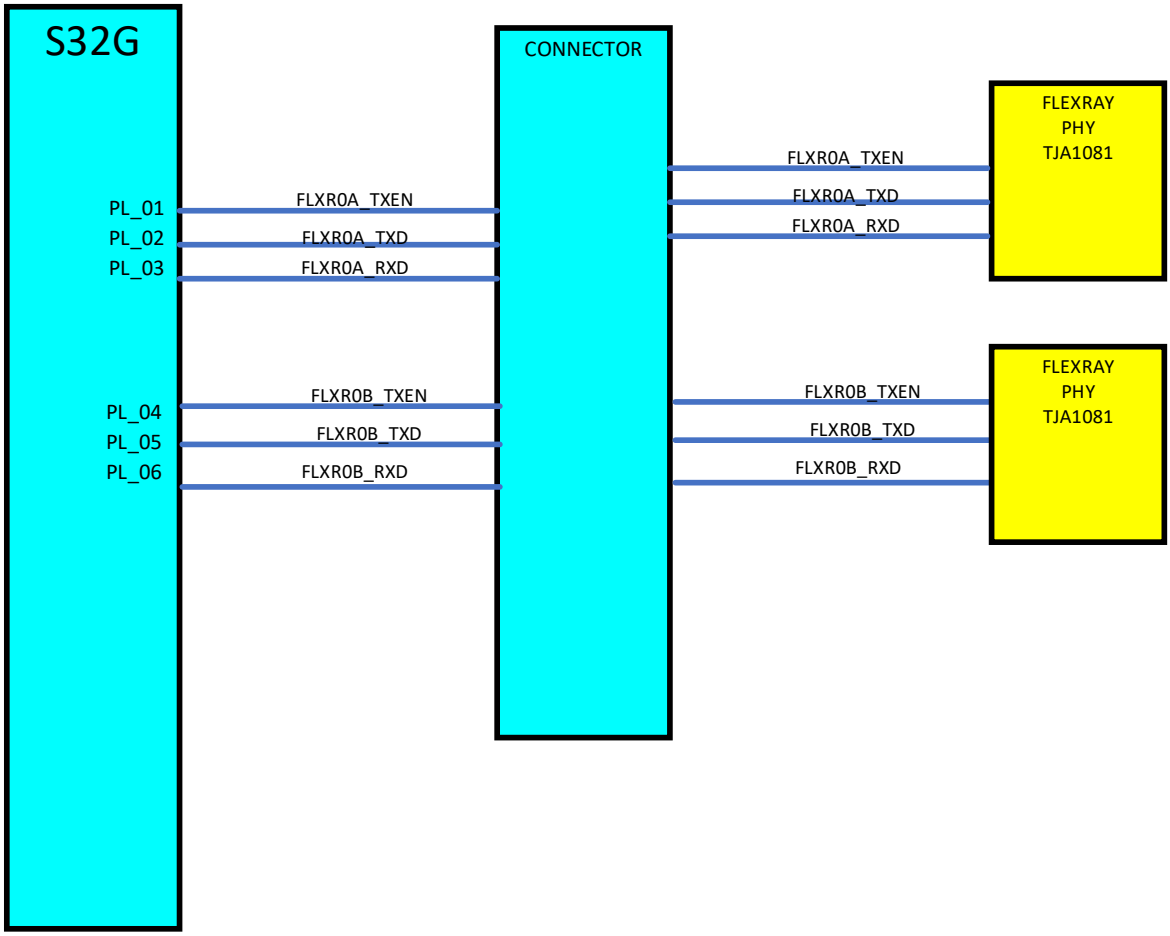

Figure 18. **FlexRAY interfacing with S32G-VNP-EVB3**

6.4 DSPI interface

The following figure shows the DSPI signals on S32G-VNP-EVB3.

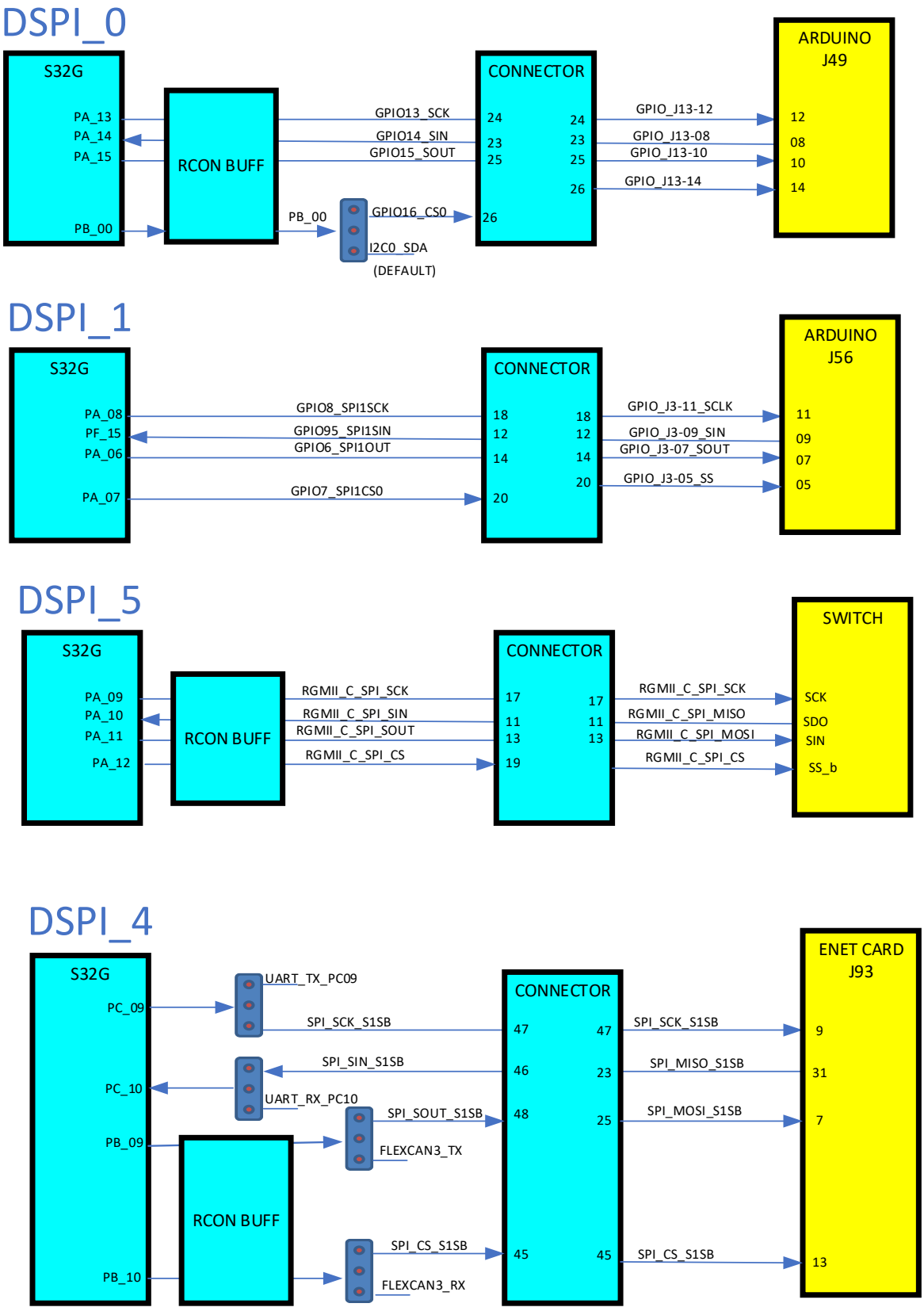

Figure 19. **DSPI interfacing with S32G-VNP-EVB3**

6.5 I2C interface

The following diagram shows I2C signals on S32G-VNP-EVB3.

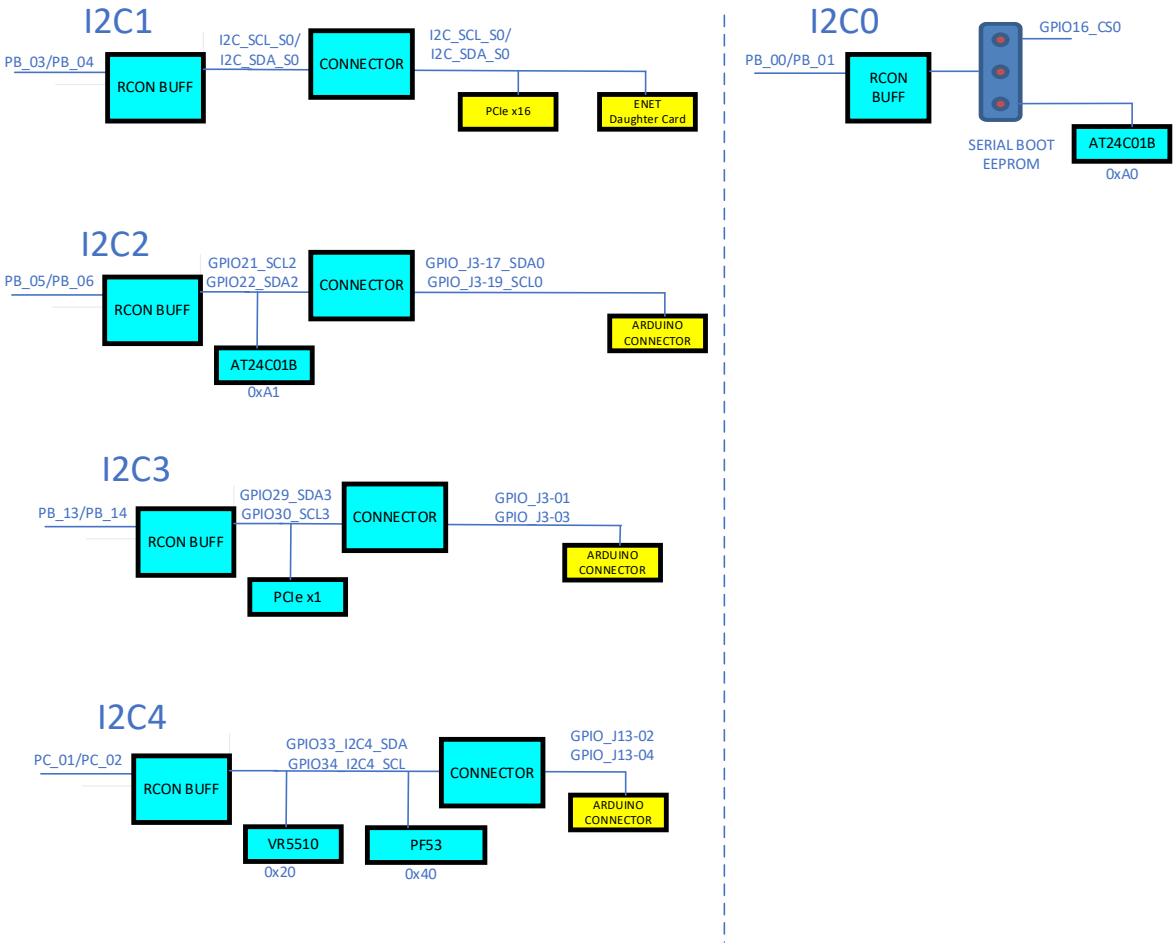

Figure 20. **I2C interfacing with S32G-VNP-EVB3**

6.6 RGMII interface

The following diagram shows the RGMII signals on S32G-VNP-EVB3.

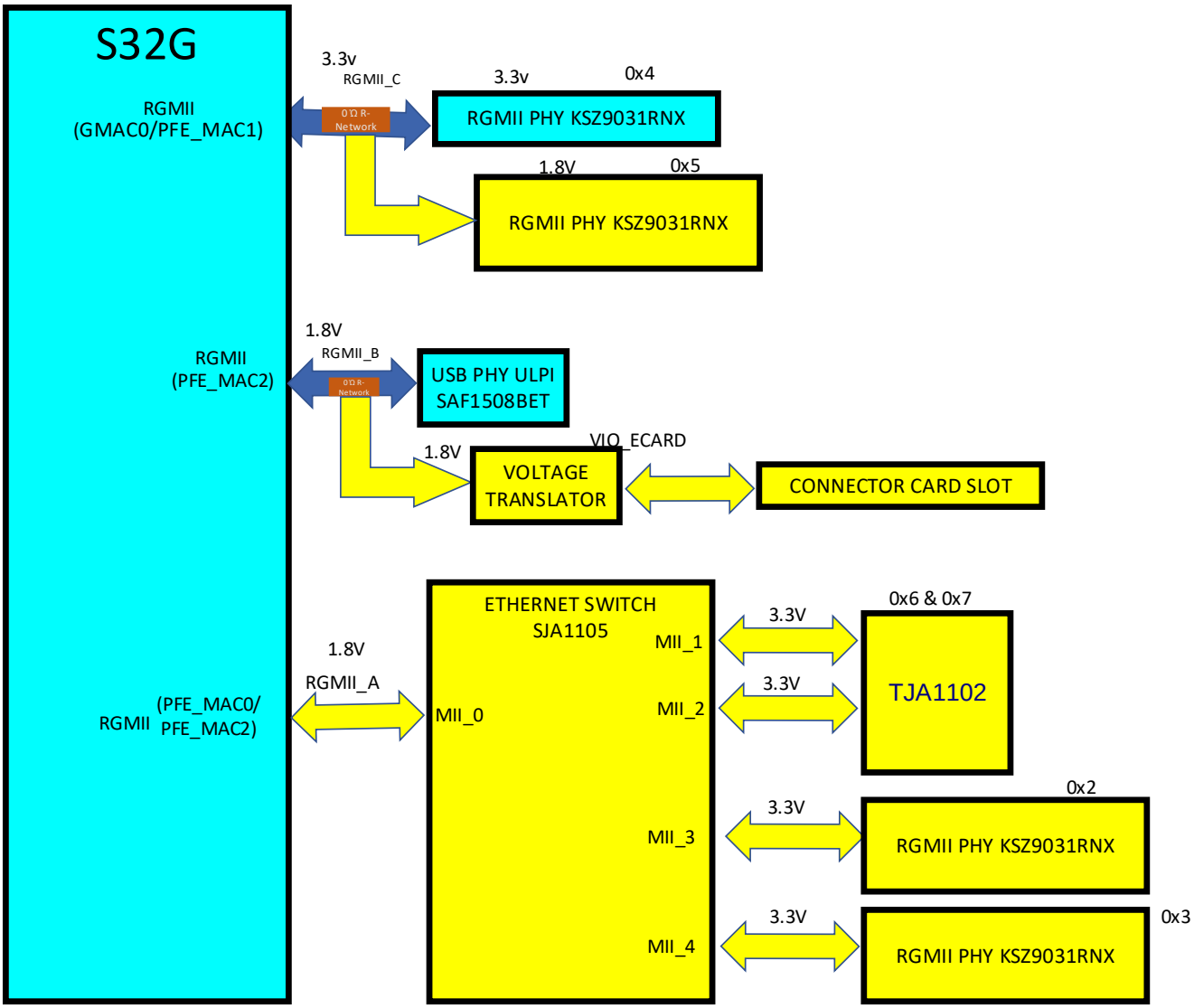

Figure 21. **RGMII signal path on S32G-VNP-EVB3**

6.7 SERDES interface

The following diagram shows the SERDES interface on S32G-VNP-EVB3.

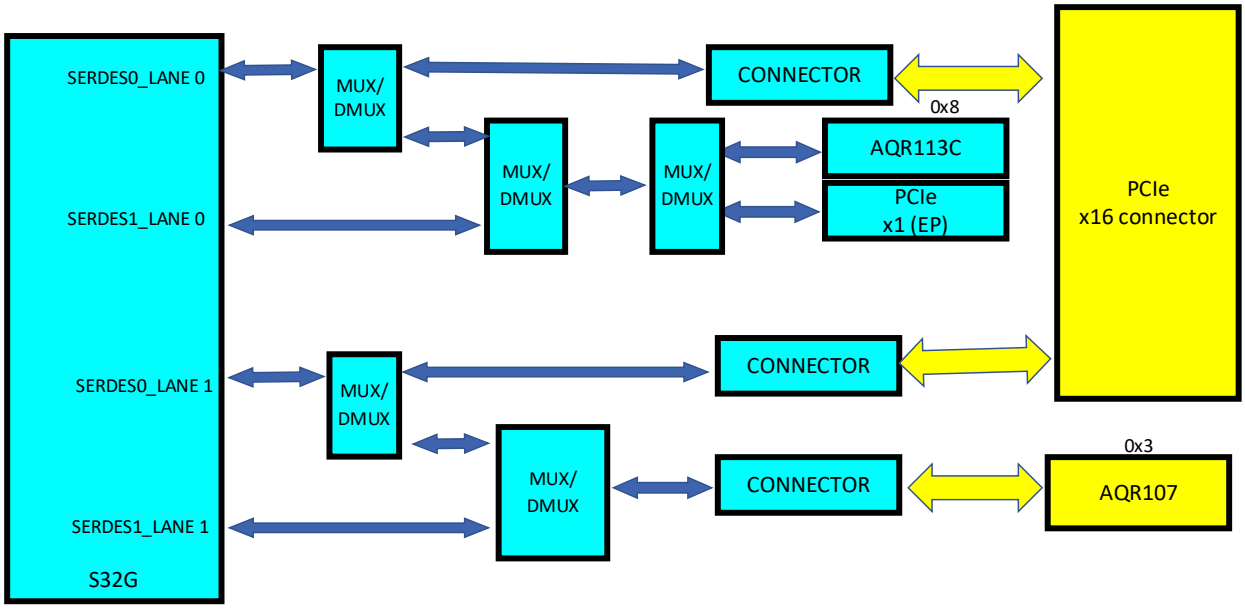

Figure 22. **SERDES interface on S32G-VNP-EVB3**

6.8 QSPI controller

The following diagram shows S32G connections to QSPI controller on S32G-VNP-EVB3.

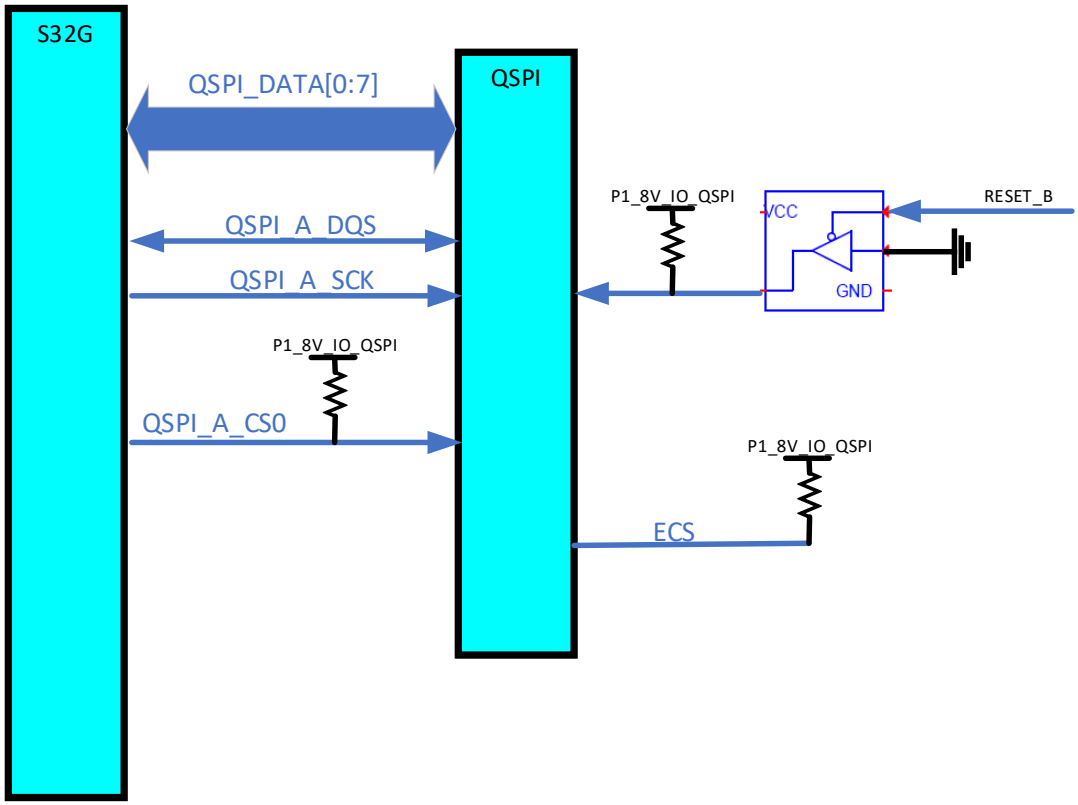

Figure 23. **S32G connections to QSPI controller on S32G-VNP-EVB3**

6.9 uSDHC controller

The following diagram shows S32G connections to uSDHC controller on S32G-VNP-EVB3.

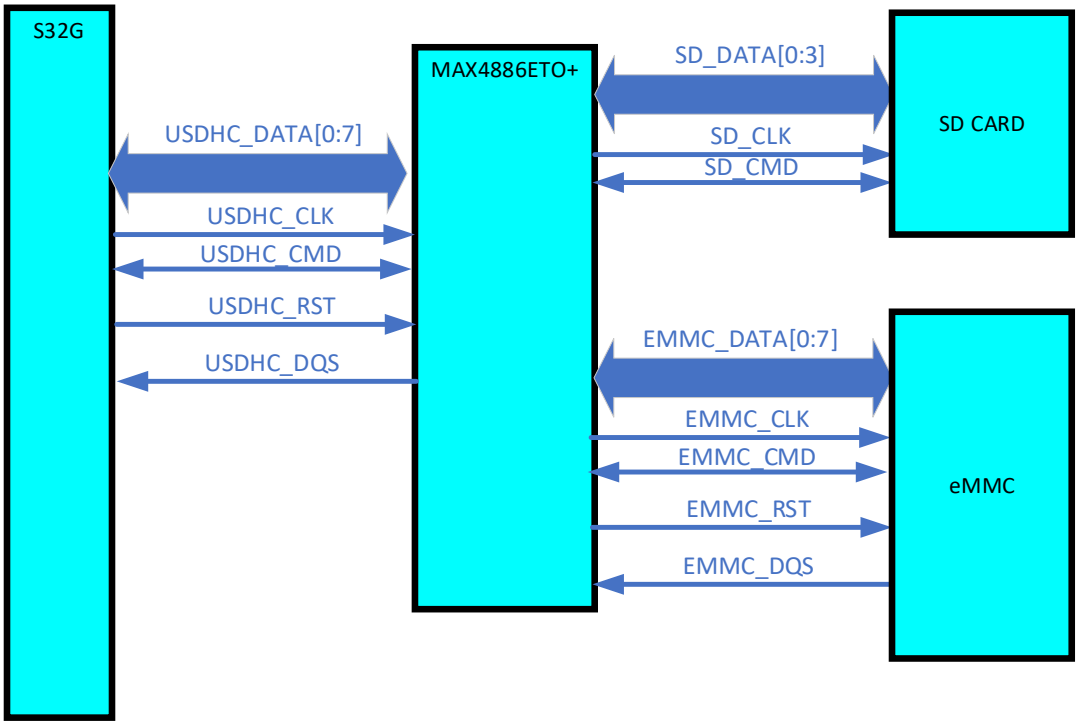

Figure 24. **S32G connections to uSDHC controller on S32G-VNP-EVB3**

6.10 USB ULPI controller

The following diagram shows S32G connections to USB ULPI controller on S32G-VNP-EVB3.

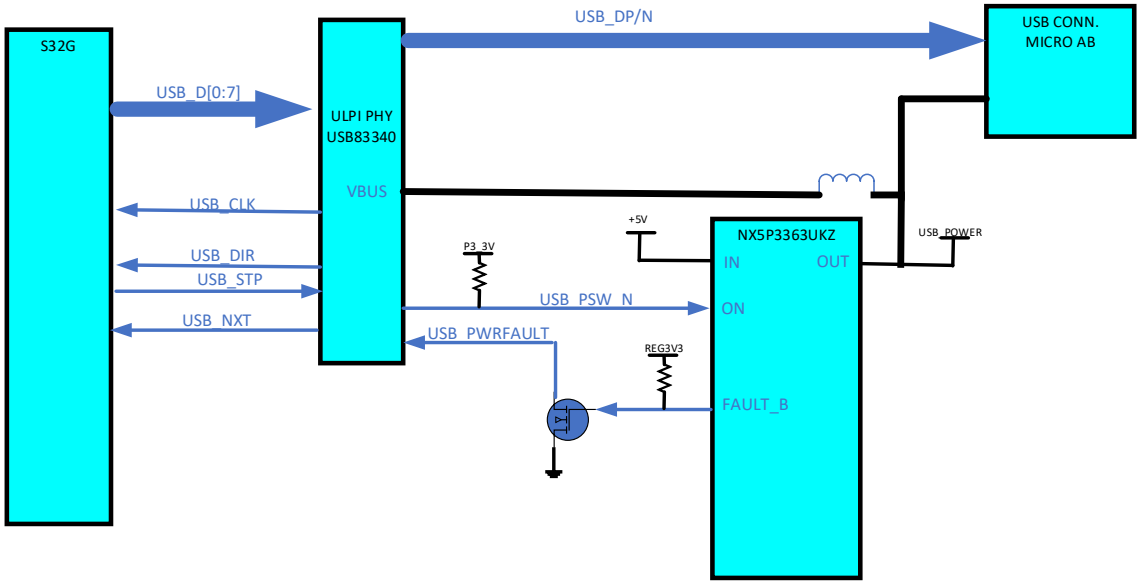

Figure 25. **S32G connections to USB ULPI controller on S32G-VNP-EVB3**

6.11 LPDDR4 controller

The following diagram shows S32G connections to LPDDR4 controller on S32G-VNP-EVB3.

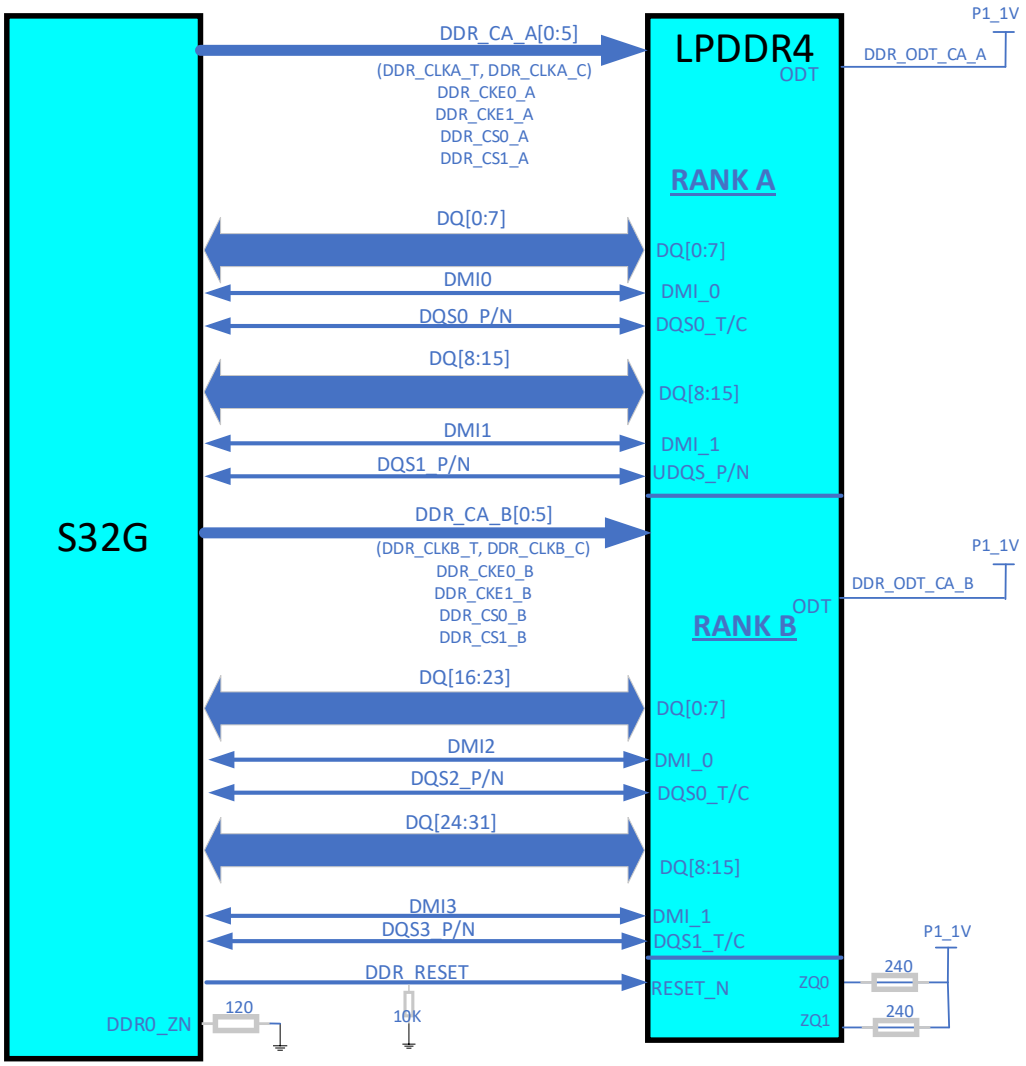

Figure 26. **S32G connections to LPDDR4 controller on S32G-VNP-EVB3**

6.12 OpenSDA controller

The following diagram shows S32G connections to OpenSDA controller on S32G-VNP-EVB3.

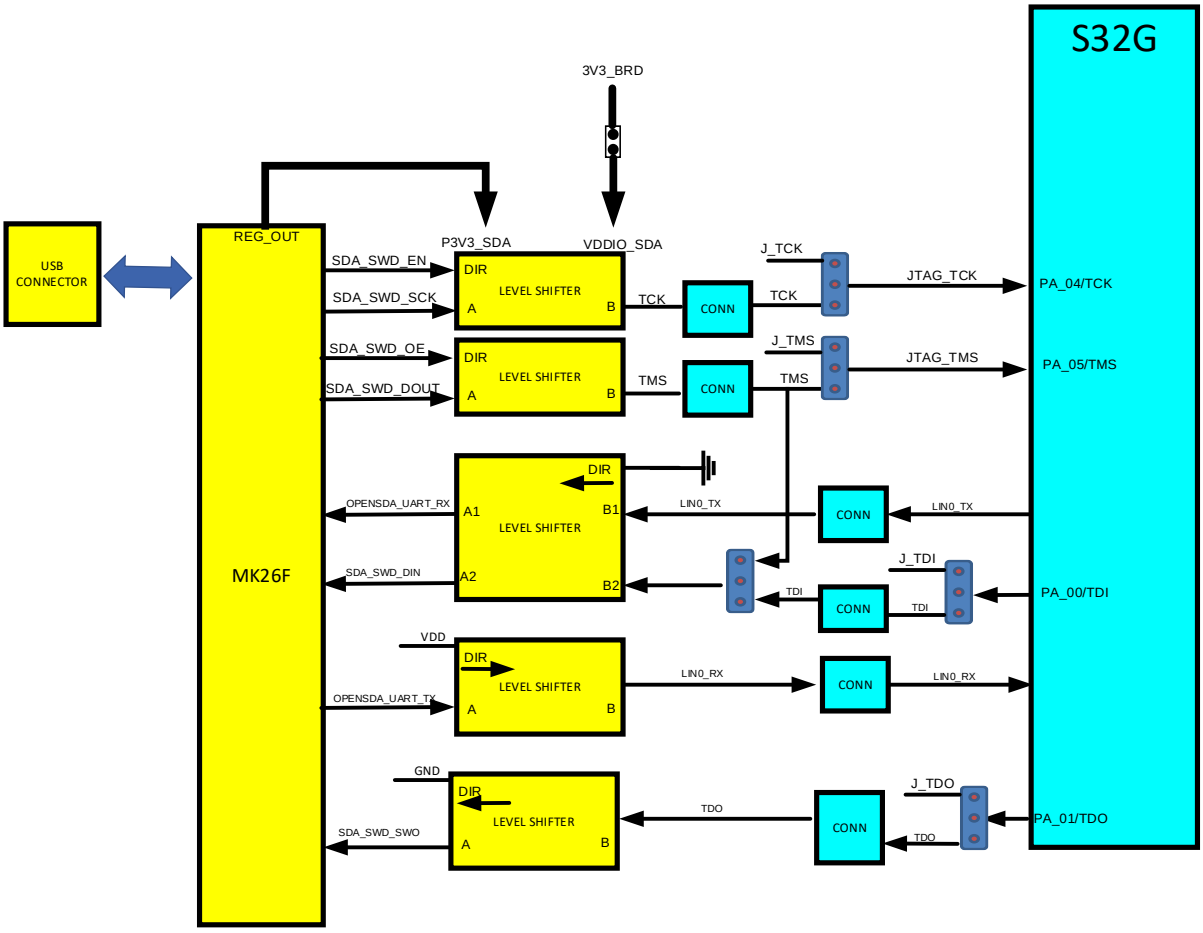

Figure 27. **S32G connections to OpenSDA controller on S32G-VNP-EVB3**

7.Hardware Modifications required on S32G-VNP-EVB3 to Support Multiple Configurations

The following sections provides information on hardware modifications required on S32G-VNP-EVB3 to support multiple configurations.

7.1 External clock using SMA connector

To use external clock using SMA connector, instead of default crystal do the following hardware modifications on S32G-PROCEVB3-S:

1. Remove resistor R157
2. Move 0Ω resistor from position A (1-2) to position B (3-2) for R160.
3. Feed external clock through SMA Connector J54.

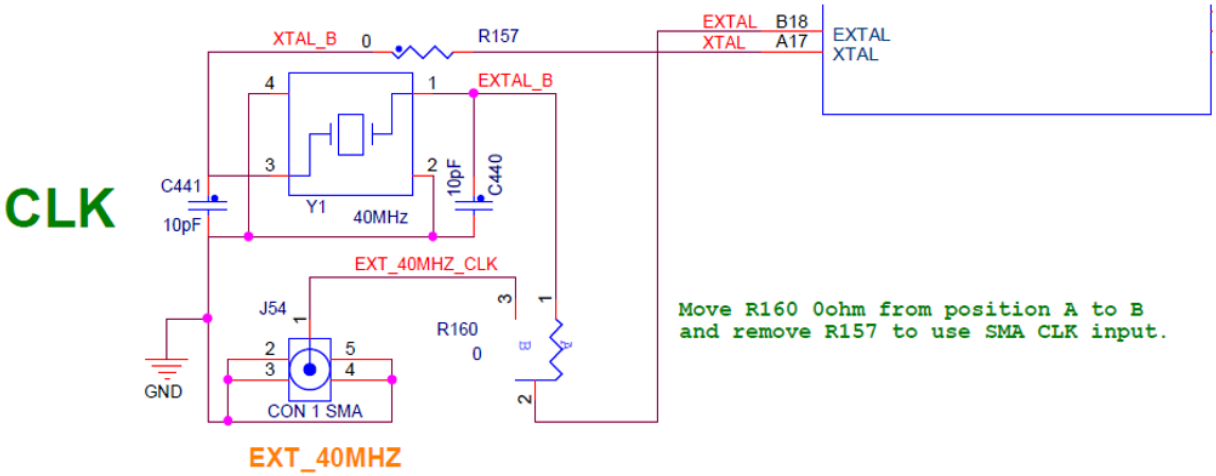

Figure 28. **Schematics snapshot showing default clock connection**

7.2 Use of KSZ PHY

To use KSZ PHY (1.8 V) on S32G-PLATEVB, instead of default KSZ PHY on S32G-PROCEVB3-S, do the following hardware modifications on S32G-PROCEVB3-S:

1. Move jumper J129 on S32G-PROCEVB3-S from position 2-3 to position 1-2 for VDD_IO_GMAC0 of 1.8 V.

2. Move 0Ω resistor from position A (1-2) to position B (3-2) for R579 to R590.

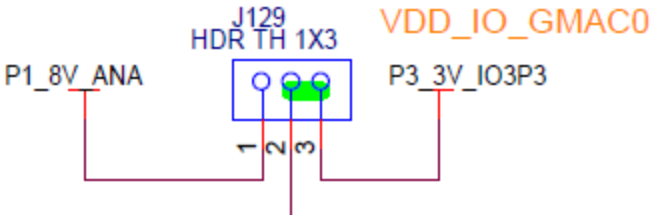

Figure 29. **Schematics snapshot showing default position of J129**

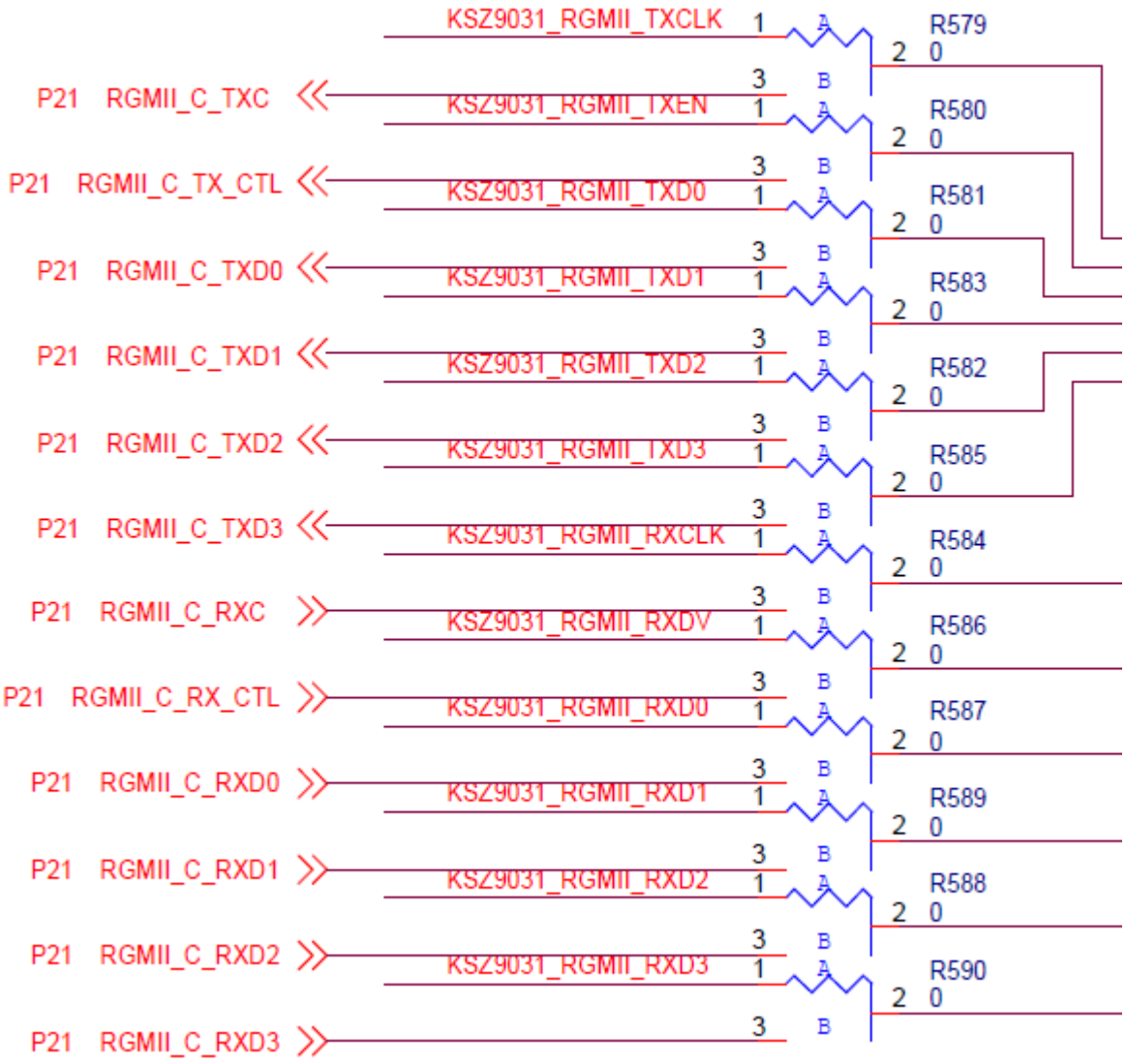

Figure 30. **Schematics snapshot showing default position of R579 to R590**

7.3 Using Ethernet card

To use an ethernet card on SABRE connector present on S32G-PLATEVB, instead of default USB ULPI PHY on S32G-PROCEVB3-S, do the following hardware modifications on S32G-PROCEVB3-S.

Move 0Ω resistor from position A (1-2) to position B (3-2) for R555 to R566.

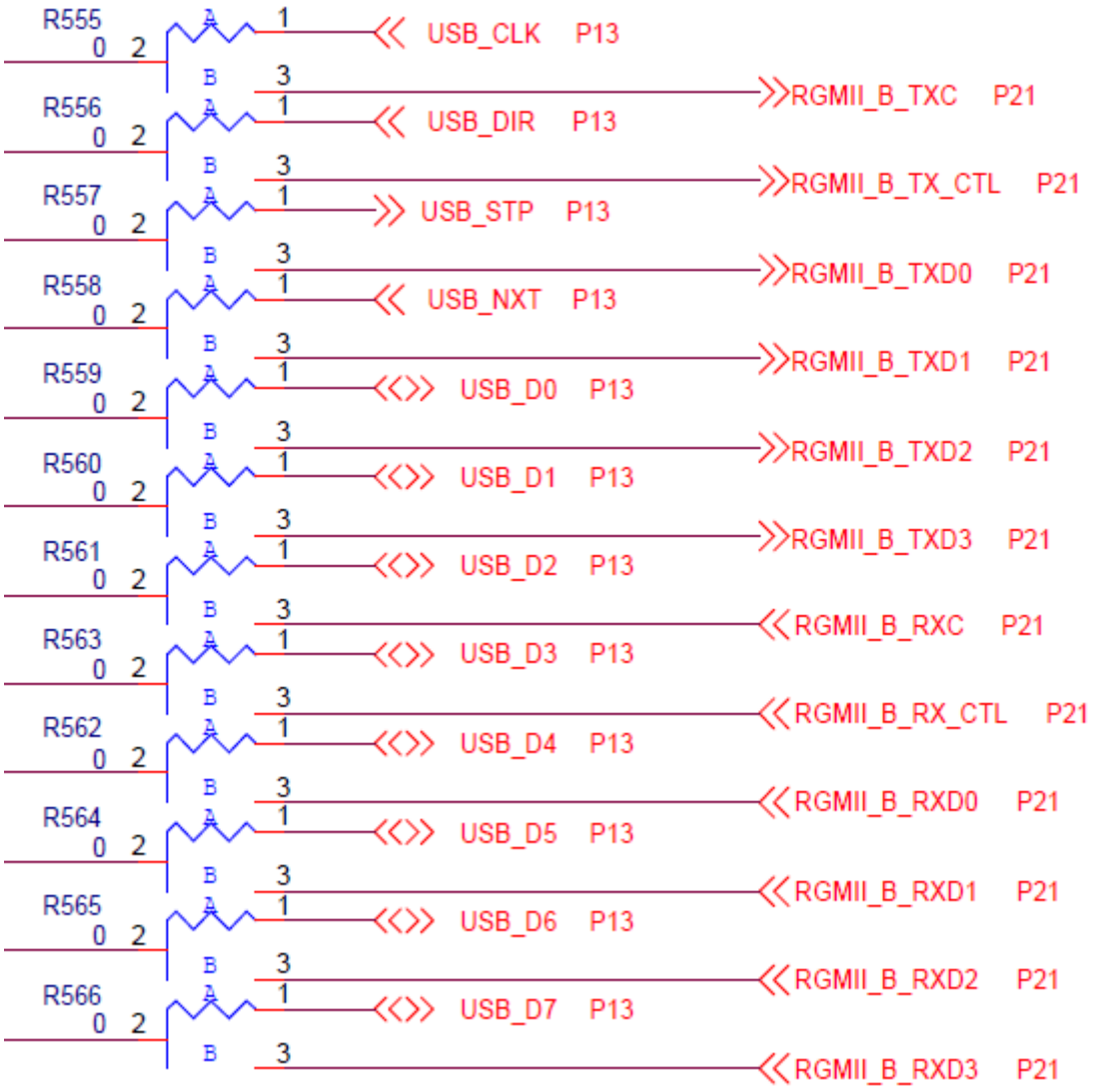

Figure 31. **Schematics snapshot showing default position of R555 to R566**

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