

DATASHEET

2G bits DDR3L SDRAM

D1216ECMDXGJD(I)-U (128M words x 16 bits) D1216ECMDXGME(I/Y)-U (128M words x 16 bits)

Specifications

- Density: 2G bits
- Organization
- 16M words x 16 bits x 8 banks
- Package
- 96-ball FBGA
- Lead-free (RoHS compliant) and Halogen-free
- Power supply: 1.35V (Typ)
- VDD, VDDQ = 1.283V to 1.45V
- Backward compatible for VDD, VDDQ=1.5V \pm 0.075V
- Data rate
- 2133Mbps/1866Mbps/1600Mbps/1333Mbps (max.)
- Backward compatible
- 2KB page size
- Row address: A0 to A13
- Column address: A0 to A9
- · Eight internal banks for concurrent operation
- Burst lengths (BL): 8 and 4 with Burst Chop (BC)
- Burst type (BT):
- Sequential (8, 4 with BC)
- Interleave (8, 4 with BC)
- Programmable /CAS (Read) Latency (CL)
- Programmable /CAS Write Latency (CWL)
- Precharge: auto precharge option for each burst access
- Driver strength: RZQ/7, RZQ/6 (RZQ = 240Ω)
- · Refresh: auto-refresh, self-refresh
- · Refresh cycles
- Average refresh period
- 7.8μs at -40°C ≤ Temperature ≤ +85°C
- 3.9μs at +85°C ≤ Temperature ≤ +105°C
- Operating Case temperature range
- 0°C to +95°C (Commercial Temperature)
- -40°C to +95°C (Industrial Temperature)
- -40°C to +105°C (Automotive Temperature)

Features

- Double-data-rate architecture: two data transfers per
- The high-speed data transfer is realized by the 8 bits prefetch pipelined architecture
- Bi-directional differential data strobe (DQS and /DQS) is transmitted/received with data for capturing data at the receiver
- DQS is edge-aligned with data for READs; centeraligned with data for WRITEs
- Differential clock inputs (CK and /CK)
- DLL aligns DQ and DQS transitions with CK transitions
- · Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- · Data mask (DM) for write data
- Posted /CAS by programmable additive latency for better command and data bus efficiency
- On-Die Termination (ODT) for better signal quality
- Synchronous ODT
- Dynamic ODT
- Asynchronous ODT
- Multi Purpose Register (MPR) for pre-defined pattern
- · ZQ calibration for DQ drive and ODT
- · Automatic self refresh (ASR)
- /RESET pin for Power-up sequence and reset function
- SRT range:
- Normal/extended
- Programmable Output driver impedance control



Revision History

Revision No.	History	Release date	Editor	Approved by
1.0	Initial release	Feb 2019		
1.1	Add Data rate 2133 and I-temp	Mar 2019		
1.2	Add P/N and A-temp	Sept 2019		
1.3	Revise file name	Nov 2019		
1.4	Add P/N	Nov 2019		
1.5	Add P/N	Dec 2019		
1.6	Remove x8 and automotive P/N	Sept 2022		
1.7	Revise timings in Table 4	Nov 2023	Jona Lee	Knuckles Shih / CK Wang
1.8	Add Automotive Temperature	Nov 2023	Jona Lee	Knuckles Shih / CK Wang

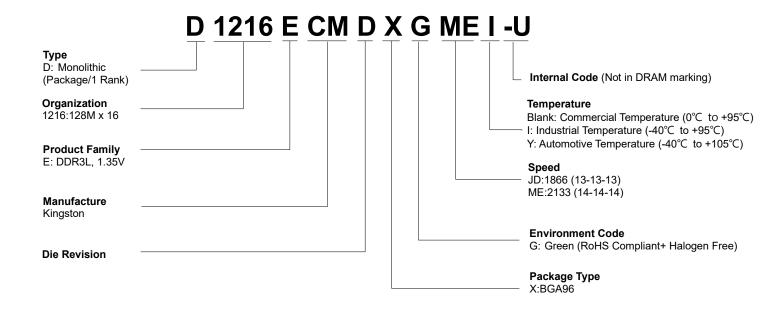
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Ordering Information

Part Number	Die revision	Organization (words x bits)	Internal Banks	JEDEC speed bin (CL-tRCD-tRP)	Pakage
D1216ECMDXGJD-U D1216ECMDXGJDI-U	D	128M x 16	8	DDR3L-1866 (13-13-13)	96-ball FBGA
D1216ECMDXGME-U D1216ECMDXGMEI-U D1216ECMDXGMEY-U	D	128M x 16	8	DDR3L-2133 (14-14-14)	96-ball FBGA

Part Number





Pin Configurations

Pin Configurations (x16 configuration)

/xxx indicates active low signal

96-ball FBGA

	1 2 3	7 8 9
Α	O O O O VDDQ DQU5 DQU7	O O O DQU4 VDDQ VSS
В	VSSQ VDD VSS	/DQSU DQU6 VSSQ
С	VDDQ DQU3 DQU1	DQSU DQU2 VDDQ
D	VSSQ VDDQ DMU	DQU0 VSSQ VDD
E	VSS VSSQ DQL0	DML VSSQ VDDQ
F	VDDQ DQL2 DQSL	DQL1 DQL3 VSSQ
G	VSSQ DQL6 /DQSL	O O O VDD VSS VSSQ
Н	VREFDQ VDDQ DQL4	DQL7 DQL5 VDDQ
J	O O O NC VSS /RAS	O O O
K	ODT VDD /CAS	CK VDD CKE
L	NC /CS /WE	A10(AP) ZQ NC
M	VSS BA0 BA2	NC VREFCA VSS
N	VDD A3 A0	A12(/BC) BA1 VDD
Р	VSS A5 A2	O O O O A1 A4 VSS
R	VDD A7 A9	O O O O
Т	VSS /RESET A13	O O O

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Pin	Function
A0 to A13*2	Address inputs A10(AP) : Auto precharge A12(/BC) : Burst chop
BA0 to BA2*2	Bank select
DQU0 to DQU7 DQL0 to DQL7	Data input/output
DQSU, /DQSU DQSL, /DQSL	Differential data strobe
/CS*2	Chip select
/RAS, /CAS, /WE*2	Command input
CKE ^{*2}	Clock enable
CK, /CK	Differential clock input
DMU, DML	Write data mask
ODT*2	ODT control

Pin name	Function
/RESET*2	Active low asynchronous reset
VDD	Supply voltage for internal circuit
VSS	Ground for internal circuit
VDDQ	Supply voltage for DQ circuit
VSSQ	Ground for DQ circuit
VREFDQ	Reference voltage for DQ
VREFCA	Reference voltage for CA
ZQ	Reference pin for ZQ calibration
NC*1	No connection

Notes: 1. Not internally connected with die.

^{2.} Input only pins (address, command, CKE,ODT and /RESET) do not supply termination.



CONTENTS

Spe	ecificatio	ons	
Fea	atures		1
Re	vision H	History	2
Ord	dering Ir	nformation	
Pai	t Numb	per	3
Pin	Config	urations	4
1.	Electri	ical Conditions	6
	1.1	Absolute Maximum Ratings	6
	1.2	Operating Temperature Condition	6
	1.3	Recommended DC Operating Conditions	7
	1.4	IDD and IDDQ Measurement Conditions	8
2.	Electri	ical Specifications	21
	2.1	DC Characteristics	21
	2.2	Pin Capacitance	23
	2.3	Standard Speed Bins	24
3.	Packa	age Drawing	29
		96-ball FBGA	



1. Electrical Conditions

- · All voltages are referenced to VSS (GND)
- · Execute power-up and Initialization sequence before proper device operation is achieved.

1.1 Absolute Maximum Ratings

Table 1: Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Notes
Power supply voltage	VDD	-0.4 to +1.80	V	1, 3
Power supply voltage for output	VDDQ	-0.4 to +1.80	V	1, 3
Input voltage	VIN	-0.4 to +1.80	V	1
Output voltage	VOUT	-0.4 to +1.80	V	1
Reference voltage	VREFCA	0.49 to 0.51 × VDD	V	3
Reference voltage for DQ	VREFDQ	0.49 to 0.51 × VDDQ	V	3
Storage temperature	Tstg	–55 to +100	°C	
Power dissipation	PD	1.0	W	1
Short circuit output current	IOUT	50	mA	1

- Notes: 1. Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
 - 2. Storage temperature is the case surface temperature on the center/top side of the DRAM.
 - 3. VDD and VDDQ must be within 300mV of each other at all times; and VREF must be no greater than $0.6 \times VDDQ$, When VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.

Caution: Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

1.2 Operating Temperature Condition

Table 2: Operating Temperature Condition

Parameter	Rating	Unit	Notes
Commercial temperature	0 to +95	°C	1, 2, 3
Industrial temperature	-40 to +95	°C	1, 2, 3
Automotive temperature	-40 to +105	°C	1, 2, 3

- Notes: 1. Operating temperature is the case surface temperature on the center/top side of the DRAM.
 - 2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM temperature must be maintained between 0°C to +85°C for commercial temperature, -40°C to +85°C for industrial/automotive temperature under all operating conditions.
 - 3. Some applications require operation of the DRAM in the Extended Temperature Range between +85°C to +95°C for commercial/industrial operating temperature and +85°C to +105°C for automotive operating temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
 - a) Refresh commands must be doubled in frequency, therefore reducing the refresh interval tREFI to 3.9 µs. (This double refresh requirement may not apply for some devices.)
 - b) If Self-refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 bit [A6, A7] = [0, 1]) or enable the optional Auto Self-Refresh mode (MR2 bit [A6, A7] = [1, 0]).



1.3 Recommended DC Operating Conditions

Table 3-a: Recommended DC Operating Conditions, DDR3L Operation.

Parameter	Symbol	min	typ	max	Unit	Notes
Supply voltage	VDD	1.283	1.35	1.45	V	1, 2, 3
Supply voltage for DQ	VDDQ	1.283	1.35	1.45	V	1, 2, 3

Notes:1. Under all conditions VDDQ must be less than or equal to VDD.

- 2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
- 3. Commercial Temperature 0°C to +95°C, Industrial Temperature -40°C to +95° and Automotive Temperature -40°C to +105°C.

Table 3-b: Recommended DC Operating Conditions, DDR3 Operation.

Parameter	Symbol	min	typ	max	Unit	Notes
Supply voltage	VDD	1.425	1.5	1.575	V	1, 2, 3
Supply voltage for DQ	VDDQ	1.425	1.5	1.575	V	1, 2, 3

Notes: 1. Under all conditions VDDQ must be less than or equal to VDD.

- 2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
- 3. Commercial Temperature 0°C to +95°C, Industrial Temperature -40°C to +95° and Automotive Temperature -40°C to +105°C.



1.4 IDD and IDDQ Measurement Conditions

In this chapter, IDD and IDDQ measurement conditions such as test load and patterns are defined.

The figure Measurement Setup and Test Load for IDD and IDDQ Measurements shows the setup and test load for IDD and IDDQ measurements.

- IDD currents (such as IDD0, IDD1, IDD2N, IDD2NT, IDD2P0, IDD2P1, IDD2Q, IDD3N, IDD3P, IDD4R, IDD4W, IDD5B, IDD6, IDD6ET and IDD7) are measured as time-averaged currents with all VDD balls of the DDR3 SDRAM under test tied together. Any IDDQ current is not included in IDD currents.
- IDDQ currents (such as IDDQ2NT and IDDQ4R) are measured as time-averaged currents with all VDDQ balls of the DDR3 SDRAM under test tied together. Any IDD current is not included in IDDQ currents.

Note:IDDQ values cannot be directly used to calculate I/O power of the DDR3 SDRAM. They can be used to support correlation of simulated I/O power to actual I/O power as outlined in correlation from simulated channel I/O power to actual channel I/O power supported by IDDQ measurement.

For IDD and IDDQ measurements, the following definitions apply:

- L and 0: VIN ≤ VIL(AC)max
- H and 1: VIN ≥ VIH(AC)min
- MID-LEVEL: defined as inputs are VREF = VDDQ / 2
- FLOATING: don't care or floating around VREF.
- Timings used for IDD and IDDQ measurement-loop patterns are provided in Timings used for IDD and IDDQ Measurement-Loop Patterns table.
- Basic IDD and IDDQ measurement conditions are described in Basic IDD and IDDQ Measurement Conditions table.

Note: The IDD and IDDQ measurement-loop patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.

- Detailed IDD and IDDQ measurement-loop patterns are described in IDD0 Measurement-Loop Pattern table through IDD7 Measurement-Loop Pattern table.
- IDD Measurements are done after properly initializing the DDR3 SDRAM. This includes but is not limited to setting. RON = RZQ/7 (34 Ω in MR1);

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Qoff = 0B (Output Buffer enabled in MR1);
RTT_Nom = RZQ/6 (40\Omega in MR1);
RTT_WR = RZQ/2 (120\Omega in MR2);
TDQS Feature disabled in MR1
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- Define D = {/CS, /RAS, /CAS, /WE} : = {H, L, L, L}
- Define /D = {/CS, /RAS, /CAS, /WE} : = {H, H, H, H}



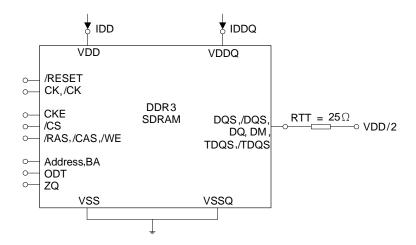


Figure 1: Measurement Setup and Test Load for IDD and IDDQ Measurements

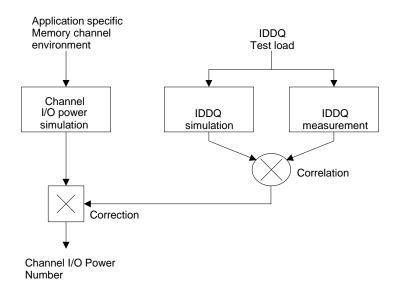


Figure 2: Correlation from Simulated Channel I/O Power to Actual Channel I/O Power Supported by IDDQ Measurement



1.4.1 Timings Used for IDD and IDDQ Measurement-Loop Patterns

Table 4: Timings Used for IDD and IDDQ Measurement-Loop Patterns

	DDR3L-1333	DDR3L-1600	DDR3L-1866	DDR3L-2133	
Parameter	9-9-9	11-11-11	13-13-13	14-14-14	Unit
CL	9	11	13	14	nCK
tCK(min)	1.5	1.25	1.071	0.938	ns
nRCD(min)	9	11	13	14	nCK
nRC(min)	33	39	45	50	nCK
nRAS(min)	24	28	32	36	nCK
nRP(min)	9	11	13	14	nCK
nFAW	30	32	33	38	nCK
nRRD	5	6	6	7	nCK
nRFC	107	128	150	172	nCK

Basic IDD and IDDQ Measurement Conditions Table 5: Basic IDD and IDDQ Measurement Conditions

Parameter	Symbol	Description
Operating one bank active precharge current	IDD0	CKE: H; External clock: on; tCK, nRC, nRAS, CL: see Table 4; BL: 8*1; AL: 0; /CS: H between ACT and PRE; Command, address, bank address inputs: partially toggling according to Table 6; Data I/O: MID-LEVEL; DM: stable at 0; Bank activity: cycling with one bank active at a time: 0,0,1,1,2,2, (see Table 6); Output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; Pattern details: see Table 6
Operating one bank active-read-precharge current	IDD1	CKE: H; External clock: On; tCK, nRC, nRAS, nRCD, CL: see Table 4; BL: 8*1, *6; AL: 0; /CS: H between ACT, RD and PRE; Command, address, bank address inputs, data I/O: partially toggling according to Table 7; DM: stable at 0; Bank activity: cycling with one bank active at a time: 0,0,1,1,2,2, (see Table 7); Output buffer and RTT: enabled in MR*2; ODT Signal: stable at 0; Pattern details: see Table 7
Precharge standby current	IDD2N	CKE: H; External clock: on; tCK, CL: see Table 4 BL: 8*1; AL: 0; /CS: stable at 1; Command, address, bank address Inputs: partially toggling according to Table 8; data I/O: MID-LEVEL; DM: stable at 0; bank activity: all banks closed; output buffer and RTT: enabled in mode registers*2; ODT signal: stable at 0; pattern details: see Table 8
Precharge standby ODT current	IDD2NT	CKE: H; External clock: on; tCK, CL: see Table 4; BL: 8*1; AL: 0; /CS: stable at 1; Command, address, bank address Inputs: partially toggling according to Table 9; data I/O: MID-LEVEL; DM: stable at 0; bank activity: all banks closed; output buffer and RTT: enabled in MR*2; ODT signal: toggling according to Table 9; pattern details: see Table 9
Precharge standby ODT IDDQ current	IDDQ2NT	Same definition like for IDD2NT, however measuring IDDQ current instead of IDD current
Precharge power-down current slow exit	IDD2P0	CKE: L; External clock: on; tCK, CL: see Table 4; BL: 8*1; AL: 0; /CS: stable at 1; Command, address, bank address inputs: stable at 0; data I/O: MID-LEVEL; DM: stable at 0; bank activity: all banks closed; output buffer and RTT: EMR*2; ODT signal: stable at 0; precharge power down mode: slow exit*3
Precharge power-down current fast exit	IDD2P1	CKE: L; External clock: on; tCK, CL: see Table 4; BL: 8*1; AL: 0; /CS: stable at 1; Command, address, bank address Inputs: stable at 0; data I/O: MID-LEVEL; DM:stable at 0; bank activity: all banks closed; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; precharge power down mode: fast exit*3
Precharge quiet standby current	IDD2Q	CKE: H; External clock: On; tCK, CL: see Table 4; BL: 8*1; AL: 0; /CS: stable at 1; Command, address, bank address Inputs: stable at 0; data I/O: MID-LEVEL; DM: stable at 0;bank activity: all banks closed; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0
Active standby current	IDD3N	CKE: H; External clock: on; tCK, CL: see Table 4; BL: 8*1; AL: 0; /CS: stable at 1; Command, address, bank address Inputs: partially toggling according to Table 8; data I/O: MID-LEVEL; DM: stable at 0; bank activity: all banks open; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; pattern details: see Table 8
Active power-down current	IDD3P	CKE: L; External clock: on; tCK, CL: see Table 4; BL: 8*1; AL: 0; /CS: stable at 1; Command, address, bank address inputs: stable at 0; data I/O: MID-LEVEL; DM:stable at 0; bank activity: all banks open; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0
Operating burst read current	IDD4R	CKE: H; External clock: on; tCK, CL: see Table 4; BL: 8*1, *6; AL: 0; /CS: H between RD; Command, address, bank address Inputs: partially toggling according to Table 11; data I/O: seamless read data burst with different data between one burst and the next one according to Table 11; DM: stable at 0; bank activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2, (see Table 11); Output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; pattern details: see Table 11



Table 5: Basic IDD and IDDQ Measurement Conditions (cont'd)

Parameter	Symbol	Description
Operating burst write current	IDD4W	CKE: H; External clock: on; tCK, CL: see Table 4; BL: 8*1; AL: 0; /CS: H between WR; command, address, bank address inputs: partially toggling according to Table 12; data I/O: seamless write data burst with different data between one burst and the next one according to IDD4W Measurement-Loop Pattern table; DM: stable at 0; bank activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2, (see Table 12); Output buffer and RTT: enabled in MR*2; ODT signal: stable at H; pattern details: see Table 12
Burst refresh current	IDD5B	CKE: H; External clock: on; tCK, CL, nRFC: see Table 4; BL: 8*1; AL: 0; /CS: H between REF; Command, address, bank address Inputs: partially toggling according to Table 13; data I/O: MID-LEVEL; DM: stable at 0; bank activity: REF command every nRFC (Table 12); output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; pattern details: see Table 13
Self-refresh current: normal temperature range	IDD6	Commercial temperature: 0 to 85°C and Industrial temperature -40 to 85°C; ASR: disabled*4; SRT: Normal*5; CKE: L; External clock: off; CK and /CK: L; CL: see Table 4; BL: 8*1;AL: 0; /CS, command, address, bank address, data I/O: MID-LEVEL; DM: stable at 0; bank activity: Self-refresh operation; output buffer and RTT: enabled in MR*2; ODT signal: MID-LEVEL
Self-refresh current: extended temperature range	IDD6ET	Commercial temperature 0 to 95°C, Industrial temperature -40 to 95°C and Automotive temperature -40 to 105°C; ASR: Disabled*4; SRT: Extended*5; CKE: L; External clock: off; CK and /CK: L; CL: Table 4; BL: 8*1; AL: 0; /CS, command, address, bank address, data I/O: MID-LEVEL; DM: stable at 0; bank activity: Extended temperature self-refresh operation; output buffer and RTT: enabled in MR*2; ODT signal: MID-LEVEL
Operating bank interleave read current	IDD7	CKE: H; External clock: on; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: see Table 4; BL: 8*1, *6; AL: CL-1; /CS: H between ACT and RDA; Command, address, bank address Inputs: partially toggling according to Table 15; data I/O: read data bursts with different data between one burst and the next one according to Table 15; DM: stable at 0; bank activity: two times interleaved cycling through banks (0, 1, ···7) with different addressing, see Table 15; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; pattern details: see Table 15
RESET low current	IDD8	/RESET: low; External clock: off; CK and /CK: low; CKE: FLOATING; /CS, command, address, bank address, Data IO: FLOATING; ODT signal: FLOATING RESET low current reading is valid once power is stable and /RESET has been low for at least 1ms.

Notes: 1. Burst Length: BL8 fixed by MRS: MR0 bits [1,0] = [0,0].

- 2. MR: Mode Register
 - Output buffer enable: set MR1 bit A12 = 1 and MR1 bits [5, 1] = [0,1];
 - RTT_Nom enable: set MR1 bits [9, 6, 2] = [0, 1, 1]; RTT_WR enable: set MR2 bits [10, 9] = [1,0].
- 3. Precharge power down mode: set MR0 bit A12= 0 for Slow Exit or MR0 bit A12 = 1 for fast exit.
- 4. Auto self-refresh (ASR): set MR2 bit A6 = 0 to disable or 1 to enable feature.
- 5. Self-refresh temperature range (SRT): set MR0 bit A7= 0 for normal or 1 for extended temperature range.
- 6. Read burst type: nibble sequential, set MR0 bit A3 = 0



Table 6: IDD0 Measurement-Loop Pattern

CK, /CK	CKE	Sub -Loop	Cycle number	Com- mand	/CS	/RAS	/CAS	/WE	ODT	BA*3	A11 -Am	A10	A7 -A9	A3 -A6	A0 -A2	Data*2
			0	ACT	0	0	1	1	0	0	0	0	0	0	0	
			1, 2	D, D	1	0	0	0	0	0	0	0	0	0	0	
			3, 4	/D, /D	1	1	1	1	0	0	0	0	0	0	0	
				Repea	t patter	n 14 ເ	until nR	AS - 1,	trunca	te if ned	cessary	,				
			nRAS	PRE	0	0	1	0	0	0	0	0	0	0	0	
				Repea	t patter	n 14 ເ	until nR	C - 1, tı	runcate	if nece	ssary					
		0	1 x nRC + 0	ACT	0	0	1	1	0	0	0	0	0	F	0	
	H O	0	1 x nRC + 1, 2	D, D	1	0	0	0	0	0	0	0	0	F	0	
	Toggling Static H		1 x nRC + 3,4	/D, /D	1	1	1	1	0	0	0	0	0	F	0	
	ggli			Repea	t patter	n nRC -	+ 1,,4	until 1	*nRC +	nRAS	- 1, trui	ncate if	neces	sary		
	2		1 x nRC + nRAS	PRE	0	0	1	0	0	0	0	0	0	F	0	
				Repea	t nRC +	+ 1,,4	until 2	k nRC -	1, trun	cate if r	necessa	ary				
		1	2 x nRC	Repea	t Sub-L	.oop 0, ı	use BA:	= 1 inst	ead							
		2	4 x nRC	Repea	t Sub-L	.oop 0, ı	use BA:	= 2 inst	ead							
		3	6 x nRC	Repea	t Sub-L	.oop 0, ı	use BA:	= 3 inst	ead							
		4	8 x nRC	Repea	t Sub-L	.oop 0, ı	use BA:	= 4 inst	ead							
		5	10 x nRC	Repea	t Sub-L	.oop 0,	use BA:	= 5 inst	ead							
		6	12 x nRC	Repea	t Sub-L	.oop 0,	use BA:	= 6 inst	ead							
		7	14 x nRC	Repea	t Sub-L	.oop 0,	use BA:	= 7 inst	ead							

Notes: 1. DM must be driven low all the time. DQS, /DQS are FLOATING.

- 2. DQ signals are FLOATING.
- 3. BA: BA0 to BA2.
- 4. Am: m means Most Significant Bit (MSB) of Row address.



Table 7: IDD1 Measurement-Loop Pattern

CK, /CK	CKE	Sub -Loop	Cycle number	Com- mand	/CS	/RAS	/CAS	/WE	ODT	BA*3	A11 -Am	A10	A7 -A9	A3 -A6	A0 -A2	Data*2
			0	ACT	0	0	1	1	0	0	0	0	0	0	0	_
			1, 2	D, D	1	0	0	0	0	0	0	0	0	0	0	
			3, 4	/D, /D	1	1	1	1	0	0	0	0	0	0	0	
				Repeat	-							U	U	0	U	
					-							0	0	^	^	0000000
			nRCD	RD	0	1	0	1	0	0	0	0	0	0	0	00000000
				Repeat	•		ntil nR <i>A</i>									
			nRAS	PRE	0	0	1	0	0	0	0	0	0	0	0	<u> </u>
				Repeat	pattern	14 u	ntil nRC	C - 1, tru	ıncate i	f neces	sary					
		0	1 x nRC + 0	ACT	0	0	1	1	0	0	0	0	0	F	0	_
	I	Ü	1 x nRC + 1, 2	D, D	1	0	0	0	0	0	0	0	0	F	0	_
	Static		1 x nRC + 3, 4	/D, /D	1	1	1	1	0	0	0	0	0	F	0	_
	ng (Repeat	pattern	nRC +	1,, 4	until nf	RC + nF	RCD - 1	, trunca	ite if ne	cessa	ry		
	Toggling Static H		1 x nRC + nRCD	RD	0	1	0	1	0	0	0	0	0	F	0	00110011
	_			Repeat	pattern	nRC +	1,, 4	until nf	RC + nF	RAS - 1	, trunca	te if ne	cessa	ry		
			1 x nRC + nRAS	PRE	0	0	1	0	0	0	0	0	0	F	0	_
				Repeat	pattern	nRC +	1,, 4	until 2	x nRC -	1, trun	cate if r	necessa	ary			
	•	1	2×nRC	Repeat	Sub-Lo	op 0, u	se BA=	: 1 inste	ead							
	•	2	4 × nRC	Repeat	Sub-Lo	op 0, u	se BA=	2 inste	ead							
	•	3	6 × nRC	Repeat	Sub-Lo	op 0, u	se BA=	: 3 inste	ead							
	•	4	8 × nRC	Repeat	Sub-Lo	op 0, u	se BA=	4 inste	ead							
	•	5	10 × nRC	Repeat	Sub-Lo	op 0, u	se BA=	5 inste	ead							
	;	6	12 × nRC	Repeat	Sub-Lo	op 0, u	se BA=	6 inste	ead							
	•	7	14 × nRC	Repeat	Sub-Lo	op 0, u	se BA=	7 inste	ead							_

Notes: 1. DM must be driven low all the time. DQS, /DQS are used according to read commands, otherwise FLOATING.



^{2.} Burst sequence driven on each DQ signal by read command. Outside burst operation, DQ signals are FLOATING.

^{3.} BA: BA0 to BA2.

^{4.} Am: m means Most Significant Bit (MSB) of Row address.

Table 8: IDD2N and IDD3N Measurement-Loop Pattern

CK, /CK	CKE	Sub -Loop	Cycle number	Com- mand	/CS	/RAS	/CAS	/WE	ODT	BA*3	A11 -Am	A10	A7 -A9	A3 -A6	A0 -A2 Data* ²
			0	D	1	0	0	0	0	0	0	0	0	0	0
		0	1	D	1	0	0	0	0	0	0	0	0	0	0
		0	2	/D	1	1	1	1	0	0	0	0	0	F	0
	I		3	/D	1	1	1	1	0	0	0	0	0	F	0
	Static	1	4 to 7	Repeat	Sub-Lo	oop 0, u	se BA=	= 1 inste	ead						
	S	2	8 to 11	Repeat	Sub-Lo	oop 0, u	se BA=	2 inste	ead						
	Toggling	3	12 to 15	Repeat	Sub-Lo	oop 0, u	se BA=	3 inste	ead						
	Tog	4	16 to 19	Repeat	Sub-Lo	oop 0, u	se BA=	4 inste	ead						
	•	5	20 to 23	Repeat	Sub-Lo	oop 0, u	se BA=	5 inste	ead						
		6	24 to 27	Repeat	Sub-Lo	oop 0, u	se BA=	6 inste	ead						
		7	28 to 31	Repeat	Sub-Lo	oop 0, u	se BA=	7 inste	ead						

Notes: 1. DM must be driven low all the time. DQS, /DQS are FLOATING.

- 2. DQ signals are FLOATING.
- 3. BA: BA0 to BA2.
- 4. Am: m means Most Significant Bit (MSB) of Row address.

Table 9: IDD2NT and IDDQ2NT Measurement-Loop Pattern

CK,		Sub	Cycle	Com-							A11		Α7	А3	A0
/CK	CKE	-Loop	number	mand	/CS	/RAS	/CAS	/WE	ODT	BA*3	-Am	A10	-A9	-A6	-A2 Data*2
			0	D	1	0	0	0	0	0	0	0	0	0	0
		0	1	D	1	0	0	0	0	0	0	0	0	0	0
		0	2	/D	1	1	1	1	0	0	0	0	0	F	0
	I S		3	/D	1	1	1	1	0	0	0	0	0	F	0
	Static	1	4 to 7	Repeat	Sub-Lo	op 0, b	ut ODT	= 0 an	d BA=	1					_
	S Di	2	8 to 11	Repeat	Sub-Lo	op 0, b	ut ODT	= 1 an	d BA=	2					_
	glir	3	12 to 15	Repeat	Sub-Lo	op 0, b	ut ODT	= 1 an	d BA=	3					_
	Toggling	4	16 to 19	Repeat	Sub-Lo	op 0, b	ut ODT	= 0 an	d BA=	4					
	•	5	20 to 23	Repeat	Sub-Lo	op 0, b	ut ODT	= 0 an	d BA=	5					
		6	24 to 27	Repeat	Sub-Lo	op 0, b	ut ODT	= 1 an	d BA=	6					
	-	7	28 to 31	Repeat	Sub-Lo	op 0, b	ut ODT	= 1 an	d BA=	7					

Notes: 1. DM must be driven low all the time. DQS, /DQS are FLOATING.

- 2. DQ signals are FLOATING.
- 3. BA: BA0 to BA2.
- 4. Am: m means Most Significant Bit (MSB) of Row address.



Table 10: IDD2P0, IDD2P1, IDD2Q and IDD3P Measurement-Loop Pattern

External Clock	Name	СК	CKE	RC	RAS	RCD	RRD	CL	AL	CSB	Comm and	A0- Am	ВА	DM	ODT			Active banks	ldle banks	Data
	IDD2P0 Precharge Power-Down Current (Slow Exit)	CK (MIN) IDD	0	N/A	N/A	N/A	N/A	N/A	N/A	1	0	0	0	0	Acted, off	Acted	8	None	All	Midlevel
Toggling	IDD2P1 Precharge Power-Down Current (Fast Exit)	CK (MIN) IDD	0	N/A	N/A	N/A	N/A	N/A	N/A	1	0	0	0	0	Acted, off	Acted	8	None	All	Midlevel
Ď	IDD2Q Precharge Quiet Standby Current	CK (MIN) IDD	1	N/A	N/A	N/A	N/A	N/A	N/A	1	0	0	0	0	Acted, off	Acted	8	None	All	Midlevel
	IDD3P Active Power-Down Current	CK (MIN) IDD	0	N/A	N/A	N/A	N/A	N/A	N/A	1	0	0	0	0	Acted, off	Acted	8	All	None	Midlevel

Notes: 1. MR0[12] defines DLL on/off behavior during precharge power-down only; DLL on (fast exit, MR0[12] = 1) and DLL off (slow exit, MR0[12] = 0).

^{2. &}quot;Acted, off" means the MR bits are enabled, but the signal is LOW.

Table 11: IDD4R and Measurement-Loop Pattern

CK,		Sub	Cycle	Com-							A11		Α7	А3	A0	
/CK	CKE	-Loop	number	mand	/CS	/RAS	/CAS	/WE	ODT	BA*3	-Am	A10	-A9	-A6	-A2	Data*2
			0	RD	0	1	0	1	0	0	0	0	0	0	0	00000000
			1	D	1	0	0	0	0	0	0	0	0	0	0	
		0	2,3	/D, /D	1	1	1	1	0	0	0	0	0	0	0	_
		U	4	RD	0	1	0	1	0	0	0	0	0	F	0	00110011
	I		5	D	1	0	0	0	0	0	0	0	0	F	0	_
	Static		6,7	/D, /D	1	1	1	1	0	0	0	0	0	F	0	_
	S Gu	1	8 to 15	Repeat	Sub-Lo	op 0, b	ut BA=	1								_
	Toggling -	2	16 to 23	Repeat	Sub-Lo	op 0, b	ut BA=	2								
	Tog	3	24 to 31	Repeat	Sub-Lo	op 0, b	ut BA=	3								
	-	4	32 to 39	Repeat	Sub-Lo	op 0, b	ut BA=	4								
	-	5	40 to 47	Repeat	Sub-Lo	op 0, b	ut BA=	5								
	-	6	48 to 55	Repeat	Sub-Lo	op 0, b	ut BA=	6								
	-	7	56 to 63	Repeat	Sub-Lo	op 0, b	ut BA=	7								

Notes: 1. DM must be driven low all the time. DQS, /DQS are used according to read commands, otherwise FLOATING.

2. Burst sequence driven on each DQ signal by read command. Outside burst operation, DQ signals are FLOATING.

- 3. BA: BA0 to BA2.
- 4. Am: m means Most Significant Bit (MSB) of Row address.



Table 12: IDD4W Measurement-Loop Pattern

CK,		Sub	Cycle	Com-							A11		A7	А3	Α0	
/CK	CKE	-Loop	number	mand	/CS	/RAS	/CAS	/WE	ODT	BA* ³	-Am	A10	-A9	-A6	-A2	Data*2
			0	WR	0	1	0	0	1	0	0	0	0	0	0	00000000
			1	D	1	0	0	0	1	0	0	0	0	0	0	
		0	23	/D, /D	1	1	1	1	1	0	0	0	0	0	0	_
		0	4	RD	0	1	0	0	1	0	0	0	0	F	0	00110011
	I		5	D	1	0	0	0	1	0	0	0	0	F	0	_
	Static		6,7	/D, /D	1	1	1	1	1	0	0	0	0	F	0	_
	S	1	8 to 15	Repeat	Sub-Lo	op 0, b	ut BA=	1								
	Toggling	2	16 to 23	Repeat	Sub-Lo	op 0, b	ut BA=	2								
	Tog	3	24 to 31	Repeat	Sub-Lo	op 0, b	ut BA=	3								
	•	4	32 to 39	Repeat	Sub-Lo	op 0, b	ut BA=	4								
	=	5	40 to 47	Repeat	Sub-Lo	op 0, b	ut BA=	5								
	-	6	48 to 55	Repeat	Sub-Lo	op 0, b	ut BA=	6								
	-	7	56 to 63	Repeat	Sub-Lo	oop 0, b	ut BA=	7								

Notes: 1. DM must be driven low all the time. DQS, /DQS are used according to read commands, otherwise FLOATING.

2. Burst sequence driven on each DQ signal by read command. Outside burst operation, DQ signals are FLOATING.

- 3. BA: BA0 to BA2.
- 4. Am: m means Most Significant Bit (MSB) of Row address.

Table 13: IDD5B Measurement-Loop Pattern

CK,		Sub	Cycle	Com-							A11		Α7	А3	A0	
/CK	CKE	-Loop	number	mand	/CS	/RAS	/CAS	/WE	ODT	BA*3	-Am	A10	-A9	-A6	-A2	Data*2
		0	0	REF	0	0	0	1	0	0	0	0	0	0	0	_
			1, 2	D	1	0	0	0	0	0	0	0	0	0	0	_
			3,4	/D, /D	1	1	1	1	0	0	0	0	0	F	0	_
I			5 to 8	Repeat	cycles	14, b	ut BA=	1								
Toggling Static			9 to 12	Repeat	cycles	14, b	ut BA=	2								
ķ		1	13 to 16	Repeat	cycles	14, t	out BA=	3								
ji Si			17 to 20	Repeat	cycles	14, b	ut BA=	4								
) Ogo			21 to 24	Repeat	cycles	14, b	ut BA=	5								
_			25 to 28	Repeat	cycles	14, b	ut BA=	6								
			29 to 32	Repeat	cycles	14, b	ut BA=	7								
	•	2	33 to nRFC - 1	Repeat	Sub-L	oop 1, ι	until nR	FC - 1.	Trunca	ite, if n	ecessa	ıry				

Notes: 1. $\,$ DM must be driven low all the time. DQS, /DQS are FLOATING.

- DQ signals are FLOATING.
 BA: BA0 to BA2.
- 4. Am: m means Most Significant Bit (MSB) of Row address



Table 14: IDD6, IDD6ET and IDD8 Measurement-Loop Pattern

External Clock	Name	СК	CKE	RC RA	AS RCD	RRD	CL	AL/	cs	Comm and	A0- Am	ВА	SRT	ASR	ODT	DQ, DQS	Burst length	Active banks	ldle banks	Data
/CK	IDD6: Self Refresh Current Normal Temperature Range 0°C to +85°C	N/A	0		N/	'A				Midlev	/el		Disabled (normal)	Disabled	Acted, Midlev el	Acted	N/A	None	All	Midlevel I
Off, CK and /CK	IDD6ET: Self Refresh Current Extended Temperature Range 0°C to +105°C	N/A	0		N/	'A				Midlev	/el		Enabled (extended)	Disabled	Acted, Midlev el	Acted	N/A	None	All	Midlevel I
Midlevel	IDD8: Reset	N/A	Midle vel		N/	'A				Midle	/el		N/A	N/A	Midleve I	Midle vel	N/A	None	All	Midlevel I

Notes: 1. "Acted, midlevel" means the MR command is enabled, but the signal is midlevel.



^{2.} During a cold boot RESET (initialization), current reading is valid after power is stable and RESET has been LOW for 1ms; During a warm boot RESET (while operating), current reading is valid after RESET has been LOW for 200ns + tRFC.

Table 15: IDD7 Measurement-Loop Pattern

CKE	Sub -Loop	Cycle number	Com- mand	/cs	/RAS	/CAS	/WE	ODT	BA*3	A11 -Am	A10	A7 -A9	A3 -A6	A0 -A2	Data*2
		0	ACT	0	0	1	1	0	0	0	0	0	0	0	_
	0	1	RDA	0	1	0	1	0	0	0	1	0	0	0	00000000
	0	2	D	1	0	0	0	0	0	0	0	0	0	0	_
			Repeat	above [O Comn	nand ur	ntil nRl	RD – 1							
		nRRD	ACT	0	0	1	1	0	1	0	0	0	F	0	_
		nRRD + 1	RDA	0	1	0	1	0	1	0	1	0	F	0	00110011
	1	nRRD + 2	D	1	0	0	0	0	1	0	0	0	F	0	_
			Repeat	above [O Comn	nand ur	ntil 2 x	nRRD	- 1						
- 5	2	2 x RRD	Repeat	Sub-Lo	op 0, bu	ıt BA= 2	2								
•	3	3 x RRD	Repeat	Sub-Lo	op 1, bu	ıt BA= 3	3								
•			D	1	0	0	0	0	3	0	0	0	F	0	_
	4	4 x nRRD	Assert a	nd rene									-		
-	5	nFAW	Repeat						/	-,,		Jul. 7			
	<u> </u>	nFAW +	riopout	000 20	op 0, 50		•								
	6	nRRD	Repeat	Sub-Lo	op 1, bu	ut BA=	5								
	7	nFAW + 2 x nRRD	Repeat	Sub-Lo	op 0, bu	ut BA= 6	6								
_	8	nFAW + 3 x nRRD	Repeat	Sub-Lo	op 1, bı	ut BA= 7	7								
	•	nFAW + 4 x	D	1	0	0	0	0	7	0	0	0	F	0	_
_	9	nRRD	Assert a	and repe	eat abov	ve D Co	mmar	nd until	2 x nF	4W – 1	, if ne	cessa	ry		
atic F		2 x nFAW +	ACT	0	0	1	1	0	0	0	0	0	F	0	_
Toggling Static H	10	2 x nFAW +	RDA	0	1	0	1	0	0	0	1	0	F	0	0011001
ilg		2 x nFAW +	D	1	0	0	0	0	0	0	0	0	F	0	_
õ		2	Repeat	above [) Comn	nand ur	ntil 2 x	nFAW	+ nRRI) ₋ 1					
•		2 5 [1 1 1 1		400101	0011111	ilaila ai	1011 <u>-</u> X	,							
		2 x nFAW + nRRD	ACT	0	0	1	1	0	1	0	0	0	0	0	_
	11	2 x nFAW + nRRD + 1	RDA	0	1	0	1	0	1	0	1	0	0	0	00000000
		2 x nFAW +	D	1	0	0	0	0	1	0	0	0	0	0	_
		nRRD + 2	Repeat	above [O Comn	nand ur	ntil 2 x	nFAW	+ 2 x n	RRD –	1				
•	12	2 x nFAW + 2 x nRRD	Repeat	Sub-Lo	op 10, k	out BA=	: 2								
-	13	2 x nFAW + 3 x nRRD	Repeat	Sub-Lo	op 11, k	out BA=	: 3								
•		2 x nFAW +	D	1	0	0	0	0	3	0	0	0	0	0	_
	14	4 x nRRD	Assert a	and repe	at abov	ve D Co	mmar	nd until	3 x nF	AW – 1	I, if ne	cessa	ry		
-	15	3 x nFAW	Repeat	Sub-Lo	op 10. k	out BA=	: 4								
-	16	3 x nFAW + nRRD	Repeat												
-	17	3 x nFAW + 2 + nRRD	Repeat	Sub-Lo	op 10, k	out BA=	: 6								
-	18	3 x nFAW + 3 + nRRD	Repeat	Sub-Lo	op 11, k	out BA=	: 7								
-		3 x nFAW +	D	1	0	0	0	0	7	0	0	0	0	0	_
	19	4 + nRRD	Assert a												

Notes: 1. DM must be driven low all the time. DQS, /DQS are used according to read commands, otherwise FLOATING.



^{2.} Burst sequence driven on each DQ signal by read command. Outside burst operation, DQ signals are FLOATING.

^{3.} BA: BA0 to BA2.

^{4.} Am: m means Most Significant Bit (MSB) of Row address

2. Electrical Specifications

2.1 DC Characteristics

Table 16: DC Characteristics 1 (VDD, VDDQ = 1.283V to 1.45V)

Parameter	Symbol	Data rate (Mbps)	x8(max)	x16(max)	unit	Notes
Operating current (ACT-PRE)		1333	43	46		
	IDDO	1600	45	47	A	
	IDD0	1866	47	49	mA	
		2133	49	51		
		1333	57	65		
Operating current	1004	1600	59	67		
(ACT-RD-PRE)	IDD1	1866	62	70	mA	
,		2133	65	73		
		1333	7	11		
		1600	7	11		
	IDD2P0	1866	7	11	mA	SlowPD Exit
Precharge power-down		2133	7	11		
standby current	-	1333	10	14		
Starioty Sarroin		1600	12	14		
	IDD2P1	1866	14	14	mA	FastPD Exit
		2133	16	14		
			20	22		
		1333 1600	20 22	22		
Precharge standby current	IDD2N		22 24		mA	
		1866		22		
		2133	26	22		
D		1333	24	34		
Precharge standby	IDD2NT	1600	26	35	mA	
ODT current	1002111	1866	28	37		
		2133	30	39		
	IDD2Q	1333	20	21	mA	
Precharge quiet standby		1600	22	21		
current		1866	24	21		
		2133	26	21		
		1333	22	21	mA	
Active power-down current	IDD3P	1600	24	21		
(Always fast exit)		1866	26	21		
		2133	28	21		
	IDD3N	1333	26	34		
A stive standby surrent		1600	28	35	A	
Active standby current		1866	30	37	mA	
		2133	32	39		
		1333	133	110		
Operating current	100.10	1600	143	130		
(Burst read operating)	IDD4R	1866	153	150	mA	
(1 11 111 1 1 1 1 1 3)		2133	163	170		
		1333	133	122		
Operating current		1600	143	141		
(Burst write operating)	IDD4W	1866	153	159	mA	
(Barst write operating)		2133	163	176		
		1333	226	151		
Burst refresh current		1600	233	152		
	IDD5B	1866	240	153	mA	
		2133	247	154		
All book intolloons and				174		
		1333	168			
All bank interleave read	IDD7	1600	178	197	mA	
current		1866	188	221		
		2133	198	246		
		1333		10		
RESET low current	IDD8	1600	IDD2P+2	10	mA	
		1866	·-	10		
		2133		10		



Table 17: Self-Refresh Current (VDD, VDDQ = 1.283V to 1.45V)

Parameter	Symbol	x8(max)	x16(max)	unit	Notes
Self-refresh current normal temperature range	IDD6	10	11	mA	Max
Self-refresh current extended temperature range	IDD6ET	14	12	mA	Max@105'C



2.2 Pin Capacitance

Table 18: Pin Capacitance [DDR3L-1333 to 2133] (Operating Temperature = 25°C, VDD, VDDQ = 1.283V to 1.45V)

	_	DDR3L-1333		DDR3	DDR3L-1600		DDR3L-1866		DDR3L-2133		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
Input/output	CIO	1.4	2.4	1.4	2.3	1.4	2.2	1.4	2.1	pF	1,2
Input capacitance, CK and /CK	CCK	0.8	1.4	0.8	1.4	0.8	1.3	0.8	1.3	pF	2
Input capacitance delta, CK and /CK	CDCK	0	0.15	0	0.15	0	0.15	0	0.15	pF	2, 3
Input/output capacitance delta, DQS and /DQS	CDDQS	0	0.15	0	0.15	0	0.15	0	0.15	pF	2, 4
Input capacitance, (control, address, command, input-only pins)	CI	0.75	1.3	0.75	1.3	0.75	1.2	0.75	1.2	pF	2, 5
Input capacitance delta, (All control input-only pins)	CDI_CTRL	-0.4	0.2	-0.4	0.2	-0.4	0.2	-0.4	0.2	pF	2, 6, 7
Input capacitance delta, (All address/command input-only pins)	CDI_ADD_ CMD	-0.4	0.4	-0.4	0.4	-0.4	0.4	-0.4	0.4	pF	2, 8, 9
Input/output capacitance delta, DQ,DM, DQS, /DQS, TDQS, /TDQS	CDIO	-0.5	0.3	-0.5	0.3	-0.5	0.3	-0.5	0.3	pF	2, 10
Input/output capacitance of ZQ pin	CZQ	_	3	-	3	-	3	-	3	pF	2, 11

Notes: 1. Although the DM, TDQS and /TDQS pins have different functions, the loading matches DQ and DQS.



^{2.} VDD, VDDQ, VSS, VSSQ applied and all other pins floating (except the pin under test, CKE, /RESET and ODT as necessary). VDD = VDDQ = 1.5V, VBIAS=VDD/2 and on-die termination off.

^{3.} Absolute value of CCK-C/CK.

^{4.} Absolute value of CIO(DQS)-CIO(/DQS).

^{5.} CI applies to ODT, /CS, CKE, A0-A14, BA0-BA2, /RAS, /CAS and /WE.

^{6.} CDI_CTRL applies to ODT, /CS and CKE.

^{7.} $CDI_CTRL = CI(CTRL) - 0.5 \times (CI(CLK) + CI(/CLK))$.

^{8.} CDI_ADD_CMD applies to A0-A15, BA0-BA2, /RAS, /CAS and /WE.

^{9.} $\mathsf{CDI_ADD_CMD} = \mathsf{CI}(\mathsf{ADD_CMD}) - 0.5 \times (\mathsf{CI}(\mathsf{CLK}) + \mathsf{CI}(/\mathsf{CLK})).$

^{10.} $CDIO=CIO(DQ,DM) - 0.5 \times (CIO(DQS)+CIO(/DQS))$.

^{11.} Maximum external load capacitance on ZQ pin: 5pF.

2.3 Standard SpeedBins

Table 19: DDR3L-1333 Speed Bins

Speed Bin		DDR3L-1333			
CL-tRCD-tRP		9-9-9			
Symbol	/CAS write latency	min	max	Unit	Notes
tAA		13.5	20	ns	10
		(13.125)		115	
tRCD		13.5		ns	10
INCD		(13.125)		115	10
tRP		13.5		ns	10
IIXF		(13.125)		115	10
tRC		49.5		ne	10
IRC		(49.125)	_	ns	10
tRAS		36	9 x tREFI	ns	5
+C(() @ C _ F	CWL=5	3.0	3.3	ns	1, 2, 3, 4, 5, 9
tCK(avg)@CL=5	CWL=6, 7,	Reserved	Reserved	ns	4
	CWL=5	2.5	3.3	ns	1, 2, 3, 5
tCK(avg)@CL=6	CWL=6	Reserved	Reserved	ns	1, 2, 3, 4, 5
	CWL=7,	Reserved	Reserved	ns	4
	CWL=5	Reserved	Reserved	ns	4
tCK(avg)@CL=7	CWL=6	1.875	< 2.5	ns	1, 2, 3, 4, 5
	CWL=7	Reserved	Reserved	ns	1, 2, 3, 4, 5
	CWL=5	Reserved	Reserved	ns	4
tCK(avg)@CL=8	CWL=6	1.875	<2.5	ns	1, 2, 3, 5
	CWL=7	Reserved	Reserved	ns	1, 2, 3, 4, 5
tCK(ava)@CL 0	CWL=5, 6	Reserved	Reserved	ns	4
tCK(avg)@CL=9	CWL=7	1.5	<1.875	ns	1, 2, 3, 4, 5
+CI/(=::=) @ CI	CWL=5, 6	Reserved	Reserved	ns	4
tCK(avg)@CL=10	CWL=7	1.5	<1.875	ns	1, 2, 3, 5
Supported CL settings			5, 6, (7), 8, 9, (10)	nCK	
Supported CWL settings	3		5, 6, 7	nCK	



Table 20: DDR3L-1600 Speed Bins

Speed Bin		DDR3L-1600			
CL-tRCD-tRP	_	11-11-11			
Symbol	/CAS write latency	min	max	Unit	Notes
tAA		13.75	-20	ns	11
LAA		(13.125)	20		11
tRCD		13.75		20	11
IKCD		(13.125)	_	ns	11
tRP		13.75			4.4
IRP		(13.125)	_	ns	11
4D.C		48.75			4.4
tRC		(48.125)		ns	11
tRAS		35	9 x tREFI	ns	9
+CV()@CL_F	CWL=5	3.0	3.3	ns	1, 2, 3, 4, 6, 9
tCK(avg)@CL=5	CWL=6, 7, 8	Reserved	Reserved	ns	4
	CWL=5	2.5	3.3	ns	1, 2, 3, 6
tCK(avg)@CL=6	CWL=6	Reserved	Reserved	ns	1, 2, 3, 4, 6
	CWL=7, 8	Reserved	Reserved	ns	4
	CWL=5	Reserved	Reserved	ns	4
+CI/() @ CI 7	CWL=6	1.875	< 2.5	ns	1, 2, 3, 4, 6
tCK(avg)@CL=7	CWL=7	Reserved	Reserved	ns	1, 2, 3, 4, 6
	CWL=8	Reserved	Reserved	ns	4
	CWL=5	Reserved	Reserved	ns	4
tCl(/aa)@Cl 0	CWL=6	1.875	<2.5	ns	1, 2, 3, 6
tCK(avg)@CL=8	CWL=7	Reserved	Reserved	ns	1, 2, 3, 4, 6
	CWL=8	Reserved	Reserved	ns	1, 2, 3, 4
	CWL=5, 6	Reserved	Reserved	ns	4
tCK(avg)@CL=9	CWL=7	1.5	<1.875	ns	1, 2, 3, 4, 6
	CWL=8	Reserved	Reserved	ns	1, 2, 3, 4
	CWL=5, 6	Reserved	Reserved	ns	4
tCK(avg)@CL=10	CWL=7	1.5	<1.875	ns	1, 2, 3, 6
	CWL=8	Reserved	Reserved	ns	1, 2, 3, 4
tCK(avg)@CL=11	CWL=5, 6, 7	Reserved	Reserved	ns	4
	CWL=8	1.25	<1.5	ns	1, 2, 3
Supported CL settings			5, 6, (7), 8, (9), 10, 11	nCK	
Supported CWL settings			5, 6, 7, 8	nCK	



Table 21: DDR3L-1866 Speed Bins

Speed Bin	DDR3L-1866
CL-tRCD-tRP	13-13-13

CL-tRCD-tRP	_	13-13-13			
Symbol	/CAS write latency	min	max	Unit	Notes
		13.91	00		
tAA		(13.125)	20	ns	
DOD		13.91			
RCD		(13.125)	-	ns	
:RP		13.91			
KP		(13.125)	_	ns	
RC		47.91		ne	
KC .		(47.125)	_	ns	
RAS		34	9 x tREFI	ns	
CK(avg)@CL=5	CWL=5	Reserved	Reserved	ns	1, 2, 3, 4, 7
on(avg)@CL=3	CWL=6, 7, 8, 9	Reserved	Reserved	ns	4,
	CWL=5	2.5	3.3	ns	1, 2, 3, 7
CK(avg)@CL=6	CWL=6	Reserved	Reserved	ns	1, 2, 3, 4, 7
	CWL=7, 8, 9	Reserved	Reserved	ns	4
	CWL=5	Reserved	Reserved	ns	4
CK(avg)@CL=7	CWL=6	1.875	< 2.5	ns	1, 2, 3, 4, 7
	CWL=7, 8, 9	Reserved	Reserved	ns	4
	CWL=5	Reserved	Reserved	ns	4
CI/() @ CI	CWL=6	1.875	< 2.5	ns	1, 2, 3, 7
CK(avg)@CL=8	CWL=7	Reserved	Reserved	ns	1, 2, 3, 4, 7
	CWL=8,9	Reserved	Reserved	ns	4
	CWL=5, 6	Reserved	Reserved	ns	4
	CWL=7	1.5	< 1.875	ns	1, 2, 3, 4, 7
CK(avg)@CL=9	CWL=8	Reserved	Reserved	ns	4
	CWL=9	Reserved	Reserved	ns	1, 2, 3, 4, 7
	CWL=5, 6	Reserved	Reserved	ns	4
CK(avg)@CL=10	CWL=7	1.5	< 1.875	ns	1, 2, 3, 7
	CWL=8	Reserved	Reserved	ns	1, 2, 3, 4, 7
	CWL=5, 6, 7	Reserved	Reserved	ns	4
tCK(avg)@CL=11	CWL=8	1.25	< 1.5	ns	1, 2, 3, 4, 7
	CWL=9	Reserved	Reserved	ns	1, 2, 3, 4
tCK(avg)@CL=12	CWL=5, 6, 7, 8	Reserved	Reserved	ns	4
	CWL=9	Reserved	Reserved	ns	1, 2, 3, 4
101/() @ 01 10	CWL=5, 6, 7, 8	Reserved	Reserved	ns	4
CK(avg)@CL=13	CWL=9	1.07	< 1.25	ns	1, 2, 3
Supported CL settings			6, (7), 8, (9), 10, (11), 13	nCK	
Supported CWL settings			5, 6, 7, 8, 9	nCK	



Table 22: DDR3L-2133 Speed Bins

DDR3L-2133 Speed Bin CL-tRCD-tRP 14-14-14 Symbol /CAS write latency min max Unit **Notes** tAA 13.09 20 ns tRCD 13.09 ns tRP 13.09 ns tRC 46.09 ns 9 x tREFI tRAS 33.0 ns tCK(avg)@CL=5 Reserved Reserved CWL=6,7, 8, 9,10 1, 2, 3, 4, 8 ns CWL=5 2.5 3.3 1, 2, 3, 8 tCK(avg)@CL=6 CWL=6 Reserved Reserved ns 1, 2, 3, 4, 8 CWL=7, 8, 9,10 Reserved Reserved ns 4 CWL=5 Reserved Reserved 4 ns CWL=6 1.875 < 2.5 1, 2, 3, 8 ns tCK(avg)@CL=7 Reserved CWL=7 Reserved ns 1, 2, 3, 4, 8 CWL=8, 9,10 Reserved Reserved ns 4 CWL=5 Reserved Reserved ns 4 CWL=6 1.875 < 2.5 1, 2, 3, 8 ns tCK(avg)@CL=8 CWL=7 Reserved Reserved 1, 2, 3, 4, 8 CWL=8, 9,10 Reserved Reserved ns Reserved Reserved CWL=5, 6 ns 4 < 1.875 1, 2, 3, 8 CWL=7 1.5 ns tCK(avg)@CL=9 CWL=8 Reserved Reserved 1, 2, 3, 4, 8 ns CWL=9,10 Reserved Reserved ns 4 CWL=5, 6 Reserved Reserved ns CWL=7 1.5 < 1.875 1, 2, 3, 8 tCK(avg)@CL=10 CWL=8, 9 Reserved Reserved 1, 2, 3, 4, 8 ns CWL=10 Reserved Reserved ns CWL=5, 6, 7 Reserved Reserved 4 ns CWL=8 1.25 < 1.5 ns 1, 2, 3, 8 tCK(avg)@CL=11 CWL=9 Reserved Reserved 1, 2, 3, 4, 8 ns CWL=10 Reserved Reserved ns 1, 2, 3, 4, 8 CWL=5, 6, 7, 8 Reserved Reserved 4 ns tCK(avg)@CL=12 CWL=9 Reserved Reserved ns 1, 2, 3, 4, 8 CWL=10 Reserved Reserved ns 1, 2, 3, 4 CWL=5, 6, 7, 8 Reserved Reserved ns tCK(avg)@CL=13 CWL=9 1.07 < 1.25 ns 1, 2, 3, 8 CWL=10 Reserved Reserved ns 1, 2, 3, 4 CWL=5, 6, 7, 8,9 Reserved Reserved ns 4 tCK(avg)@CL=14 CWL=10 0.938 < 1.07 1, 2, 3, 5 ns Supported CL settings 5, 6, 7, 8, 9, 10, 11, 12, 13, 14 nCK Supported CWL settings 5, 6, 7, 8, 9, 10 nCK



Electrical Characteristics & AC Timing for DDR3L-1600 to DDR3L-2133 (Cont'd) Standard Speed Bins (Cont'd)

- **NOTE 1.** The CL setting and CWL setting result in tCK(AVG).MIN and tCK(AVG).MAX requirements. When making a selection of tCK(AVG), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
- NOTE 2. tCK(AVG).MIN limits: Since CAS Latency is not purely analog data and strobe output are synchronized by the DLL all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(AVG) value (3.0, 2.5, 1.875, 1.5, 1.25, 1.07, or 0.938 ns) when calculating CL [nCK] = tAA [ns] / tCK(AVG) [ns], rounding up to the next 'Supported CL', where tCK(AVG) = 3.0 ns should only be used for CL = 5 calculation.
- NOTE 3. tCK(AVG).MAX limits: Calculate tCK(AVG) = tAA.MAX / CL SELECTED and round the resulting tCK(AVG) down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875 ns or 1.5 ns or 1.25 ns or 1.07 ns or 0.938 ns). This result is tCK(AVG).MAX corresponding to CL SELECTED.
- NOTE 4. 'Reserved' settings are not allowed. User must program a different value.
- **NOTE 5.** Any DDR3L-1333 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
- **NOTE 6.** Any DDR3L-1600 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
- **NOTE 7.** Any DDR3L-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
- **NOTE 8.** Any DDR3L-2133 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
- **NOTE 9.** For CL5 support, refer to DIMM SPD information. DRAM is required to support CL5. CL5 is not mandatory in SPD coding.
- NOTE 10. tREFI depends on operating commercial temperature and industrial temperature.
- **NOTE 11.** For devices supporting optional down binning to CL=11 and CL=9, tAA/tRCD/tRPmin must be 13.125ns. SPD setting must be programed to match.

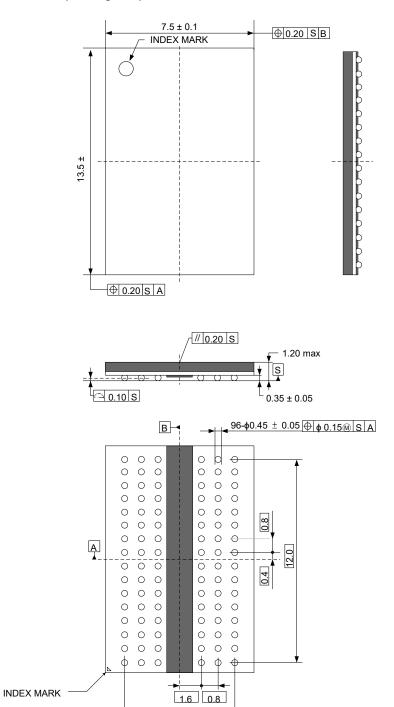


3. Package Drawing

3.1 96-ball FBGA

Solder ball: Lead free (Sn-Ag-Cu)

Unit: mm



6.4

NOTES FOR CMOS DEVICES

1 PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

(2) HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

(3) STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.



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- 3) Usage involving exposure to significant amounts of corrosive gas, including sea air, CL2, H2S, NH3, SO2, and NOx.
- 4) Usage in environments with static electricity, or strong electromagnetic waves or radiation.

5) Usage in places where dew forms.

6) Usage in environments with mechanical vibration, impact, or stress.

7) Usage near heating elements, igniters, or flammable items.

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