Automotive Three Phase Sinusoidal Fan Driver

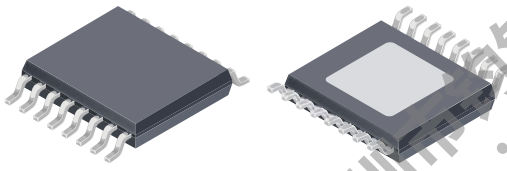
Features and Benefits

- Full 3-phase sinusoidal drive
- PWM speed input
- Analog speed input
- FG speed output
- Lock detection
- Current limiting
- Output short circuit protection
- Dynamic lead angle control

Applications:

- Automotive blower
- Air conditioning
- Air movement

Package: 16-pin TSSOP with Exposed Thermal Pad (suffix LP)



Not to scale

Description

The A4946 is a low noise, three phase motor driver with integrated power bridge suitable for driving small fans and blowers in automotive systems. Motor audible noise and vibration is reduced by driving the phases with sinusoidal PWM excitation. Motor current is controlled using PWM techniques to minimize the power dissipation.

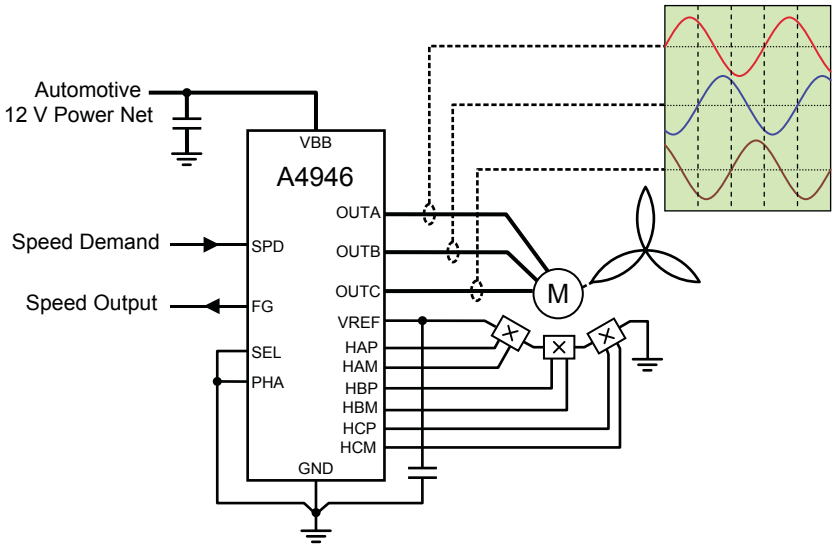
Rotor position is determined by Hall effect elements. These provide direct inputs to the integrated commutation and excitation logic.

In addition to speed control by varying the supply voltage, motor speed can be controlled using a variable duty cycle PWM input or a variable voltage analog input. This allows system cost savings by eliminating the requirement for an external variable power supply. Motor speed is indicated each full commutation cycle by a single digital output.

The A4946 incorporates motor lock detection, current limiting, supply overvoltage and undervoltage detection, short circuit protection, and overtemperature protection.

The A4946 is supplied in a 16-pin TSSOP power package with an exposed thermal pad (package type LP). This package is lead (Pb) free with 100% matte-tin lead frame plating.

Typical Application Diagram



Selection Guide

Part Number	Packing	Package
A4946GLPTR-T	1500 pieces per reel	4.4 mm x 5 mm, 1.2 mm nominal height 16-pin TSSOP with exposed thermal pad

Absolute Maximum Ratings with respect to GND

Characteristic	Symbol	Notes	Rating	Unit
Drive Supply Voltage	V_{BB}		–0.3 to 50	V
Pins SPD, SEL, PHA	–		–0.3 to 6	V
Pin FG	–		–0.3 to 6	V
Pins HAP, HAM, HBP, HBM, HCP, HCM	–		–0.3 to 6	V
Pin VREF	–		–0.3 to 6	V
Ambient Operating Temperature Range	T_A	Temperature Range G, limited by power dissipation	–40 to 105	°C
Maximum Continuous Junction Temperature	$T_{J(max)}$		150	°C
Storage Temperature Range	T_{stg}		–55 to 150	°C

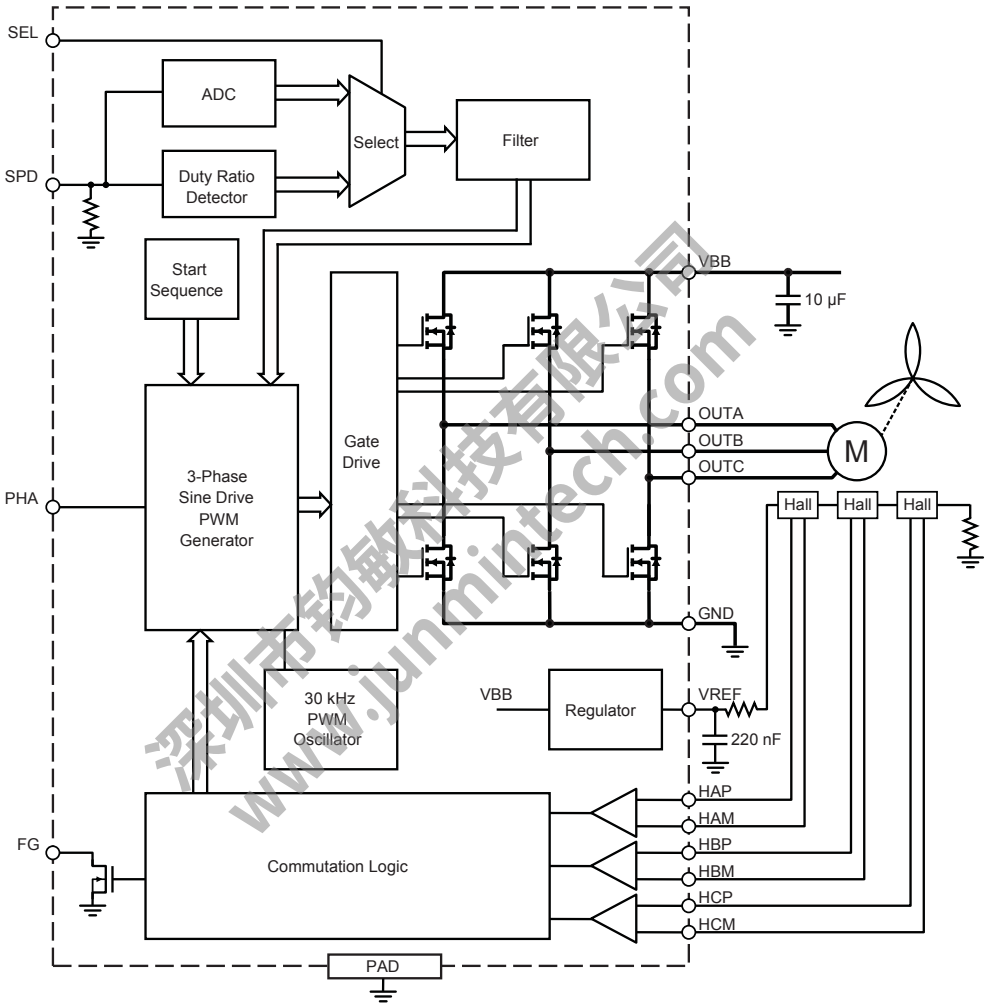
Thermal Characteristics may require derating at maximum conditions, see application information

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	On 4-layer PCB based on JEDEC standard	34	°C/W
		On 2-layer PCB with 3.8 in.^{2} of copper area each side	43	°C/W

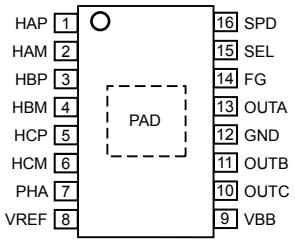
*Additional thermal information available on the Allegro website.

Table of Contents

Functional Block Diagram



Pin-out Diagram



Terminal List Table

Number	Name	Function
1	HAP	Hall element A input
2	HAM	Hall element A input
3	HBP	Hall element B input
4	HBM	Hall element B input
5	HCP	Hall element C Input
6	HCM	Hall element C input
7	PHA	Phase advance input
8	VREF	Analog reference voltage
9	VBB	Supply voltage
10	OUTC	Motor phase C output
11	OUTB	Motor phase B output
12	GND	Ground
13	OUTA	Motor phase A output
14	FG	Speed output
15	SEL	Speed control mode input
16	SPD	Speed demand input
–	PAD	Exposed thermal pad, connect to GND

ELECTRICAL CHARACTERISTICS Valid at T_J = –40°C to 150°C, V_{BB} = 6.5 to 28 V; unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Supplies						
Supply Voltage Range[1]	V_{BB}	Functional, no unsafe states	0	–	50	V
		Outputs Driving	4.8	–	V_{BBOV}	V
Supply Quiescent Current	I_{BBQ}		–	–	12	mA
Reference Output Voltage	V_{REF}	0 mA > I_{REF} > –30 mA	4.75	5	5.25	V
Reference Dropout Voltage	V_{REFDO}	V_{BB} = 4.8 V, I_{REF} = –20 mA	–	500	–	mV
Reference Current Limit	I_{REFLIM}		–	50	–	mA
Motor Bridge Output						
Total On-Resistance (High-Side Plus Low-Side)	$R_{DS(on)}$	V_{BB} = 12 V, T_J = 25°C	–	0.54	0.65	Ω
		V_{BB} = 12 V, T_J = 150°C	–	0.9	1.1	Ω
		V_{BB} = 7.0 V, T_J = 25°C	–	0.85	1	Ω
Output Sense Current[2]	I_{SENSE}	V_{OUT} = 0 V, outputs not driving	–35	–110	–185	µA
Current Control						
Dead Time	t_{DEAD}		–	400	–	ns
Motor PWM Frequency	f_{PWM}		28	30	32	kHz
Current Limit Threshold	I_{CL}	Per phase	1.35	1.63	1.91	A
Overcurrent Off-Time	t_{OFF}		–	24	–	µs
Motor Control						
Start Time	t_{ST}		–	1	–	s
Disable Time	t_{LD}		–	8	–	s
Commutation Period[3]	t_{COMM}		100	–	–	µs
Drive Mode Selection Period	t_{SINOK}	Sinusoidal mode selected when t_{COMM} < t_{SINOK}	33	52	58	ms
SPD Maximum Demand (100%)	$VSPD_{MAX}$	SEL = 0; V_{BB} ≥ 6.5 V and monotonic from 0 V to $VSPD_{MAX}$	4.15	4.25	4.35	V
SPD On Threshold (25%)	$VSPD_{ON}$	SEL = 0	1.02	1.12	1.22	V
SPD Off Threshold (12.5%)	$VSPD_{OFF}$	SEL = 0	480	580	680	mV
Duty Cycle On Threshold for SPD	D_{ON}	SEL = 1	23.75	25	26.25	%
Duty Cycle Off Threshold for SPD	D_{OFF}	SEL = 1	11.88	12.5	13.12	%
Internal Speed Demand Slew Rate	t_{RR}		–	15.33	–	ms/%FS
Logic Input and Output						
Input Low Voltage (PHA, SEL, SPD)	V_{IL}		–	–	0.8	V
Input High Voltage (PHA, SEL, SPD)	V_{IH}		2.0	–	–	V
Input Open Voltage Condition (PHA)	V_{IOpen}		47.4	–	52.6	%V_{REF}
Input Hysteresis (PHA, SEL, SPD)	V_{Ihys}		100	300	–	mV

Continued on the next page…

ELECTRICAL CHARACTERISTICS (continued) Valid at T_J = –40°C to 150°C, V_{BB} = 6.5 to 28 V; unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Logic Input and Output (continued)						
Input Pull-Down Resistor	R_{PD}	SEL pin	–	50	–	kΩ
		PHA, SPD pins	–	100	–	kΩ
Input Pull-Up Resistor (PHA)	R_{PU}		–	100	–	kΩ
Output Low Voltage (FG)	V_{OL}	I_{OL} = 2 mA	–	–	0.4	V
Output Leakage[2] (FG)	I_O	0 V < V_O < 5 V	–1	–	1	µA
Hall Element Input						
Hall Differential Input Drive Voltage	V_{HD}		±30	–	–	mV_{pk-pk}
Hall Input Common Mode Range	V_{HICMR}		1	–	4	V
Hall Input Offset Voltage	V_{HO}		–	±5	–	mV
Hall Input Hysteresis Voltage	V_{HDHys}		–	±13	–	mV
Diagnostics And Protection						
VBB Overvoltage Threshold	V_{BBOV}	V_{BB} rising	32	–	36	V
		V_{BB} falling	28	–	31	V
VBB Overvoltage Hysteresis	$V_{BBOVHys}$		–	3.5	–	V
VBB Undervoltage Threshold	V_{BBUV}	V_{BB} rising	3.6	–	4.1	V
		V_{BB} falling	3.35	3.55	3.7	V
VBB Undervoltage Hysteresis	V_{BBHys}		–	300	–	mV
VREF Undervoltage Threshold	V_{REFUV}	V_{REF} rising	3.5	–	4.0	V
		V_{REF} falling	3.25	3.45	3.6	V
VREF Undervoltage Hysteresis	V_{REFHys}		–	300	–	mV
Short Circuit Current Protection Thresholds[4]	V_{DS}		1.6	–	5.5	V
Overtemperature Shut Down	T_{JF}	Temperature increasing	155	170	–	ºC
Overtemperature Hysteresis	T_{Jhys}	Recovery = T_{JF} – T_{Jhys}	–	15	–	ºC

[1]The term “functional” indicates correct operation but parameters may not be within specification above or below the general limits (6.5 V < V_{BB} < 28 V), and outputs are not operational above V_{BBOV} or below V_{BBUV}.
[2]For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device pin.
[3]Parameter t_{COMM} = 1 / (6 × FG pin frequency) under steady motor speed conditions.
[4]Parameter V_{DS} = V_{OUTx} to GND or V_{BB} – V_{OUTx}.

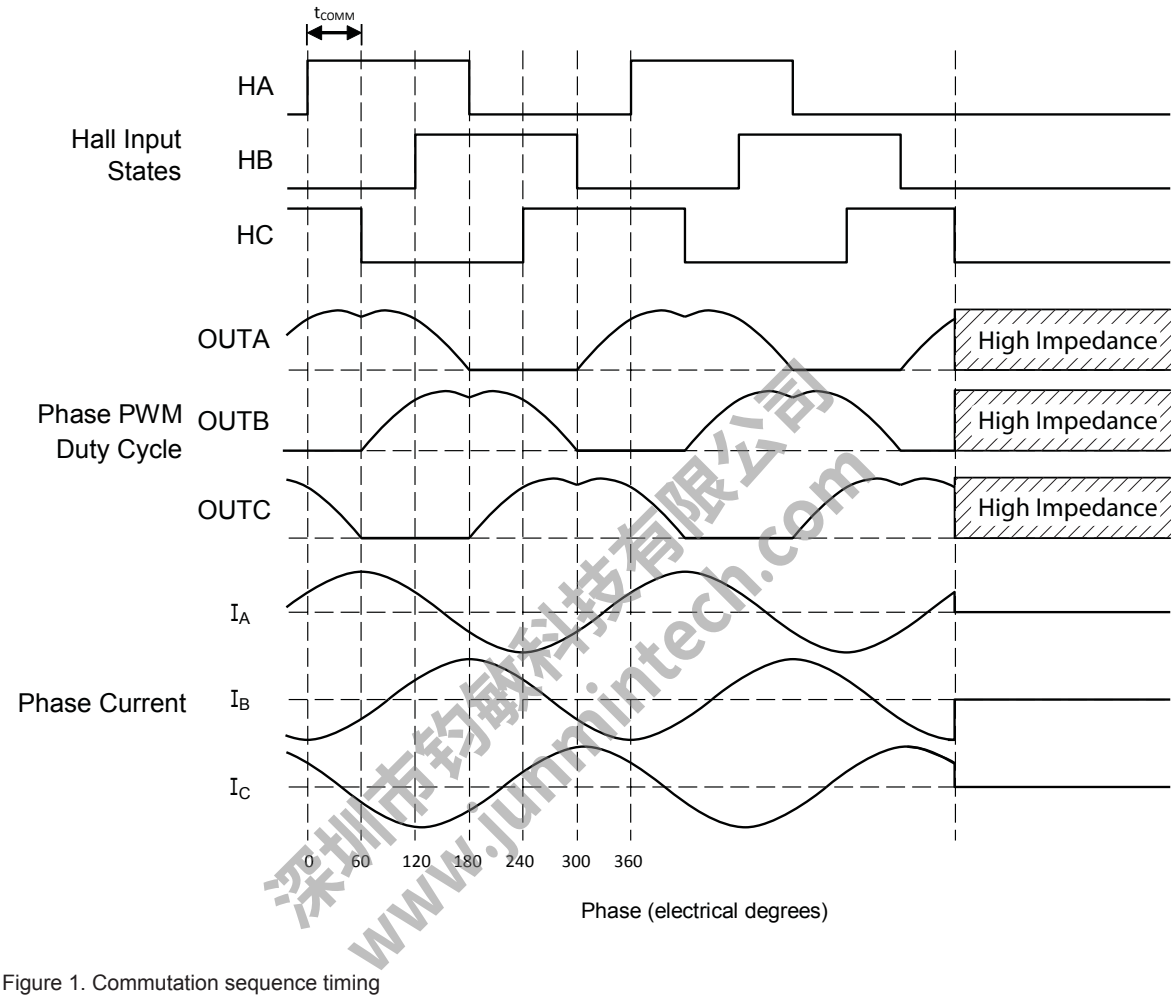


Figure 1. Commutation sequence timing

Table 1. Commutation State Table

Commutation Input State*			Output Mode					
			Trapezoidal Mode			Sinusoidal Mode		
HA	HB	HC	OUTA	OUTB	OUTC	OUTA	OUTB	OUTC
H	L	H	High	Low	Z	Sine PWM	Low	Sine PWM
H	L	L	High	Z	Low	Sine PWM	Sine PWM	Low
H	H	L	Z	High	Low	Sine PWM	Sine PWM	Low
L	H	L	Low	High	Z	Low	Sine PWM	Sine PWM
L	H	H	Low	Z	High	Low	Sine PWM	Sine PWM
L	L	H	Z	Low	High	Sine PWM	Low	Sine PWM
H	H	H	Z	Z	Z	Z	Z	Z
L	L	L	Z	Z	Z	Z	Z	Z

Note: Z = high impedance
*H = $V_{HxP} > V_{HxM}$, L = $V_{HxM} > V_{HxP}$

Table 2. Phase Advance Table

FG Output (Hz)	PHA Input State		
	Low (Electrical degrees)	High (Electrical degrees)	Open (Electrical degrees)
0	0	0	5.6
80	0	3.8	5.6
100	0	7.5	5.6
120	0	9.4	5.6
140	0	11.3	5.6
160	0	13.1	5.6
180	0	13.1	5.6
250	0	13.1	5.6
300	0	13.1	5.6
>300	0	13.1	5.6

Functional Description

The A4946 is a three phase motor driver with integrated power bridge suitable for driving small fans and blowers in automotive applications. Typically average continuous motor phase current up to 1.25 A is possible in ambient temperatures up to 80°C, depending on the thermal resistance of the assembly. Peak phase current up to 1.63 A (typ) is controlled by fixed off-time PWM current limiting.

Motor audible noise and vibration is reduced by driving the phases with three 120 degree spaced sinusoidal currents. The motor current is determined by variable duty cycle PWM switching of the three motor phase connections. The PWM duty cycle is generated automatically, depending on the rotor position and the demanded speed.

Rotor position is determined by Hall effect elements. These provide direct inputs to the integrated commutation and excitation logic.

In addition to speed control by varying the supply voltage, motor speed can be controlled using digital PWM or analog voltage inputs, allowing system cost savings by eliminating an external variable power supply. Motor speed is indicated each full electrical commutation cycle by a single digital output.

The A4946 incorporates motor lock detection, current limiting, supply overvoltage and undervoltage detection, overcurrent protection, and overtemperature protection.

Pin Functions

VBB Main motor supply and chip supply for internal regulators and charge pump. VBB should be decoupled to ground with a low ESR electrolytic capacitor greater than 10 µF, and a 100 nF (50 V) X7R ceramic capacitor in parallel.

VREF Regulated 5 V output for Hall element supply up to 30 mA. Also used for internal logic and analog supply. Should be decoupled to ground with a 220 nF (10 V minimum) X7R ceramic capacitor.

GND Supply return and analog reference ground.

HAP, HAM Hall element A inputs. Hall input A (HA) is defined as high when the voltage at HAP is greater than the voltage at HAM. Low is when HAM voltage is greater than HAP.

HBP, HBM Hall element B inputs. Hall input B (HB) is defined as high when the voltage at HBP is greater than the voltage at HBM. Low is when HBM voltage is greater than HBP.

HCP, HCM Hall element C inputs. Hall input C (HC) is defined as high when the voltage at HCP is greater than the voltage at HCM. Low is when HCM voltage is greater than HCP.

OUTA, OUTB, OUTC Motor phase connections.

FG Speed output indicator provides a logical output equivalent of the Hall A (HA) status, one period per electrical revolution of the motor.

SEL Selects analog (voltage) or digital (PWM duty cycle) input for the SPD pin.

SPD Speed demand input. Analog voltage input or digital PWM duty cycle input selected by the SEL input.

PHA Phase advance logical input. When high, or open, phase advance is enabled. When low, phase advance is disabled.

Operation

The three sinusoidal phase currents in the motor phase windings are generated, using variable duty cycle PWM, by a three-phase MOSFET power bridge. A three phase sine drive PWM generator provides the controlling inputs to the power bridge based on rotor position derived from Hall element inputs and a speed demand input. The PWM duty cycle modulation relative to the Hall signals is shown in figure 1.

The first three waveforms, HA, HB, and HC, in figure 1 show the Hall sequence derived from 120° (electrical) spaced Hall elements. The A4946 incorporates sensitive comparators with a large common mode capability, allowing the Hall elements to be connected in series or in parallel. The Hall inputs provide the commutation points to the sine drive generator. This produces the continuously varying duty cycle for each phase, based on the timing between the commutation points as shown in waveforms OUTA, OUTB, and OUTC in figure 1. Note that figure 1 shows the internal duty cycle value applied to the PWM generator in each phase, not the voltage waveform at the phase output.

The three sine wave phase currents, I_A, I_B, and I_C, resulting from the three phase PWM outputs are shown in the bottom three waveforms in figure 1.

Speed Control

The speed demand input modulates the range of the three PWM duty cycles to directly control the effective average voltage applied to the motor windings and therefore the current in the motor windings. The speed demand applied to the internal PWM generator is a digital value derived from the speed demand input pin, SPD. This input can be a variable duty cycle PWM signal with a frequency of typically 20 kHz, or a linear voltage input depending on the state of the SEL input.

When SEL is low, a voltage can be applied to the SPD input. This voltage is converted to a digital value by an internal 9-bit A-to-D converter, and then is used as the internal speed demand value. The input voltage range is from 0 V to typically 4.25 V. However when the input is less than 0.5 V, the motor speed demand will be zero. Between 1 and 4.3 V, the motor speed demand increases linearly from 25% to 100%. The relationship between the voltage on SPD, V_{SPD}, and the motor speed demand is shown in figure 2. The 0.5 V of hysteresis related to the start and stop response of the motor can also be seen in figure 2.

When SEL is high, a variable duty cycle digital signal can be applied to the SPD input. This signal should be at a frequency of typically 20 kHz. The signal timing is used to convert the input duty cycle to a 9-bit digital value, which is used as the motor speed demand value. The input duty cycle range is 0% to 100%. However, when the input duty cycle is less than 12.5%, the motor speed demand will be zero. Between 25% and 100% the motor speed demand increases linearly from 25% to 100%.

The relationship between the duty cycle of the PWM signal on the SPD pin, DCSPD, and the motor speed demand is shown in figure 2. The 12.5% of hysteresis related to the start and stop response of the motor is also be shown in figure 2.

Operation During Start

Note: Parameters used in the following descriptions are listed in the Motor Control section of the Electrical Characteristics table.

As the motor turns, it produces commutation codes that generate a speed related signal, t_{COMM}, which is used by the internal controller of the A4946 to detect two conditions:

- Locked rotor
- The transition from trapezoidal drive mode to sinusoidal drive mode

The relationship between t_{COMM} and the rotational speed of a motor measured at the FG pin is shown in figure 3. The curve is based on electrical cycles of the motor commutation system and

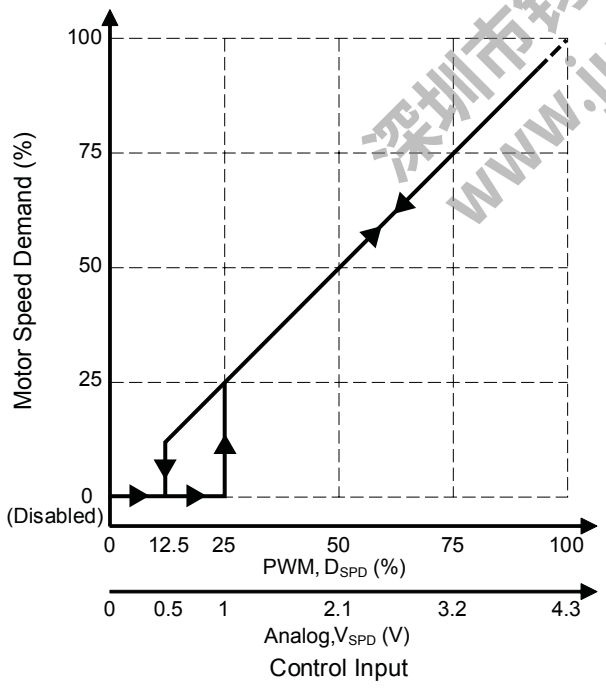


Figure 2. Control input mapping to speed demand

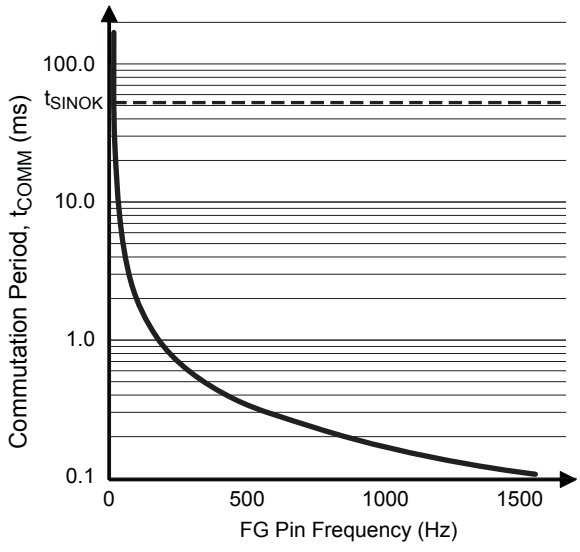


Figure 3. Relationship between t_{COMM} and FG frequency

this relationship will remain constant irrespective of the number of pole pairs the motor has. The number of poles will modify the relationship between the frequency measured on the FG pin and the actual mechanical rotational speed, in rpm, of the motor.

Figure 4 illustrates the conditions during a full start time period, t_{ST}, if the motor rotor is locked while driving a very high friction or inertia mechanical load. All these conditions will prevent the value of t_{COMM} reducing to a value less than the t_{SINOK} period before t_{ST} times out. After t_{ST} has timed out, the drive to the motor will be turned off for approximately 8 s, the t_{LD} period.

It can be seen in figure 4 that a start condition is commanded immediately when the control setting on the SPD pin exceeds the 25% level. If the initial condition on the SPD pin is less than 25% there will be a time delay, based on initial conditions, before a start is commanded (discussed in the Soft Start section).

During the start condition, trapezoidal drive mode is selected, also speed demand and motor current are controlled internally by the A4946. To aid starting the motor, current is incremented in steps every 50 ms in an attempt to increase the torque in the motor and increase rotational speed, thereby reducing the value of t_{COMM}.

Transition to Sinusoidal Operating Mode

Figure 5 shows a successful transition to sinusoidal mode. Here the starting condition is the same as in figure 4, but now the motor reaches a higher speed during the t_{ST} period and the value of t_{COMM} reduces to values less than the t_{SINOK} threshold . This results in sinusoidal drive mode being selected at the next commutation point.

After sinusoidal drive mode is commanded, the internal current limit is raised to I_{CL} and the internal speed demand is lowered to 25%. Then controlled by the soft start feature in the A4946, the speed demand will increase during the period t_{SS}, to the external speed demand setting set on the SPD pin.

Soft Start

A soft start function is integrated into the 4946. This is achieved by limiting the internal speed response slew rate to a maximum value, t_{RR}, to slow the rate of change of PWM duty cycle delivered to the motor phases.

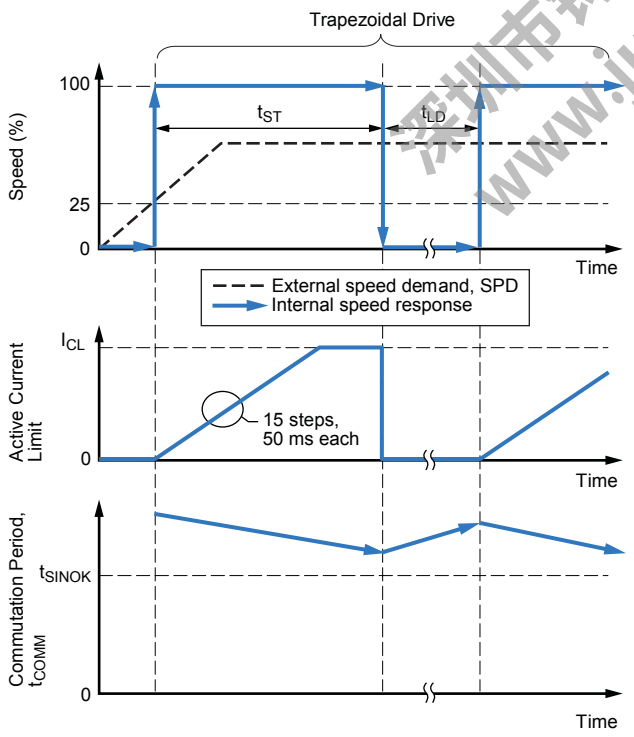


Figure 4. Locked rotor case; no transition to sinusoidal mode

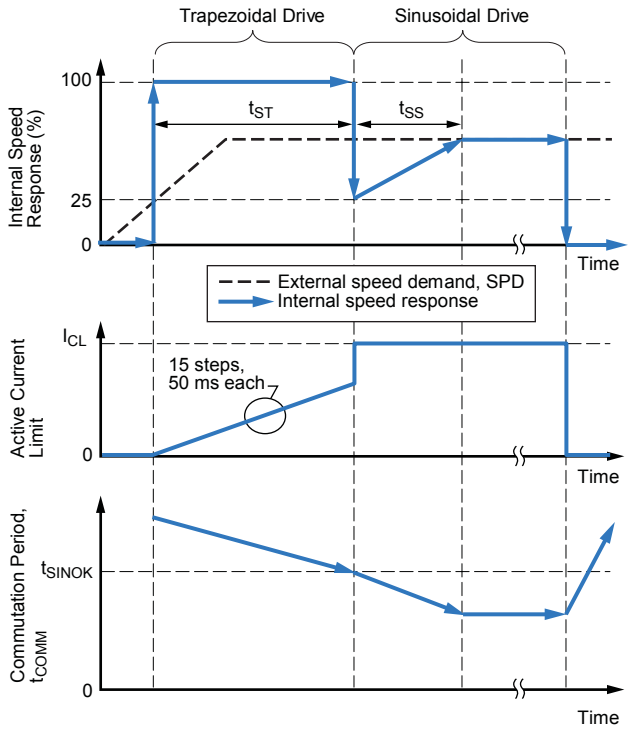


Figure 5. Successful start and transition to sinusoidal mode

This results in limiting the acceleration or deceleration of the motor between two speed demand levels input on the SPD pin. The end effect is to lower the average current demand from the power supply.

The speed change time, t_{SS}, is defined by:

$$|t_{SS}| = (SPD1 - SPD2) \times t_{RR},$$

where SPDn is the setting on the SPD pin, in % of full scale. This is the time it takes the internally generated PWM duty cycle to change between demand settings, SPD1 and SPD2, input on the SPD pin.

Applying the above equation, the maximum value of t_{SS} in sinusoidal mode would be when SPD1 = 12.5% and SPD2 = 100%:

$$t_{SS} = 87.5\ (\%) \times 15.33\ (ms) = 1.345\ s,$$

and the maximum time to a motor start command would be when SPD1 = 0% and SPD2 = 25%:

$$t_{SS} = 25\ (\%) \times 15.33\ (ms) = 383\ ms.$$

The exception is when the signal on SPD is rapidly reduced to zero. This will cause all three drivers to enter the high impedance condition shown in table 1 immediately. This action is not modified by the state on the SEL pin. The end result is all three half bridges turn off and the motor will coast to a halt.

Lock Detect

Rotor lock is a functional state where the motor is turning too slowly to change from trapezoidal to sinusoidal mode. It can occur during two conditions. The first is during initial motor start up and the second is when the motor is running in sinusoidal mode and is forced to slow down by an external force.

Motor speed is continuously sensed by measuring the time between consecutive motor commutation points, and the value is stored as the parameter t_{COMM}. The relationship between t_{COMM} and the frequency available in the FG pin is shown in figure 3.

At the end of the start-up time, t_{ST}, if the value of t_{COMM} is greater than the drive mode selection parameter, t_{SINOK}, all phases will be disabled for a disable period, t_{LD}. An attempt to restart the motor is made when t_{LD} times out. The typical values of t_{ST} and t_{LD} are 1 s and 8 s respectively. Restart attempts based on these times will continue while the speed demand setting on the SPD pin is greater than 12.5%.

If the motor is running in sinusoidal mode when an external force causes it to slow down to a speed where t_{COMM} is greater than t_{SINOK}, the A4946 will initiate a full start up sequence as shown in figure 4. If the force slowing the motor is no longer present, the motor will successfully re-start and switch to sinuisoidal mode as shown in figure 5. If the force is still present, then the start sequence described in figure 4 will result.

Current Limit

Load current on each active output is continuously monitored on the high-side sourcing MOSFET in each half bridge. If the current exceeds I_{CL}, the source driver is turned off for 24 µs. During this fixed off time, the driver operates in slow decay, synchronous rectification, mode.

During start up in trapezoidal mode, the value of I_{CL} is ramped from zero to aid starting and protect the outputs when the motor is locked. In sinusoidal mode the value of I_{CL} is fixed. See figures 4 and 5 for more information.

Output Short Circuit Protection

The output short circuit protection feature operates to protect the A4946 if the current through any OUTx pin causes the source to drain voltage, V_{DS}, across active MOSFETs to exceed safe values. This could be the result of a short to ground, STG, a short to battery, STB, or a shorted load, STL, condition being detected. If any of these conditions occur, the A4946 disables the drives to all three OUTx pins and coasts the motor.

To reset the driver and attempt to restart the motor, the speed demand setting on the SPD pin must be reduced to a value less than 12.5%, and then increased to greater than 25% to initiate an attempt to start the motor. If the STx condition is still present the coast condition will be commanded again.

Phase Advance

To improve motor efficiency, the A4946 includes a dynamic phase advance feature. The advance is based on electrical cycle degrees and is enabled by setting PHA input to high or to open (table 2).

As speed increases, the phase excitation sequence advances ahead of the commutation sequence (shown in figure 1) by the values at each speed threshold in table 2. Rapid switching between advance values due to speed jitter is prevented by a hysteresis of about 10 Hz. When PHA is low, no phase advance is introduced.

Application Information

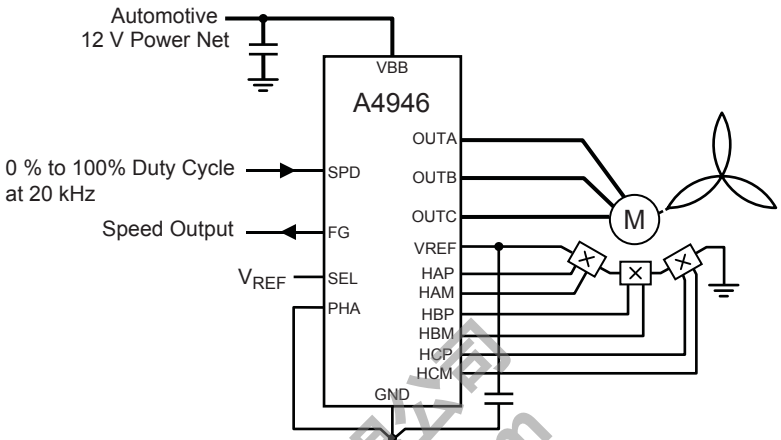


Figure 6. Digital PWM speed control

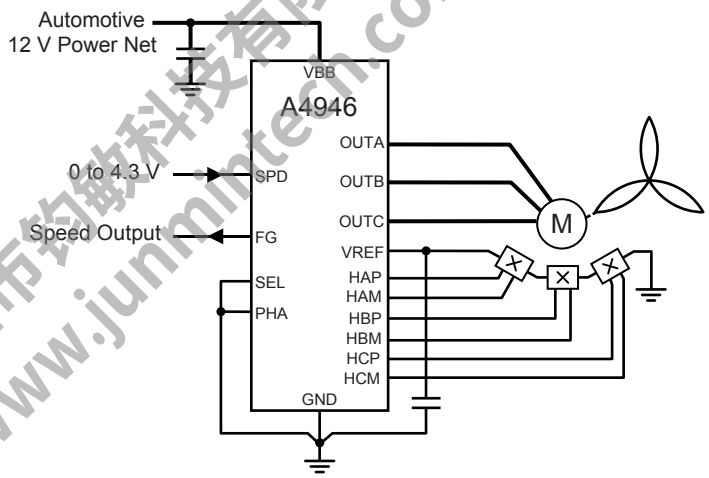


Figure 7. Analog voltage speed control

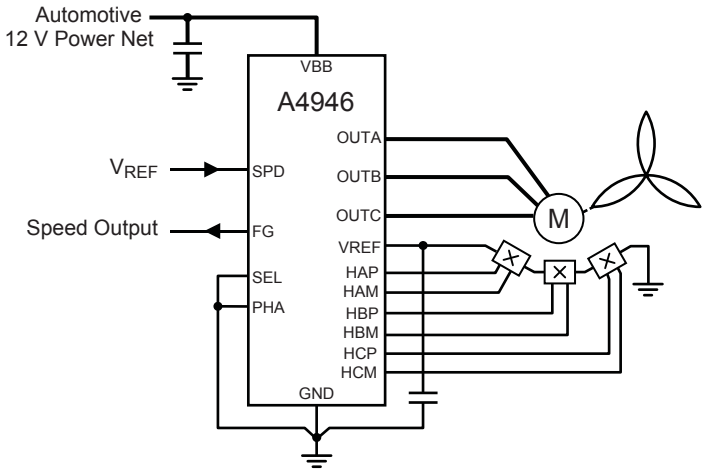
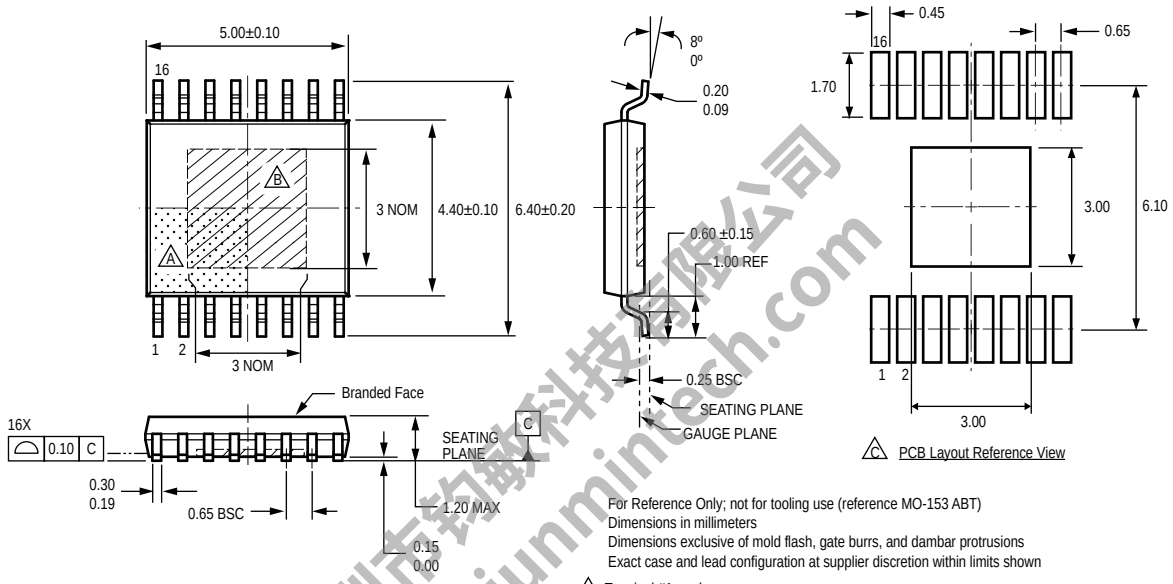


Figure 8. VBB voltage mode speed control

Package LP, 16-Pin TSSOP
With Exposed Thermal Pad



For Reference Only; not for tooling use (reference MO-153 ABT)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (bottom surface); dimensions may vary with device

C Reference land pattern layout (reference IPC7351 SOP65P640X110-17M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

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