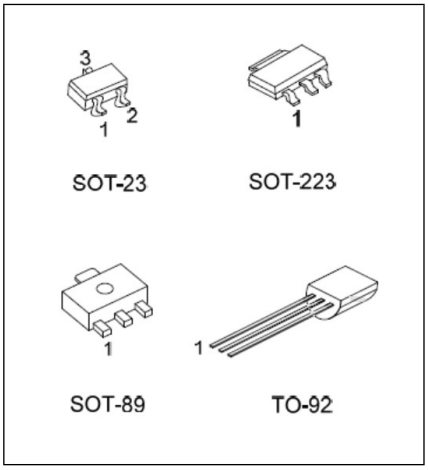
BT131

FEATURES

- Direct interfacing to logic level ICs
- Direct interfacing to low power gate drive circuits and microcontrollers
- High blocking voltage capability
- Planar passivated for voltage ruggedness and reliability
- Triggering in all four quadrants
- Very sensitive gate

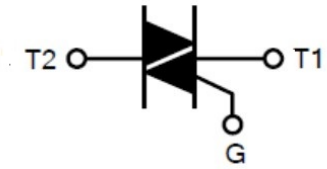


APPLICATIONS

- General purpose bi-directional switching and phase control application.
- Air conditioner indoor fan control
- General purpose motor control
- General purpose switching

Package	Pin assignment		
	1	2	3
TO-92	T1	G	T2
SOT-223	T1	T2	G
SOT-89	T1	T2	G
SOT-23	T1	G	T2

SYMBOL:



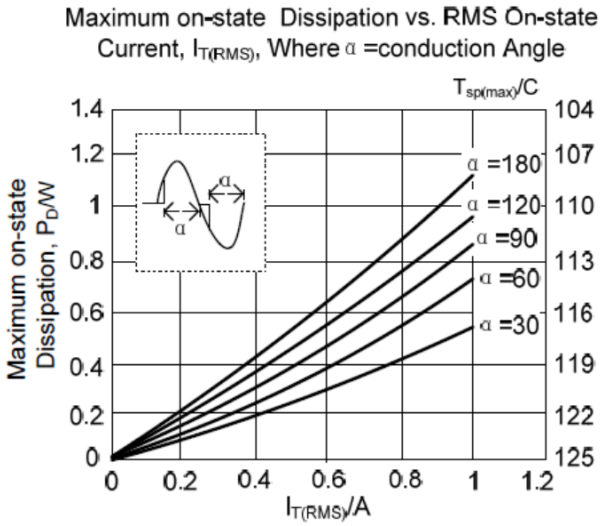
ABSOLUTE MAXIMUM RATINGS

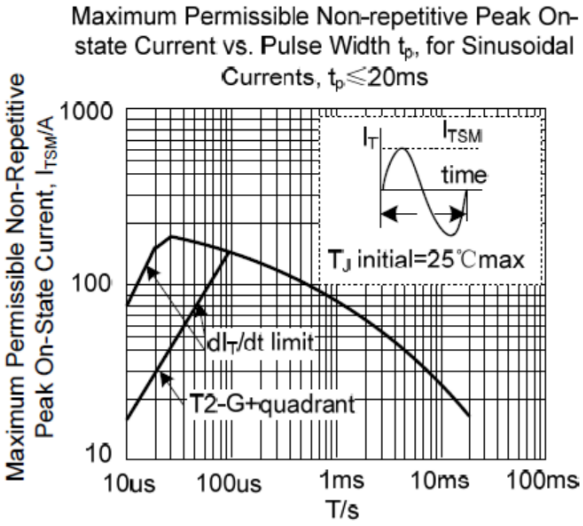
PARAMETER	SYMBOL	VALUE		UNIT
Repetitive Peak Off-State Voltages	V_{DRM}, V_{RRM}	600		V
RMS on-State Current	$I_{T(RMS)}$	1		A
Non-Repetitive Peak On-State Current	I_{TSM}	16		A
I^2t for fusing	I^2t	1.28		A^2s
Repetitive rate of rise of on-state current after triggering	dIT/dt	I	50	A/uS
		II	50	
		III	50	
		IV	10	
Peak gate current	I_{GM}	2		A
Peak Gate Voltage	V_{GM}	5		V
Peak Gate Power	P_{GM}	5		W
Average Gate Power	$P_{G(AV)}$	0.5		W
Operating junction temperature	T_J	+125		℃
Storage Temperature	T_{STG}	-40 ~ +150		℃

ELECTRICAL CHARACTERISTICS (TJ=25°C)

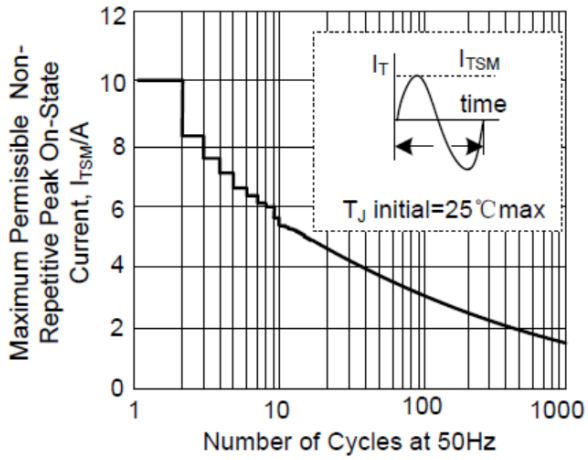
PARAMETER	SYMBOL	TEST CONDITIONS		MIN	MAX	UNITS
Peak Repetitive Forward or Reverse Blocking Current	I_{DRM} I_{RRM}	V_{AK} = Rated V_{DRM} or V_{RRM};			0.5	mA
Gate Trigger Current	I_{GT}	V_D=12V, R_L=100Ω	I		5.0	mA
			II		5.0	
			III		5.0	
			IV		10	
Gate Trigger Voltage	V_{GT}	V_D=12V, I_T=100mA			1.5	V
Peak Forward On-State Voltage	V_{TM}	IT=2.0A			1.5	V
Latch Current	I_L	V_D=12V I_G=0.1A,	I		5.0	mA
			II		8.0	
			III		5.0	
			IV		5.0	
Holding Current	I_H	V_D=12V ,I_G=0.1A			5	mA
Gate Non-Trigger Voltage	V_{GD}	V_D=V_{DRM}		0.2		V
Critical Rate of Rise of Off-State Voltage	dV/dt	V_D=67%V_{DRM}, R_{GK}=1kΩ		5		V/μs

ELECTRICAL CHARACTERISTIC CURVE

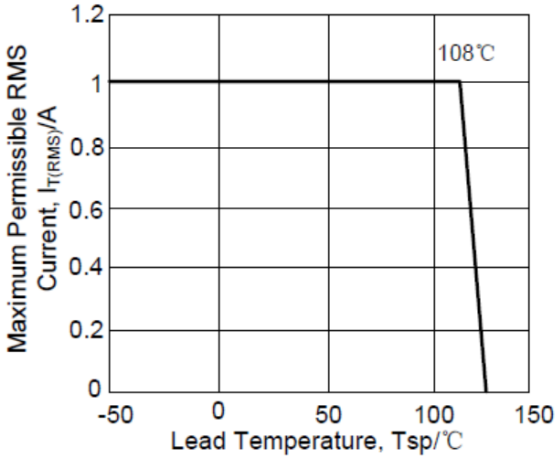




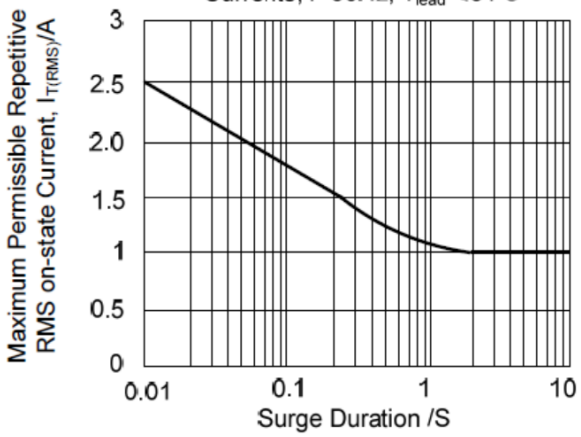
Maximum Permissible Non-Repetitive Peak On-State Current vs. Number of Cycles, for Sinusoidal Currents



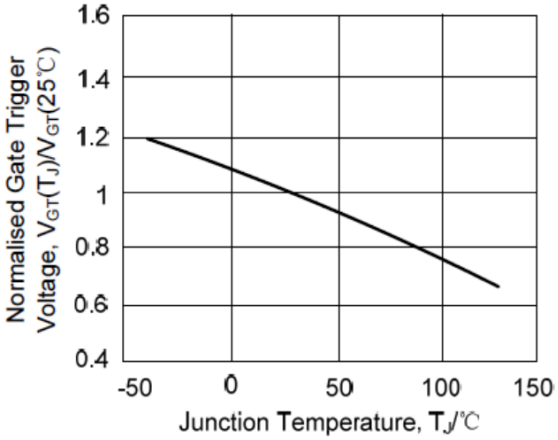
Maximum Permissible RMS Current $I_{T(RMS)}$ vs. Lead Temperature



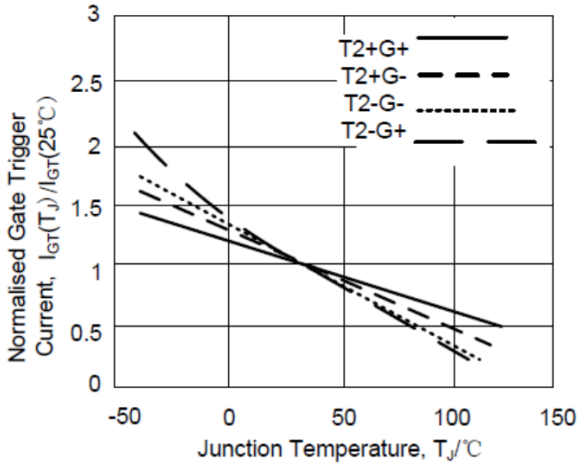
Maximum Permissible Repetitive RMS on-state Current vs. Surge Duration, for Sinusoidal Currents, f=50Hz; T_{lead}≤51℃



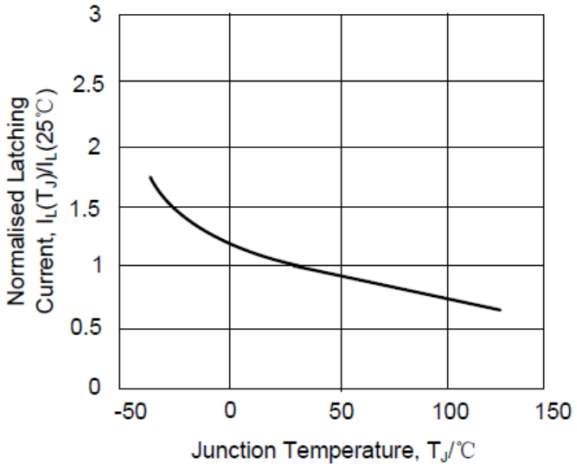
Normalised Gate Trigger Voltage vs. Junction Temperature

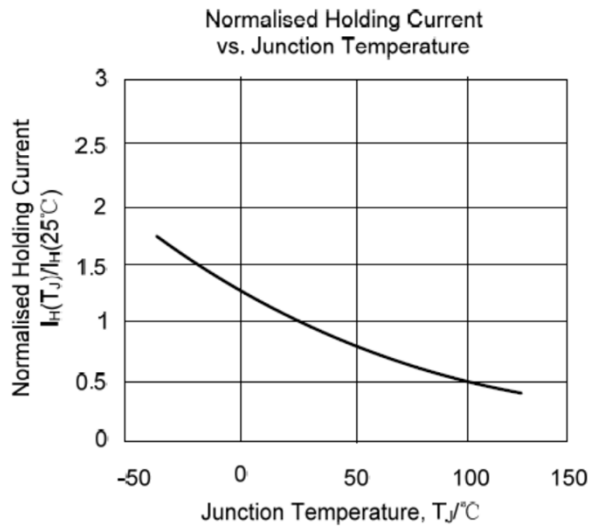


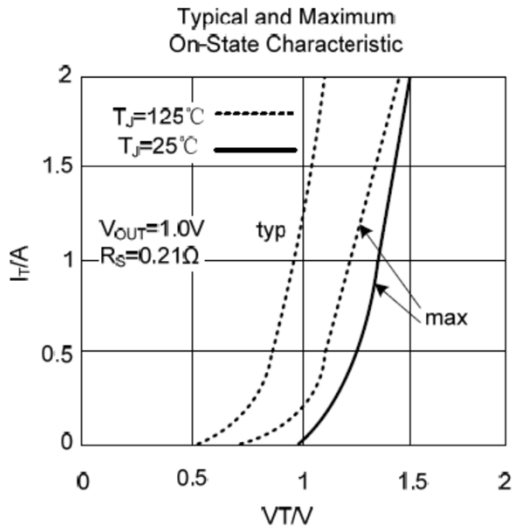
Normalised Gate Trigger Current vs. Junction Temperature

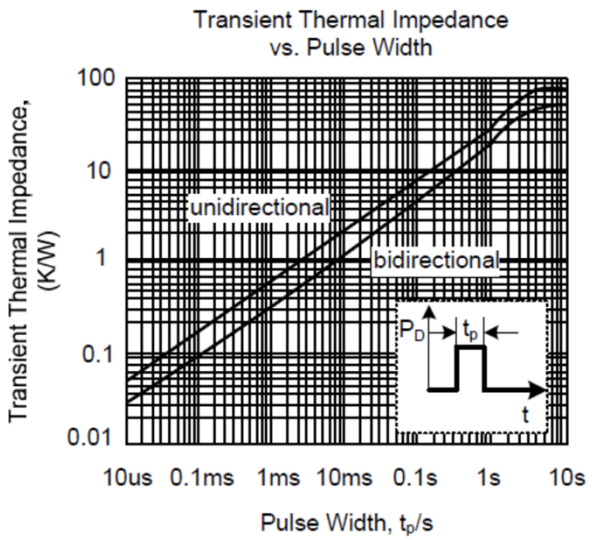


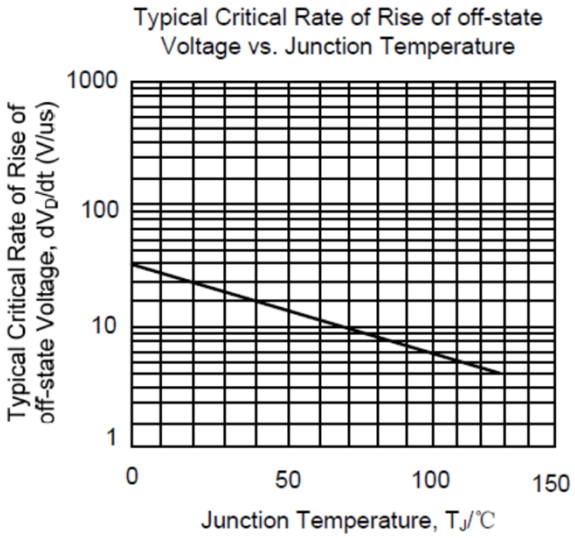
Normalised Latching Current vs. Junction Temperature




Normalised Holding Current
vs. Junction Temperature
Normalised Holding Current
IH(TJ)/IH(25℃)
3
2.5
2
1.5
1
0.5
0
-50
0
50
100
150
Junction Temperature, TJ/℃


Typical and Maximum
On-State Characteristic
TJ=125℃
TJ=25℃
VOUT=1.0V
RS=0.21Ω
typ
max
IT/A
2
1.5
1
0.5
0
0
0.5
1
1.5
2
VT/V


Transient Thermal Impedance
vs. Pulse Width
Transient Thermal Impedance,
(K/W)
100
10
1
0.1
0.01
unidirectional
bidirectional
PD
tp
t
10us
0.1ms
1ms
10ms
0.1s
1s
10s
Pulse Width, tp/s


Typical Critical Rate of Rise of off-state
Voltage vs. Junction Temperature
Typical Critical Rate of Rise of
off-state Voltage, dVD/dt (V/us)
1000
100
10
1
0
50
100
150
Junction Temperature, TJ/℃