DATA SHEET

PCF7922ATT

Keyless Entry Controller and Radio Transmitter (KEECART)

Product Specification

2015 May 11

Confidential

CONTENTS

1 FEATURES

- Single chip Keyless Entry solution with on-chip UHF Transmitter
- RISC programmable device features
- 512 Byte EEPROM for extended data storage
- 32 bit quasi unique device and product type identification
- Single Lithium cell operation, 2.1V to 3.6V
- 20-Pin TSSO package

Calculation Unit

- Hardwired security algorithm
- 48 (96) bit Secret Key

RISC Controller

- 8 Bit RISC Architecture (MRK II)
- 8 kByte or 16 kByte E-ROM
- 4 kByte ROM (device firmware and library functions)
- 192 Byte user RAM
- 7 general purpose I/O
- Two 8 Bit Timer/Counter
- Watchdog
- Single level interrupt architecture
- On-chip RC Oscillator (< ±8%)
- Short instruction execution time (as fast as 0.5 μs)
- Low power consumption
  RUN: 220 μA, IDLE: 20μA, PD: 100 nA
- Programmable battery low detection

UHF Transmitter

- Highly integrated, PLL stabilized design
- Carrier frequency 315 MHz or 434 MHz
- Programmable reference crystal load capacitance
- Programmable ASK and FSK modulation properties
- Up to 20 kbps modulation data rate (Manchester)
- Programmable and stabilized output power
- Low power consumption
  TRANSMIT: 9.8mA; 9dBm @ 434MHz,
  LOCKED: 1.5mA

2 GENERAL DESCRIPTION

The PCF7922 is low power single chip Keyless Entry solution, ideally suited for automotive applications.

Device operation is controlled by E-ROM (FLASH like features) based RISC Controller, powered by NXP' low power 8-Bit MICRO RISC KERNEL (MRK II). The RISC employs a 2-stage pipeline architecture in order to execute an instruction in a single clock cycle. The instruction set is compatible with the MRK I family. Device timing is derived from an on-chip low tolerance RC Oscillator that provides a programmable system clock, with a frequency up to 2 MHz. The system clock may also be derived from the PLL reference clock, if desired.

Rolling code generation may be accomplished by the application program and the hardwired Calculation Unit. The Calculation Unit may operate in standard HITAG2 (48 bit Shift Register) or Enhanced mode (96 bit Secret Key). A number of general purpose I/Os are provided for command buttons, LED, IR or other optional external circuitry. The on-chip UHF Transmitter required no external components to operate at 315MHz or 434MHz except for the reference crystal and the loop antenna matching circuitry.

The PCF7922 incorporates an advanced power management that supports voltage measurement, for battery low detection. For increased battery lifetime, the device features and extremely low quiescent current in POWER-OFF state, achieved by disconnecting the battery from most of the internal circuitry.

The device comes in a 20 pin TSSO Package. The device is available as E-ROM (FLASH like features) and supports in-circuit program download and. debugging.

The device is fully RoHS compliant and Dark Green (DG). DG means use of flame retardants free of halogen and antimony.

3 ORDERING INFORMATION

EXTENDED	PACKAGE		TEMPERATURE
TYPE NUMBER	NAME	OUTLINE VERSION	RANGE (°C)
PCF7922ATT/D1Ax0700	TSSOP20	SOT360-1	-40°C to +85°C
PCF7922ATT/D1Axrrff	TSSOP20	SOT360-1	-40°C to +85°C

Note

1. PCF7922ATT/D1Ax0700 represents the catalog products for which E-ROM programming shall be performed by the customer. The Monitor and Download Interface (MSDA/MSCL) supports E-ROM download and ERASE/WRITE as fast as 700ms for 4 kByte.
2. Factory programmed versions with custom EROM content are available. The actual customer application code and customer EEPROM fabkey is specified by a 2 digit code at location marked “ff”. The ROM code is specified by a 2 digit code at location marked „rr’
3. „x“ indicates E-ROM memory size and is defined as ‘B’=4kB, ‘C’=8kB and ‘E’=16kB in general. Please refer to later sections of this datasheet for the actually available E-ROM size options of this particular device.

4 TYPICAL APPLICATION

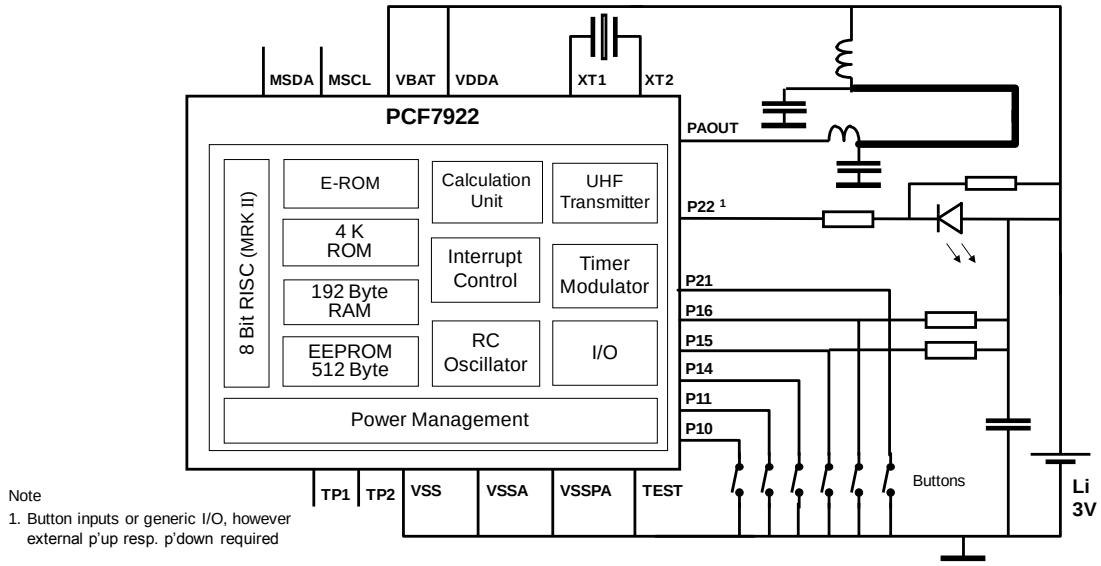


Figure 1. Typical Application Schematic

Note

1. Since most of the device ports do not feature an on-chip pull-up or pull-down, corresponding application measures are required to avoid a floating port, when operating as input (e.g. during POWER-OFF mode). This is applicable for ports P15, P16 and P22.

5 BLOCK DIAGRAM

The PCF7922 features a high level of integration and requires few external components only. The device incorporates the following circuitry. See Figure 2.

Power Management

- Supply Switch
- Supply Switch Logic
- Power On Reset
- Port Up Sense

Calculation Unit

Test/Debug Logic

RISC Controller

- 8 Bit RISC (MRK II family)
- ROM, System Code Memory
- E-ROM, Application Code Memory
- RAM
- EEPROM
- Interrupt Control
- Timers / Counters
- I/O Ports
- Programmable Voltage Comparator
- System Clock (including on-chip RC oscillator)
- Watchdog Timer

UHF Transmitter

- XTAL Oscillator
- Phase Locked Loop (PLL)
- Power Amplifier
- Control Logic

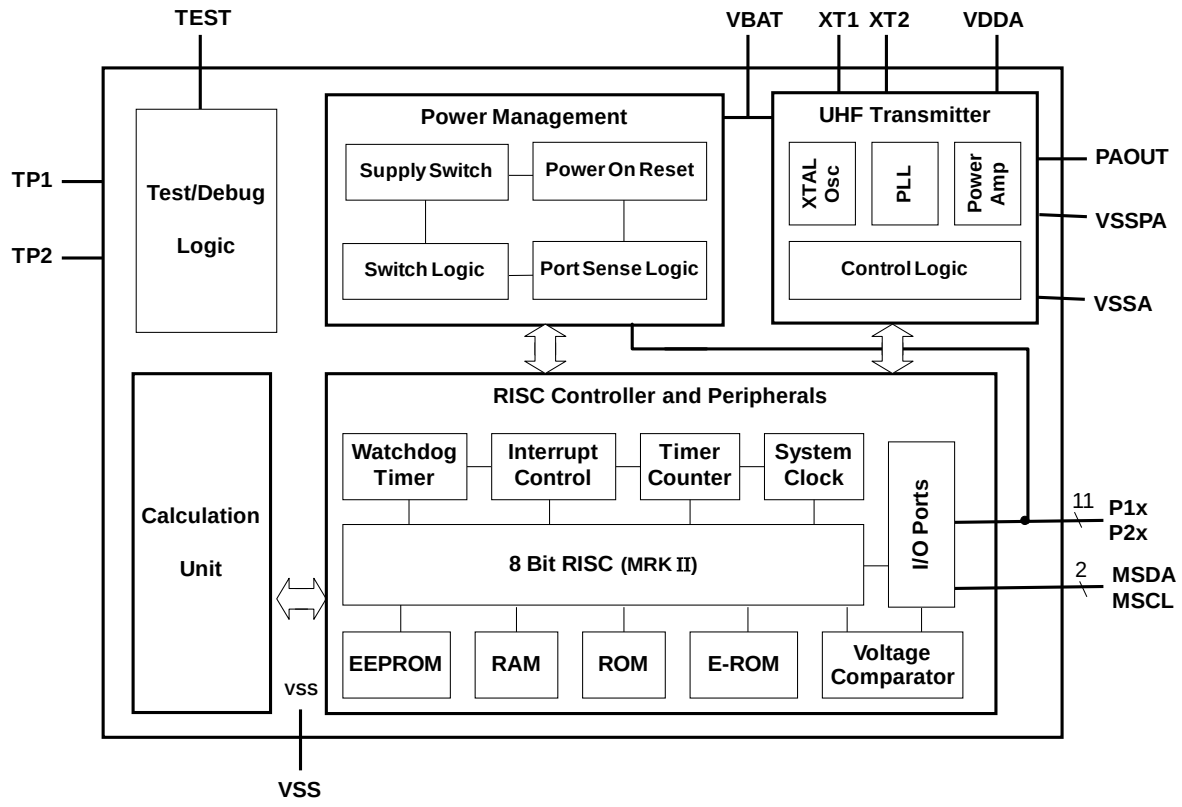


Figure 2. Block Diagram

6 QUICK REFERENCE DATA

RISC Operation

PARAMETER	VALUE	UNIT
Operating supply voltage (RISC)	2.1 – 3.6	V
Power-down current	100	nA
ROM (System Code Memory)	4 k	Byte
E-ROM (Application Code Memory)	4 k / 8 k / 16 k	Byte
RAM (user)	192	Byte
EEPROM	512	Byte
General purpose I/O	7 (TSSOP20)	
Operating speed, as derived from on-chip RC oscillator	0.125 – 2	MHz
Special Features	• EEPROM Erase/Write over full operating voltage range (2.1 to 3.6 V) • Programmable voltage comparator for battery voltage monitoring • PWM generation • Watchdog timer • Up to seven dedicated button inputs • 32 bit serial number and product type identifier	
Calculation Unit	• Supports HITAG2 or HITAG3 security algorithm (Secret Key 48 or 96 bit) • Supports Pseudo Random Number generation (Rolling Code)	

UHF Transmitter

PARAMETER	VALUE	UNIT
Operating supply voltage	2.1 – 3.6	V
Supply current (434 MHz)		
TRANSMIT mode	9.8	mA
LOCKED mode	1.5	mA
Carrier frequency	315 or 434	MHz
Output power (434 MHz)	9	dBm
Special Features	• Programmable XTAL load capacitance • Programmable FSK modulation characteristics • Programmable output amplitude • Programmable ASK modulation characteristics	

7 PINNING

FUNCTION	DESCRIPTION	PIN TSSOP20	NOTE
TP1	Reserved for test purposes	1	2
TP2	Reserved for test purposes	2	2
P14	General purpose I/O with switchable internal pull-up and Wake Up sense	3	
VBAT	Battery Supply Voltage (Battery pos. Terminal)	4	
P11	General purpose I/O with internal pull-up and Wake Up sense	5	
P22	General purpose I/O, Wake Up sense and Timer 1 compare output (PWM)	6	
P21	General purpose I/O, with switch able internal pull-up, Wake Up sense and Timer/Counter 1 Capture input / Interrupt input	7	
MSCL	ROM Monitor Serial Clock Output	8	1
MSDA	ROM Monitor Serial Data with internal pull-up	9	1
XTAL2	XTAL Oscillator	10	
XTAL1	XTAL Oscillator	11	
VSSA	Transmitter analogue ground	12	
VDDA	Transmitter analogue supply voltage	13	
VSSPA	Transmitter power amplifier ground	14	
PAOUT	Transmitter power amplifier output	15	
P10	General purpose I/O with internal pull-up and Wake Up sense	16	
P15	General purpose I/O, external clock input and Wake Up sense	17	
P16	General purpose I/O, Voltage comparator input and Wake Up sense	18	
VSS	Common Ground (Battery neg. Terminal)	19	
TEST	Test purposes	20	3

Note

1. MSCL is an open drain output in PUSH configuration and must be left unconnected in the application. During in-circuit flashing or debugging an external pull down resistor is required for proper operation. MSDA features an on-chip pull-up to VBAT. MSDA may be left open or terminated to VBAT, as desired. For field use, the device shall be configured for PROTECTED mode, after the application code has been flashed, see section 11.
2. For proper device operation the pins TP1 and TP2 must not be connected (floating) or connected to ground (VSS).
3. For proper device operation, pin TEST has to be connected to ground (VSS)

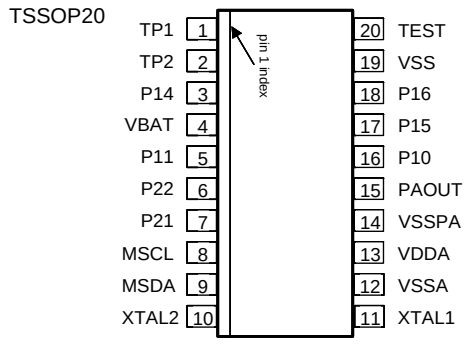


Figure 3. Pin Configuration

8 POWER MANAGEMENT DESCRIPTION

The PCF7922 features a quasi unique Power Management enabling the device to disconnect most of the internal circuitry from the external battery, in order to consume lowest power in POWER-OFF mode, see Figure 4.

The Power Management utilizes a Supply Switch that is controlled by the Supply Switch Logic and the ROM implemented device BOOT sequence. The two Supply Switch states correspond to certain operating modes, referred to as BATTERY Mode (PMODE = 1) and POWER-OFF Mode (PMODE = 0). Thus, the device is supplied either from an external battery (BATTERY Mode) or virtually consumes no power at all (POWER-OFF Mode).

During device power-up, the Supply Switch Logic closes (PMODE = 1) and the RISC Controller will commence program execution, starting with the BOOT sequence, before the application program is executed finally. When the application program completed its desired task, the device shall be forced into the POWER-OFF mode again, by opening the Supply Switch (PMODE = 0).

The Power Management features a set of control bits and flags to influence the Supply Switch state and program execution as desired.

In any case, a Power On Reset circuitry monitors the device supply voltage (V_{DD}), forcing the device into the reset state (MRST), in case the chip supply voltage drops below the Power On Reset threshold voltage. The Power On Reset circuitry is able to detect voltage dips as short as 10 us and features a hysteresis of typical 80 mV. Once triggered, the Power On Reset will be prolonged ($t_{POR-HLD}$) by a corresponding mono-flop, to ensure proper device start-up. Moreover, a device reset may be forced upon instruction, by triggering the control bit RST.

After battery power-up, the device enters either POWER-OFF or BATTERY Mode. Thus, the application program cannot detect, that the battery has been changed or has been inserted, see also section 21.6.

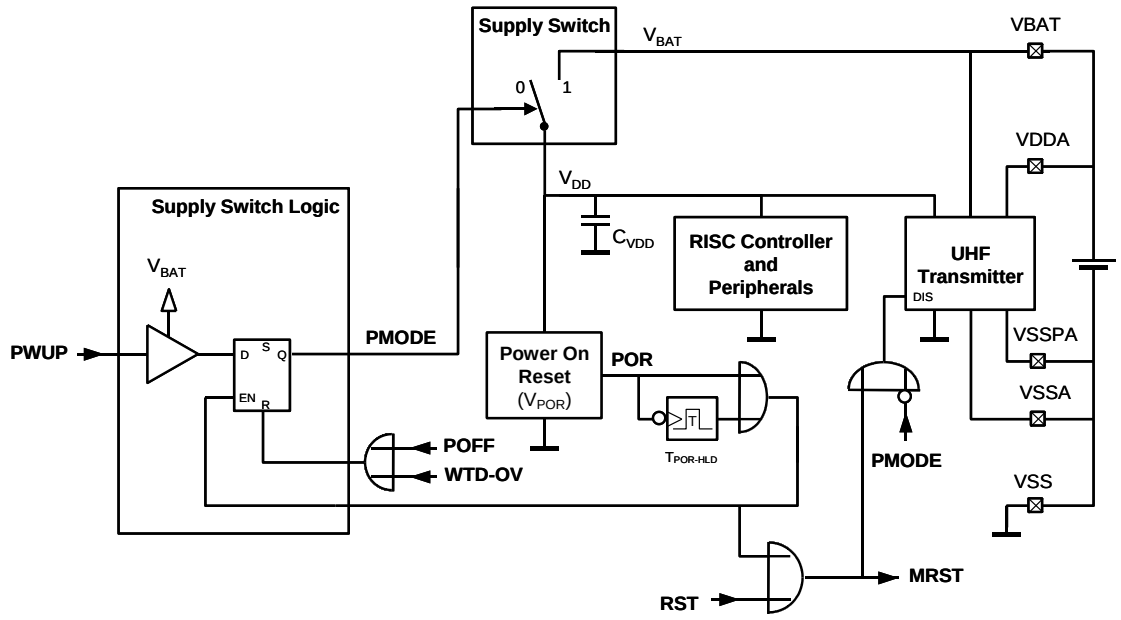


Figure 4. Power Management

Note

1. For information only, the on-chip capacitor C_{VDD} yields 2 nF for the PCF7922.

8.1 Supply Switch Logic

The Supply Logic controls the Supply Switch and responds to a Port Wake-Up (PWUP), see Figure 4.

The Supply Switch is controlled by a flip-flop that is forced into transparent state, whenever the device supply voltage (V_{DD}) stays below the Power On Reset threshold (POR = 1). In case a Port Wake Up condition is present, e.g. one of the button input is forced low, the flip-flop is forced into high state (PMODE = 1). Consequently, the device is connected to the battery. As soon as the chip supply voltage (V_{DD}) exceeds the Power On Reset threshold voltage ($V_{POR,BAT}$), POR becomes low. After a short delay ($T_{POR,HLD}$), the flip-flop is forced into latch state freezing the state of the supply switch and the RISC Controller becomes operational. Program execution commences starting with the BOOT routine, before the application Program is being invoked, see Figure 5 (see also section 13).

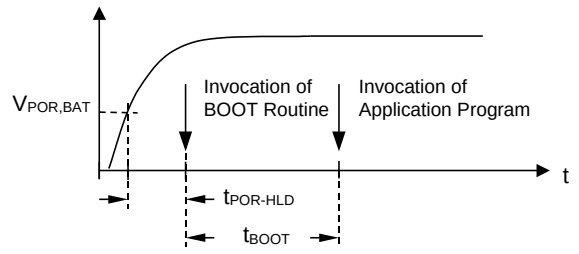


Figure 5. Power up timing

During RISC operation, the Supply Switch may be opened upon instruction, by triggering the control bit POFF. Thus, the device would enter the POWER-OFF mode, until a Port Wake Up is detected again.

Similar, if the Watchdog Timer is allowed to overflow the device also enters POWER-OFF mode, see also section 10.6.

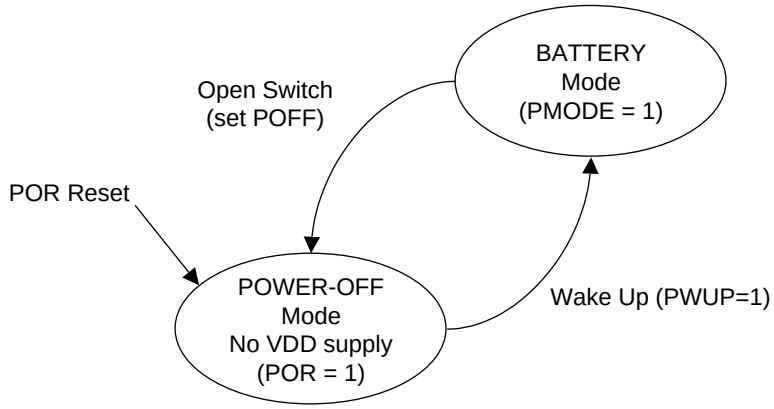


Figure 6. Device Operating Modes

8.2 Device Operating Modes

The device resides in one of two modes, POWER-OFF or BATTERY Mode, Figure 6.

Both modes correspond to a certain device supply condition. Hence, the device is supplied from an external battery (BATTERY Mode) or virtually consumes no power from the battery at all (POWER-OFF Mode).

8.2.1 POWER-OFF Mode

The device resides in POWER-OFF Mode any time a Power On Reset condition is applicable, either because of a weak supply condition or forced by the application program.

In POWER-OFF Mode, the internal Supply Switch disconnects the device from the battery (PMODE = 0), making the device to drain virtually no current from the battery. The internal device supply voltage (V_{DD}) stays below the power on reset threshold voltage ($V_{POR,FLD}$) and device operation is halted. Only a minimum of circuitry remains operational, like the Power Management and I/O Port circuitry, however, latter one is configured for input mode in any case.

The POWER-OFF Mode is terminated and BATTERY Mode entered, upon a Port Wake Up (WUP = 1). Thus, at least one of the button inputs has been forced low (see also section 8.3). Once the device supply has settled and the BOOT sequence completed, the device commences execution of the application program.

8.2.2 BATTERY Mode

In BATTERY Mode, the internal Supply Switch connects the external battery with the device supply (PMODE = 1) and powering the device.

Device operation is controlled by the RISC and the corresponding program code. Program execution starts with the BOOT sequence before control is passed to the WARM BOOT vector (0000_H) enabling the application code to take control (see also section 13).

Upon instruction, the application code may terminate the BATTERY Mode at any time, by clearing the latch PMODE. This is accomplished, by triggering the control bit POFF. Subsequently, the Supply Switch opens, the device enters POWER-OFF mode and the Supply Switch Logic takes over device control.

However, the effects of residual internal charge need to be taken into account, in order avoid undesired device operation, see section 21.4.

8.3 Port Sense Logic

The Port Sense Logic provides means to wake up the device from POWER-OFF mode or to trigger a corresponding interrupt during program execution, by designated I/O ports (button inputs), according to Figure 7.

Upon a high-to-low transition the corresponding port mono-flop is triggered and remains set for the specified time (T_{PSMF}), regardless of the subsequent port state. The mono-flop is triggered again upon a high-to-low transition only. Provided the corresponding port is configured for input mode and is not being used in a different context, Port Trigger occurs and a corresponding interrupt request is generated.

When the device resides in POWER-OFF Mode, hence POR (Power On Reset) being high, Port Trigger will set a flip-flop, signaling a Port Wake-Up event. As the RISC Controller resides in Power On Reset state, the Port Interrupt is not being detected. The Supply Switch Logic monitors the state of this flip-flop and will respond to the Port Wake-Up event accordingly, section 8.1.

The Port Wake Up flip-flop is cleared in the moment the device Power On Reset (POR) vanishes, e.g. as soon as the power-on reset circuitry detects a valid operating voltage, causing the device to commence program execution. Subsequent Port Trigger events, e.g. possibly caused by button bouncing, will be handled as Port Interrupts and the application program shall respond as desired.

In any case, Port Trigger is supported only, if the designated ports are configured for input mode, hence the corresponding port direction control bit is cleared (IOxx), see section 10.7. Further, the ports must not be used in a different context, possibly overruling the port direction control bit. E.g. P15 as external Timer Counter clock input, see section Timer/Counter 0 respectively section 10.5; P16 as external Voltage Comparator input, see section 10.9, P21 as Timer 1 Capture input respectively P22 as Timer 1 Pulse Width Modulator output, see section 10.5.

While the device resides in POWER-OFF mode, any of the above mentioned ports generates a Port Wake Up event, because the I/O port are in any case forced into input mode and the Wake Up feature can not be disabled. In order to avoid unintended device Wake Up, special care is required, when using one of the above ports as an ordinary I/O, see section 21.5.

In any case, it is necessary to establish static non-floating conditions in port input mode, in order to avoid an undesired quiescent current to be drawn from the battery. As the ports are falling edge sensitive, both, pull-up or pull-down measures are allowed to define the static level. Please note that P10 and P11 already feature an on-chip pull-up and Port P14 and P21 an on-chip pull-up that is active only, when the port operates in input mode.

After battery power-up, the device either enters POWER-OFF or BATTERY Mode. Thus, the application program can not detect, that the battery has been changed or has been inserted, see also section 21.6.

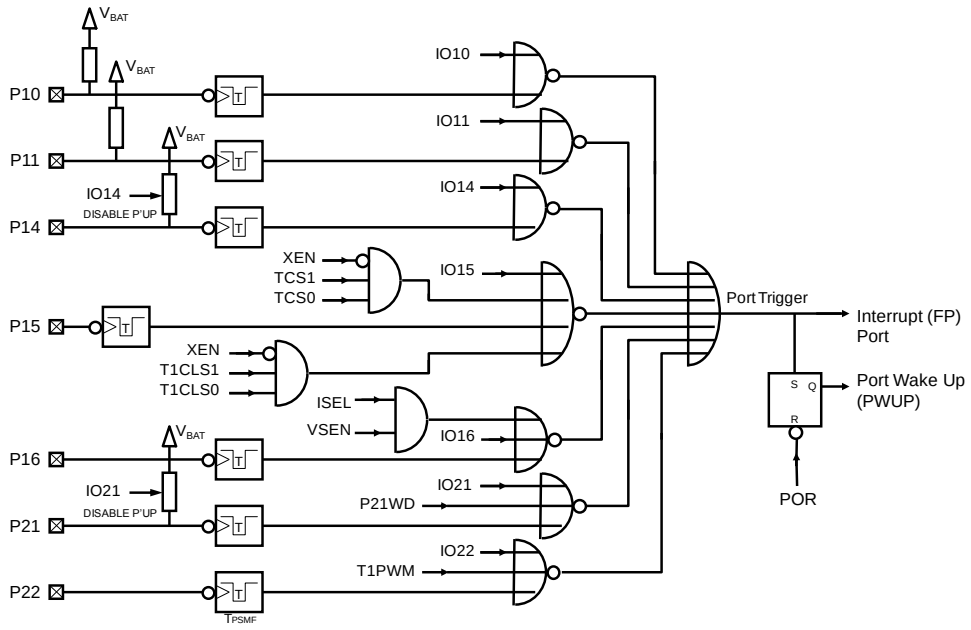


Figure 7. Port Sense Logic

8.4 Power Management Control Register

The Power Management features a set of control bits and flags to influence device operation, arranged in the Power Control register, PCON, that is located in the SFR space of the data memory, see Table 1.

Table 1 Power Control Register, PCON

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
X	X	X	PMODE	RST	X	POFF	IDLE
R/W	W0	R	R	R0/W1	W0	R0/W1	R0/W

Note Address = 26H

1. Bits marked ‘X’ are not connected and reserved for future use. Any read operation yields an undefined result. For future compatibility, any write operation should assign a ‘0’.
2. RST, POFF and IDLE provide a trigger signal for the corresponding circuitry. Any read operation yields zero as result.
3. RST must not be set to ‘1’ simultaneously POFF.

PMODE, Power Mode

The flag PMODE signals the current state of the Supply Switch. The state of PMODE can not be altered directly. Instead, indirect control is provided by the control bits POFF.

POFF, Power Off

The control bit POFF provides means to open the Supply Switch and to disconnect the battery from most of the device circuitry. Any access that writes a ‘1’ to POFF will open the Supply Switch (PMODE = 0).

RST, RESET device

The control bit RST provides means to immediately reset the entire device, causing the device to initialize all Special Function Register to their corresponding reset value and to invoke the boot sequence. The Supply Switch state is not affected by the reset.

IDLE, IDLE Mode

The control bit IDLE, provides means to force the RISC Controller into IDLE mode. Any access that writes a ‘1’ to IDLE will cause the device to halt program execution after completion of the corresponding instruction, by inhibiting the CPU clock. However, the system clock and all peripherals stay operational. The IDLE mode terminates and program execution is resumed upon a corresponding event, see Interrupt System and IDLE Control, section 10.2.5.

9 RISC CONTROLLER DESCRIPTION

The PCF7922 is powered by NXP' 2nd generation low power 8-Bit MICRO RISC KERNEL (MRK II) to control device operation.

The MRK II utilize a Harvard architecture featuring an 8 bit ALU and 16 bit instruction width. Due to the two stage pipeline concept, instructions virtually execute in a single clock cycle, resulting in an ultra low power consumption. The applicable instruction set is downward compatible to the MRK I Family of products, featuring a number of extended addressing modes and architectural enhancements. For a general description of the MRK II core, please refer to the specification MRK II Family, Architecture and Instruction Set, see section 22. However, the PCF7922 specific implementation of the MRK II core is described below.

9.1 Application Code Memory

The PCF7922ATT provides up to 16 kByte of Application Code. Each instruction consists of 16 bit and thus occupies two bytes, see Figure 8.

After a device reset, program execution starts with the BOOT sequence and subsequently continues with the Application Code, commencing at the WARM BOOT vector (see section 13).

Unresolved SYS calls feature a dedicated vector that is accessed in the corresponding event.

The PCF7922 features 4 interrupt vectors. Each vector is assigned to a fixed location in the memory. INT 0, INT 5 and INT 6 are reserved for future use.

Interrupt vectors INT 1 to INT 4 can independently be enabled or disabled. If an interrupt is enabled, it causes the RISC controller to perform a CALL operation to the corresponding location, where execution of the Interrupt Service Routine, ISR, commences. E.g. in case of an INT 2 interrupt (Timer 0 Overflow) program execution would commence at memory location 0006H. A JMP instruction needs to be placed at the corresponding location, in order to redirect program execution to the final location of the ISR (interrupt service routine). It is recommended to place a RETI instruction at all interrupt vectors not used.

In the case of simultaneous interrupts, the interrupt with the lowest vector address is executed first.

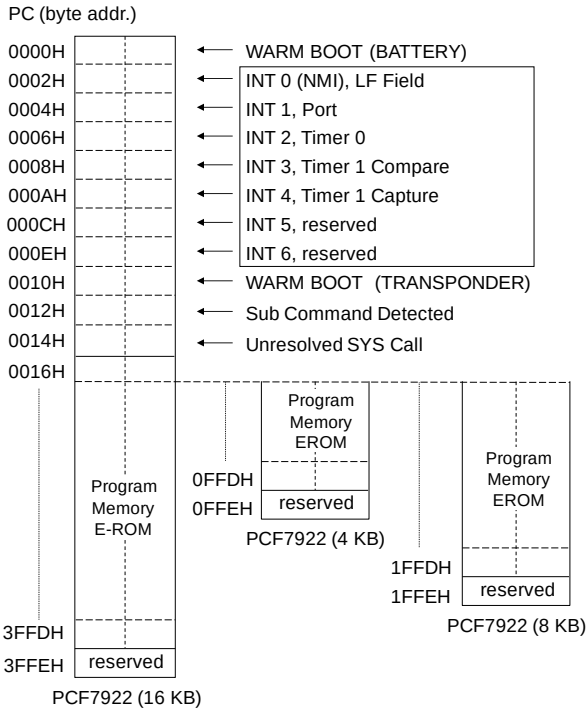


Figure 8. Application Code Memory

Note

1. The upper two bytes are reserved for device configuration purposes in any case and are not available to the application.

9.2 System Code Memory

The PCF7922 features 4 kByte of System Code Memory that holds a predefined NXP implemented ROM Library featuring a set of library functions, the device Boot routine and controls the in-circuit Monitor and Download Interface. The System Code Memory is not visible to the application. The ROM Library functions are invoked by a System Call (SYS instruction) that passes control back to the application program, when completed.

The Interrupt System is disabled during execution of system code. Thus, any interrupt request is latched only and execution delayed until control is returned to the application code. For a detailed description of the ROM Library, please refer to specification PCF7x41 ROM Library, Implementation and Description, see also section 22.

Boot Routine

The BOOT routine is invoked immediately after a device reset. The BOOT routine configures the device, evaluates device protection flags and passes control to the Application Code finally, see section 13.

ROM Library

The ROM library features a set of generic functions. The corresponding functions are invoked from the application program by a System Call (SYS instruction). For more detailed usage, please refer to the specification PCF79x41 ROM Library, Implementation and Description, see also section 22.

In-Circuit Monitor and Download Routine

The in-circuit Monitor and Download Interface provides means for E-ROM and EEPROM initialization and to monitor and manipulate the embedded peripherals in the context of system debugging, employing communication via a two-wire serial interface (MSDA / MSCL), see section 14.

9.3 Data Memory

The PCF7922 Data Memory address space is split into a Register File (R0 to R7), reserved space, Special Function Registers (SFR) and 192 byte User RAM, see Figure 9.

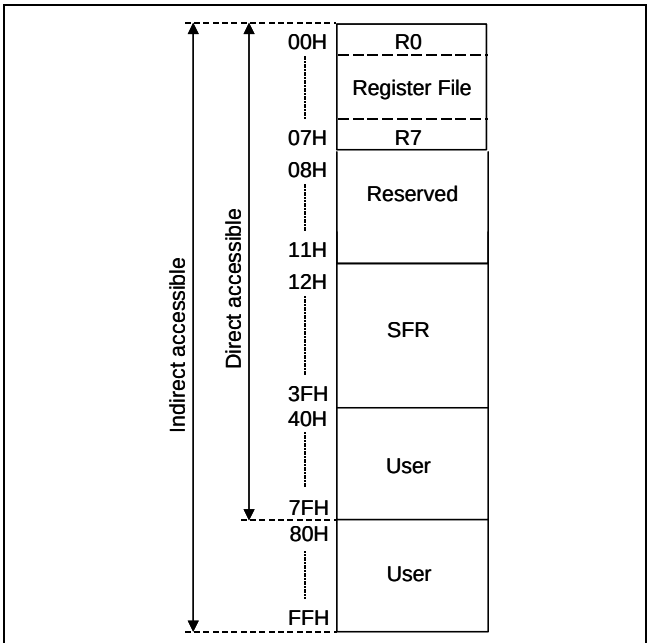


Figure 9. Data Memory, RAM

The application program may not address the reserved address space from 08H to 11H in order to prevent unintended results.

The Special Function Register, SFR, space enables I/O from/to the peripherals and EEPROM as well as control of the interrupt system. The User segment provides RAM for volatile application data and Stack storage. RAM space up to address $7F_H$ supports direct and indirect addressing, while RAM space beyond $7F_H$ supports indirect addressing only. For details, refer to the specification MRK II Family, Architecture and Instruction Set, see section 22.

10 PERIPHERIAL DESCRIPTION

In order to enable access to the peripherals like the EEPROM as well as to control operation of the Interrupt System Power Management and UHF Transmitter, a set of Special Function Register, SFR, is provided. Table 2 provides a comprehensive overview of the SFR organization and their corresponding values after a device reset.

Table 2 Special Function Register Summary

NAME	DESCRIPTION	ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	RESET VALUE
PSW	Program Status Word	12_H	C	H	OV	X	C‘	H‘	OV‘	X’	
SP	Stack Pointer	13_H	SP7	SP6	SP5	SP4	SP3	SP2	SP1		$0000000X_B$
SBIT	Indirect Bit Address	14_H	MAP					SBIT2	SBIT1	SBIT0	
SPTR	Indirect Byte Address	15_H	SPTR7	SPTR6	SPTR5	SPTR4	SPTR3	SPTR2	SPTR1	SPTR0	
IE	Interrupt Enable	16_H	EA		EE	ET1A	ET1O	ET0	EP		$0X00000X_B$
IFF	Interrupt Flag	17_H			FE	FT1A	FT1O	FT0	FP		$XX00000X_B$
T0	Timer/Counter 0	18_H									
TR0	Timer/Counter 0 Reload	19_H									
TCON	Timer/Counter 0 Control	$1A_H$		TPS2	TPS1	TPS0	TCS1	TCS0		TRS0	$X00000X0_B$
WTCON	Watchdog Timer Control	$1B_H$		WPS2	WPS1	WPS0				WCLR	$X000XXXX_B$
	Reserved		Reserved								
MODCON	Modulator Control	$1D_H$	MDB	EFM	EAM	TSEL	SCEN	EP17	EP20		$X00X000X_B$
CRYP1	Calculation Unit I/O	$1E_H$	CRIO								
CRYP2	Calculation Unit Control	$1F_H$						CRM2	CRM1	CRM0	
P1OUT	Port 1 Output	20_H	P17	P16	P15	P14	P13	P12	P11	P10	
P1INS	Port 1 Input sense	21_H	P17S	P16S	P15S	P14S	P13S	P12S	P11S	P10S	
P1DIR	Port 1 Direction	22_H	IO17	IO16	IO15	IO14	IO13	IO12	IO11	IO10	00000000_B
P2OUT	Port 2 Output	23_H		P26		P24	P23	P22	P21	P20	$X0X00000_B$
P2INS	Port 2 Input sense	24_H				P24S	P23S	P22S	P21S	P20S	
P2DIR	Port 2 Direction / Control	25_H	P21WD	P2CIS		IO24	IO23	IO22	IO21	IO20	$00X00000_B$
PCON	Power Control	26_H				PMODE	RST		POFF	IDLE	$0XXX0000_B$
SCSL	System Clock Select	27_H						CSL2	CSL1	CSL0	$XX0X0000_B$
T1CON1	Timer/Counter 1 Control 1	28_H	T1RUN	T1RES	T1RC	T1OTC	T1CF	T1CR	T1CSS	T1CM	$0XXXXX00_B$
T1CON2	Timer/Counter 1 Control 2	29_H	T1PWM	T1RCAP	T1RCMP	T1S2	T1S1	T1S0	T1CLS1	T1CLS0	$00XXXX00_B$
T1CAP	Timer/Counter 1 Capture	$2A_H$									
T1CMP	Timer/Counter 1 Compare	$2B_H$									
EEDAT	EEPROM Data	$2C_H$	EEIO								
EECON	EEPROM Control	$2D_H$	BUSY	PERR	WR	POEE	PG6	PG5	PG4	PG3	$0000XXXX_B$
EEADR	EEPROM Address	$2E_H$	PG2	PG1	PG0	BYTE1	BYTE0	BIT2	BIT1	BIT0	
VCON	Voltage Comp. Control	$2F_H$	VCMP	VSEN	ISEL		VST3	VST2	VST1	VST0	$X0XXXXXX_B$
XFCON	XTAL Frequency Control	30_H			XFC5	XFC4	XFC3	XFC2	XFC1	XFC0	$XX000000_B$
PACON	Power Amplifier Control	31_H	AMH3	AMH2	AMH1	AMH0	AML3	AML2	AML1	AML0	$XXXX0000_B$
TXCON1	Transmitter Control 1	32_H			XCD	XFCS	TM	OG1	OG0	XEN	$XX001000_B$
TXCON2	Transmitter Control 2	33_H			FBSL		VOSL	PAM1	PAM0	TXON	00000000_B

Note

1. Address locations not mentioned are reserved for future use and shall not be accessed.

10.1 EEPROM

The PCF7922 incorporates 512 byte of non-volatile memory (EEPROM). Reading and writing of EEPROM data is supported in sequential order, bit wise addressing with auto increment is implemented for the read operation, while an ERASE/WRITE operation does always affect a complete byte. Up to four bytes may be subject to an ERASE/WRITE operation at the same time.

10.1.1 Organisation

The 512 byte of non-volatile memory (EEPROM) are organized as 128 pages, each page assembled by four byte with a total of 32 bit per page, see Figure 10.

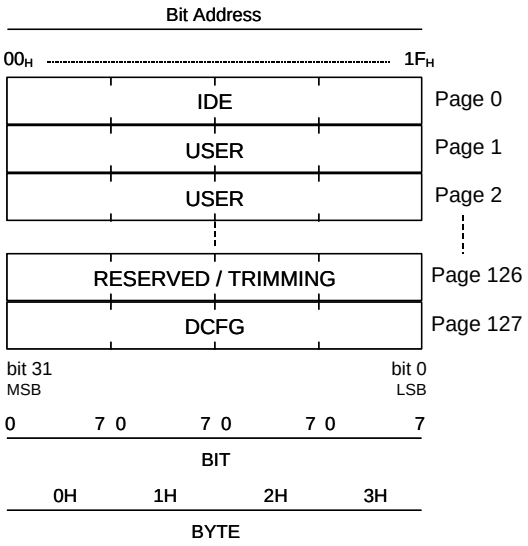


Figure 10. EEPROM Memory Organization

Page 0 holds the device Identifier, IDE, page 126 is reserved and page 127 holds device configuration data (DCFG). Both are programmed during device manufacturing and locked against overwriting, according to section 15. Pages 1 to 126 are available for user data storage.

The Bit Address referred to is assembled by the BYTE and related BIT address, as specified by the corresponding control register, see below. For compatibility reasons, with respect to the products PCF7946/47 and PCF7941/42/43/44, the logical bit designators (e.g. bit31, MSB and bit0, LSB) are provided in addition.

10.1.1.1 Identifier, IDE

The Identifier, IDE, is a factory programmed quasi unique 32 bit pattern that serves the function of a device serial number (SN) and product type identification (PI) and can not be altered. The Identifier is located page 0 and only supports reading, see Figure 11.

The product type identification is located in the bits 4 to 7 and factory programmed for all PCF7922 devices to 8_H.

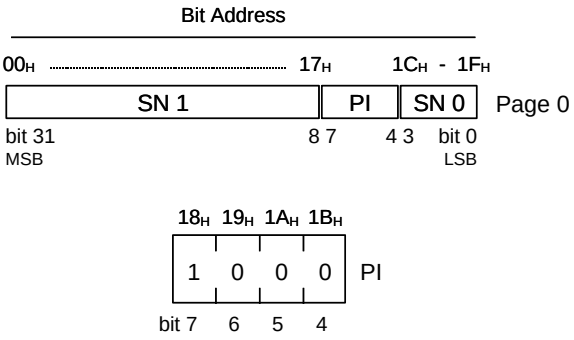


Figure 11. Identifier Organization, IDE

The Identifier is typically employed in the process rolling code or challenge response generation for keyless entry applications. The use of the factory supplied Identifier is not mandatory, instead the device can be configured (DCFG) to employ a 32 bit pattern located in any page in the range 0 to 126.

10.1.2 High-Level EEPROM Access

A set of firmware functions for EEPROM ERASE/WRITE access are readily available, in order to ease development of the application software. For details refer to the specification PCF7x41 ROM Library, Implementation and Description, see section 22.

In case the EEPROM is accessed through one of the ROM Library functions, memory access restrictions are implemented according to Table 3.

Table 3 EEPROM Access Rights via ROM Library

Page	Bit	ROM Library	Note
0	All	Read Only	
1 to 125	All	Read/Write	
126 to 127	All	Read Only	

The application program may restrict the EEPROM access further as required and desired, in order to virtually protect more memory locations against alteration or access.

In addition, the EEPROM can be accessed via the Monitor and Download Interface, in order to customize the EEPROM content during device personalization. In case the EEPROM is accessed through the Monitor and Download Interface, memory access restrictions depend on the Device Mode (INIT respectively PROTECTED, see also section 11) and are implemented according to Table 4.

Table 4 EEPROM Access Rights via Monitor Interface

Page	Bit	INIT	PROTECTED	Note
0	All	Read Only	No Access	
1 to 125	All	Read/Write	No Access	
126	All	Read Only	No Access	
127	00_H to $0F_H$	Read Only	No Access	
127	10_H to $1F_H$	Read/Write	No Access	

10.1.3 Low-Level EEPROM Access

The application program will typically utilize the high-level EEPROM access only. The low-level access scheme is described below for the sake of completeness. Because of the access restriction desired by the application, the low-level EEPROM access is restricted according to Table 5.

Table 5 Low-Level EEPROM Access Rights

Page	System Code	Application Code	Note
0	Read/Write	Read Only	
1 to 125	Read/Write	Read/Write	
126 to 127	Read/Write	Read Only	

Any application code can access the EEPROM in accordance with the access restriction only, whereas the system code (e.g. Boot routine, ROM Library, Monitor and Download Routine) supports unlimited reading and writing. However, the system code is factory programmed and can not be altered by the user.

Read/write access to the EEPROM utilizes a set of control registers, in order to specify the designated EEPROM location, the type of operation to be performed and provides status information. The control registers are located in the Special Function Register range and comprise of the Control/Status register EECON, see Table 6, the address register EEADR, see Table 7 and the data register EEDAT, see Table 8.

Table 6 EEPROM control register, EECON

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
BUSY	PERR	WR	POEE	PG6	PG5	PG4	PG3
R	R/W1	R/W	R/W	R/W	R/W	R/W	R/W

Address = 2DH

Table 7 EEPROM address register, EEADR

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
PG2	PG1	PG0	BYTE1	BYTE0	BIT2	BIT1	BIT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address = 2EH

Table 8 EEPROM data register, EEDAT

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
EEIO	X	X	X	X	X	X	X
R/W0	W0	W0	W0	W0	W0	W0	W0

Note Address = 2CH

1. Bits marked ‘X’ are not connected and reserved for future use. Any read operation yields an undefined result. For future compatibility, any write operation should assign a ‘0’.

Read Operation

Reading of EEPROM data is supported in sequential order, featuring bit wise addressing with auto increment.

Due to the given EEPROM access delay ($t_{EE,DLY}$), repeated reading from the EEPROM requires to introduce a corresponding delay in between to consecutive read operations, in accordance with the CPU clock rate selected, see Table 9.

Table 9 EEPROM Read Delay

CPU clock	Number of instructions between two consecutive EEPROM read operations
125 kHz	0
250 kHz	1
500 kHz	1
1 MHz	3
2 MHz	6

Write Operation

Writing of EEPROM data is supported page wise in sequential order, featuring bit wise addressing with auto increment. The device supports ERASE/WRITE of a single byte within a page, without stressing the unaffected bytes of that page. Anyhow, four byte (one page) may be altered at one time, thus during the same EARSE/WRITE cycled.

Before actually altering the EEPROM array, write operations target the 32 bit (4 byte) EEPROM write buffer that is required to be initialized prior to each EEPROM write operation. Once the buffer content is set as desired, an EEPROM ERASE/WRITE operation has to be requested, in order to change the EEPROM array according to the buffer content finally. Latter one, when requested from the application code, has to be interrogated by a system call (EE_BURN), in order to verify the write request against the access restriction eventually in place and return an error in such a case. Please refer to the ROM Library description for details regarding EE_BRUN, see section 22.

However, the EEPROM ERASE/WRITE sequencer will only alter bytes of the selected EEPROM page that have been previously accessed in the buffer, either a single bit of it or the complete byte. In case that a byte has been accessed only partly, all remaining bits of that byte are set to “1” by default. Hence, writing a single bit to the buffer will cause the corresponding byte of the EEPROM page being altered, erasing seven bits (“1”) and setting the designated bit as intended. The remaining bytes of the page will not be affected nor subject to an ERASE/WRITE operation.

Once the EEPROM write buffer is initialized, either partly or all 32 bit of it, only the page address is of significance during the final ERASE/WRITE operation and the bit and byte address are not regarded.

The EEPROM ERASE/WRITE operation takes a certain time (t_{ERWR}), independent of the number of bytes (one to four) that are being altered within the designated page. Some readily available EEPROM functions of the ROM Library may perform multiple ERASE/WRITE operations, e.g. WRITE_SYNC command, as well as add execution time. As a result, the calling application program will recognize a different timing, see also section 22

The EEPROM cell ERASE operation corresponds to a logic one (“1”), while the WRITE operation affects cells that shall be set to logic zero. (For information only, the physical EEPROM cell always yields a state inverse to the logical one, ensuring compatibility with the existing product family and the corresponding LOCK bit features).

POEE, Power On EEPROM

The EEPROM circuitry is enabled for reading or writing by setting the control bit POEE. As a result the sense amplifier and other EEPROM circuitry will be biased and need to settle (t_{EEPU}) before any read or write access is feasible. In addition, the write buffer needs to be initialized before a write operation shall be performed, for details refer to the control PERR.

For power consumption reasons, POEE shall be cleared, whenever EEPROM access is not required.

PG[6…0], Page Address

The seven bit control word PG[6…0] provides means to specify the EEPROM page designated for access. When changing the page address, the EEPROM access delay ($t_{EE,DLY}$) must timeout, prior to any EEPROM read/write access via the control bit EEIO, see below.

The control bits are partly located in the control register EECON (PG6 to PG3) and partly in EEADR (PG2 to PG0).

BYTE[1…0], Byte Address

The two bit control word BYTE[1…0] provides means to specify the byte within an EEPROM page designated for access. When changing the byte address, the EEPROM access delay ($t_{EE,DLY}$) must timeout, prior to any EEPROM read/write access via the control bit EEIO, see below

BIT[2…0], Bit Address

The three bit control word BIT[2…0] provides means to specify the bit location within an EEPROM byte designated for access. When changing the bit address, the EEPROM access delay ($t_{EE,DLY}$) must timeout prior to any EEPROM read/write access via the control bit EEIO, see below

WR, Select Write/Read

The control bit WR specifies the access direction. If cleared, the EEPROM is accessed for read. If set, it is accessed for write.

Please note that any write attempt, when requested from the application code, needs to be interrogated by a system call (EE_BURN, please refer to the ROM Library description for details, see section 22), in order to verify the write request against the access restriction eventually in place.

The control bit WR must not be cleared, while an EEPROM ERASE/WRITE operation is in progress, hence while the status bit BUSY is set.

EEIO, EEPROM Data I/O

The control bit EEIO provides means to read a single data bit from the EEPROM array or to write to the EEPROM write buffer, in accordance with the access direction as specified by the control bit WR.

In case EEPROM read operation is selected (WR = 0), repeated reading from EEIO will automatically and modulo increment the address pointer, comprising of the bit (BIT[2…0], byte (BYTE[1…0]) and page (PG[6…0]) address, after any EEIO read operation (post-increment). Consequently, the address pointer sequentially steps through the entire EEPROM space bit by bit. Thus requires setting the start address only. Writing to EEIO is not allowed in this mode, in order to avoid that the EEPROM address is anciently incremented.

Due to the given EEPROM access delay ($t_{EE,DLY}$), repeated reading from the EEPROM by EEIO requires to introduce a corresponding delay in between to consecutive read operations, see Table 9.

In case EEPROM write operation is selected (WR = 1), repeated writing to EEIO will automatically and modulo increment part of the address pointer, affecting the bit (BIT[2…0] and byte (BYTE[1…0]) only. The address pointer increments after any EEIO write operation (post-increment). However, the page address is not altered.

As writing to EEIO only targets the EEPROM write buffer, an EEPROM ERASE/WRITE operation has to be requested finally, in order to change the EEPROM array according to the buffer content. Latter one, when requested from the application code, has to be interrogated by a system call (EE_BURN), in order to verify the write request against the access restriction eventually in place and return an error in such a case. Please refer to the ROM Library description for details regarding the function EE_BURN, see section 22.

Since the EEPROM write buffer is set to all “1” by default, EEIO supports clearing of the corresponding bit only. Once cleared, the corresponding bit can not be set to one again, except the write buffer is initialized again, using the control bit PERR. However, the application program needs to write a “1” and “0” to the buffer as desired, in order to signal to the ERASE/WRITE sequencer, which of the EEPROM bytes shall be subject to an ERASE/WRITE operation.

BUSY, Busy

The status bit BUSY provides means to detect completion of the EEPROM erase/write operation. When set the EEPROM erase/write operation is in progress. Otherwise, when cleared, has completed.

In addition, the high-low transition of BUSY does trigger an interrupt flip-flop signaling that the EEPROM ERASE/WRITE operation finished, providing means to release the device from IDLE mode. A dedicated interrupt is not provided, see section 10.2. In addition does initialize the ERASE/WRITE sequencer and sets the write buffer to its default value, all “1”.

PERR, Programming Error

The status bit PERR provides means to verify, if the EEPROM on-chip charge-pump is within specification in the moment the ERASE/WRITE sequence has been started.

In case the status bit PERR is found set, after the EARSE/WRITE sequence completed, the designated EEPROM location may be corrupted and its content is undefined.

If PERR is cleared, the EEPROM ERASE/WRITE sequence completed as desired. However, any supply voltage dip during the ERASE/WRITE sequence may cause a device reset and corrupt the designated EEPROM location leaving its content undefined. By circuit design, it is granted that no other EEPROM page is affected in this condition, because the page address is not reset and the on-chip charge-pump is discharged, while the supply voltage is below the power on reset threshold.

The status bit stays set until the next programming is started. PERR my be cleared by writing a one to itself, which in addition will reset the ERASE/WRITE sequencer and sets the EEPROM write buffer to its default value, hence all “1”. Latter one shall be performed, before any EEPROM write operation is intended. Clearing PERR has no effect.

10.2 Interrupt System and IDLE Control

The PCF7922 employs a single level interrupt architecture with four independently maskable interrupt sources (INT1 to INT4), see Figure 12. Interrupt masking is accomplished by the Interrupt Enable register, IE. The Interrupt Flag register, IFF, signals interrupt requests pending that were generated by the corresponding peripheral.

The interrupt sources operate at a common priority level, meaning that any interrupt service cannot be interrupted by subsequent interrupt requests until it is terminated by a RETI instruction. However, a multi-level interrupt structure can be constructed in software by setting the EA flag during interrupt service.

In the case of simultaneous interrupts (e.g. occurred during the execution of an interrupt service), the interrupt with the lowest vector address will be serviced next. However, at least one instruction of the main program is executed between successive interrupts.

Interrupt INT5 is not assigned to any interrupt vector, however the corresponding bits in the Interrupt Enable (IE) and Interrupt Flag (IFF) registers are used in conjunction with the IDLE mode.

Interrupt vectors INT1 to INT4 are assigned to fixed locations in the Program Memory, see section 9.1.

All interrupts are initially disabled after a device Reset.

Interrupt service is not supported at all while executing from the ROM Library, thus from System Code Memory.

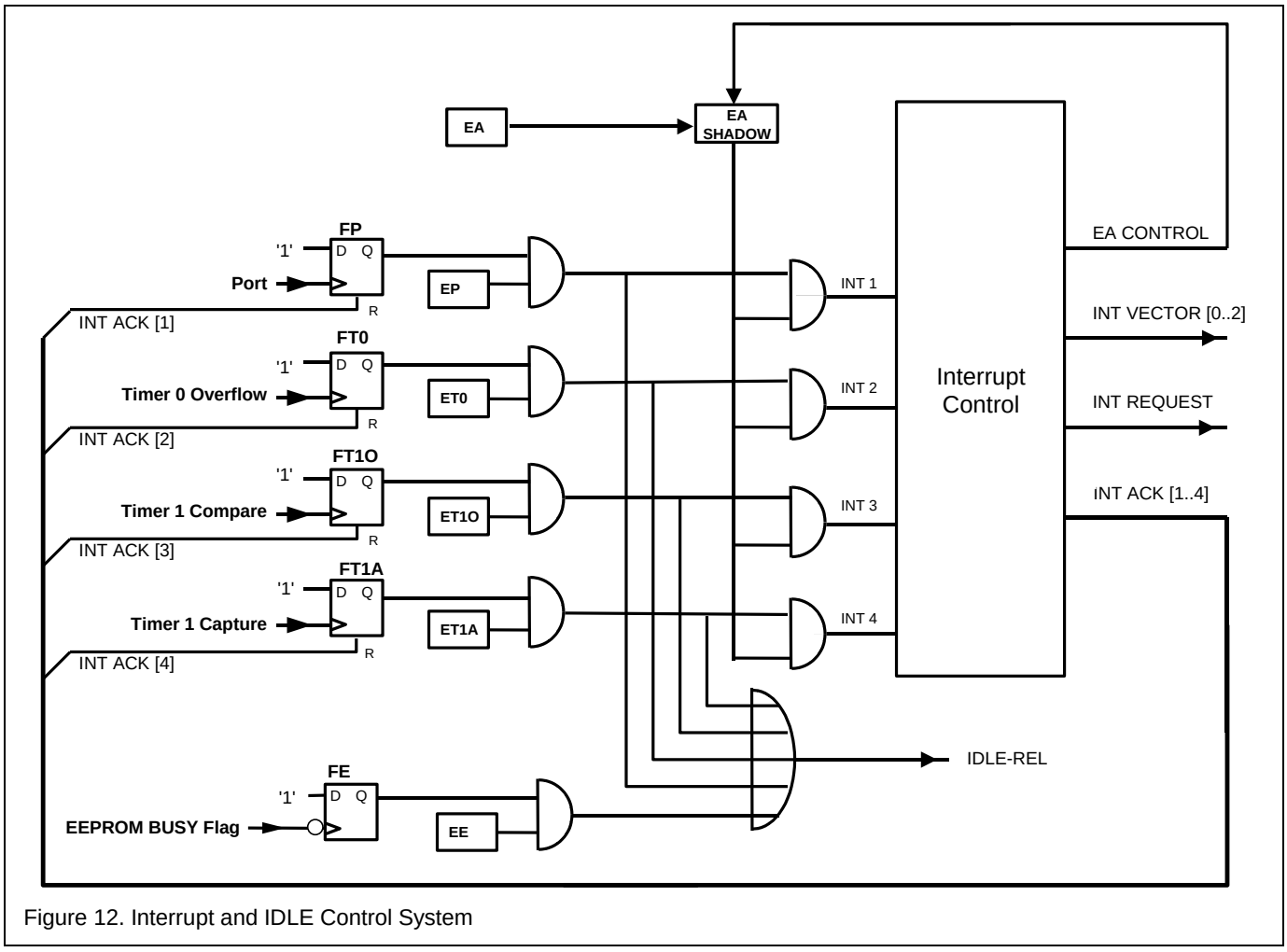


Figure 12. Interrupt and IDLE Control System

10.2.1 Interrupt Enable Register

The Interrupt Enable register, IE, is located in the SFR address space and contains several bits that control the interrupt system to feature interrupt masking, see Table 10.

The control bit EA enables or disables all interrupts. Interrupts will not be serviced while EA is cleared. If EA is set, interrupts are serviced according to the setting of the corresponding interrupt enable bit. In any case, interrupts will be latched until vectored and may alternatively serve to terminate the IDLE mode, if enabled by the corresponding bit, see also section 10.2.5.

Table 10 Interrupt Enable Register, IE

bit 7							bit 0
EA	X	EE	ET1A	ET1O	ET0	EP	X
R/W	W0	R/W	R/W	R/W	R/W	R/W	W0

Note Address = 16H

1. Bits marked ‘X’ are not connected and reserved for future use. Any read operation yields an undefined result. For future compatibility, a write operation should assign a ‘0’.
2. Interrupt service is not available for events assigned to bit EE (INT 5), since this interrupt event is not assigned a vector address.

10.2.2 Interrupt Request Flags

Interrupt requests are latched in corresponding flags of the Interrupt Flag register, IFF, see Table 11.

Table 11 Interrupt Flag Register, IFF

bit 7							bit 0
X	X	FE	FT1A	FT1O	FT0	FP	X
W1	W1	R/0	R/0	R/0	R/0	R/0	W1

Note Address = 17H

1. Bits marked ‘X’ are not connected and reserved for future use. For future compatibility, a write operation should assign a ‘1’.
2. Bits marked ‘R/0’ may be cleared only by a corresponding instruction (INTA). Any set operation does not affect the bit at all.

The corresponding interrupt request flip-flop is cleared automatically when the interrupt is serviced, except for the interrupt flag FE, which serves a dedicated function in the context of IDLE mode release.

10.2.3 Interrupt Source Assignment

The interrupt vectors, located in the Program Memory, are assigned to the sources as listed in Table 12. Since each interrupt vector leaves space for not more than a single instruction, the application program should place a JMP instruction to the address of the actual interrupt service routine. A RETI instruction should be placed instead at all unused vector addresses.

Table 12 Interrupt Source Assignment

Vector	Address	Source	Note
INT 0	0002H	Reserved	
INT 1	0004H	Port	
INT 2	0006H	Timer 0	
INT 3	0008H	Timer 1 Compare	
INT 4	000AH	Timer 1 Capture	
INT 5	000CH	Reserved	
INT 6	000EH	Reserved	

10.2.4 Interrupt Service

Interrupt service is executed as follows. When an interrupt request is detected, the Interrupt Control logic clears the EA SHADOW flag rather than the EA bit itself, to prevent subsequent interrupt requests from being serviced. However, the subsequent interrupt is latched.

The interrupt in service is acknowledged automatically by the Interrupt Control logic, by clearing the corresponding bit in the IFF register. Subsequently, the RISC is forced to perform a CALL instruction to the corresponding vector address. The CALL instruction saves the processor status (Program Counter, PC and Program Status Word, PSW) on the Call Stack.

The Interrupt Service Routine has to terminate, after the request has been processed, by executing a RETI instruction. The RETI instruction restores the program status (PC and PSW), in order to resume program execution at the corresponding location. Subsequently, the Interrupt Logic sets the EA SHADOW flag to enable pending or new interrupts to be serviced.

To enable interrupt nesting, the application program may set the EA flag, during an interrupt service, causing the EA SHADOW flag to be set again, enabling interrupt nesting and service for pending or future interrupts.

10.2.5 IDLE mode

Via the IDLE mode, the device provides additional means for the application program to synchronize with internal or external events. The IDLE mode is entered upon instruction, by setting the control bit IDLE, located in Power Control Register, PCON, see also section 8.4.

Any interrupts that are enabled by setting their corresponding bit in the IE register will terminate IDLE mode and force the device to resume program execution, see Figure 12.

The IDLE mode is typically used alternatively and mutually exclusive to interrupt services. Thus, the Global Interrupt Enable bit EA is cleared in this case and no interrupts are invoked. However, if the control bit EA is set, thus general interrupt service is enabled, the corresponding interrupt will be serviced after termination of the IDLE mode.

However, in any case the device executes the instruction following the one that forced the device into IDLE mode first, before the corresponding interrupt is serviced.

The IDLE mode will not be entered, if the corresponding interrupt flag (IFF) is already set for an interrupt that is enabled, while EA is cleared. Thus, the corresponding bits in the IFF register should be acknowledged prior to IDLE mode invocation. The Interrupt Control logic does not perform this step, because interrupts are not serviced while EA is cleared.

IDLE invocation

The involved steps before and after using the IDLE mode are as follows:

1. The application programs the IE register by clearing the EA bit and setting the corresponding bits of all interrupt sources that shall be able to release the IDLE mode. The same bits in the IFF register should be cleared, in case they are set by unintended interrupt requests that occurred in the past.
2. The application program sets the IDLE bit and enters the IDLE mode.
3. The IDLE control logic detects an enabled interrupt request and clears the IDLE bit, terminating the IDLE mode (wakeup).
4. The application program continues with the instruction that follows the one, which had set the IDLE bit before. If more than one interrupt source was enabled in step 1, the IFF register should be read to determine the source, which has caused the wakeup. In any case, the application program is obliged to clear the corresponding bit in the IFF register to acknowledge the interrupt request. Note that the Interrupt Control logic does not perform this step, because the interrupt has not been processed and vectored in this case (see section 10.2.4).

Clearing of any interrupt request bits should be accomplished by the INTA instruction, while masking all bits with “1” that shall not be affected. The interrupt request bits do not support setting by instruction. A Read-Modify-Write instruction (such as bit manipulation) should not be used, in order to avoid unintentional clearing of interrupt request bits and potential loss of an interrupt event, when latter one occurs after the Read but before the Write phase of the instruction.

10.3 System Clock Generation

The PCF7922 features a versatile system clock generation scheme, for timing purposes and to derive the RISC clock, see Figure 13.

Due to the synchronization ability of the clock generation circuitry, the application program may change the clock configuration at any time “on-the-fly”.

The System Clock Control register is located in the Special Function Register SCSL see Table 13.

Table 13 System Clock Select Register, SCSL

bit 7					bit 2		bit 0
X	X	X	X	X	CSL2	CSL1	CSL0
W0	W0	W0	W0	W0	R/W	R/W	R/W

Note Address = 27H

1. Bits marked ‘X’ are not connected and reserved for future use. Any read operation yields an undefined result. For future compatibility, any write operation should assign a ‘0’.
2. If the control bit CSSL is zero, the state of RCON is irrelevant, since the RC Oscillator is enabled anyway.

Initially after reset, the SCSL register is cleared and the lowest RC Oscillator clock is selected.

CSL[2...0], Clock Select

Typically the RISC clock is derived from an on-chip RC Oscillator (T_{OSC}), which operates at a nominal frequency of 4 MHz and is divided by two, prior to usage for duty cycle reasons. The resulting clock ($T_{OSC,D}$) is fed to a programmable divider, in order to enable clock rate selection for the RISC (T_{CPU}) and its peripherals (T_{SYS}) according to the speed and power consumption requirements of the application program.

The Clock Select control bits, CSL, determine the final system clock, TSYS, according to Table 14.

Table 14 Clock Select, CSL (CSSL = 0)

CSL2	CSL1	CSL0	T_{SYS}	T_{SYS} (typ)	Note
0	0	X	T_{OSC} * 32	8 µs	
0	1	0	T_{OSC} * 16	4 µs	
0	1	1	T_{OSC} * 8	2 µs	
1	0	0	T_{OSC} * 4	1 µs	
1	0	1	T_{OSC} * 2	0,5 µs	
1	1	0	Reserved	Reserved	1
1	1	1	Reserved	Reserved	1

Note

1. Reserved for device test purposes.

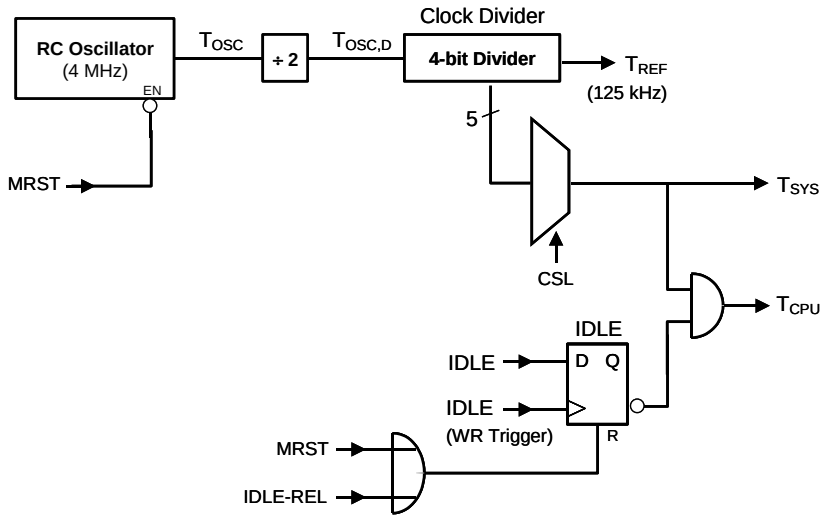


Figure 13. System Clock Generation

IDLE Mode

In IDLE mode the RISC clock (T_{CPU}) is inhibited as long as the control signal IDLE is high, while the clock for peripherals (T_{SYS}) is not affected.

T_{REF}, Reference Clock

For system timing purposes, especially for use with the EEPROM, in order to generate appropriate programming timings, a 125 kHz (TYP) clock reference is derived from the clock source. Anyhow, the reference clock is also available for other peripherals.

In order to meet the circuit requirements regarding the timing derived from the reference clock (T_{REF}) the XTAL Clock (T_{XDCLK}) must satisfy certain requirements as specified, when it is selected as system clock source (CSSL = 1), see section 17.3.

10.4 Timer/Counter 0

Timer/Counter 0 features an asynchronous 8-bit architecture with auto reload and a 6-bit prescaler, Figure 14.

The Timer/Counter 0 control bits are located in the Special Function Register TCON, see Table 15.

Table 15 Timer/counter 0 Control Register, TCON

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
X	TPS2	TPS1	TPS0	TCS1	TCS0	X	TRS0
W0	R/W	R/W	R/W	R/W	R/W	W0	R/W

Note Address = 1AH

1. Bits marked 'X' are not connected and reserved for future use. Any read operation yields an undefined result. For future compatibility, a write operation should assign a '0'.

The timer/counter 0 control register is initially cleared after reset and the timer is stopped.

TCS[1…0], Timer/Counter 0 Clock Source

Timer/Counter 0 can operate as timer or as event counter, depending on the clock source selected by the corresponding control bits TCS, see Table 16.

TPS[2…0], Timer/Counter 0 Prescaler

Timer/Counter 0 features a programmable 6-bit prescaler that provides prescaler values of 2^N for N = 0 to 6, selected by TPS, see Table 17. Writing to and reading from the prescaler is not supported at all.

Table 16 Timer/Counter 0 Clock Source Select, TCS

TCS1	TCS0	Clock Source	Note
0	0	Reference clock, T_{REF}	
0	1	System clock, T_{SYS}	
1	0	Reserved	
1	1	External clock source XEN = 0: External clock/event at Port P15, $P15_{CLK}$ XEN = 1: XTAL Oscillator divided clock, T_{XDCLK}	1

Note

1. The clock source has to fit the requirements as specified by T_{SYS} respectively $P15_{CLK}$.

Table 17 Timer/counter 0 Prescaler Select, TPS

TPS2	TPS1	TPS0	Prescaler Value	Note
0	0	0	1	
0	0	1	2	
0	1	0	4	
0	1	1	8	
1	0	0	16	
1	0	1	32	
1	1	0	64	
1	1	1	reserved	

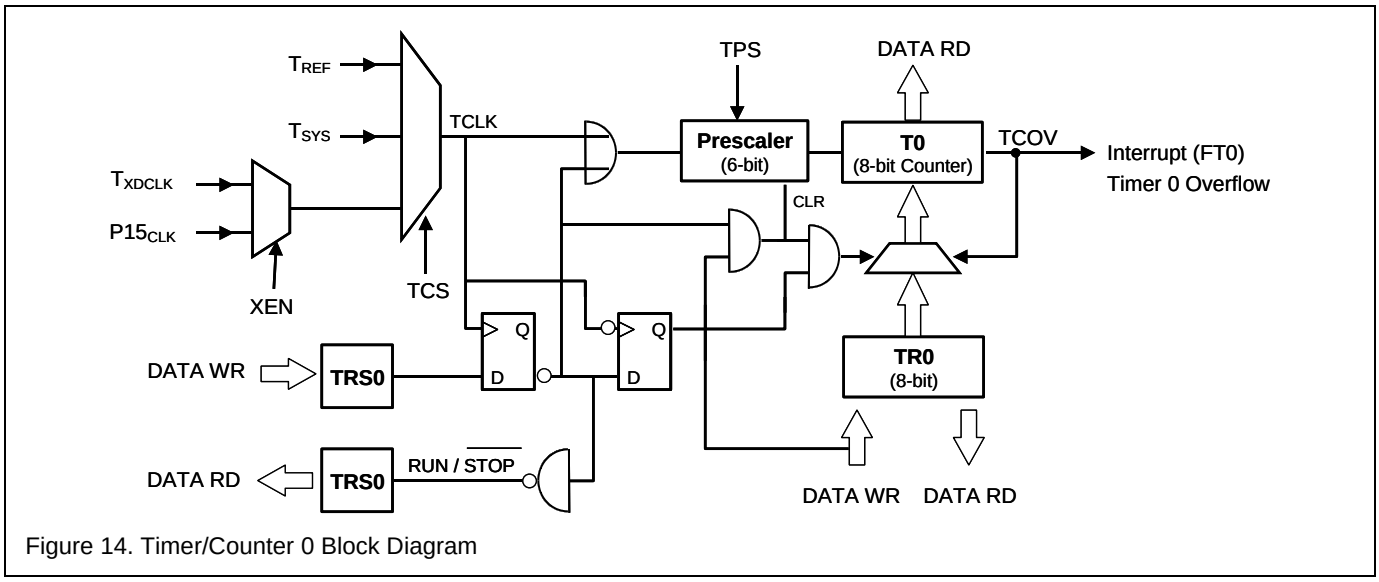


Figure 14. Timer/Counter 0 Block Diagram

TRS0, Timer/Counter 0 Run/Stop

The Run/Stop control bit TRS0 controls the operation of timer/counter 0. A Run/Stop request is synchronized with the clock source (TCLK) and the timer/counter is incremented in response to a rising edge of the clock (TCLK), according to Figure 15.

To force timer/counter 0 into Run mode, a '1' has to be written to the TRS0 flip-flop. To force the Stop mode, a '0' has to be written. The corresponding request is latched upon the next rising edge of the clock signal TCLK and signaled by the Run/Stop mode flip-flop. Subsequent clocks will be recognized respectively ignored by the timer/counter. Please note that the prescaler does not recognize the clock, which acknowledges the RUN mode, while it does recognize the clock, which acknowledges the STOP mode, Figure 15.

Anyhow, the counter and prescaler states are not changed in Stop mode. Reading the control bit TRS0 signals, if timer/counter 0 is running or stopped.

Upon overflow of the Timer/Counter register T0, the Timer/Counter 0 interrupt request flag FT0 is set. At the same time, the timer/counter register is overwritten with the value stored in the timer/counter reload register TR0.

TR0, Timer/Counter 0 Reload

The Timer/Counter reload register, TR0, is located in the SFR address range and available for reading and writing.

In case Timer/Counter 0 is stopped (TRS0 = 0), writing to TR0 will clear the prescaler and affect register T0, since T0 does receive a copy of the value loaded into TR0.

If the Timer/Counter is running (TRS0 =1), writing to TR0 has no effect.

T0, Timer/Counter 0 Counter Register

The timer/counter register, T0, is located in the SFR address range and available for reading only. A write operation has no effect. The timer/counter register, T0, may be initialized via the reload register TR0 only.

It is important to notice that the system clock (instruction clock) and timer/counter 0 clock may be asynchronous to each other, depending on the selected clock sources. Thus reading from T0 by software may happen at the exact moment in which the timer/counter is incremented. In such a case, the read value may be undefined. Thus, the timer/counter should be stopped before reading T0. Alternatively, successive readings of T0 should be performed in order to verify the read results against each other.

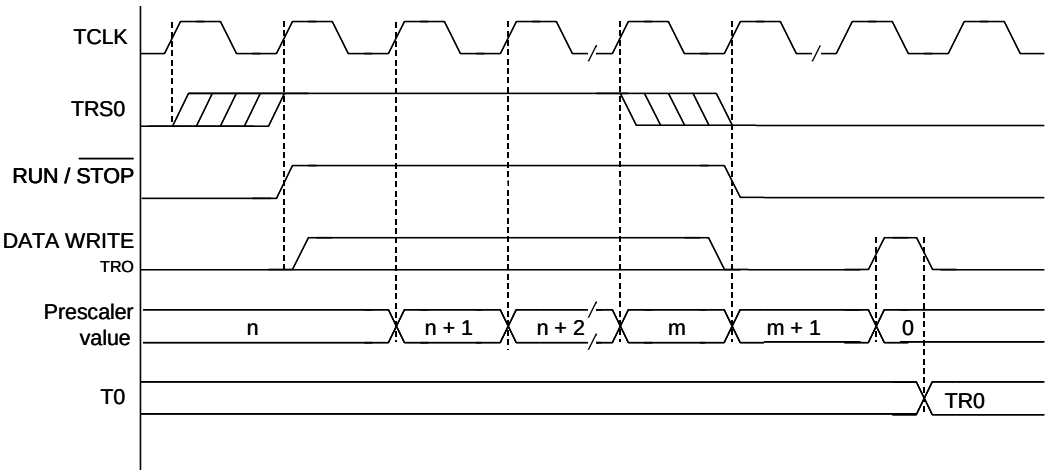


Figure 15. Timer/Counter 0 Timing

10.5 Timer/Counter 1

Timer/Counter 1 features an 8-bit architecture with 7-bit prescaler, Capture/Compare, Auto-Reset and Pulse Width Modulation circuitry, Figure 16 and Figure 20.

The timer/counter 1 control bits are located in the Special Function Register T1CON1 and T1CON2, see Table 18 and Table 19.

Table 18 Timer/counter 1 Control Register, T1CON1

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
T1RUN	T1RES	T1RC	T1OTC	T1CF	T1CR	T1CSS	T1CM
R/W	R0/W1	R0/W1	R/W	R/W	R/W	R/W	R/W

Address = 28H

Table 19 Timer/counter 1 Control Register, T1CON2

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
T1PWM	T1RCAP	T1RCMP	T1S2	T1S1	T1S0	T1CLS1	T1CLS0
R/W	R0/W	R/W	R/W	R/W	R/W	R/W	R/W

Address = 29_H

Notice that the prescaler and Timer 1 register can not be accessed directly, instead, may be cleared upon instruction only. However, the Timer 1 register value may be captured upon instruction, any time desired.

T1CLS[1,0], Timer/Counter 1 Clock Source

Timer/counter 1 can operate as timer or as event counter, depending on the clock source selected by the corresponding control bits T1CLS, see Table 20.

Table 20 Timer/Counter 1 Clock Source Select, T1CLS

T1CLS1	T1CLS0	Clock Source	Note
0	0	Reference clock, T_{REF}	
0	1	4MHz RC Oscillator clock, T_{OSC}	
1	0	Reserved	
1	1	External clock source XEN = 0: External clock/event at Port P15, $P15_{CLK}$ XEN = 1: XTAL Oscillator divided clock, T_{XDCLK}	1

Note

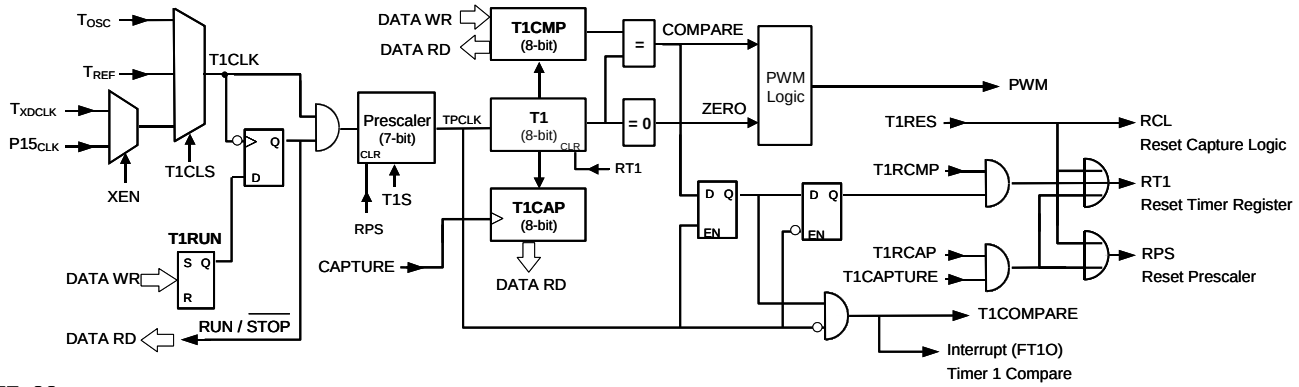
1. The clock source has to fit the requirements as specified by T_{SYS} respectively $P15_{CLK}$.

T1S[2…0], Timer/Counter 1 Prescaler Select

Timer/counter 1 features a programmable 7-bit prescaler that provides prescaler values of 2^N for N = 0 to 7, selected by T1S, see Table 21. Writing to and reading from the prescaler counter is not supported at all.

Table 21 Timer/counter 1 Prescaler Select, T1S

T1S2	T1S1	T1S0	Prescaler Value	Note
0	0	0	1	
0	0	1	2	
0	1	0	4	
0	1	1	8	
1	0	0	16	
1	0	1	32	
1	1	0	64	
1	1	1	128	



PCF7x22

Figure 16. Timer/Counter 1 and Auto-Reset Block Diagram

T1RUN, Timer/Counter 1 Run/Stop

The Run/Stop control bit T1RUN controls the operation of timer/counter 1. A Run/Stop request is synchronized with the clock source (T1CLK) and the timer/counter is incremented in response to a rising edge of the clock (T1CLK), according to Figure 17.

To force timer/counter 1 into Run mode, a '1' has to be written to the T1RUN flip-flop. To force the Stop mode, a '0' has to be written. With the next falling edge of the clock signal T1CLK, the timer/counter will enter the requested mode, which is signaled by the Run/Stop mode flip-flop. Subsequent clocks will be recognized respectively ignored by the timer/counter. Anyhow, the counter and prescaler state are not changed in Stop mode. Reading the control bit T1RUN signals, if timer/counter 1 is running or stopped.

T1CMP, Timer/Counter 1 Compare Register

The value stored in the Timer/counter 1 Compare register, T1CMP, is continuously compared against the Timer/Counter 1 value, T1. If equal a "COMPARE" signal is generated to trigger the interrupt request Timer 1 Compare (FT1O), as well as to serve as input for the Pulse Width Modulation, PWM, and Auto-Reset Logic. According to Figure 18, the interrupt is triggered upon the falling edge of the Timer/Counter clock (T1CLK).

Similarly the Timer/Counter 1 value is continuously compared against "ZERO" and a corresponding signal generated for use with the Pulse Width Modulation, PWM, Logic.

The Timer/counter 1 Compare register, T1CMP, is located in the SFR address range and available for reading and writing.

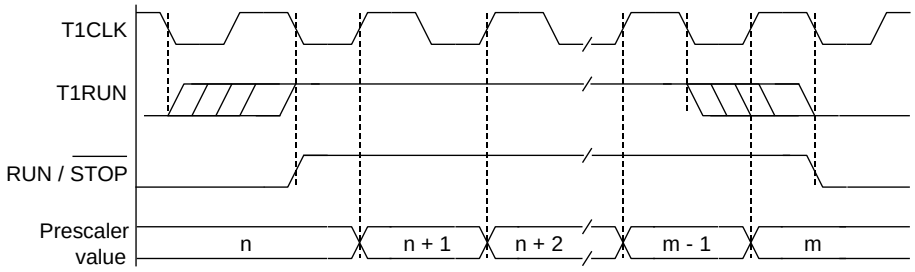


Figure 17. Timer/Counter 1 Timing

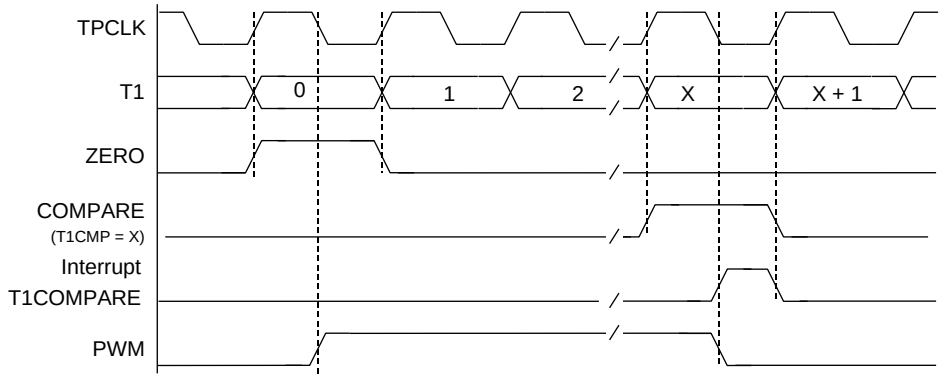


Figure 18. Timer/Counter 1 Compare and PWM timing

T1PWM, Timer/Counter 1 Pulse Width Modulation Control

Setting the control bit T1PWM enables the PWM Logic and causes the direction flip-flop of port P22 to be overruled, forcing the port P22 to be configured for output mode, see Figure 19.

The state of P22 is defined by the XOR function of the output bit of P22 (P22) and the logical level of the PWM signal. The PWM signal is set upon “ZERO” and cleared upon “COMPARE”. Latter one is assigned priority in case “ZERO” also is applicable in that moment, see Figure 18.

Hence, the pulse width is determined according to the value of T1CMP, featuring a range of 0/256 to 255/256. Consequently, when T1CMP is set to 00h, PWM yields always ‘0’.

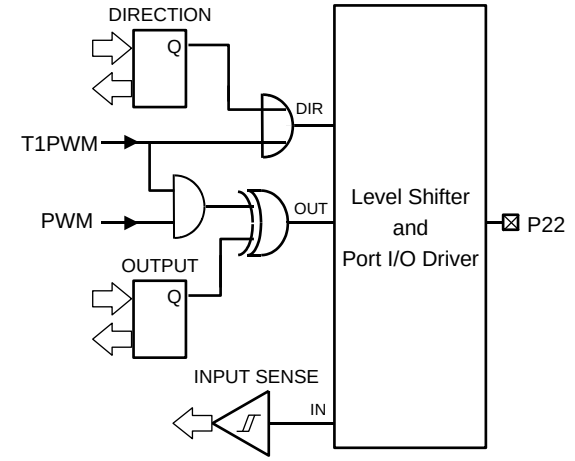


Figure 19. PWM Control

T1CAP, Timer/Counter 1 Capture Register

Timer/counter 1 features an 8-bit capture register, T1CAP, able to capture the current Timer/Counter value in response to a capture request (CAPTURE) as generated by the Timer/Counter 1 Capture Logic, see Figure 20.

The capture trigger (CAPTRG) can be derived from a number of sources and events, and in such an event, the interrupt request Timer 1 Capture (FT1A) is triggered. However, forcing a Manual Capture by instruction, will not trigger the interrupt, see Figure 21

The Timer/counter 1 capture register, T1CAP, is located in the SFR address range and available for reading only.

T1CSS, Timer/Counter 1 Capture Source Select

The capture event may be derived from port P2, as selected by the control bit T1CSS, see Table 22.

Table 22 Timer/Counter 1 Capture Source Select, T1CSS

T1CSS	Capture Source	Note
0	Reserved	
1	Port P2 (P21 respectively P26I)	2

Note

1. Writing to T1CSS, while the timer is running (T1RUN reads '1'), is not recommended, because it may generate a malicious capture event.
2. As a function of the control bit P2CIS, either P21 or P26I is used as Capture Source input, see section 0.

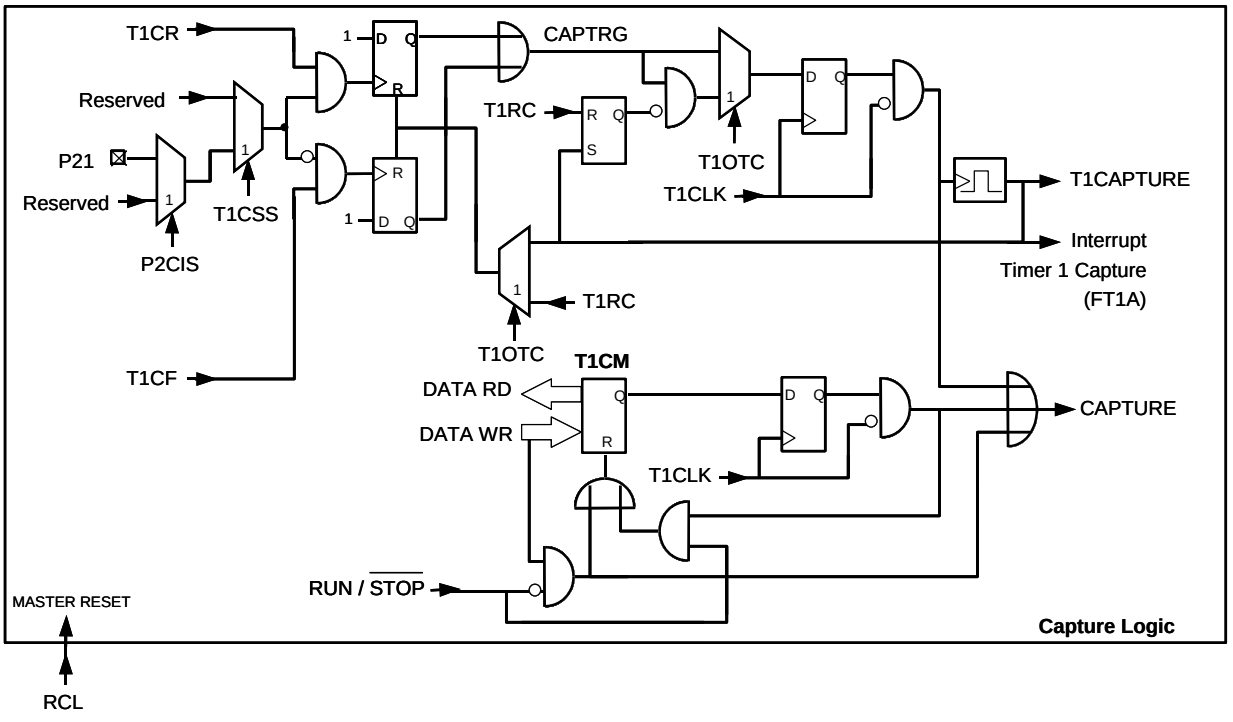


Figure 20. Timer/Counter 1 Capture Logic

T1CR and T1CF, Timer/Counter 1 Capture Configuration

The capture event may be configured to occur on the rising and/or falling edge of the capture source, as selected by the control bit T1CR and T1CF, see Table 23.

If both control bits are set, a capture trigger will be generated upon any change of the input signal.

Due to synchronization of the capture input signals with the timer clock (T1CLK), the repetition rate of the capture events is limited accordingly.

Table 23 Timer/Counter 1 Capture Enable

	Capture Event Configuration	Note
T1CR	Capture on rising edge ('0' -> '1')	1
T1CF	Capture on falling edge ('1' -> '0')	1

Note

1. Writing a ‘1’ to T1CR or T1CF while the timer is running (T1RUN reads ‘1’) is not recommended, and may generate a malicious capture event.

T1CM, Timer/Counter 1 Capture Manual

A capture operation may be requested manually at any time as desired, by writing a ‘1’ to the control bit T1CM, in order to read the current value of the Timer/Counter 1 register, T1, in RUN or STOP mode. As direct reading of the Timer/Counter 1 register is not supported, Capture Manual is the only means to read the Timer/Counter 1 register.

Once set by the application, T1CM will stay '1' until the capture request has been executed, causing the control bit to be cleared. Thus, T1CM can be polled by the application to verify, if the capture request has been carried out. However, T1CM may be cleared any time, by writing a ‘0’ to it, see Figure 21.

Note that operating the control bit T1CM does not trigger a Timer/Counter Reset Upon Capture nor the Timer 1 Capture interrupt.

T1OTC, Timer/Counter 1 One Time Capture

The Timer/counter 1 Capture feature supports 'Single-Shot’ operation, which is enabled by setting the control bit T1OTC. In this case, the capture logic can be triggered “One-Time” only and locks itself, ignoring subsequent events. The capture logic may be unlocked any time, by writing a '1' to the control bit T1RC, see Figure 21.

The 'Single-Shot’ operation is useful to ensure that a capture event is processed properly, e.g. the correct reading is taken from the capture register. In continuous capture mode, a second capture event may cause a new capture value to be stored in the T1CAP register, before the first value has been read out.

T1RC, Timer/Counter 1 Reset Capture

In case the capture logic has been trigged, when operating in Single-Shot mode (T1OTC = 1), the capture logic may be unlocked at any time, by writing a '1' to the control bit T1RC. Writing a '0' to bit T1RC has no effect. T1RC is not latched internally, thus reading from it always yields ‘0’.

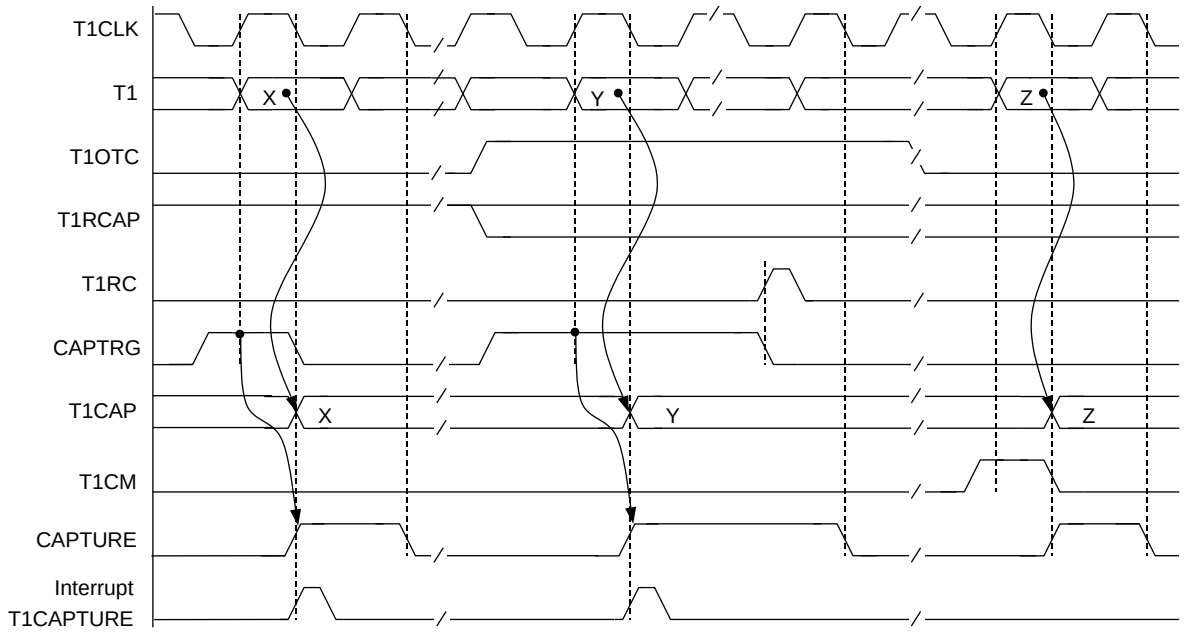


Figure 21. Timer/Counter 1 Capture Logic Timing

T1RES, Timer/Counter 1 Reset

The control bit T1RES provides means to manually reset the Timer/Counter 1 at any time as desired. As the timer/counter RUN/STOP logic is not affected, this feature must not be triggered, as long as the Timer/Counter 1 is in RUN mode. Otherwise, the Timer/Counter registers may hold an undefined value afterwards, because this feature is not synchronized with the Timer/Counter clock. Thus, the Timer/Counter 1 shall be forced into STOP mode, before triggering the control bit T1RES.

Writing a '1' to the control bit T1RES clears the register Timer/Counter 1 (T1), the prescaler and resets the Capture Logic. However, the output state of the PWM circuitry (PWM) will depend on the actual compare register value (T1CMP), see T1PWM, Timer/Counter 1 Pulse Width Modulation . Writing a '0' to bit T1RES has no effect. T1RES is not latched internally; reading from it always yields ‘0’.

T1RCMP, Timer/Counter 1 Reset Upon Compare

Setting the control bit T1RCMP to '1' enables the "Reset Upon Compare" feature. When set, the Timer/Counter register (T1) is cleared, whenever a compare match is detected. Latter one applies, when the Timer/Counter register (T1) equals the Compare Register (T1CMP).

The clear operation is synchronized with the clock that is provided by the prescaler (TPCLK), see Figure 22.

Consequently, the Timer/Counter 1 features a compare match repetition rate equal to [T1CMP + 1] clocks.

T1RCAP, Timer/Counter 1 Reset Upon Capture

Setting the control bit T1RCAP to '1' enables the "Reset Upon Capture" feature. When set, the Timer/Counter register (T1) and the prescaler are cleared, whenever a capture event is detected, see Figure 23.

However, the capture operation will not be affected and completed properly, before the Timer/Counter register (T1) is cleared. Writing a '0' to bit T1RCAP has no effect.

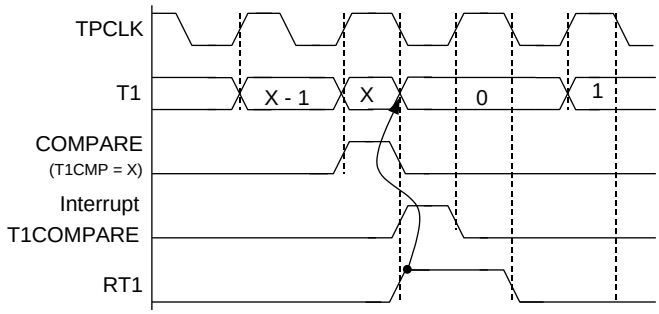


Figure 22. Timer/Counter 1 Reset Upon Compare Timing

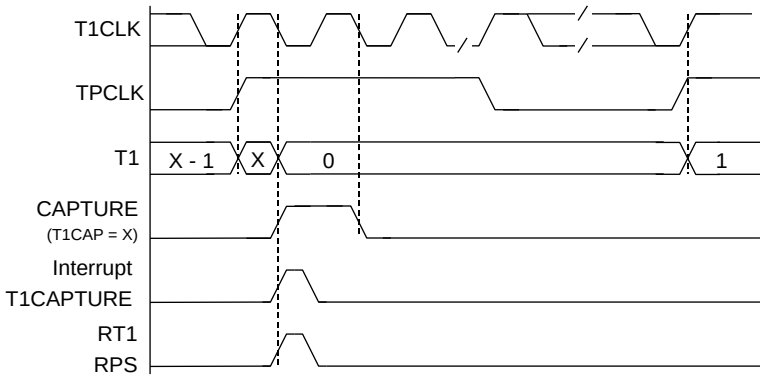


Figure 23. Timer/Counter 1 Reset Upon Capture Timing

10.6 Watchdog Timer, WT

The device incorporates a watchdog timer, WT, to recover the system from situations, in which the application program has run into a deadlock situation. This avoids that the connected battery is drained unnecessarily.

The watchdog timer consists of a programmable 8-bit prescaler and 8-bit main timer, WT, clocked from the reference clock (T_{ref}, see section 10.2), according to Figure 24.

The watchdog timer is always active when the device operates in BATTERY mode (PMODE = 1).

When the watchdog is not continuously restarted and allowed to timeout, it will force the Supply Switch logic to open the Supply Switch (PMODE = 0), see also section 8.1 (Figure 4). Consequently, the device is forced into POWER-OFF Mode.

The watchdog timer control bits are located in the Special Function Register WTCON, see Table 24.

Table 24 Watchdog Timer Control Register, WTCON

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
X	WPS2	WPS1	WPS0	X	X	X	WCLR
W0	R/W	R/W	R/W	W0	W0	W0	R0/W1

Note Address = 1BH

1. Bits marked ‘X’ are not connected and reserved for future use. Any read operation yields an undefined result. For future compatibility, a write operation should assign a ‘0’.
2. Reading of the bit WCLR yields a ‘0’.

Initially after reset, the WTCON register is cleared, which configures the longest possible timeout period.

WPS[2…0], Watchdog Prescaler Select

The Watchdog main counter is clocked by a tap taken from the prescaler, according to Table 25.

Table 25 Watchdog Prescaler Select, WPS

WPS2	WPS1	WPS0	Prescaler Ratio	Note
0	0	0	256	
0	0	1	128	
0	1	0	64	
0	1	1	32	
1	0	0	16	
1	0	1	8	
1	1	0	4	
1	1	1	2	

WCLR, Watchdog Clear

To prevent the Watchdog Timer from overflowing, a ‘1’ has to be written periodically to the control bit WCLR by the application program. Writing a ‘0’ to WCLR has no effect. WCLR is not latched internally and reading from it always yields ‘0’.

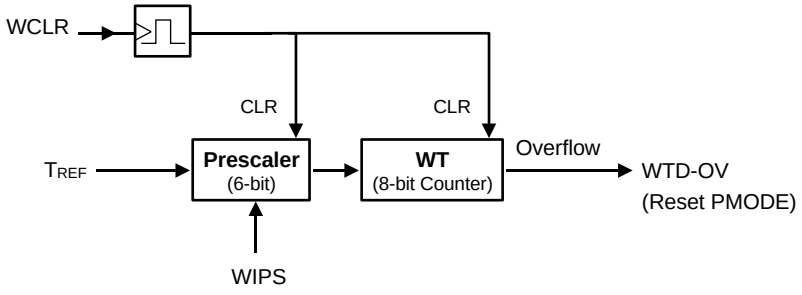


Figure 24. Watchdog Timer Block Diagram

10.7 I/O Ports

The device incorporates two quasi-identical I/O port structures, Port 1 and Port 2, with in total 14 port lines. The ports serve as button inputs (device Wake Up), control external peripherals and partly provide extended functions. In case of the package version TSSOP20 only seven of the 14 I/O ports are available externally.

Port 1 consists of eight independently configurable bi-directional ports. According to Figure 25a, the port lines are configured in “push-pull” fashion, when used in output mode. Port P10, P11, P14, P15 and P16 may serve as button input (device Wake Up) and partly feature on-chip pull-up resistors, see also section 8.3.

Port 2 consists of six I/O lines, featuring five independently configurable bi-directional port lines (P20 to P24). According to Figure 25a, the port lines are configured in “push-pull” fashion, when used in output mode. Port P21 and P22 may serve as button input (device Wake Up). Port P20, P21, P23 and P24 features on-chip switch able pull-up resistors, which are only active, if the corresponding port line operates in input mode.

In addition Port 2 provides one directional port line (P26ON) that assembles a dedicated output port line. According to Figure 25b, the output function is configured for open-drain and features an extended output voltage HIGH specification (V_{OH}).

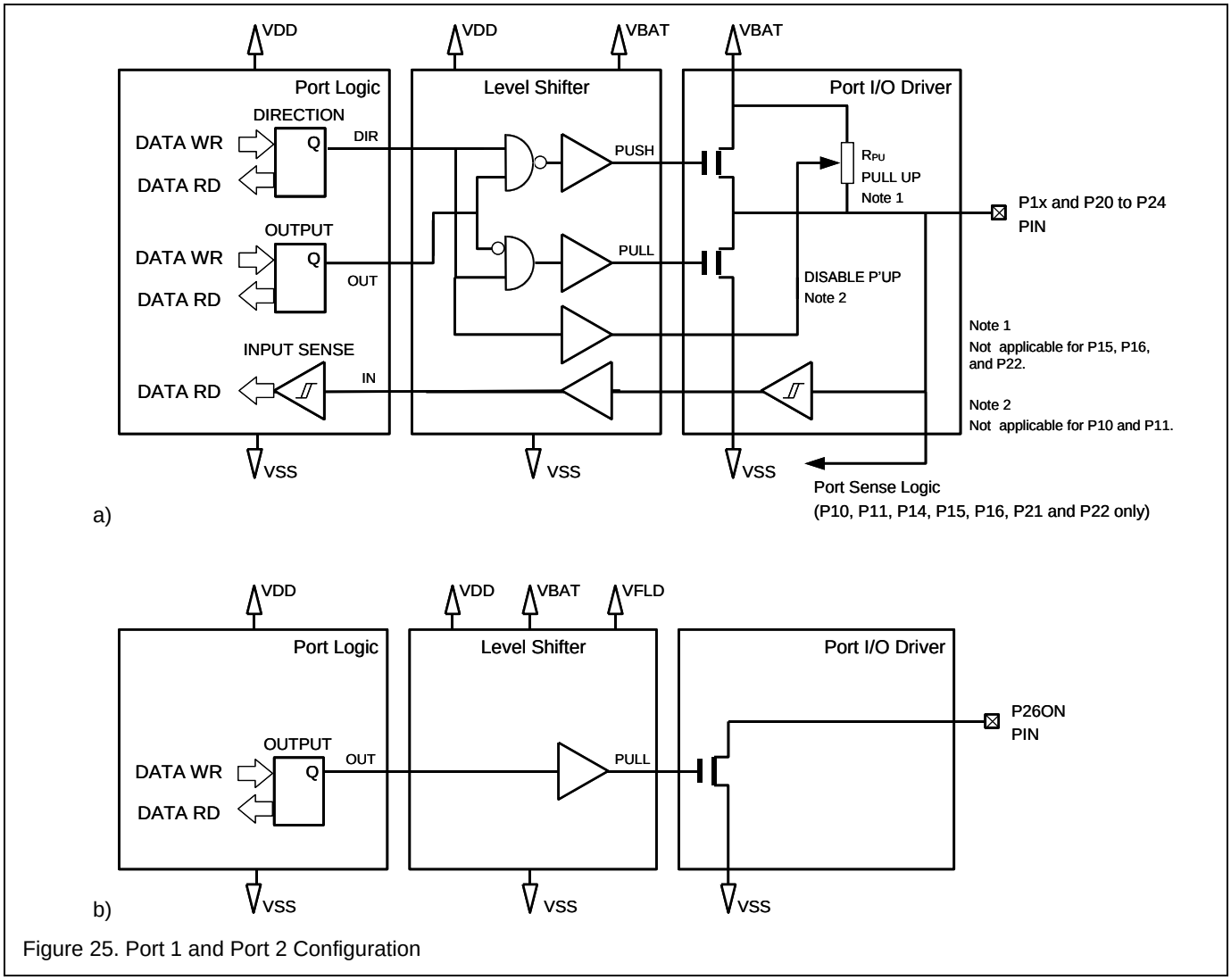


Figure 25. Port 1 and Port 2 Configuration

Configuration of and access to the I/O Ports is provided by means of a Direction, Output and Input Sense Register located in the Special Function Register range, see below.

When configured for input mode, floating port terminals must be avoided and external pull-up or pull-down means eventually need to be provided accordingly. During device Reset and POWER-OFF mode, the port direction and output flip-flops are cleared, automatically configuring all port lines for input. In this situation, ports P15, P16 and P22 must feature external pull-down or pull-up measures to VSS or VBAT. The remaining ports feature on-chip measures. However, pull-down measures for P15, P16 and P22 must be considered carefully, as an undesired device wake up may occur when the device is about to enter POWER-OFF mode, see section 21.5.

Although of generic nature and fully controlled by the application program, some I/O lines feature extended control functions according to Table 26.

P10, P11, P14 to P16, P21 and P22, Wake-Up Sense and Port Interrupt

The port lines P10, P11, P14 to P16, P21 and P22 are connected to the Port Sense Logic and may serve as button inputs for device wake-up. Thus, provide means to release the device from POWER-OFF mode, in response to a high-to-low transition, see section 8.3.

Apart from the device wake up function, these ports may also be used to trigger a port interrupt during program execution. Subsequent port polling might be required to distinguish between button activation and port interrupt.

P15, External Clock Input

Port line P15 may serve as an external clock input in combination with Timer/Counter 0 and Timer/Counter 1, see section 10.4 respectively section 10.5. If used for this purpose, P15 should be operated in input mode only, to avoid unintentional short circuit conditions. The Port Interrupt feature (Port Sense Logic) will be disabled accordingly, see section 8.3.

P16, Voltage Comparator Input

Port line P16 may serve as analog input for the on-chip voltage comparator. If used for this purpose, the port I/O driver, input sense control will be overruled and the Port Interrupt feature (Port Sense Logic) will be disabled accordingly, see section 10.9 and 8.3.

P17, P20, Digital Modulator Output

The port lines P17 and P20 may be controlled from the on-chip digital modulator circuitry that supports signal train generation, e.g. Manchester/Bi-Phase, etc.. If used for this purpose, the port direction control will be overruled accordingly, see section 10.7.

P21, Timer 1 Capture Trigger Input

Port line P21 may serve as external Capture trigger input in combination with Timer/Counter 1, or alternatively as external interrupt input utilizing the Capture Interrupt vector, see section 10.5.

In this case, Port P21 should be operated in input mode only, to avoid unintentional short circuit conditions. The Port Interrupt feature (Port Sense Logic) may be disabled by the control bit P21WD as desired, see section 0.

P22, Timer 1 PWM Output

Port line P22 may serve as Pulse Width Modulator (PWM) output in combination with Timer/Counter 1. If used for this purpose, the port direction control will be overruled and the Port Interrupt feature (Port Sense Logic) will be disabled accordingly, see section 10.5 and 8.3.

Table 26 Port configuration and function assignment

Port Feature	Port 1								Port 2						Note
	10	11	12	13	14	15	16	17	20	21	22	23	24	26ON	
Internal Pull Up (Down)	•	•													
Internal switch able Pull Up			•	•	•			•	•	•		•	•		1
Wake Up Sense / Port Interrupt	•	•			•	•	•			•	•				
Voltage Comparator Input							•								
Digital Modulator Output								•	•						
Timer 1 Capture Trigger External Interrupt										•					
Timer 1 PWM Output											•				
External Clock Input						•									

Note

1. Active only, if the port line operates in input mode.

10.7.1 PxDIR, Port Direction Control

All port lines may be configured independently for input or output, as defined by the Special Function Register Port Direction, see Table 27 and Table 28.

Table 27 P1 Direction Register, P1DIR

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
IO17	IO16	IO15	IO14	IO13	IO12	IO11	IO10
R/W	R/W	R/W	R/W	R/w	R/W	R/W	R/W

Address = 22H

Table 28 P2 Direction Register, P2DIR

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
P21WD	P2CIS	X	IO24	IO23	IO22	IO21	IO20
R/W	W0	W0	R/W	R/W	R/W	R/W	R/W

Note Address = 25H

1 Bits marked ‘X’ are not connected and reserved for future use. Any read operation yields an undefined result. For future compatibility, a write operation should assign a ‘0’.

IO2x, Port Direction Control

If the corresponding direction bit is set, the port line is configured for output and the corresponding port I/O driver forces the port line high or low, depending on the state of the output flip-flop. If the corresponding direction bit is cleared, the I/O port driver is configured for input and the corresponding PUSH-PULL stage is forced into tri-state.

As mentioned above, the port direction control bit is overruled by other peripherals under certain condition, see section 10.7.

P21WD, Port 21 Wake Up Disable

When set to ‘1’, the control bit P21WD provides means to inhibit Port Interrupt generation for Port 21, during device operation, see also section 8.3. This feature is useful, in case Port 21 serves as trigger input for the Timer/Counter 1 Capture function, see also section 10.5.

However, P21WD is cleared, while the device resides in POWER-OFF mode. Thus, Port 21 supports device Wake Up in any case. The control bit P21WD is located in the Port 2 Direction register, P2DIR.

P2CIS, Port 2 Capture Input Source

The control bit P2SCI serves the function to select the port line that is used as Capture Source input for Timer/Counter 1, in case the Capture event shall be derived from Port 2 (T1CSS = 1, see section 10.5).

P2CIS must not be set to ‘1’, as this mode is reserved for compatibility reasons. Instead, P2CIS shall be set to ‘0’, in order to select P21 as Capture Source input.

10.7.2 PxOUT, Port Output Control

The port output flip-flop controls the state of the corresponding port line, if latter one is configured for output mode. Any read operation from the port output flip-flop will be executed by sampling the state of the flip-flop rather than the state of the port line.

The port output register are located in the Special Function Register range, see Table 29and Table 30.

Table 29 P1 Output Register, P1OUT

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
P17	P16	P15	P14	P13	P12	P11	P10
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address = 20H

Table 30 P2 Output Register, P2OUT

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
X	P26	X	P24	P23	P22	P21	P20
W0	W0	W0	W0	W0	R/W	R/W	R/W

Note Address = 23H

1 Bits marked ‘X’ are not connected and reserved for future use. Any read operation yields an undefined result. For future compatibility, a write operation should assign a ‘0’.

10.7.3 PxINS, Port Input Sense

Reading from the port lines is accomplished by means of the Special Function Register Port Input Sense, see Table 31 and Table 32.

Table 31 P1 Input Sense Register, P1INS

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
P17S	P16S	P15S	P14S	P13S	P12S	P11S	P10S
R	R	R	R	R	R	R	R

Address = 21H

Table 32 P2 Input Sense Register, P2INS

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
X	X	X	P24S	P23S	P22S	P21S	P20S
					R	R	R

Note Address = 24H

1. Bits marked ‘X’ are not connected and reserved for future use.

P1INS and P2INS directly sense the port pin and return the corresponding states of the I/O lines, see Figure 25.

10.8 Digital Modulator

The device features an on-chip digital modulator circuitry, for use with the port lines P17 and P20 or the UHF Transmitter in the context of FSK and ASK modulation of the UHF carrier, see Figure 26.

The digital modulator supports signal train generation, e.g. with Manchester/BiPhase or Pulse Width coding, provides a bit buffer and features a sub-carrier mode. Digital modulator operation is configured by the control bits located in the Special Function Register MODCON, see Table 33.

Table 33 Modulator Control Register, MODCON

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
MDB	EFM	EAM	TSEL	SCEN	EP17	EP20	X
R/W	R/W	R/W	R/W	R/W	R/W	R/W	W0

Note Address = 1DH

1. Bits marked ‘X’ are not connected and reserved for future use. Any read operation yields an undefined result. For future compatibility, a write operation should assign a ‘0’.

Initially after reset, the Modulator Control register, MODCON, is cleared, disabling the modulator by default.

EP17, Enable P17

Setting the control bit EP17 will force the Port P17 into output mode. The port output state is determined by the XOR function of the modulator output and the port data output flip-flop, establishing the desired port state before and after modulator operation.

EP20, Enable P20

Setting the control bit EP20 will force the Port P20 into output mode. The port output state is determined by the XOR function of the modulator output and the port data output flip-flop, establishing the desired port state before and after modulator operation.

EAM, Enable Amplitude Modulation

Setting the control bit EAM provide means for ASK modulation of the UHF Transmitter, in accordance with the control signal AMOUT, see also 11.4.3.

EFM, Enable Frequency Modulation

Setting the control bit EFM provide means for FSK modulation of the UHF Transmitter, in accordance with the control signal FMOUT, see also section 11.4.2.

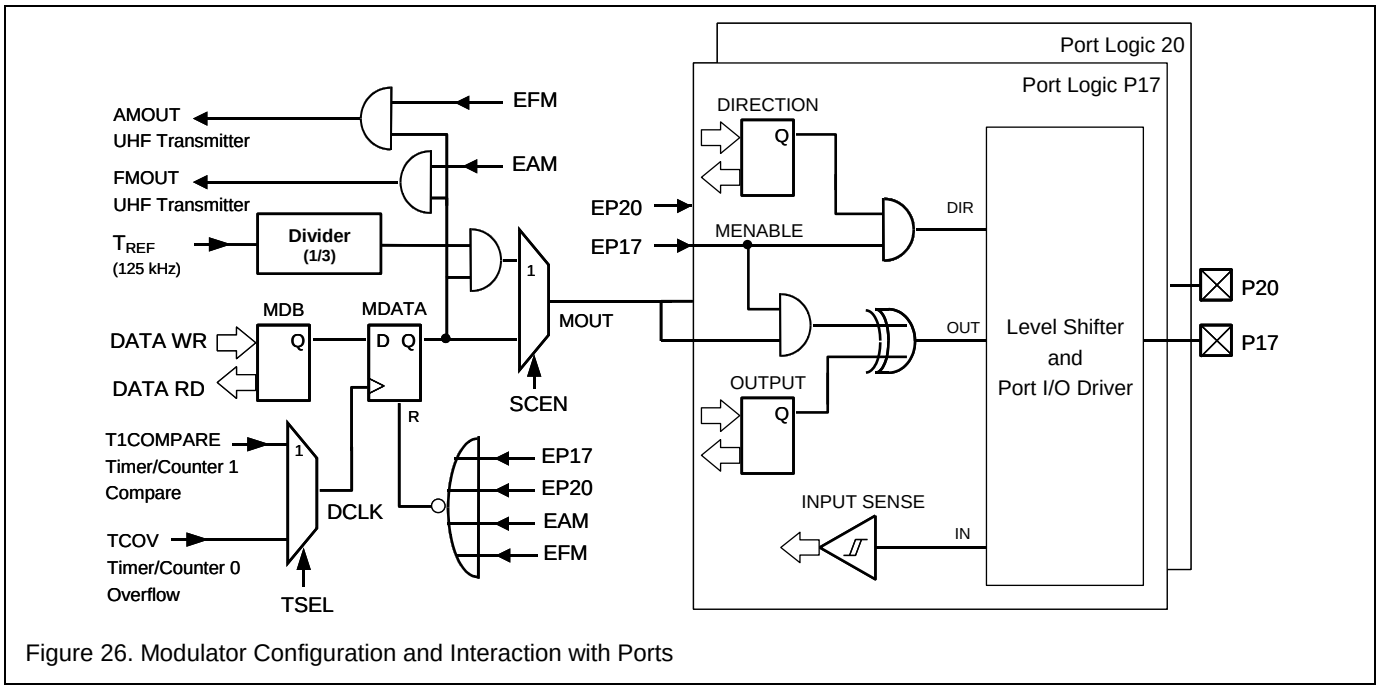


Figure 26. Modulator Configuration and Interaction with Ports

TSEL, Timer Select

The digital modulator data clock (DCLK) is derived from either the Timer/Counter 0 overflow event (see section 10.4) or from the Timer/Counter 1 Compare match (see section 10.5). The corresponding clock source is selected by TSEL, according to Table 34.

Table 34 Modulator Timer Select, TSEL

TSEL	Used clock	Note
0	Timer/Counter 0 Overflow	
1	Timer/Counter 1 Compare match	

MDB, Modulator Data Bit

The modulator data flip-flop is clocked by the data clock (DCLK) as selected, and in response to a rising edge it latches the data stored in the Modulator Data Buffer, MDB. Subsequently, the corresponding Timer/Counter interrupt service routine shall serve the Modulator Data Buffer with the bit value designated to be output upon the next clock cycle, see Figure 27.

In case Manchester coding shall be implemented, the Timer/Counter consequently need to be operated at twice the desired bit rate.

The data flip-flop MDATA is cleared, in case neither port P17 (EP17) nor P20 (EP20) nor the UHF Transmitter (EAM, EFM) are controlled by the modulator.

SCEN, Sub-Carrier Enable

The modulator circuitry features a sub-carrier mode, that can be applied for the signal train generated at port P17 or P20, e.g. for use with Infra-Red transmissions. The sub-carrier is enabled, if the control bit SCEN is set. The sub-carrier is derived from the reference clock by division by three and features a duty cycle of 33%. However, is not synchronized with the bit clock (DCLK), see Figure 28.

The SCEN bit should be cleared while the modulator is not used, in order to minimize power consumption.

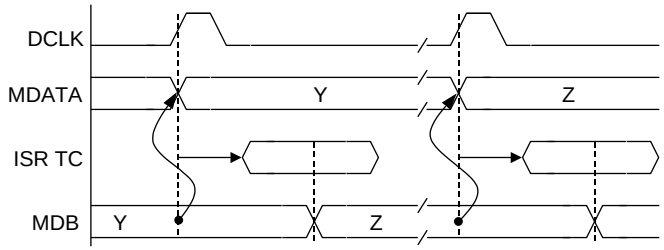


Figure 27. Port Modulator Timing

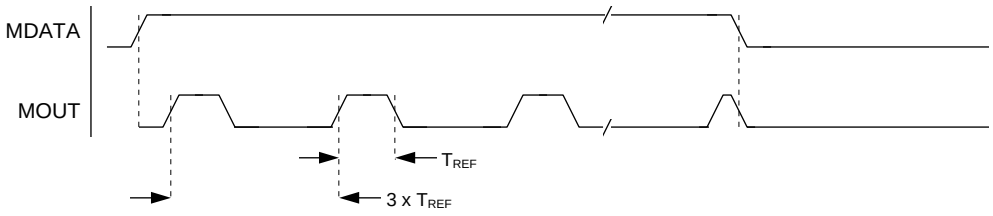


Figure 28. Sub-carrier Timing

10.9 Voltage Comparator

The device features a voltage comparator with programmable and temperature stabilized reference voltage that is able to monitor the battery supply voltage or a voltage from an external source applied to port P16, see Figure 30.

Utilizing the scheme of a programmable reference voltage and subsequent comparator, an A/D conversion employing the method of successive approximation can be implemented. Latter one is readily available as a library function provided by firmware ROM, see section 22.

The voltage comparator is controlled via the Special Function Register VCON, Table 35.

Table 35 Voltage Comparator Control, VCON

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VCMP	VSEN	ISEL	X	VST3	VST2	VST1	VST0
R	R/W	R/W	W0	R/W	R/W	R/W	R/W

Note Address = 2FH

1. Bits marked ‘X’ are not connected and reserved for future use. Any read operation yields an undefined result. For future compatibility, a write operation should assign a ‘0’.

VSEN, Voltage Comparator Enable

The voltage comparator is enabled by setting the control bit VSEN. The circuitry needs to settle (t_{RSET}), before the status bit VCMP provides a valid result, see Figure 31.

For power consumption reasons, VSEN should be cleared while operation of the voltage comparator is not required.

ISEL, Input Select

The control bit ISEL provides means to either monitor the battery voltage or a voltage from an external source applied to port P16, see Table 36.

Table 36 Voltage Comparator Input Select, ISEL

ISEL	Source	Note
0	VBAT pin	
1	Port P16	

After changing the voltage source, the circuitry needs to settle (t_{CSET}), before the status bit VCMP provides a valid result, see Figure 31.

In case the battery voltage is monitored, a weak resistive divider loads the battery, adjusting the comparator input voltage to a convenient measurement range.

In case an external voltage source is monitored, meaning that the control bit VSEN and ISEL are set at the same time, the direction flip-flop of port P16 is being overruled. Consequently, the corresponding input gate is disabled, forcing port P16 into tri-state, allowing analog operation for P16, see Figure 29.

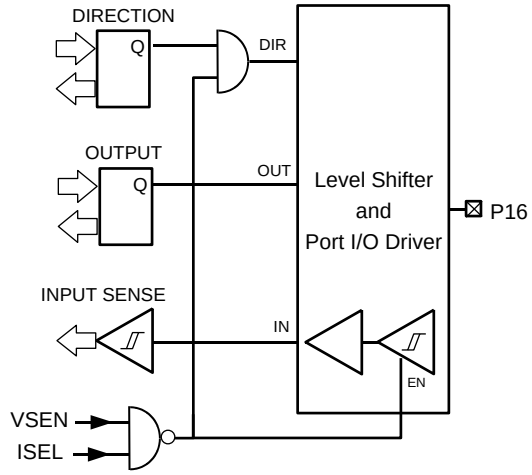


Figure 29. Interaction with Port P16

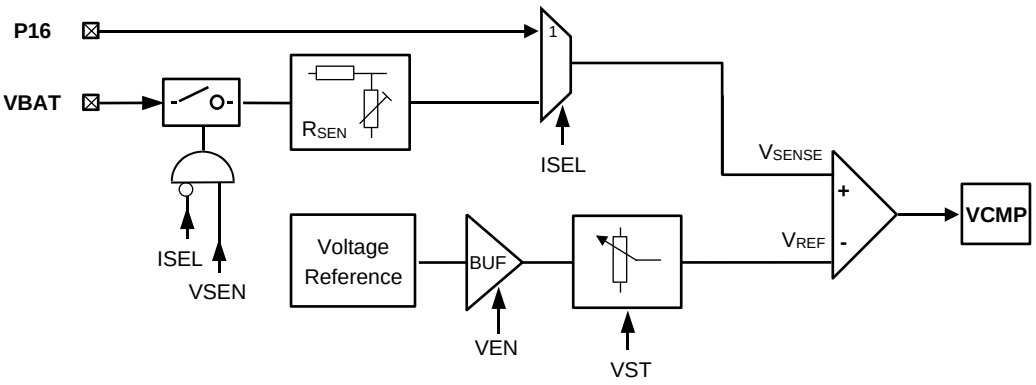


Figure 30. Programmable Voltage Comparator

VCMP, Voltage Compare

The comparator continuously compares the voltage sensed from the selected source (V_{SENSE}) against the programmable reference voltage (V_{REF}). If the sense voltage exceeds the reference voltage, the status bit VCMP is set, otherwise it is cleared.

VST, Reference Voltage Set

The programmable reference voltage can be set to the values as given in Table 37.

The available voltage range and accuracy is different for the two sources (VBAT and P16), as selected by ISEL.

After changing the reference voltage, the circuitry needs to settle (t_{CSET}), before the status bit VCMP provides a valid result, see Figure 31.

Table 37 Comparator Reference Voltage Control, VST

VST3	VST2	VST1	VST0	V_{BAT} [V] (typ)	V_{REF} [V] (typ)
0	0	0	0	1.90	0.59
0	0	0	1	1.99	0.62
0	0	1	0	2.08	0.65
0	0	1	1	2.17	0.68
0	1	0	0	2.26	0.71
0	1	0	1	2.35	0.73
0	1	1	0	2.44	0.76
0	1	1	1	2.53	0.79
1	0	0	0	2.62	0.82
1	0	0	1	2.71	0.85
1	0	1	0	2.80	0.88
1	0	1	1	2.89	0.90
1	1	0	0	2.98	0.93
1	1	0	1	3.07	0.96
1	1	1	0	3.16	0.99
1	1	1	1	3.25	1.02

ISEL	0	1

Note

1. The listed voltages indicate the voltage levels that must typically be applied to VBAT respectively to P16, in order to match the internal reference voltage.

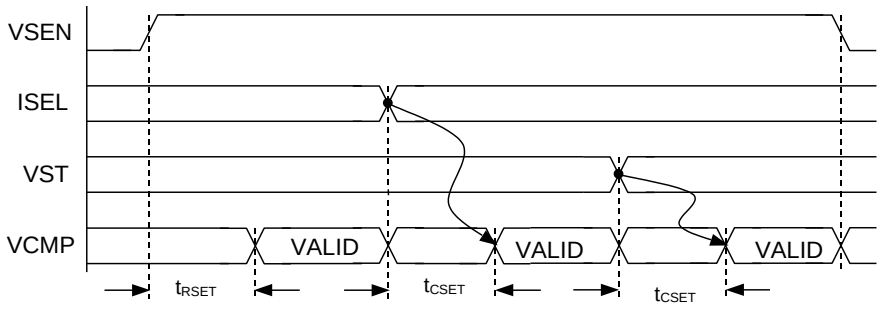


Figure 31. Voltage Comparator Timing

10.10 Calculation Unit

The PCF7922 employs a calculation unit for hardware accelerated device authentication, message encryption and rolling code generation.

Details concerning the security algorithm implementation are specified in a separate Application Note. Please contact your local NXP representative for more information.

The application program may operate the Calculation Unit in HITAG2 mode or in Enhanced mode. Operating the Calculation Unit in HITAG2 mode involves a 32 bit Identifier, a 48 bit Secret Key and a 32 bit Random Number. The algorithm operates on a 48 bit Shift Register. The Enhanced mode involves a 96 bit Secret Key, a 64 bit Random Number, and a 64 bit Shift Register. In both modes, all values are fully determined by the application program.

The Calculation unit consists of a 64 bit shift register with linear feedback (LF) and nonlinear feedback (OWF, One Way Function) capabilities that feature different characteristics for HITAG2 and Enhanced mode, see Figure 32.

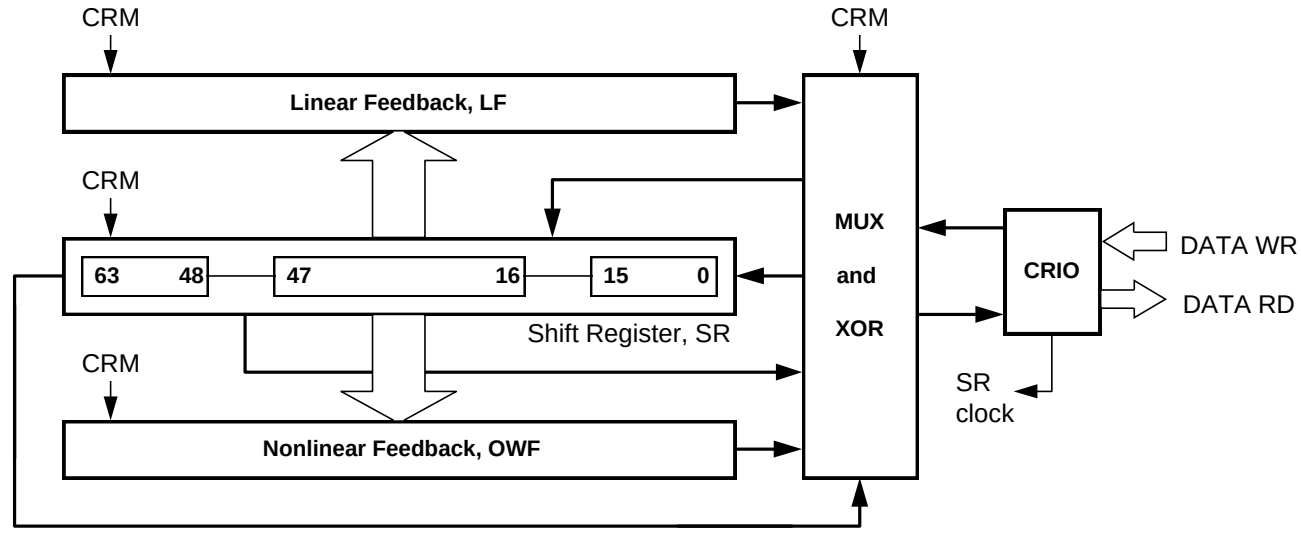


Figure 32. Calculation Unit Block Diagram

Operation of the Calculation Unit is managed by a set of Special Function Registers, CRYP1 and CRYP2, see Table 38.

The Identifier, Random Number, Secret Key and data processed are fed into the Calculation Unit and executed bit by bit under application program control. Their origin is not determined by the circuit design at all. Reading from and writing to the Calculation Unit is provided via the control bit CRIO. Upon each read, write or read-modify-write operation applied to CRYP1, the Calculation Unit Shift Register (SR) is clocked once, causing the Calculation Unit to convey its current value to the new value. This process is completed within one RISC instruction cycle.

The Calculation Unit initialization and operation is managed by a number of functions selected by the control bits CRM, as listed in Table 39.

Switching between the functions does not clock the Calculation Unit at all. However, it may change the value of CRIO, depending on the output value of the linear (LF) or nonlinear feedback (OWF), see the description of functions in the following.

Table 38 Calculation Unit I/O and Control Register

CRYP1, Calculation Unit I/O

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CRIO	X	X	X	X	X	X	X
R/W	W0	W0	W0	W0	W0	W0	W0

Address = 1EH

CRYP2, Calculation Unit Control

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
X	X	X	X	X	CRM2	CRM1	CRM0
W0	W0	W0	W0	W0	R/W	R/W	R/W

Note Address = 1FH

1. Bits marked ‘X’ are not connected and reserved for future use. Any read operation yields an undefined result. For future compatibility, a write operation should assign a ‘0’.

Table 39 Crypt Mode, CRM

CRM2	CRM1	CRM0	Function/Mode	Note
0	0	0	Load 16-HITAG2	
0	0	1	Load 16-Enhanced	
0	1	0	Load 0-HITAG2	
0	1	1	Load 0-Enhanced	
1	0	0	LF- HITAG2	
1	0	1	LF-Enhanced	
1	1	0	OWF- HITAG2	
1	1	1	OWF-Enhanced	

Function 0, Load 16-HITAG2

Function 0 is typically used, when the Calculation Unit is operated in HITAG2 mode, in order to initialize the Shift Register bit by bit. The Shift Register (SR) is operated in 48 bit fashion, bit 48 to bit 63 are not applicable and their values are undefined. The following course of events is triggered with each clock applied to the Calculation Unit:

$(SR_{N}^{+}) \leftarrow (SR_{N-1}); \quad N = 15 - 1$

$(SR_{0}^{+}) \leftarrow (SR_{47})$

$(SR_{N}^{+}) \leftarrow (SR_{N-1}); \quad N = 47 - 17$

$(SR_{16}^{+}) \leftarrow (CRIO)$

$(CRIO^{+}) \leftarrow OWF_{HITAG2}\,(SR^{+})$

Note

1. Read operations on CRIO are not allowed and may cause undefined results that are fed into the shift register (Bit 16).

Function 1, Load 16-Enhanced

Function 1 is typically used, when the Calculation Unit is operated in Enhanced mode, in order to initialize the Shift Register bit by bit. The Shift Register (SR) is operated in 64 bit fashion. The following course of events is triggered with each clock applied to the Calculation Unit:

$(SR_{N}^{+}) \leftarrow (SR_{N-1}); \quad N = 15 - 1$

$(SR_{0}^{+}) \leftarrow (SR_{63})$

$(SR_{N}^{+}) \leftarrow (SR_{N-1}); \quad N = 63 - 17$

$(SR_{16}^{+}) \leftarrow (CRIO)$

$(CRIO^{+}) \leftarrow OWF_{ENHANCED}\,(SR^{+})$

Note

1. Read operations on CRIO are not allowed and may cause undefined results that are fed into the shift register (Bit 16).

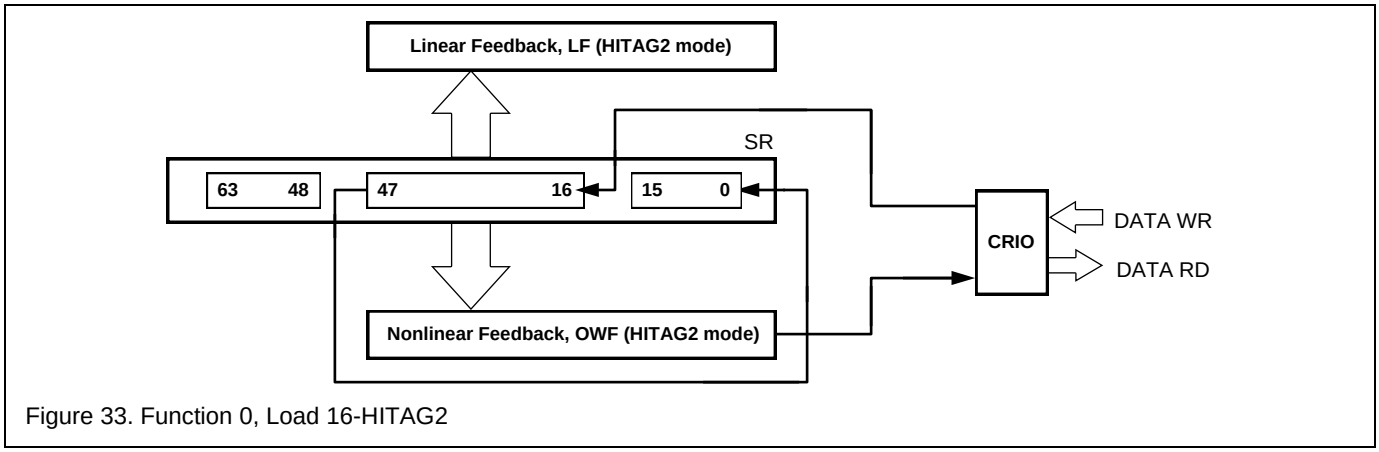


Figure 33. Function 0, Load 16-HITAG2

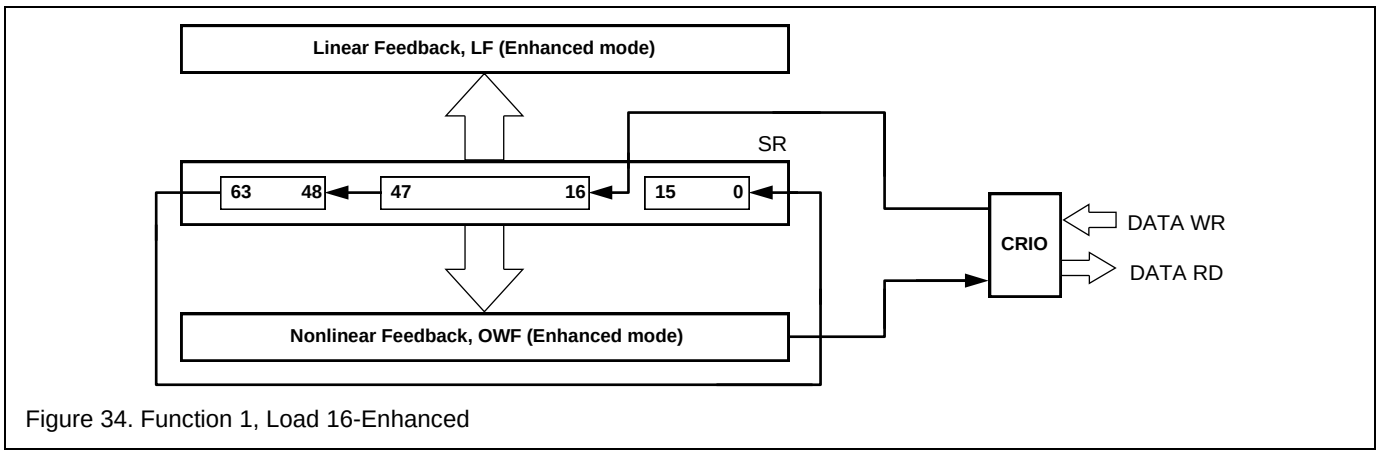


Figure 34. Function 1, Load 16-Enhanced

Function 2, Load 0-HITAG2

Function 2 is typically used, when the Calculation Unit operates in HITAG2 mode, in order to initialize the Shift Register (SR) bit by bit. The Shift Register (SR) is operated in 48 bit fashion, bit 48 to bit 63 are not applicable and their value is undefined. The following course of events is triggered with each clock applied to the Calculation Unit:

$(SR_{N}^{+}) \leftarrow (SR_{N-1})$; N = 47 - 1

$(SR_{0}^{+}) \leftarrow (CRIO)$

$(CRIO^{+}) \leftarrow OWF_{HITAG2}(SR^{+})$

Note

1. Read operations on CRIO are not allowed and may cause undefined results that are fed into the shift register (Bit 0).

Function 3, Load 0-Enhanced

Function 3 is typically used, when the Calculation Unit operates in Enhanced mode, in order to initialize the Shift Register (SR) bit by bit. The following course of events is triggered with each clock applied to the Calculation Unit:

$(SR_{N}^{+}) \leftarrow (SR_{N-1})$; N = 63 - 1

$(SR_{0}^{+}) \leftarrow (CRIO)$

$(CRIO^{+}) \leftarrow OWF_{ENHANCED}(SR^{+})$

Note

1. Read operations on CRIO are not allowed and may cause undefined results that are fed into the shift register (Bit 0).

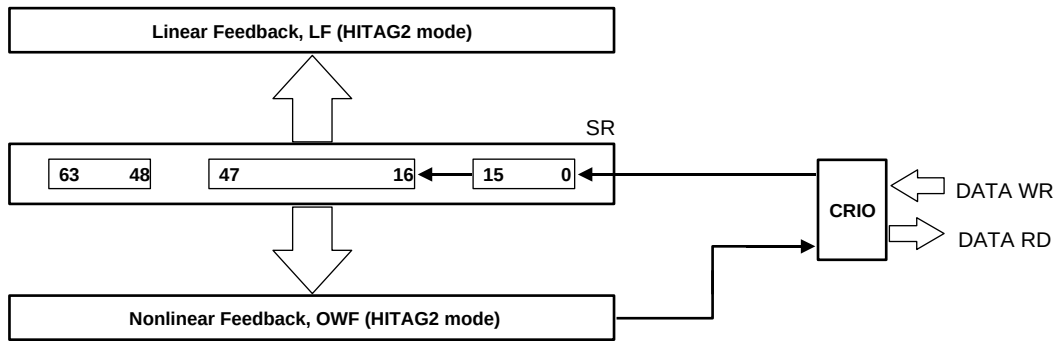


Figure 35. Function 2, Load 0-HITAG2

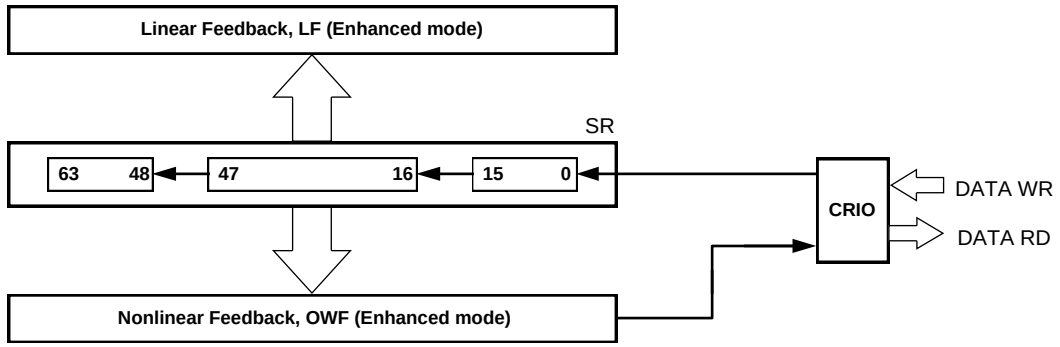


Figure 36. Function 3, Load 0-Enhanced

Function 4, LF-HITAG2

Function 4 is typically used, when the Calculation Unit is operated in HITAG2 mode, in order to convey the Shift Register (SR) bit by bit involving the linear feedback, which operates in HITAG2 mode. The Shift Register (SR) is operated in 48 bit fashion, bit 48 to bit 63 are not applicable and their value is undefined.. The following course of events is triggered with each clock applied to the Calculation Unit:

$(SR_{N}^{+}) \leftarrow (SR_{N-1}); \quad N = 47 - 1$

$(SR_{0}^{+}) \leftarrow LF_{HITAG2}(SR)$

$(CRIO^{+}) \leftarrow OWF_{HITAG2}(SR^{+})$

Note

1. In case a write operation is executed for CRIO, the value written is discarded and finally replaced by new output value of the nonlinear feedback, OWF_{HITAG2} (SR+), after the clock cycle completed.

Function 5, LF-Enhanced

Function 5 is typically used, when the Calculation Unit is operated in Enhanced mode, in order to convey the Shift Register bit by bit involving the linear feedback, which operates in Enhanced mode. The Shift Register (SR) is operated in 64 bit fashion. The following course of events is triggered with each clock applied to the Calculation Unit:

$(SR_{N}^{+}) \leftarrow (SR_{N-1}); \quad N = 63 - 1$

$(SR_{0}^{+}) \leftarrow LF_{ENHANCED}(SR)$

$(CRIO^{+}) \leftarrow OWF_{ENHANCED}(SR^{+})$

Note

1. In case a write operation is executed for CRIO, the value written is discarded and finally replaced by new output value of the nonlinear feedback, $OWF_{ENHANCED}$ (SR^{+}), after the clock cycle completed.

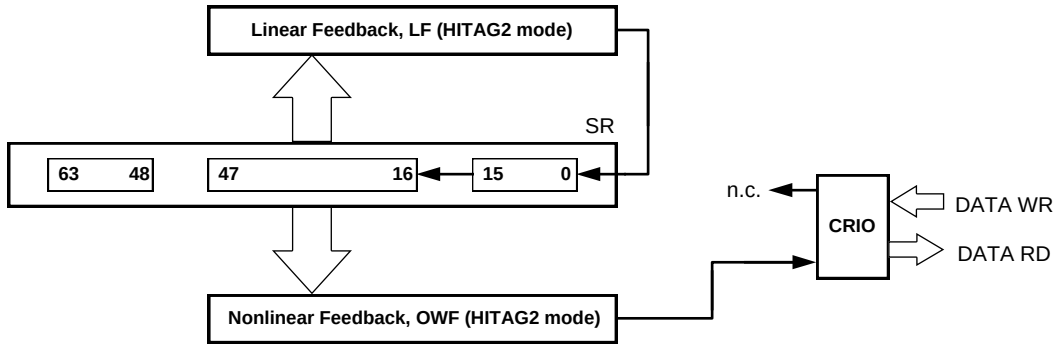


Figure 37. Function 4, Linear Feedback-HITAG2

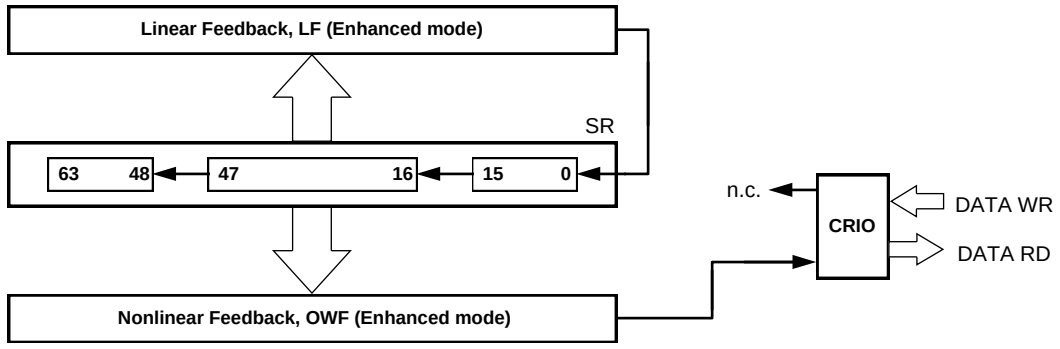


Figure 38. Function 5, Linear Feedback-Enhanced

Function 6, OWF-HITAG2

Function 6 is typically used, when the Calculation Unit is operated in HITAG2 mode, in order to convey the Shift Register bit by bit involving the nonlinear feedback, which operates in HITAG2 mode. The Shift Register (SR) is operated in 48 bit fashion, bit 48 to bit 63 are not applicable and their value is undefined. The following course of events is triggered with each clock applied to the Calculation Unit:

$(SR_{N}^{+}) \leftarrow (SR_{N-1}); \quad N = 47 - 1$

$(SR_{0}^{+}) \leftarrow (CRIO) \oplus OWF_{HITAG2}(SR)$

$(CRIO^{+}) \leftarrow OWF_{HITAG2}(SR^{+})$

Note

1. Read operations on CRIO are not allowed and may cause undefined results that are fed into the shift register (Bit 0).

Function 7, OWF-Enhanced

Function 7 is typically used, when the Calculation Unit is operated in Enhanced mode, in order to convey the Shift Register bit by bit involving the nonlinear feedback, which operates in Enhanced mode. The Shift Register (SR) is operated in 64 bit fashion. The following course of events is triggered with each clock applied to the Calculation Unit:

$(SR_{N}^{+}) \leftarrow (SR_{N-1}); \quad N = 63 - 1$

$(SR_{0}^{+}) \leftarrow (CRIO) \oplus (SR_{63}) \oplus OWF_{ENHANCED}(SR)$

$(CRIO^{+}) \leftarrow OWF_{ENHANCED}(SR^{+})$

Note

1. Read operations on CRIO are not allowed and may cause undefined results that are fed into the shift register (Bit 0).

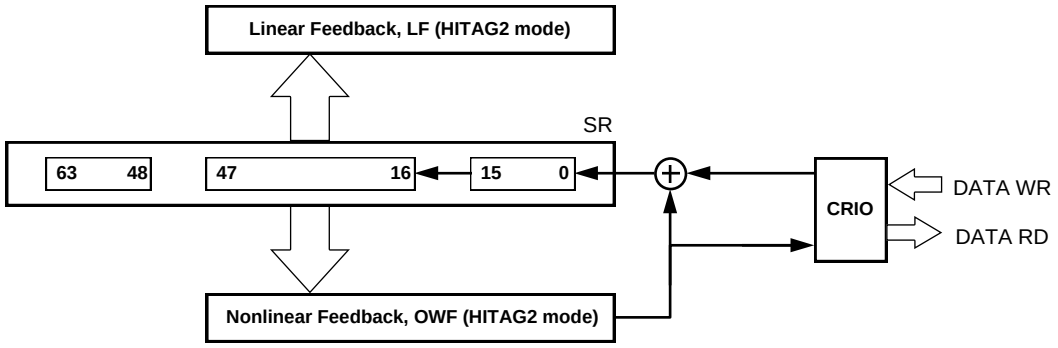


Figure 39. Function 6, Nonlinear Feedback-HITAG2

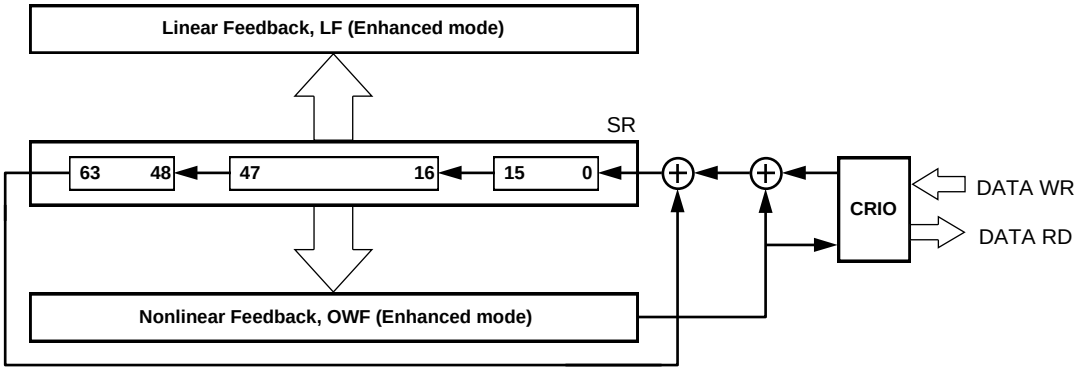


Figure 40. Function 7, Nonlinear Feedback-Enhanced

11 UHF TRANSMITTER DECRIPTION

The PCF7922 features a sophisticated on-chip ASK/FSK UHF Transmitter designed for use in the ISM frequency range 315 MHz or 434 MHz. The UHF Transmitter incorporates an XTAL Oscillator, fully integrated PLL Synthesizer and a Power Amplifier to drive an external antenna, see Figure 41.

The UHF Transmitter allows fine-tuning of the XTAL Oscillator by means of a programmable on-chip XTAL load capacitance, in order to compensate manufacturing tolerances of the crystal. Except for the XTAL itself, no additional external components are required. The Power Amplifier provides means to adjust and stabilize the output power, making it almost independent from battery voltage and temperature changes. It operates in singled-ended configuration and only few external components are needed to match the external antenna.

The UHF Transmitter can be used for both ASK and FSK modulation with data rates up to 20 kbps (Manchester).

The UHF Transmitter is controlled by a set of control registers located in the Control Logic and mapped into the Special Function Register range of the RISC Controller.

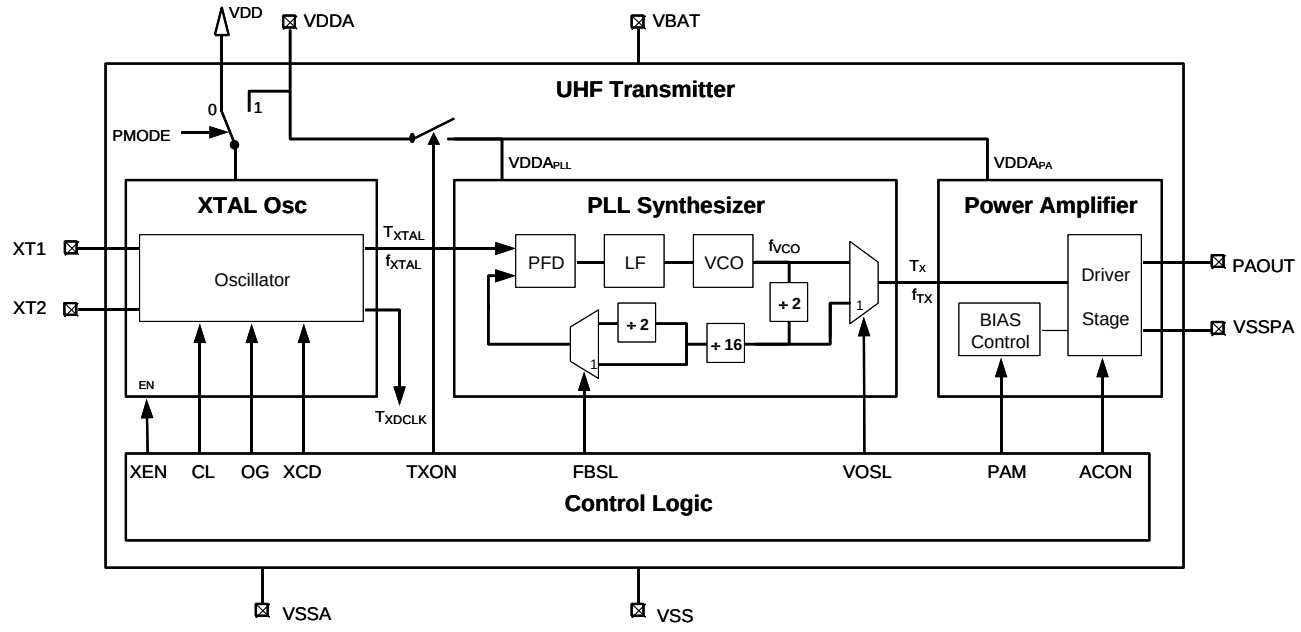


Figure 41. UHF Transmitter Block Diagram

11.1 XTAL Oscillator

The XTAL Oscillator provides the reference clock for the PLL synthesizer and if desired may be used for system timing purposes. Except for the XTAL itself, the XTAL Oscillator does not require any additional external components. The oscillator implementation selected features a programmable on-chip load capacitance for the XTAL, Figure 42.

The programmable load capacitance (CL) allows to fine tune the XTAL frequency, in order to compensate the initial frequency tolerances of the XTAL and for FSK modulation means. The load capacitance is determined via the control register XFCON, see section 11.4 for details. During XTAL start up it is recommended to set the internal load capacitance to its maximum (FCON = 0).

The actual oscillator signal at pin XT1 passes a buffer stage, before it is made available to other device circuitry (T_{XTAL}). The reference clock (T_{XREF}) for the PLL Synthesizer equals the XTAL frequency.

The Timer/Counter clock can be derived from the XTAL Oscillator. Depending on the control bit XCD the XTAL frequency is divided by 3 or 4 prior to use (T_{XDCLK}), in order to satisfy the device maximum clock frequency specification.

The XTAL Oscillator provides gain control (OG) means; in order to determine the XTAL Oscillator start-up and operation conditions, see section 11.4.1 and 21.7.

For proper XTAL oscillator operation it is mandatory to establish proper bias conditions for the XTAL Oscillator circuitry, as determined by NXP during device manufacturing and stored in a reserved EEPROM location. This task has to be accomplished by the user application program by calling (SYSCALL) the library function PLL_XO_INIT once, prior to enabling the XTAL Oscillator circuitry. The XTAL Oscillator circuitry maintains its initialization condition until a device reset occurs.

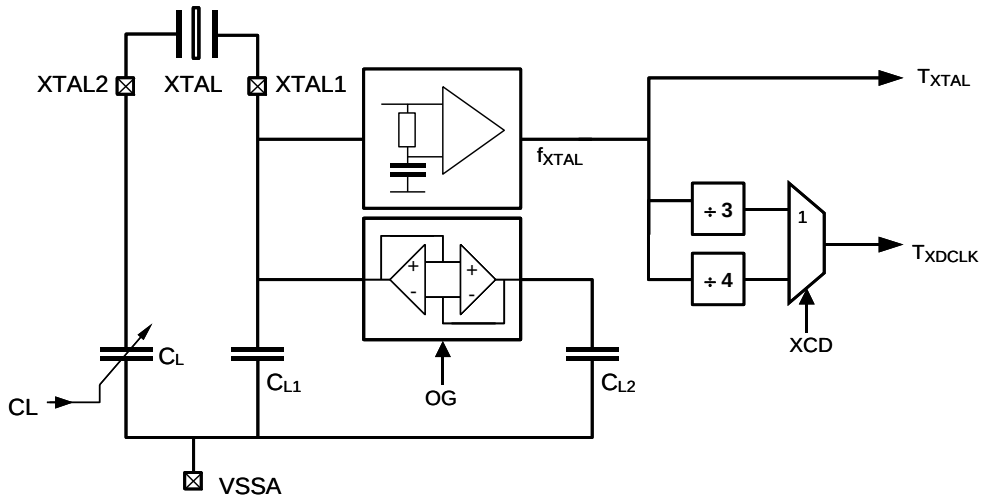


Figure 42. XTAL Oscillator Implementation T2

11.2 PLL Synthesizer

According to Figure 43 the PLL Synthesizer consist of a fully integrated VCO, Loop Filter (LF), Phase-Frequency Detector (PFD) and a divider chain providing a programmable division ratio of 32 or 64.

The reference clock (T_{XREF}) is derived from the XTAL Oscillator and feeds the Phase-Frequency Detector. The Power Amplifier is driven by the VCO output frequency directly or is divided by two prior to use, depending on the desired carrier frequency.

The divider control bits are located in the control register TXCON2, see section 11.4 for details.

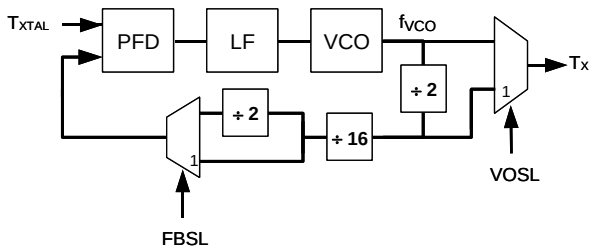


Figure 43. PLL Synthesizerr

11.3 Power Amplifier

The Power Amplifier is driven from the PLL Synthesizer and operates in single ended fashion, according to Figure 44.

The Power Amplifier consists of four binary weighted output stages, which are connected in parallel and are operational according to the amplifier control signal ACON, see section 11.4 for details.

The Power Amplifier features three regulated and one unregulated high power output Power Mode, as selected by the control bit PAM. When operating in regulated mode, the output stage drive voltage is controlled by a BIAS circuitry. Each of the three regulated Power Modes delivers a certain output power that is stabilized against supply voltage and temperature variations to a large degree. The lowest Power Mode provides the best regulation characteristics. Hence, select the lowest Power Mode acceptable for the application and eventually control the exact output power by means of the control signal ACON. Further, the available output power is a function of the actual VCO frequency. The higher the VCO frequency, hence its supply voltage (VDD_{VCO}) is, the higher the output power becomes. To select a low VCO frequency is desirable for Japan, due to the limitation in place regarding the radiated output power.

The Power Mode control bits are located in the control register TXCON2, see section 11.4 for details.

The Power Amplifier output (pin PAOUT) does require an external DC path to pin VBAT, established by the antenna loop or a dedicated bias coil. A dedicated ground pin (VSSPA) is provided to improve the RF properties of the circuitry. Pin VSSPA must be connected with pin VSS. Best performance is achieved, if the output voltage swing at pin PAOUT yields one volt less than two times the supply voltage: $V_{PAOUT\ PP} = 2\ (V_{VDDA} – 0.5V)$.

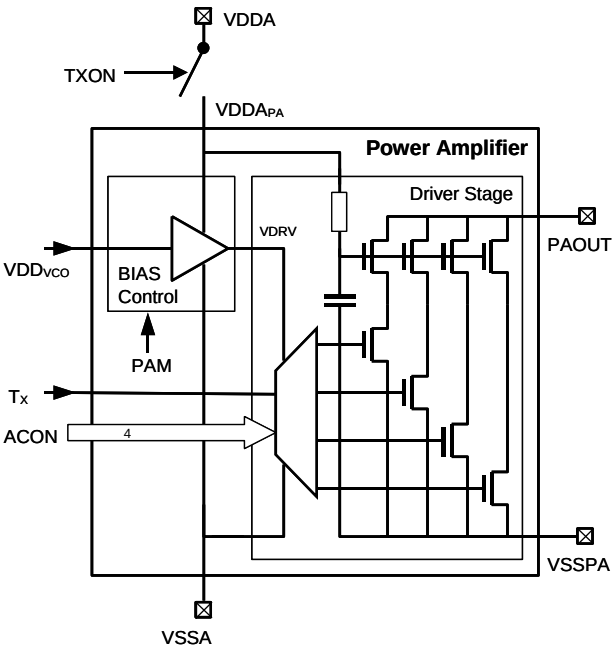


Figure 44. Power Amplifier Implementation

11.4 Control Logic

The Control Logic provides means to configure, tune and control the carrier and modulation of the UHF Transmitter utilizing a set of control register. The control registers are located in the Special Function Register range for access by the RISC Controller, Table 40 to Table 43.

Table 40 XTAL Oscillator Frequency Control, XFCON

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
X	X	XFC5	XFC4	XFC3	XFC2	XFC1	XFC0
W0	W0	R/W	R/W	R/W	R/W	R/W	R/W

Address = 30H

The control register XFCON controls the XTAL Oscillator frequency, for either frequency fine-tuning or FSK modulation means, see section 11.4.2.

Table 41 Power Amplifier Control, PACON

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
AMH3	AMH2	AMH1	AMH0	AML3	AML2	AML1	AML0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address = 31H

The control register PACON controls the Power Amplifier driver stage, for either amplitude fine-tuning or ASK modulation means, see section 11.4.1.

Table 42 Transmitter Control 1, TXCON1

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
X	X	XCD	XFCS	TM	OG1	OG0	XEN
W0	W0	R/W	R/W	R/W	R/W	R/W	R/W

Address = 32H

The control register TXCON1 holds several control bits that enable and control the XTAL Oscillator, XTAL load capacitance and features the Lock Detect flag.

Table 43 Transmitter Control 2, TXCON2

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
X	X	FBSL	X	VOSL	PAM1	PAM0	TXON
W0	W0	R/W	W0	R/W	R/W	R/W	R/W

Address = 33H

The control register TXCON2 holds more control bits that enable and control the PLL Synthesizer, select the output frequency range, control the Power Amplifier and determine the XTAL Oscillator clock edge reference.

11.4.1 Transmitter Set-Up and General Control

Before being operational the UHF Transmitter need to be configured for the desired carrier frequency and operating mode.

The UHF Transmitter may be operated in the 315 MHz or 434 MHz range, with a division ratio of 32 applicable between the desired carrier frequency (f_{TX}) and actual PLL reference frequency (f_{XREF}). Table 44 shows the recommended settings for common XTAL frequencies

Table 44 UHF Transmitter configuration

FBSL	VOSL	f_{VCO}	f_{TX}	f_{XTAL}
1	0	315 MHz	315 MHz	9.8433 MHz
1	0	434 MHz	434 MHz	13.56 MHz

Note

1. Other settings of FBSL and VOSL are not supported.

The corresponding configuration bits are located in the control register TXCON2.

FBSL, PLL Feedback Select

For proper device operation, the configuration bit FBSL has to be set (FBSL = 1). In this case the VCO frequency is divided by 32 prior to comparison with the PLL reference.

VOSL, VCO Output Select

The configuration bit VOSL determines if the nominal (VOSL = 0) or the divided (VSOL = 1) VCO frequency is fed to the Power Amplifier. Depending on the desired carrier frequency, a certain setting of VOSL is mandatory see above.

OG, XTAL Oscillator Gain Control

The configuration bits OG provide means to influence the gain control of the XTAL Oscillator. According to Table 45 a high gain setting shall be chosen during XTAL start-up, while during ASK or FSK operation a low gain is desirable. The applicable configuration depends on the actual XTAL specification, hence feasible oscillation margin and allowed XTAL drive level. In case an additional series resistor shall be introduced, in order to limit the XTAL drive level, this resistor need to be inserted between the XTAL and pin XTAL1.

Table 45 Typical XTAL Oscillator Gain, OG, settings

OG1	OG0	Gain	Usage	Note
0	0	High	XTAL start-up f_{XTAL} = 13.56 MHz	
0	1	Medium High	XTAL start-up f_{XTAL} = 9.84 MHz	
1	0	Medium Low	FSK or ASK operation f_{XTAL} = 13.56 MHz	
1	1	Low	FSK or ASK operation f_{XTAL} = 9.84 MHz	

XCD, XTAL Clock Divider

A set of clock dividers are available, to cope with a variety of XTAL clock frequencies, in case the XTAL is used as Timer/Counter clock. If the control bit XCD is set the XTAL clock is divided by 3. Otherwise, if cleared, is divided by four prior to further use.

XEN, XTAL Oscillator Enable

The control bit XEN provides means to enable (XEN = 1) the XTAL Oscillator any time desired. The XTAL Oscillator provides the reference clock for the PLL Synthesizer. In addition, the XTAL Oscillator clock (T_{XTAL}) is available to the Timer/Counters and may be used for timing purposes. If XEN is zero, the XTAL Oscillator is disabled and consumes virtually no current.

The XTAL Oscillator start-up characteristics and final frequency is controlled by dedicated control bits see section 11.4.2.

TXON, Transmitter Power On

The control bit TXON provides means to power-up (TXON = 1) the PLL Synthesizer and Power Amplifier circuitry. To avoid spurious emission, the Power Amplifier shall be muted (ACON = 0) during power-up and the PLL Synthesizer (VCO) allowed to start-up and lock first. Latter one requires that the XTAL Oscillator is operational (XEN = 1).

If TXON is zero, the PLL Synthesizer and Power Amplifier are shut-off and disconnected from the supply pin (VDDA) not drawing any significant quiescent current.

11.4.2 XTAL Oscillator Control and FSK Modulation

The XTAL Oscillator features an on-chip programmable XTAL load capacitance, capable of to fine-tune the XTAL frequency and to introduce a FSK modulation if desired. A quasi unique feature of the Programmable Load Capacitance is the ability to select a XTAL load capacitance that gives the fastest XTAL start-up, and to fine-tune the XTAL to the desired frequency once it is oscillating, see Figure 46.

The Programmable Load Capacitance comprises of 64 weighted capacitors, chosen in a way to provide an almost linear frequency shift of the XTAL frequency versus the control signal FCON, Figure 45. The actual XTAL load capacitance is calculated according to Table 46.

The applicable XTAL load capacitance is determined by the 6bit register FML (Frequency LOW) and FMH (Frequency HIGH).

XFC[5…0], XTAL Oscillator Frequency Control

The control register FML (Frequency LOW) and FMH (Frequency HIGH) can not be manipulated directly, instead are accessed for reading and writing through the control bits XFC depending on the state of the control bit XFCS.

The control bits XFC are located in the control register XFCON.

XFCS, XTAL Frequnecy Control Select

Depending on the state of the control bit XFCS either the register FMH (XFCS = 1) or FML (XFSC = 0) can be accessed for reading and writing, utilizing the control register XFC.

The control bits XFCS is located in the Control register, TXCON1.

TM, Transparent Mode

Changing the XTAL Load Capacitance typical employs an Up/Down counter, in order to implement a smooth transition from the present to the new value, step by step. When the control bit TM is set, the Up/Down counter is forced into transparent state, making any change to become effective immediately.

The control bit TM is located in the Control register, TXCON1.

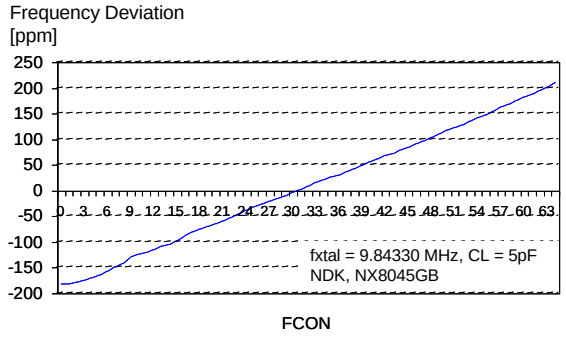


Figure 45. Programmable Load Capacitane

Table 46 XTAL Load Capacitance

FCON	CL [pF]		Note
0_D … 7_D	30.700 pF	– FCON * 2.270 pF	
8_D … 15_D	12.540 pF	– (FCON – 8D) * 0.700 pF	
16_D … 23_D	6.940 pF	– (FCON – 16D) * 0.340 pF	
23_D … 31_D	4.220 pF	– (FCON – 24D) * 0.199 pF	
32_D … 39_D	2.628 pF	– (FCON – 32D) * 0.128 pF	
40_D … 47_D	1.604 pF	– (FCON – 40D) * 0.089 pF	
48_D … 55_D	0.892 pF	– (FCON – 48D) * 0.066 pF	
56_D … 63_D	0.364 pF	– (FCON – 56D) * 0.052 pF	

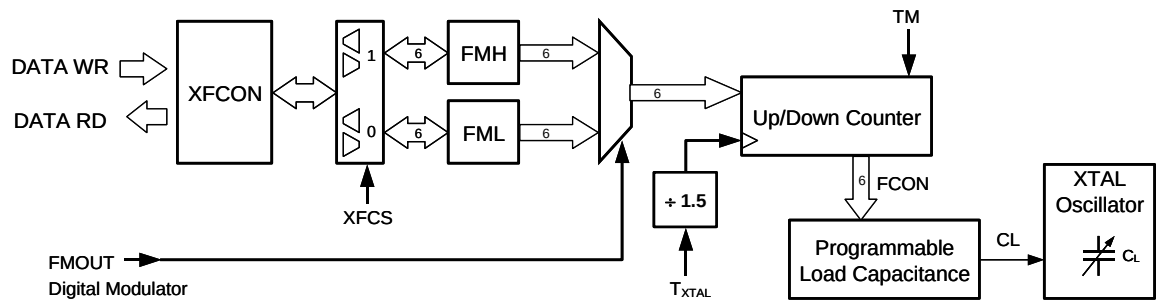


Figure 46. XTAL Load Capacitor Control

Frequency modulation of the carrier is achieved by varying the XTAL frequency. Hence, by switching between the FMH and FML register in accordance to control signal FMOUT, which is derived from the Digital Modulator, Figure 47.

If the Digital Modulator is disabled, the control signal (FMOUT) is low, enabling constant frequency operation with the XTAL frequency determined by the control register FML, see also section 10.7.

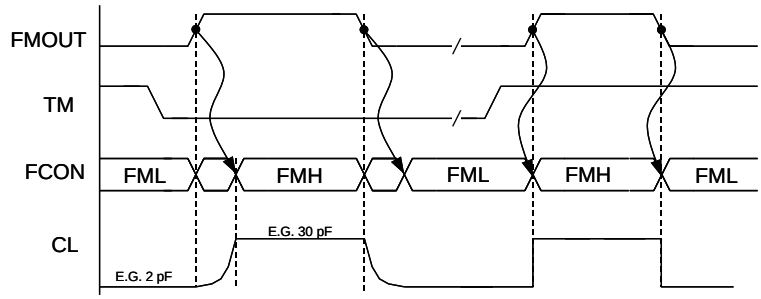


Figure 47. FSK Modulation Timing

11.4.3 Power Amplifier Control and ASK Modulation

The device features several control bits controlling the output amplitude and ASK modulation characteristics of the Power Amplifier see Figure 48.

The control register PACON features two 4bit values that set the HIGH (AMH) and LOW (AML) level during amplitude modulation of the UHF carrier. Amplitude modulation is achieved by switching between the HIGH and LOW level in accordance to control signal AM, which is derived from the Digital Modulator output (AMOUT) see section 10.7.

If the Digital Modulator is disabled, the control signal (AMOUT) is low, enabling continuous wave operation with the output amplitude determined by the control bits AML.

AMH[3…0], Amplitude Modulation HIGH

In case the control signal AM is high, the actual value of AMH determines the UHF carrier output amplitude, by controlling (ACON) the four binary weighted Power Amplifier output stages.

The control bits AMH are located in the Power Amplifier Control register, PACON.

AML[3…0], Amplitude Modulation LOW

In case the control signal AM is low, the actual value of AML determines the UHF carrier output amplitude, by controlling (ACON) the four binary weighted Power Amplifier output stages.

The control bits AML are located in the Power Amplifier Control register, PACON.

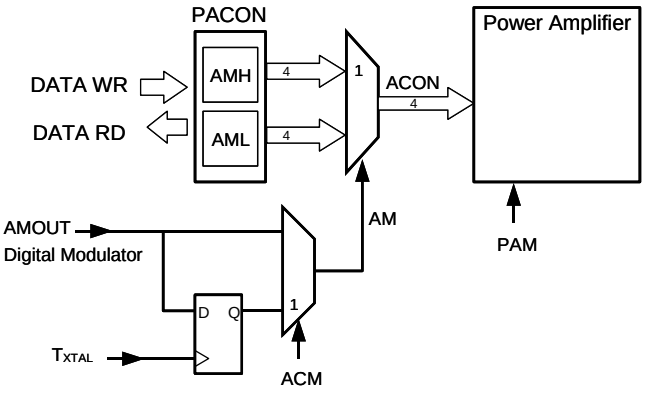


Figure 48. Power Amplifier Control

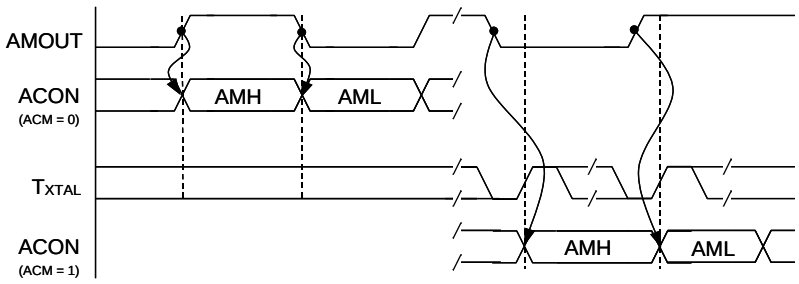


Figure 49. ASK Modulation Timing

PAM[1,0], Power Amplifier Mode

The Power Amplifier feature means to stabilize the output power against battery voltage and ambient temperature variations. If desired, the corresponding circuitry can be disabled, enabling the Power Amplifier to deliver the highest output power available, Table 47

Table 47 Power Amplifier Modes, PAM

PAM1	PAM0	Power Mode	Comment	Note
0	0	I	Low power Highest stability	
0	1	II	Medium power Medium stability	
1	0	III	High power Low stability	
1	1	IV	Maximum power Stabilization OFF	

Note

1. The lower the available output power selected, the better the stability against temperature and battery voltage variations.

The control bits PAM only determine the available output power, the actual output power is set by the Power Amplifier Control bits AMH and AML (PACON register).

The control bits PAM are located in the control register TXCON2.

12 DEVICE MODES

The device features different Device Modes affecting the overall device behavior, the Monitor and Download Interface operation and user ability to access the EEPROM and E-ROM.

The Device Mode is controlled by a set of configuration bytes, which are located in the EEPROM and E-ROM.

The configuration bytes may not be altered by the user directly, instead, requires to utilize the corresponding Monitor and Download command, see section 14.

INIT Mode

When the device is supplied from NXP, it is configured for INIT mode by default, according to section 10.1.

The INIT mode shall be used during software development only. The Monitor and Download Interface is fully operational, enabling the customer to initialize the EEPROM and E-ROM as desired for the application, in accordance with the access restrictions in place by design, see section 19.

To protect the EEPROM and E-ROM from readout and to disable the debug features, the device must be forced into PROTECTED mode finally.

Leaving the device in INIT mode, may cause the device to execute a software break, in case a LOW pulse is detected at pin MSDA. Latter one would terminate execution of the application program and would invoke build-in monitor program. In this case, execution of the application program is interrupted until a proper debug command is issued or a device reset is applied, see also section 21.3.

PROTECTED Mode

In the moment the device is set for PROTECTED mode, the EEPROM and E-ROM are protected against altering and readout via the Monitor and Download Interface, and the debug features are disabled. The PROTECTED mode has to be used during system testing and in the application finally.

The device may be forced into INIT mode again, by issuing a corresponding command (C_ER_EROM) via the Monitor and Download Interface. Latter one sets the EEPROM and the E-ROM to a predefined state before the INIT mode is resumed. Hence, discards all application related EEPROM data and the E-ROM based application program. However, in case this sequence does not complete successfully, the device enters TAMPERED mode.

TAMPERED Mode

The TAMPERED mode is entered temporarily during the sequence, which forces the device from PROTECTED mode back into INIT mode. If this sequence does not complete successfully, thus is interrupted, the TAMPERED mode will be entered.

The device may be forced into INIT mode, by again issuing a corresponding command (C_ER_EROM) via the Monitor and Download Interface. Latter one sets the EEPROM and the E-ROM to a predefined state before the INIT mode is resumed. Hence, discards all application related EEPROM data and the E-ROM based application program. However, in case this sequence does not complete successfully, the device remains in TAMPERED mode until a new attempt is made, by issuing the command (C_ER_EROM) again.

VIRGIN Mode

After manufacturing the device operates in VIRGIN mode, enabling extended device test and device configuration. Finally, NXP forced the device into INIT mode and the VIRGIN mode is irreversible locked, in order to ensure it can not be activated again.

13 BOOT ROUTINE

After any device reset forced by a Port Wake Up condition or interrogated by the application program, program execution starts with the ROM based BOOT routine. The BOOT routine executes a sequence of instructions that configures the device and evaluates the device mode. Subsequently, invokes the Application Program (WARM BOOT) or the Monitor, see Figure 50.

13.1 Functional Description

In the moment the BOOT routine commences, the pin MSCL is set high for test purposes in the context of Debug Monitor Mode activation. Subsequently, the on-chip RC Oscillator and other device circuitry are initialized according to the Device Configuration (DCFG) values stored in the EEPROM.

Next, the present device mode is evaluated. In case the device signals TAMPERED mode, device operation is halted, to render the device useless. Latter one is signaled by a MSCL low-to-high transition. Unless MSDA is detected low, causing the device to interrogate the MONITOR routine. See below.

Next, the device will set the WARM BOOT vector to 0000_H and finally verifies the Device Mode again. This time in order to eventually enable the debug features, in case the device is configured for INIT mode. Otherwise, if the device is set to PROTECTED mode, the debug features are not available. Prior to passing device control to the corresponding WARM BOOT location in the Application Code Memory, the pin MSDA is tested. If MSDA is high, the WARM BOOT is executed. In case MSDA is detected low, the MONITOR routine is interrogated. See below.

Any other coding of the Device Mode configuration bits is not valid and is handled like the device being in TAMPERED Mode, causing to halt device operation, to render the device useless. Latter one is signaled by a MSCL low-to-high transition. Unless MSDA is detected low, causing the device to interrogate the MONITOR routine.

In case the BOOT sequence leads to interrogation of the MONITOR routine, the device either uses an internal or external device clock, according to the timing of MSCL and MSDA. For a detailed description, reference is made to the PCF7922 Monitor and Download Interface specification, see section 22.

It is worth mentioning that in case the MONITOR has been entered accidentally, while the device is set to PROTECTED Mode, the on-chip Watchdog Timer terminates the Monitor mode again, in case no valid monitor command is received.

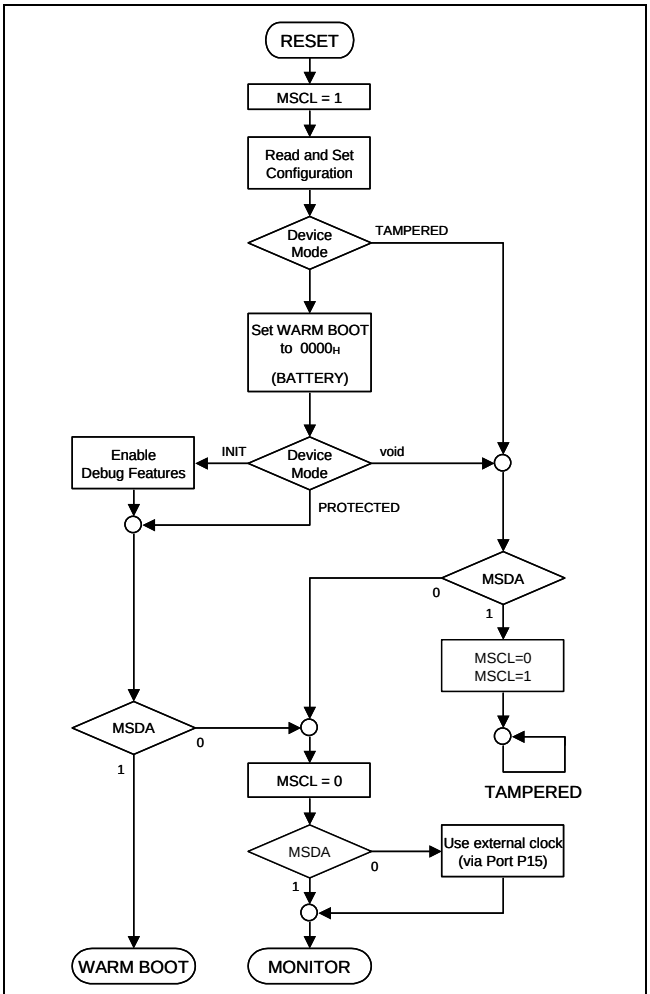


Figure 50. Flow Chart BOOT Routine

13.2 Execution Time

The total execution time of the BOOT routine (t_{BOOT}) depends on the device configuration and application conditions. According to Figure 51, the BOOT routine commences as soon as the power on reset hold delay timeouts and terminates with the invocation of the Application Program (WARM BOOT), see also section 8.1.

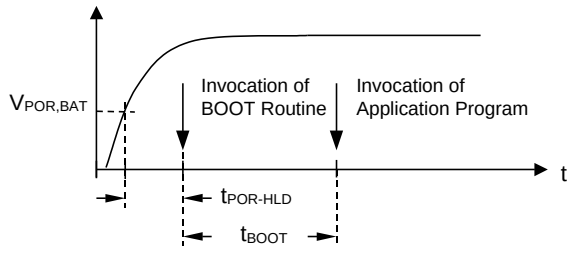


Figure 51. Power up timing

The BOOT routine execution time yields a value as specified, see section 17.3.

14 MONITOR AND DOWNLOAD INTERFACE

The Monitor and Download Interface is implemented as a serial interface that utilize the MSDA and MSCL pin. This interface provides means to initialize the EEPROM and E-ROM, as well as provides debug features during application program development. The Monitor and Download routine does occupy some Stack space, which needs to be considered during application program design.

The majority of the features provided by the Monitor and Download Interface are available only, if the device is set into INIT mode, which is the factory default setting. When performing system tests and field trials, the device shall be set to PROTECTED mode. Latter one locks the EEPROM and E-ROM content, protecting it against alteration and read out, as well as disables the debug features. The device may be forced back into INIT mode by a dedicated operation (Monitor and Download command C_ER_EROM), which will set the EEPROM and E-ROM to a predefined state, see also section 11.

For more details, please refer to the Monitor and Download Interface Functional Description, see section 22.

For development and prototyping purposes dedicated tools are available that are part of the PCF7922 development tool set, see section 23.

15 EEPROM CONTENT AT DELIVERY

The PCF7922 EEPROM content is initialized during device manufacturing, according to Table 48.

However, the EEPROM content may be changed as desired by the application, except for the page 0 and page 127. Page 0 holds the device Identifier (IDE) and serves the function of a serial number and product type ID, while page 127 holds device configuration data.

Table 48. EEPROM Content Upon Delivery

Content [HEX]	Page	Note
XX XX XX 8X	0	1
XX XX XX XX	1 to 126	
X6 XX 80 00	127	

MSB LSB

Note

1. Bit 7 to 4 of this page (Identifier) serve the function of a product type (application) identifier and are set to ‘1000’ for the PCF7922. For system compatibility reasons, PCF7x61 (SMART) uses the same product type Identifier.
2. Locations marked ‘X’ are undefined and may hold any pattern.

Consequently, the device set to INIT mode, providing full support regarding the Monitor and Download Interface, see section 11.

16 LIMITING VALUES

All values are in accordance with Absolute Maximum Rating System (IEC 134)
V_{SS} = 0V; V_{SSA} = 0V; V_{SSPA} = 0V

PARAMETER	MIN	MAX	UNIT
Operating temperature range	-40	+85	°C
Storage temperature range	-55	+125	°C
Voltage at any I/O and V_{BAT} pin to V_{SS}	-0.5	3.6	V
Voltage at V_{PAOUT} pin to V_{SS}	-0.5	7.2	V
Voltage at any I/O pin to V_{SS}	-0.5	V_{BAT} +0.3	V
Peak output current port P1x and P2x		15	mA
Latch-up current, Note 1	100		mA
ESD, human body model, Note 2	2		kV
ESD, human body model for pins V_{BAT} and V_{SS}, Note 2	3		kV
ESD, machine model, Note 3	200		V
Power dissipation		120	mW

Notes

1. According to JEDEC, JESD 17
2. According to JEDEC, JESD 22-A114
3. According to JEDEC, JESD 22-A115

17 ELECTRICAL CHARACTERISTICS

17.1 Operating Conditions

Tamb = -40 to +85°C, V_{SS} = 0V, V_{BAT} = 3.0V (Pin TEST connected to VSS).
Unless otherwise specified.

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
V_{BAT}	Battery supply voltage	Note 6	2.1	3.0	3.6	V
$I_{QQ,APP}$	POWER-OFF quiescent current in application configuration	V_{BAT} = 3.6V, Note 1, 5			1	µA
Device executes from ROM, Note 1						
$I_{BAT-R2M}$ $I_{BAT-R125k}$ $I_{BAT-RIDLE}$	RUN mode @ T_{SYS} = 2 MHz RUN mode @ T_{SYS} = 125 kHz IDLE mode	EEPROM disabled, A/D converter disabled		215 35 17	500 80 50	µA µA µA
Device executes from E-ROM, Note 1						
I_{BAT-2M} $I_{BAT-125k}$ $I_{BAT-IDLE}$	RUN mode @ T_{SYS} = 2 MHz RUN mode @ T_{SYS} = 125 kHz IDLE mode	EEPROM disabled, A/D converter disabled		450 60 30	600 100 80	µA µA µA
ΔI_{DD-EE}	Supply current EEPROM (Erase/Write)	Note 2, 3		20	50	µA
ΔI_{DD-VC}	Supply Current Voltage Comparator	Note 2, 4		20	35	µA
Power On Reset (POR)						
$V_{POR,BAT}$	Power-On Reset threshold	V_{BAT} - V_{SS}	1.8		2.1	V

Notes

1. No external clock (P15) applied to the device and input/output current of ports (P1 and P2) are zero. Value measured according to Figure 52.
2. Specifies the additional internal chip operating current caused by the corresponding circuitry, if enabled, which has to be added to the device operating current (I_{BAT}) in order to determine the total device operating current. Value measured according to Figure 52.
3. The specified current applies during the EEPROM ERASE/WRITE cycle only (t_{ERWR}).
4. When the Voltage Comparator is enabled and the VBAT pin selected as source (ISEL = 0), the battery is loaded with the sense resistor (R_{SEN}). The sense current caused needs to be added to load drawn from the battery.
5. Represents the quiescent current in a typical application wiring. Value measured according to Figure 52.
6. E-ROM ERASE/WRITE supported at VBAT ≥ 2.5 V only.

17.2 AC/DC Characteristics

Tamb = -40 to +85°C, V_{SS} = 0V, V_{BAT} = 3.0V (Pin TEST connected to VSS).
Unless otherwise specified.

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
P1, P2 (General Purpose I/O)						
C_I	Pin capacitance	V_{IN} = 0.1V_{RMS}, f = 1MHz		5		pF
C_{I-P15}	Pin capacitance	V_{IN} = 0.1V_{RMS}, f = 1MHz		5	7	pF
V_{IL}	Input low voltage		-0.1		0.2 V_{BAT}	V
V_{IH}	Input high voltage		0.8 V_{BAT}		V_{BAT} + 0.1	V
I_{IL}	Input low current	V_{IL} = 0			0.5	µA
I_{IH}	Input high current	V_{IH} = V_{BAT}			0.5	µA
V_{OL}	Output low voltage	I_O = 4mA			0.4	V
V_{OH}	Output high voltage	I_O = -4mA	V_{BAT} - 0.4			V
I_{PU}	Pull-Up current	V_I = 0V	30	75	150	µA
Port P26ON						
V_{OH}	Output high voltage				5.5	V
V_{OL}	Output low voltage	I_O = 10mA		0.1	TBD	V
V_{OL}	Output low voltage	I_O = 30mA		0.3	TBD	V

Notes see below.

Voltage Comparator, VSEN = 1						
R_{SEN}	Sense Load Resistance			150		kΩ
Battery Voltage Sense, ISEL = 0						
$V_{THR,BAT}$	Threshold voltage battery monitor	VST = 00H	1.84	1.90	1.96	V
		VST = 01H	1.93	1.99	2.05	V
		VST = 02H	2.02	2.08	2.14	V
		VST = 03H	2.11	2.17	2.23	V
		VST = 04H	2.20	2.26	2.32	V
		VST = 05H	2.29	2.35	2.41	V
		VST = 06H	2.38	2.44	2.50	V
		VST = 07H	2.47	2.53	2.59	V
		VST = 08H	2.56	2.62	2.68	V
		VST = 09H	2.65	2.71	2.77	V
		VST = 0AH	2.74	2.80	2.86	V
		VST = 0BH	2.83	2.89	2.95	V
		VST = 0CH	2.92	2.98	3.04	V
		VST = 0DH	3.01	3.07	3.13	V
		VST = 0EH	3.10	3.16	3.22	V
		VST = 0FH	3.19	3.25	3.31	V
Port (P16) Voltage Sense, ISEL = 1, Note 1						
$V_{THR,P16}$	Threshold voltage Port P16	VST = 00H		0.59		V
		VST = 01H		0.62		V
		VST = 02H		0.65		V
		VST = 03H		0.68		V
		VST = 04H		0.71		V
		VST = 05H		0.73		V
		VST = 06H		0.76		V
		VST = 07H		0.79		V
		VST = 08H		0.82		V
		VST = 09H		0.85		V
		VST = 0AH		0.88		V
		VST = 0BH		0.90		V
		VST = 0CH		0.93		V
		VST = 0DH		0.96		V
		VST = 0EH		0.99		V
		VST = 0FH		1.02		V

Notes

1. Due to reference voltage spreads, the accuracy is limited to ± 50mV.

17.3 UHF Transmitter Operating Conditions

Tamb = -20 to +70°C, $V_{BAT} = V_{DDA}$, V_{SS} = 0V
Unless otherwise specified.

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
V_{DDA}	Supply Voltage		2.1	3.0	3.6	V
$V_{DDA,SU}$	Supply Voltage, XTAL start-up	Note 2	2.2	3.0	3.6	V
I_{DDA-PD}	Supply current in Power-Down mode	XEN = 0, TXON = 0			0.5	µA
$I_{DDA-XTAL}$	Supply current XTAL Oscillator ON	V_{BAT} = 3.0V, XEN = 1, TXON = 0 FCON = 0 OG = 3, f_{TXAL} = 9.84 MHz OG = 2, f_{TXAL} = 13.56MHz		 350 400	 800 850	 µA µA
$I_{DDA-VCO}$	Supply current VCO ON	V_{BAT} = 3.0V, XEN = 1, TXON = 1 FCON = 0, ACON = 0 OG = 3, f_{TXAL} = 9.84 MHz OG = 2, f_{TXAL} = 13.56MHz		 1.2 1.5	 2 2.3	 mA mA
ΔI_{PA}	Power Amplifier current in Transmit mode f_{TX} = 315 MHz, Note 1	V_{BAT} = 3.0V XEN = 1, TXON = 1, VOSL = 0 FCON = 0, OG = 3, ACON = “1111” PAM = ‘10’, RL ~ 200 Ω PAM = ‘00’ RL ~ 700 Ω		 7.3 1.1	 9.9 2.0	 mA mA
ΔI_{PA}	Power Amplifier current in Transmit mode f_{TX} = 434 MHz, Note 1	V_{BAT} = 3.0V XEN = 1, TXON = 1, VOSL = 0 FCON = 0, OG = 2, ACON = “1111” PAM = ‘10’, RL ~ 200 Ω PAM = ‘00’ RL ~ 700 Ω		 8.3 1.5	 10.9 2.4	 mA mA
$I_{DD,TX}$	Supply current in Transmit mode		$I_{BAT} + I_{DDA-VCO} + \Delta I_{PA}$			
f_{TX}	Carrier frequency range		310		450	MHz
f_{VCO}	VCO Frequency		310		450	MHz
f_{XTAL}	XTAL Oscillator Frequency		9.7		14.1	MHz

Notes

1. Load tank circuit according to Figure 53.
2. During XTAL oscillator start-up the minimum supply voltage must yield the specified value.

17.4 UHF Transmitter AC/DC Conditions

Tamb = -20 to +70°C, $V_{BAT} = V_{DDA} = 3.0V$, $V_{SS} = 0V$
Measured at 50 Ohm reference board using NDK crystal NX5032SA, unless otherwise specified.

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
XTAL Oscillator, XEN = 1, Tamb = -40 to +85°C						
R_{MARGIN}	Oscillation startup margin, Note 1	$V_{BAT} = V_{DDA} = 2.2V$, Tamb = 25°C				
		f_{TXAL} = 9.84 MHz, OG = 1_D	800	1800		Ω
		f_{TXAL} = 13.56 MHz, OG = 0	600	1200		Ω
C_{XT1}	Pin capacitance	Tamb = 25°C, OG = 3_D	14.1	17.4	20.7	pF
		Input resistance –50 Ω				
C_{XT2}	Pin capacitance	Tamb = 25°C, FCON = 0	26.3	32		pF
		Tamb = 25°C, FCON = 63_D		2	2.9	pF
t_{XTSET}	XTAL Oscillator settling time Note 2	$V_{BAT} = V_{DDA} = V_{DDA,SU}$, XFC = 0				
		OG = 1, f_{XTAL} = 9.84 MHz		0.5	1.5	ms
		OG = 0, f_{XTAL} = 13.56 MHz		0.4	1.5	ms
PLL Synthesizer, XEN = 1, TXON = 1						
B_{LOOP}	Loop bandwidth, Note 3	f_{TXAL} = 9.84 MHz		320		kHz
		f_{TXAL} = 13.56 MHz		430		kHz
PN_{PLL}	Phase noise	PAM = “10”, ACON = “1111”				
	Matched into 50 Ω, R_L ~ 200 Ω	10 kHz offset		-86	-66	dBc/Hz
		100 kHz offset		-84	-64	dBc/Hz
		1 MHz offset		-92	-72	dBc/Hz
		10 MHz offset		-115	-95	dBc/Hz
E_{REF}	Reference spurious emissions	ACON = “1111”, PAM = ‘10’		-45	-35	dBc
	$f_{TX} \pm f_{XTAL}$					
t_{ACQ}	PLL Acquisition time	XEN = 1, TXON = 1		0.1	0.5	ms
Power Amplifier, XEN = 1, TXON = 1, Note 4						
P_{OUT}	Output power	ACON = “1111”, PAM = ‘10’				
	f_{TX} = 315 MHz, matched into 50 Ω	RL ~ 200 Ω	5.8	8.5	10.6	dBm
		RL ~ 700 Ω	2.2	4.0	5.5	dBm
		ACON = “1111”, PAM = ‘00’				
		RL ~ 700 Ω	-16	-7	2	dBm
		ACON = “0000”, PAM = ‘10’			-45	dBm
P_{OUT}	Output power	ACON = “1111”, PAM = ‘10’				
	f_{TX} = 434 MHz, matched into 50 Ω	RL ~ 200 Ω	6.5	9.0	11	dBm
		RL ~ 700 Ω	2.2	4.5	6.5	dBm
		ACON = “1111”, PAM = ‘00’				
		RL ~ 700 Ω	-11.5	-4	3	dBm
		ACON = “0000”, PAM = ‘10’			-45	dBm
Power Amplifier, XEN = 1, TXON = 1 at 25°C, Note 4						

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
P_{OUT}	Output power f_{TX} = 315 MHz, matched into 50 Ω	ACON = “1111”, PAM = ‘10’ RL ~ 200 Ω RL ~ 700 Ω ACON = “1111”, PAM = ‘00’ RL ~ 700 Ω	 6.8 2.7 -15	 8.5 4.0 -7	 10.2 5.1 1	 dBm dBm dBm
P_{OUT}	Output power f_{TX} = 434 MHz, matched into 50 Ω	ACON = “1111”, PAM = ‘10’ RL ~ 200 Ω RL ~ 700 Ω ACON = “1111”, PAM = ‘00’ RL ~ 700	 7.5 3 -10.5	 9.0 4.5 -4	 10.5 6.0 2.5	 dBm dBm dBm
Modulation						
$f_{MOD,ASK}$	ASK modulation frequency	Duty cycle 50%			20	kHz
$f_{MOD,ASK}$	FSK modulation frequency	Duty cycle 50%			20	kHz
Duty Cycle of modulated signal, Note 5						
$t_{DUTY,FSK}$	Duty cycle of modulated FSK signal	Duty cycle (mod. Signal) 50%, f_{TXAL} = 9.84 MHz, Tamb = 25°C, OG = 3, Modulation: 9.6 kHz FCON = 0 - FCON = 63_D	45		55	%

Notes

1. The given RMARGIN (Oscillation margin) is tested and guaranteed only at room temperature (Tamb = 25°C) and a supply voltage of VBAT = VDDA = 2.2V and oscillator gain setting OG = 1 for fXTAL = 9.84 MHz and OG = 0 for fXTAL = 13.56 MHz. To guarantee sufficient oscillation startup margin every reference application board has to be checked individually by the customer.
2. The specified crystal oscillator settling time has been characterized using the crystal type NX5032SA from NDK. The oscillator settling time is mainly influenced by the crystal parameter C1 (motional capacitance) and R1, and also depends on the capacitive load that is provided to the pin XTAL1 (incorporating the crystal shunt capacitor C0, crystal soldering pad capacitances, application board wiring capacitances, etc.). It is recommended to customers to verify the oscillator settling time for any application in order to assess the impact of the used crystal type and board.
   At the XTAL1 pin a minimum capacitive load at of 1.7 pF is required. Going below this limit with the application design could lead to unwanted self-oscillation of the XTAL oscillator, preventing or delaying the oscillator to settle to the wanted crystal frequency. In case a crystal type with very small package is selected, it might be beneficial to add a small external capacitor to XTAL1 pin. Further details are provided in the application note AN-CAI 1410.
3. Derived from chip simulation, not tested.
4. Load tank circuit according to Figure 53.
5. Application advice, the duty cycle is not measured during production test. It is strongly recommended to check every reference application board by the customer individually, since PCB parasitic and the chosen type of XTAL influence the duty-cycle.

18 TIMING CHARACTERISTICS

18.1 General

V_{BAT} = 2.1V to 3.6V, Tamb = -40 to +85°C (Pin TEST connected to VSS).
Unless otherwise specified.

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
On-chip RC Oscillator, Note 1						
T_{OSC}	Clock period	Tamb = -20 to +85°C	0.23	0.25	0.27	µs
T_{OSC}	Clock period		0.225	0.25	0.275	µs
$T\Delta_{OSC,D}$	Oscillator clock jitter	V_{BAT} = 3.0V, Note 3			10	ns
System Clock						
T_{SYS}	System Clock				2.2	MHz
T_{XDCLK}	Divided XTAL Clock				4.4	MHz
Reference Clock						
T_{REF}	Reference Clock	Note 2	87.5	125	137.5	kHz
External Clock via P15 (XCLK)						
f_{XCLK}	External clock frequency				3.5	MHz
t_{XCH}	External clock high time		125			ns
t_{XCL}	External clock low time		125			ns
t_{XCR}	External clock rise time				0.5	µs
t_{XCF}	External clock fall time				0.5	µs
Power Management						
$T_{POR-HLD}$	Power On Reset Hold time			200	480	µs
t_{BOOT}	Device Boot time	Note 4			750	us
T_{PSMF}	Port Sense mono-flop duration		5		100	us
Voltage Comparator						
t_{CSET}	Comparator settling time				2	µs
t_{RSET}	Reference Voltage settling time				20	µs
EEPROM						
T_{RET}	Data retention time	Tamb = 50°C	20			years
N_{WR-CYL}	Write endurance EEPROM	Tamb = 25°C, Note 6	200 k			cycle
N_{E-ROM}	Write endurance E-ROM	Tamb = 25°C, Note 7	10 k			cycle
t_{EEPU}	EEPROM Power Up time				8	µs
t_{EEDLY}	EEPROM Access delay				3	µs
t_{ERWR}	ERASE/WRITE time EEPROM	Note 5		384		T_{REF}

Notes

1. Due to test concept reasons, reference is made to the RC Oscillator clock divided by two.
2. When the device is clocked from the XTAL Oscillator, the corresponding clock divider must be set in a way that the specification for T_{REF} is satisfied.
3. Value represents the maximum deviation from nominal clock period. No supply voltage ripple present.
4. Under normal operation, meaning Monitor and Download Interface disabled (MSDA = 1).
5. Value holds for the EEPROM circuitry ERASE/WRITE time. Some readily available ROM Library functions may perform multiple EARSE/WRITE operation, see also section 22.
6. Endurance test is performed by a corresponding monitor flow at a product with structural similarity regarding the EEPROM cell design. According to Arhennius' Law, assuming an activation energy of 0.15eV, the number of useful cycles at room temperature is about 2.5 times higher than at 85°C.
7. E-ROM ERASE/WRITE supported at VBAT $\geq$ 2.5 V only.

19 TEST SETUP

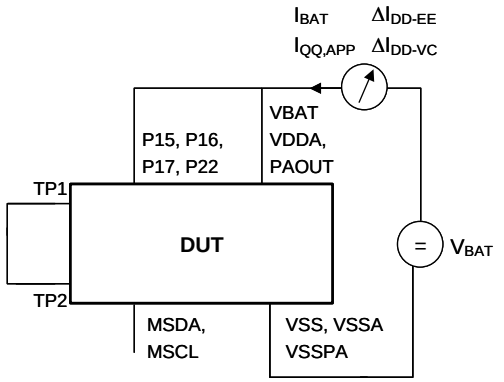
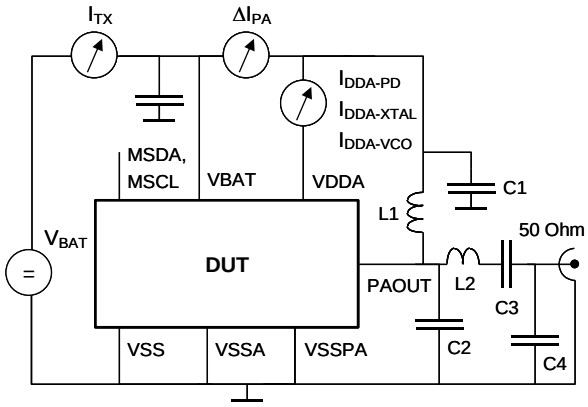


Figure 52. Operating Conditions measurement setup



f_{TX}	315 MHz		434 MHz	
RL	≈ 200 Ω	≈ 700 Ω	≈ 200 Ω	≈ 700 Ω
L1	150n	150n	120n	120n
L2	33n	33n	22n	27n
C1	330p	330p	220p	220p
C2	8p2 + 1p5	6p8 + 1p5	6p8	2p2 + 2p2
C3	56 p	56 p	27p	27p
C4	18p + 1p	39p + 3p3	12p + 3p3	22p + 2p2

Figure 53. Power Amplifier measurement setup

20 ANOMALY NOTES

This section provides additional information concerning known anomalies discovered with the device and reports changes that are subject to implementation with future device versions.

21 APPLICATION NOTES

This section provides additional information concerning device application and highlights differences in the device operation, when compared with the existing product family.

Additional information is provided by the application note AN01034 Software Development for PCF7X41ATS, which may be applied for the PCF7922 also see section 22.

21.1 Avoid leakage current in POWER-OFF mode

Some device ports (P15, P16 and P22) do not feature on-chip pull-up or pull-down and corresponding measures are required externally, when these ports are operated in input mode. Notice that all ports operate in input mode, while the device resides in POWER-OFF mode. Thus, pull-up or pull-down measures are required to avoid floating ports that would result in unwanted leakage currents draining the battery.

However, pull-down measures need to be considered carefully, as an accidental device wake up may occur when the device is about to enter POWER-OFF mode, see 21.5.

21.2 LED output configuration

In case an LED is desired for visual user acknowledgment, an additional weak shunt resistor must be provided across the LED, in order to avoid unwanted leakage current draining the battery. Please notice the typical application diagram, see section 0.

Due to the given voltage drop across the LED, the LED cannot be considered to serve as a suitable pull-up for the corresponding port, while the port operates in input mode (e.g. during device POWER-OFF mode). A weak shunt resistor across the LED terminates the corresponding port properly.

21.3 Avoid device Lock-Up in INIT

The device INIT mode is the factory supplied default and used while developing software and during device personalization, in order to initialize the EEPROM content.

Consequently, the Monitor and Download interface is operational in INIT mode and a low pulse on the MSDA pin would be treated as a breakpoint event. Consequently, the part will stop executing the application program, waiting for further debug commands. If no further commands are received, the part will idle forever, which in the user's perspective may be interpreted as a Lock-Up situation.

The device will idle until either a Download command is received or the battery is disconnected and applied again, causing the device to execute a power on reset and to terminate the Download mode.

The low pulse on the MSDA pin may origin from any kind of sources; an ESD pulse, EMC Noise or PCB cross talk.

To avoid unwanted device Lock-Ups during prototyping or in the field, the device shall be put into PROTECTED Mode once the EROM and EEPROM are initialized and device debugging is completed. In PROTECTED Mode the debug and breakpoint feature is disabled and any low pulses on MSDA pin will be ignored, causing the device to execute the application code as desired.

The device may be forced into PROTECTED mode and back into INIT mode again, by dedicated Monitor and Debugs commands, see section 11 and 14.

21.4 Entering POWER-OFF Mode

When entering the POWER-OFF mode, the application program must be aware of residual charge, which causes the device to continue program execution for a short time, before a Power On Reset condition applies and POWER-OFF mode is entered finally.

In order to cope with such situations, a sequence of instructions should be used as follows:

```
;Force the device into POWER-OFF mode
;
     SETB  POFF
inf: JMP   inf   ;Consume up residual charge
```

The first instruction clears the PMODE flip-flop and disconnects the battery from the internal supply (V_{DD}). The second instruction will be executed repeatedly, until the internal supply dropped below the power on reset threshold ($V_{POR,BAT}$) and the POWER-OFF mode is entered finally.

Note that a Port Wake Up condition may be present before (port high-to-low transition), but would not be detected and ignored, until the power on reset condition applies, enabling the Supply Switch Logic again, see also section 8.1.

Note, that a Port Interrupt is not recognized, unless the Interrupt System is configured accordingly before the endless loop is entered. The following alternate sequence of instructions tries to enter POWER-OFF mode, but accepts a Port Interrupt and generates a Reset in case:

```
;Force the device into POWER-OFF mode
;Port Interrupts are enabled
;
     SETB  EP
     SETB  POFF
     SETB  IDLE
     SETB  RST
```

In any case, please also be aware of an accidental device Wake Up, according to section 21.5.

21.5 Avoid accidental device Wake Up

In case a pull-down like load is connected to any of the three port lines of P15, P16 or P22 and the device drives the corresponding port line HIGH before entering the POWER-OFF mode, an unintended device Wake Up condition may occur. Since the mentioned ports are forced into input mode, when entering POWER-OFF mode, a high-to-low transition will occur (e.g. eventually delayed due to capacitive load) that will trigger the corresponding Port Sense mono-flop. Similar, operating the ports in output mode and forcing a high-to-low transition triggers the mono-flop also. If the mono-flop is still in its "triggered" state, in the moment the Power On Reset condition applies, the device will instantly power-up again (see also section 8.3). Depending on the application program, this may initiate an endless loop.

To prevent the application from such situations, the following sequence of instructions is recommended, before the POWER-OFF mode is entered:

```
;Force the device into POWER-OFF mode and
;avoid accidentally Wake Up
;
     CLR   P1DIR ;switch all ports to input
     CLR   P2DIR
     CALL  delay ;T = TPSMF + application delay
                 ;
     SETB  POFF  ;Disconnect battery
inf: JMP   inf   ;Wait for power-off
```

The above sequence forces all port to input mode and waits for a certain time. The delay needs to exceed the Port Sense mono-flop duration (T_{PSMF}) plus the time the external circuitry needs to establish static conditions at the port lines. Finally, the POWER-OFF mode is invoked and an endless loop is entered to consume up remaining stored charge, see also 21.4.

21.6 Device operating mode after battery power-up

In the moment of a battery power-up sequence, the device either enters POWER-OFF or BATTERY Mode. Thus, the application program can not detect, if the battery has been changed or is inserted.

E.g. during battery power-up, the Port Sense Logic may signal a Port Wake-Up condition, because battery contact noise may trigger the corresponding port mono-flop or because the port input voltage develops slower than the device supply voltage at pin VBAT. Consequently, the Port Wake UP flip-flop is set and BATTERY Mode is entered. Depending on the contact noise duration, even the Port Interrupt may be triggered.

In any case, the application program shall poll the corresponding ports to verify the Wake Up condition and act as required.

21.7 Controlling the XTAL Oscillator Gain properly

For proper XTAL oscillator operation it is mandatory to control the XTAL Oscillator Gain correctly via the control bits OG (Register TXCON1, see section 11.4.1).

Prior to XTAL Oscillator start up it is mandatory to select the appropriate gain (e. g. 9.84 MHz: OG = “01”), in order to establish the largest oscillation margin and ensure fast start up.

Once the XTAL Oscillator started, the Oscillator Gain need to be reduced accordingly, in case FSK modulation shall be applied.

Additional information is provided by the application note AN-CAI 1410 PCF7961/22 Crystal Selection & Application Board Optimization.

21.8 System Test by monitoring internal clock signals

To ease system test the device features means to monitor the clock frequency of various internal signals, e.g. XTAL Clock, RC Oscillator and System Clock.

The mentioned clock signals can be output via Port 14 and P22, by invoking the corresponding ROM Library function (PLL_CLOCK_OUT, function code: 7Ah), see Table 49. The affected Port (P14, P22) must not be driven externally during this system test, in order to avoid a short circuit situation.

Table 49 Clock Monitor Selection

R3	Clock	Port	Comment
00h			Disabled
01h	T_{XTAL}	P22	XTAL clock
02h	T_{XDCLK}	P22	Divided XTAL clock
10h	T_{OSC}	P14	4 MHz RC clock
20h	T_{XDCLK}	P14	Divided XTAL clock
30h	T_{SYS}	P14	System clock

The monitor operation is maintained until it is disabled again or a Power On Reset is applied. The mentioned ROM Library function may be invoked as follows.

```
;Activate the Clock Monitor via Port P14/ P22
;Port Interrupts are enabled
;
     MOV   R4, #7AH
     MOV   R3, Clock_under_Test
     SYS
     ; - start Test
     ;...
     ;...
     ;...
     ; - end Test-
     MOV   R4, #7AH
     MOV   R3, #00H
     SYS
```

Note

1. The system call ADD_CLOCK_OUT (function code: 7AH) uses 4 byte of STACK and executes in 21 cycles. It does configure the Port P14 and P22 as required.

22 RELATED DOCUMENTS

Type	Name / Reference	Description
Data Sheet	MRK II Family	Architecture and Instruction Set
Data Sheet	PCF7x22 ROM Library	Implementation and Description
Data Sheet	PCF7x22 Monitor and Download Interface	Functional Description
Application Note	AN01034	Software Development for PCF7X41ATS (STARC 2XLite)
Application Note	AN-CAI 1410	PCF7961/22 Crystal Selection & Application Board Optimization

23 DEVELOPMENT TOOLS

Reference	Name	Description
OM6710	RIDE	Software development suite
OM6713	Universal Download and Debug Board (U-DDB)	Hardware and software Interface between host PC and target device.

24 REVISION HISTORY

Revision	Page	Description
2003 Sep 30		First release Objective Specification (device version T2)
2004 Oct 12		First release Preliminary Specification (device version V0D)
2005 Jul 24		First release Product Specification See DETAILED REVISION HISTORY (next page) for details
2005 Oct 14		Editorial changes and corrections
	19	EEPROM Product Identifier corrected, which must yield 8H rather than 6h.
	52	XTAL Oscillator description revised, since the XTAL Oscillator need to be initialized prior to use.
	58	Power Amplifier Control and ASK Modulation corrected revised, since control bit ACM no longer supported.
	60	DEVICE MODES updated, as the device may be recovered from TAMPERED mode.
	68	UHF Transmitter AC/DC Conditions for Power Amplifier at 25°C added
	74 75	APPLICATION NOTES corrected concerning ports affected + Avoid leakage current in POWER-OFF mode + Avoid accidental device Wake Up
	75 76	APPLICATION NOTES added + Controlling the XTAL Oscillator Gain properly + System Test by monitoring internal clock signals
	72	TEST SETUP Figure 52 updated.
	75	APPLICATION NOTES Controlling the XTAL Oscillator Gain properly added
	77	RELATED DOCUMENTS updated. Reference to PCF7x22 ROM Library and Monitor and Download Interface included

		Update to NXP
2005 Jul 24		Editorial changes and corrections + Datasheet status changed to Product Specification

DETAILED REVISION HISTORY

Revision	Page	Description
	61	BOOT ROUTINE updated, as the device may be recovered from TAMPERED mode.
	19 62	Product Identifier corrected and which must yield 8H rather than 6h. The device uses the same product type identifier (PI) than PCF7x61.
	64	Operating Conditions updated to fit device characterization results + I_{QQ} removed and as it is covered by $I_{QQ,APP}$ already + Device executes from E-ROM, TYP parameters $I_{CC-125k}$, $I_{CC-IDLE}$, $I_{BAT-125k}$ and $I_{BAT-IDLE}$ revised
	67	UHF Transmitter Operating Conditions updated to fit device characterization results + Condition VBAT = 3.0V added for supply current specification + Power-Down supply current I_{DDA-PD} MAX revised + Supply current XTAL Oscillator conditions changed, $I_{DDA-XTAL}$ TYP revised and TBD closed + Supply current VCO conditions changed, $I_{DDA-VCO}$ TYP revised and TBD closed + Power Amplifier supply current conditions and I_{PA} TYP revised and TBD closed.
	68	UHF Transmitter AC/DC Conditions updated to fit characterization + C_{TX1} slightly increased, by about 2pF + C_{TX2} TYP values revised + XTAL OSC settling time, t_{XTSET}, revised and TBD closed + PLL Phase noise, $PN_{PLL,}$ revised and TBD closed + PLL Acquisition time, t_{ACQ}, revised + Reference spurious, E_{REF}, TBD closed. + Output Power, P_{OUT}; revised
	70	TIMING CHARACTERISTICS updated. +The RC Oscillator specification no longer refers to the divider clock, instead to the RC OSC output. + RC Oscillator, T_{OSC}, MAX value for –40°C to 85°C corrected.
	72	TEST SETUP Figure 53 updated.
2010 Nov 18		Editorial changes, update Legal Information
2011 Aug 16	80 7	Update legal information Update Ordering information Editorial changes Removed TSSOP28 option
2011 Aug 29		Editorial Changes.
2012 Jan 11	7 80	Corrected ORDERING INFORMATION. Update LEGAL INFORMATION. “unique” is replaced with “quasi unique”
2013 Feb 14	7 16	Update ORDERING INFORMATION. Added 8 KB E-ROM version. Update Figure Application Code Memory Editorial Changes.
2013 May 07	14	Corrected Figure 7. Port Sense Logic.
2013 Oct 18	7 16	Updated Ordering Information. Correction of Figure Application Code Memory. Editorial Changes.

Revision	Page	Description
2014 Mar 03	7	Updated ORDERING INFORMATION.
2014 Jul 30	7	Updated ORDERING INFORMATION.
2015 May 11	68 77	Chapter 17.4 UHF Transmitter AC/DC Conditions, added crystal and settling time information. Chapter, 22 RELATED DOCUMENTS, added Application Note reference to AN-CAI 1410. Editorial changes.

25 LEGAL INFORMATION

25.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification or product development
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification
Product [short] data sheet	Production	This document contains the product specification

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

25.2 Definitions

Draft

The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet

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26 Contact information

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