LITE-ON SEMICONDUCTOR

T16M5T600B

SENSITIVE GATE TRIACS
SILLICON BIDIRECTIONAL THYSISTORS

TRIACS
16 AMPERES RMS
600V VOLTS

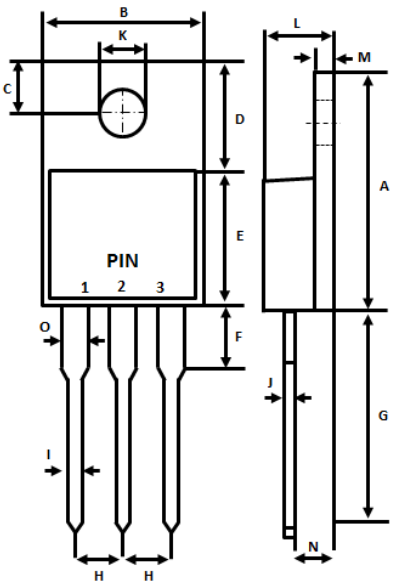
FEATURES

- Sensitive gate allows triggering by microcontrollers and other
- Maximum values of IGT, VGT and IH specified for Ease of Design
- On-state current rating of 15A RMS at 70˚C
- Blocking voltage to 600V
- Uniform gate trigger current in three quadrants, Q1, Q2, and Q3.
- Pb free package

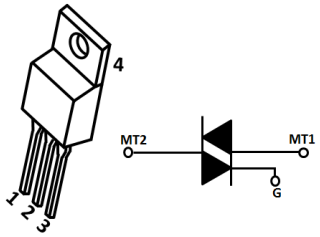
MECHANICAL DATA

- Case material: Molded plastic
- Weight: 0.07 ounces, 2.0 grams

TO-220AB



TO-220AB		
DIM.	MIN.	MAX
A	14.22	15.88
B	9.65	10.67
C	2.54	3.43
D	5.84	6.86
E	8.26	9.28
F	--	6.35
G	12.7	14.73
H	2.29	2.79
I	0.51	1.14
J	0.30	0.64
K	3.53Ø	4.09Ø
L	3.56	4.83
M	1.14	1.40
N	2.03	2.92
O	1.17	1.37
All dimensions in millimeter		



PIN ASSIGNMENT	
1	Main terminal 1
2	Main terminal 2
3	Gate
4	Main terminal 2

MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS

Ratings at 25˚C ambient temperature unless otherwise specified.

PARAMETER	SYMBOL	VALUE	UNIT
Peak repetitive off-state voltage (T_J = - 40 to 110˚C, full sine wave, 50 to 60H_Z, gate open, Note 1)	V_{DRM} V_{RRM}	600	V
On-stage RMS current (full sine wave 50 to 60H_Z, Tc = +70˚C)	$I_{T(RMS)}$	16	A
Peak non-repetitive surge current (one full sine wave @ 60H_Z, T_J = +25˚C) Preceded and followed by rated current	I_{TSM}	120	A
Circuit fusing consideration (t = 8.3ms)	I^2T	59	A^2S
Peak gate current (T_C = +70˚C, $T_P \leqq$1.0us)	P_{GM}	20	W
Peak gate power (T_C = +70˚C, t = 8.3ms)	$P_{G(AV)}$	0.5	W
Operating temperature range	T_J	-40 to +150	°C
Storage temperature range	T_{STG}	-40 to +150	°C

Notes:
1. V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

REV.6, AUG-2020, KTXC22

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RATING AND CHARACTERISTIC CURVES
T16M5T600B

THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	VALUE	UNIT
Thermal resistance from junction to heatsink	$RthJ_C$ $RthJ_A$	2.0 62.5	°C/W
Maximum lead temperature for soldering purposes (1/8" form case for 10 seconds)	TL	260	°C

OFF CHARACTERISTICS

PARAMETER		SYMBOL	MAX	UNIT
Peak repetitive forward or reverse blocking current (V_{AK} = rated V_{DRM} and V_{RRM}, gate open)	T_J = 25°C	I_{DRM} I_{RRM}	10	uA
	T_J = 110°C		2.0	mA

ON CHARACTERISTICS

PARAMETER	SYMBOL	MIN.	TYP.	MAX	UNIT
Peak forward on-state voltage (I_{TM} = ± 21A peak @ T_P ≦ 2.0 ms, duty cycle ≦ 2%)	V_{TM}	--	--	1.8	V
Gate trigger current (V_D = 12V, R_L=100Ω)	$I_{GT}1$ $I_{GT}2$ $I_{GT}3$	-- -- --	2.0 3.0 3.0	5.0	mA
Gate trigger voltage (V_D = 12V, R_L=100Ω)	$V_{GT}1$ $V_{GT}2$ $V_{GT}3$	0.45 0.45 0.45	0.62 0.20 0.65	1.5	V
Holding current (V_D = 12V, I_G= ±150mA, gate open)	I_H1	--	3.0	10	mA
Latching current (V_D = 24V, I_G= 50mA)	I_L1 I_L2 I_L3	-- -- --	5.0 10 5.0	15 20 15	mA

DYNAMIC CHARACTERISTICS

PARAMETER	SYMBOL	MIN.	TYP.	UNIT
Critical rate of rise of off-stage voltage (V_{AK} = 67% rated V_{DRM} , exponential waveform @ T_J = 150°C, gate open)	dv/dt	25	75	V/us
Rate of change of commutating current (V_D = 400V, 20V/us , T_J = 150°C)	di/dt(c)	8.0	10	A/ms

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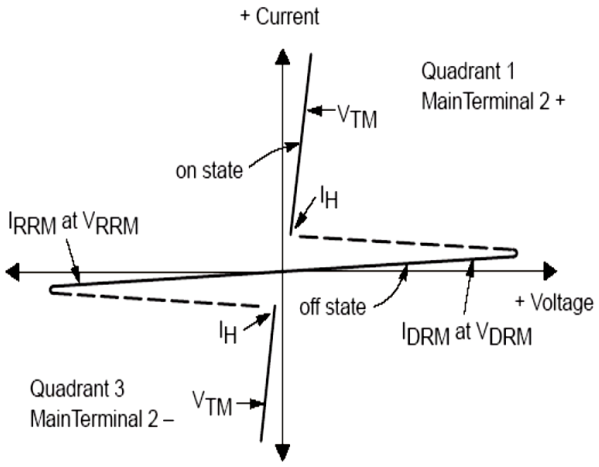
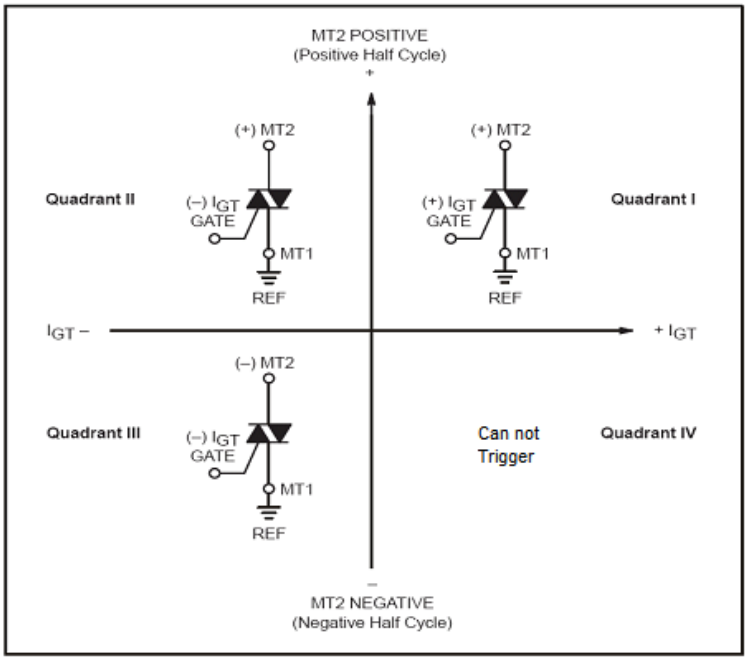
Symbol	Parameter
V_{DRM}	Peak Repetitive Forward Off State Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Reverse Off State Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Maximum On State Voltage
I_H	Holding Current





All polarities are reference to MT1,
with in-phase signal (using standard AC lines) quadrants I and III are used.

RATING AND CHARACTERISTIC CURVES
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FIG.1- RMS current derating

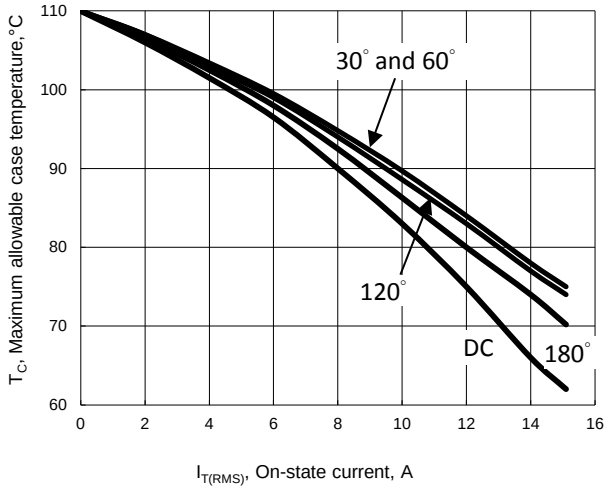

FIG.2- Maximum on-state power dissipation

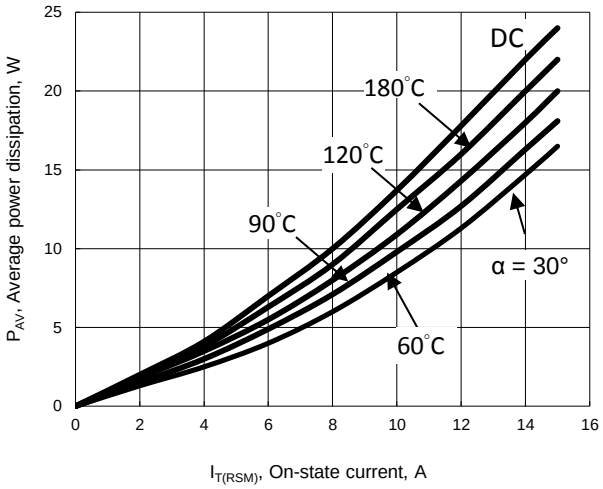

FIG.3- On-state characteristics

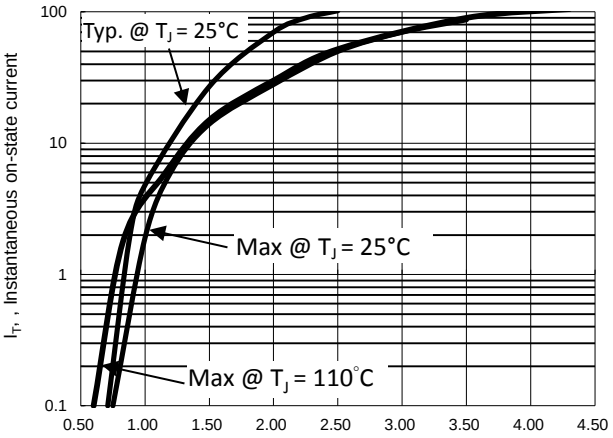

FIG.4- On-state characteristics

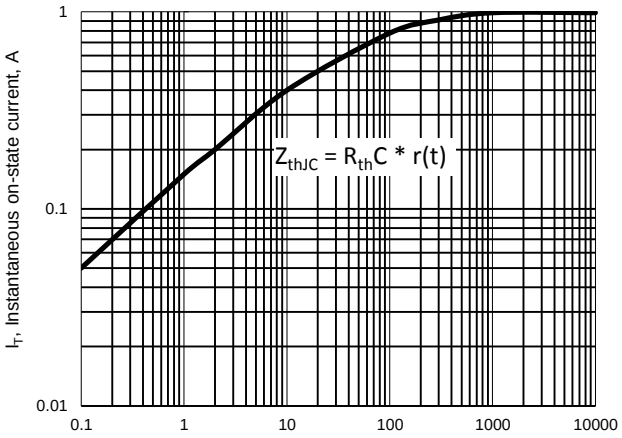

FIG.5- Typical hold current versus junction temperature

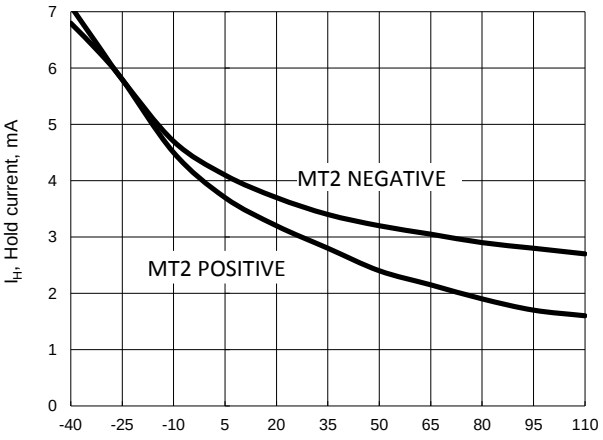

FIG.6- Typical latching current versus junction temperature

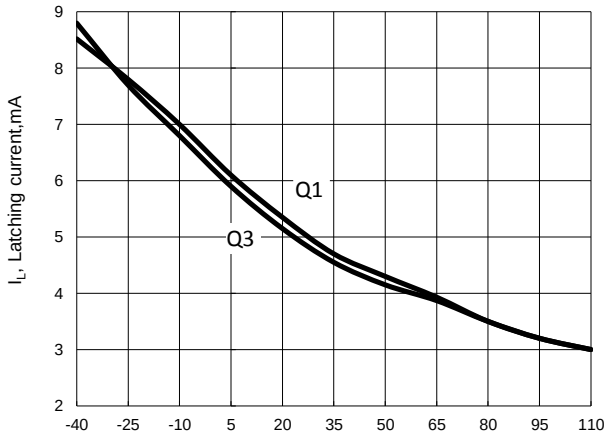

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FIG.7- Typical gate trigger current versus junction temperature

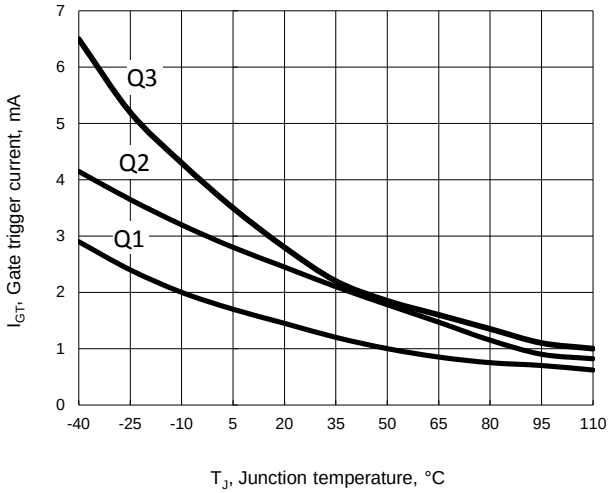


FIG.8 - Typical gate trigger voltage versus junction temperature

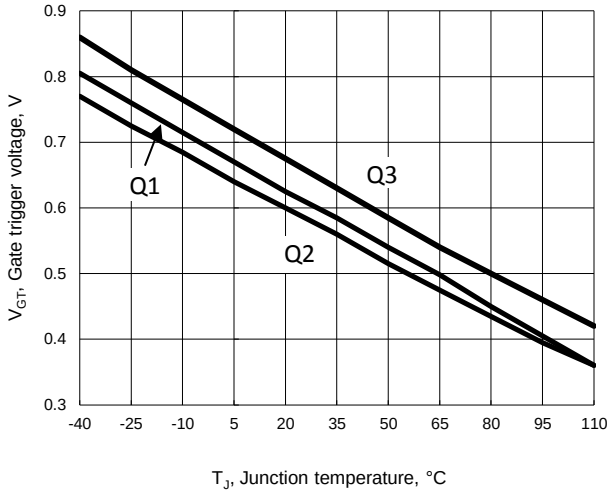


FIG.9- Typical exponential static dv/dt versus gate-MT1 resistance, MT2(+)

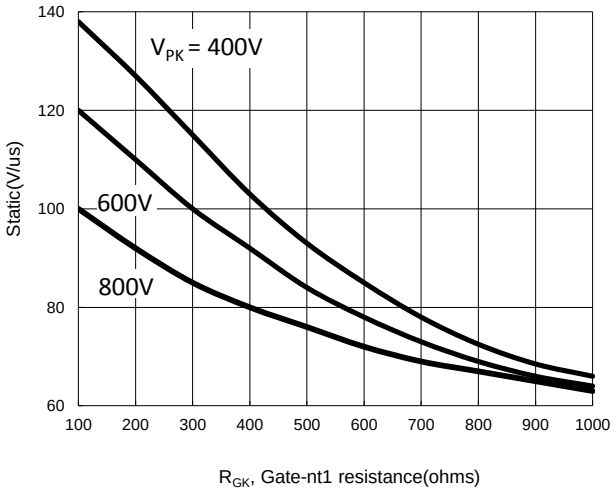


FIG.10- Typical exponential static dv/dt versus peak voltage, MT2(+)

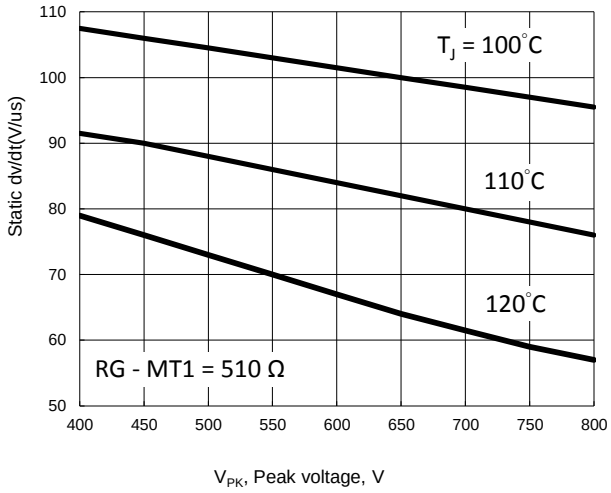


FIG.11- Typical exponential static dv/dt versus junction temperature, MT2(+)

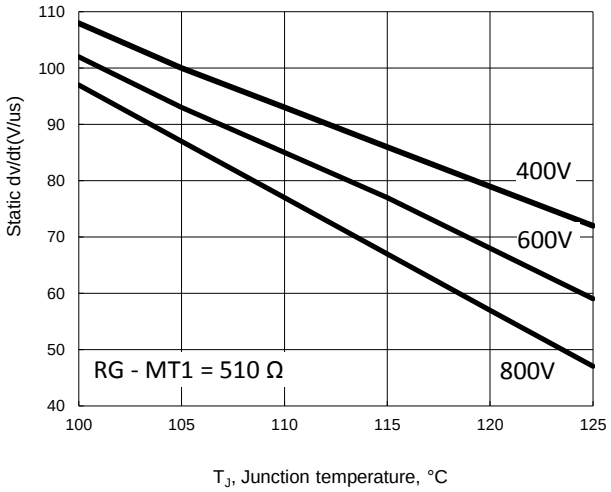
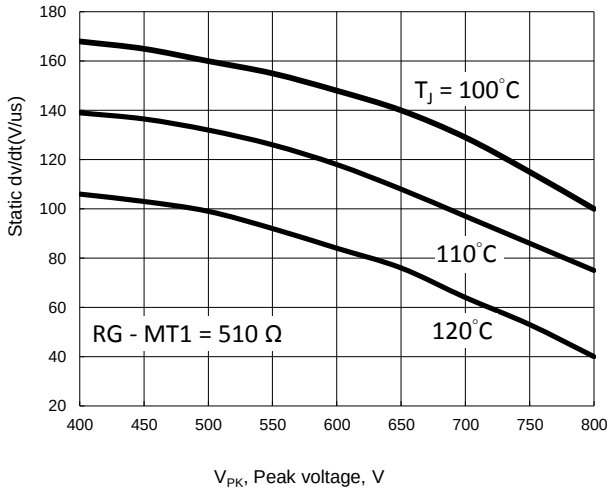


FIG.12- Typical exponential static dv/dt versus peak voltage, MT2(-)



RATING AND CHARACTERISTIC CURVES
T16M5T600HB

FIG.10- Typical exponential static dv/dt versus peak voltage, MT2(+)

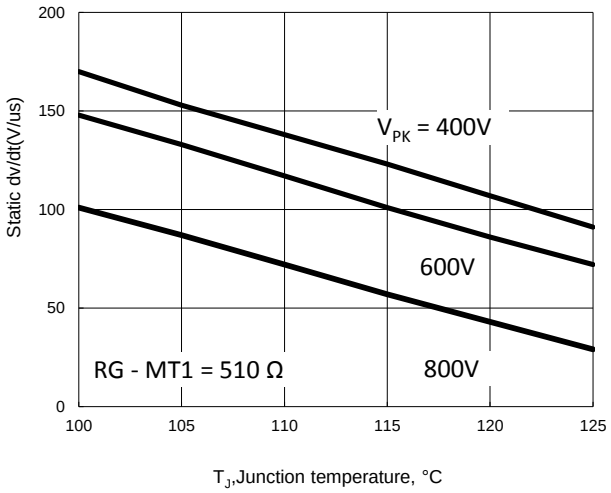
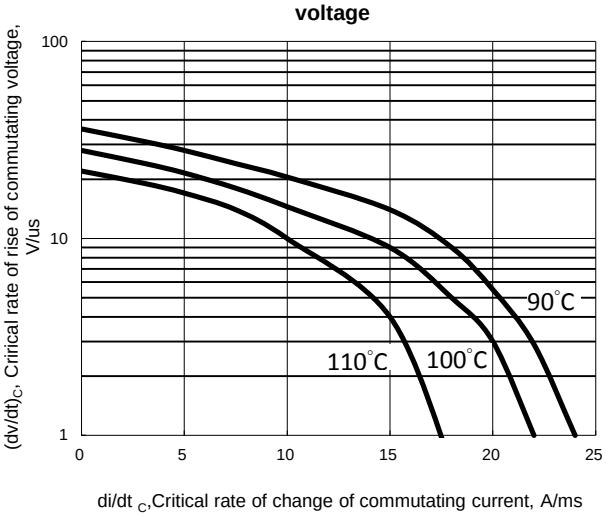


FIG.14- Critical rate of rise of commutating voltage



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