Data Sheet

# ADPL76030

55 V, 1.4 MHz Synchronous 4-Switch Buck-Boost Controller with Spread Spectrum

## FEATURES

- **4-Switch Single Inductor Architecture Allows $V_{IN}$ Above, Below, or Equal to $V_{OUT}$**
- **Up to 95% Efficiency at 1.4 MHz**
- **Proprietary Peak-Buck, Peak-Boost Current-Mode**
- **Wide $V_{IN}$ Range: 4 V to 55 V**
- **±2% Output Voltage Accuracy: 1 V ≤ $V_{OUT}$ ≤ 55 V**
- **±3% Input or Output Current Accuracy with Monitor**
- **Spread Spectrum Frequency Modulation for Low EMI**
- No Top MOSFET Refresh Noise in Buck or Boost
- Adjustable and Synchronizable: 600 kHz to 1.4 MHz
- $V_{OUT}$ Disconnected from $V_{IN}$ During Shutdown

## APPLICATIONS

- Automotive, Industrial, Telecom Systems
- High Frequency, Battery-Powered System

## GENERAL DESCRIPTION

The ADPL76030 is a synchronous 4-switch buck-boost DC/DC controller that regulates output voltage, and input or output current from an input voltage above, below, or equal to the output voltage. The proprietary peak-buck, peak-boost current-mode control scheme allows adjustable and synchronizable 600 kHz to 1.4 MHz fixed frequency operation, or internal 25% triangle spread spectrum frequency modulation for low EMI. With a 4 V to 55 V input voltage range, 0 V to 55 V output voltage capability, and seamless low noise transitions between operation regions, the ADPL76030 is ideal for voltage regulators, and battery and supercapacitor charger applications in automotive, industrial, telecom, and even battery-powered systems.

The ADPL76030 provides input or output current monitor and power good flag. Fault protection is also provided to detect output short-circuit condition, during which the ADPL76030 retries, latches off, or keeps running.



## TYPICAL APPLICATION

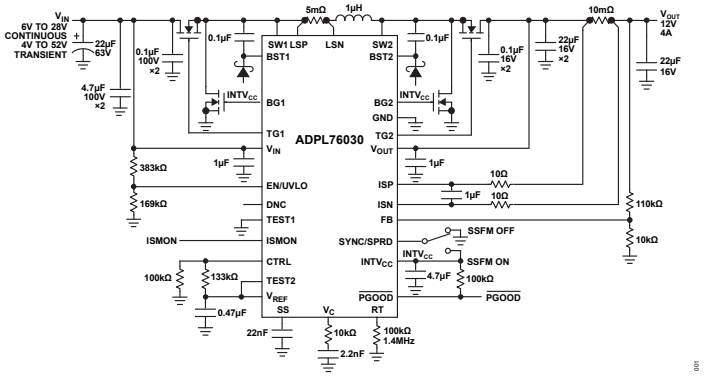


*Figure 1. 95% Efficient 48 W (12 V, 4 A,) 1.4 MHz Buck-Boost Voltage Regulator*

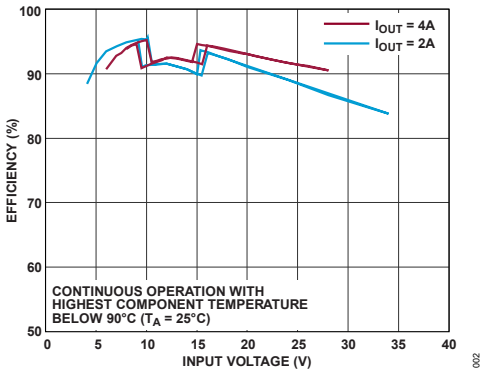


*Figure 2. Efficiency vs. $V_{IN}$*



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# SPECIFICATIONS

**Table 1. Electrical Characteristics**

(Specifications are at $T_A$ = 25°C (Note 2). $V_{IN}$ = 12 V, $V_{EN/UVLO}$ = 1.5 V, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS/COMMENTS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **Supply** | | | | | | |
| $V_{IN}$ Operating Voltage Range | | −40°C ≤ $T_J$ ≤ 125°C | 4 | | 55 | V |
| $V_{IN}$ Quiescent Current | | $V_{EN/UVLO}$ = 0.3 V | | 1 | 2 | µA |
| | | $V_{EN/UVLO}$ = 1.1 V | | 270 | | |
| | | Not Switching | | 2.1 | 2.8 | mA |
| $V_{OUT}$ Voltage Range | | −40°C ≤ $T_J$ ≤ 125°C | 0 | | 55 | V |
| $V_{OUT}$ Quiescent Current | | $V_{EN/UVLO}$ = 0.3 V, $V_{OUT}$ = 12 V | | 0.1 | 0.5 | µA |
| | | $V_{EN/UVLO}$ = 1.1 V, $V_{OUT}$ = 12 V | | 0.1 | 0.5 | |
| | | Not Switching, $V_{OUT}$ = 12 V | 20 | 40 | 60 | |
| **Linear Regulators** | | | | | | |
| $INTV_{CC}$ Regulation Voltage | | $I_{INTVCC}$ = 20 mA | 4.85 | 5.0 | 5.15 | V |
| $INTV_{CC}$ Current Limit | | $V_{INTVCC}$ = 4.5 V | 80 | 145 | 190 | mA |
| $INTV_{CC}$ Dropout Voltage ($V_{IN}$ – $INTV_{CC}$) | | $I_{INTVCC}$ = 20 mA, $V_{IN}$ = 4 V | | 160 | | mV |
| $INTV_{CC}$ Undervoltage Lockout Threshold | | Falling | 3.3 | 3.54 | 3.64 | V |
| $INTV_{CC}$ Undervoltage Lockout Hysteresis | | | | 0.24 | | V |
| $V_{REF}$ Regulation Voltage | | $I_{VREF}$ = 100 µA, −40°C ≤ $T_J$ ≤ 125°C | 1.96 | 2.00 | 2.04 | V |
| $V_{REF}$ Load Regulation | | $I_{VREF}$ = 0 mA to 1 mA | | 0.4 | | % |
| $V_{REF}$ Line Regulation | | $I_{VREF}$ = 100 µA, $V_{IN}$ = 4 V to 55 V | | 0.1 | | % |
| $V_{REF}$ Current Limit | | $V_{REF}$ = 1.8 V | 1.5 | 2.5 | 3.5 | mA |

(Specifications are at $T_A$ = 25°C (Note 2). $V_{IN}$ = 12 V, $V_{EN/UVLO}$ = 1.5 V, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS/COMMENTS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{REF}$ Undervoltage Lockout Threshold | | Falling | | | 1.84 | | V |
| $V_{REF}$ Undervoltage Lockout Hysteresis | | | | | 50 | | mV |
| **Control Inputs/Outputs** | | | | | | | |
| EN/UVLO Shutdown Threshold | | −40°C ≤ $T_J$ ≤ 125°C | | 0.3 | 0.6 | 1.0 | V |
| EN/UVLO Enable Threshold | | Falling | −40°C ≤ $T_J$ ≤ 125°C | 1.196 | 1.220 | 1.244 | V |
| EN/UVLO Hysteresis Current | | $V_{EN/UVLO}$ = 0.3 V | | −0.1 | 0 | 0.1 | µA |
| | | $V_{EN/UVLO}$ = 1.1 V | | 2.1 | 2.5 | 2.9 | |
| | | $V_{EN/UVLO}$ = 1.3 V | | −0.1 | 0 | 0.1 | |
| CTRL Input Bias Current | | $V_{CTRL}$ = 0.75 V, Current Out of Pin | | 0 | 20 | 50 | nA |
| CTRL Latch-Off Threshold | | Falling | | 285 | 300 | 315 | mV |
| CTRL Latch-Off Hysteresis | | | | | 25 | | mV |
| **Error Amplifier** | | | | | | | |
| Full Scale Current Regulation $V_{(ISP-ISN)}$ | | $V_{CTRL}$ = 2 V, $V_{ISP}$ = 12 V | −40°C ≤ $T_J$ ≤ 125°C | 96 | 100 | 104 | mV |
| | | $V_{CTRL}$ = 2 V, $V_{ISP}$ = 0 V | −40°C ≤ $T_J$ ≤ 125°C | 96 | 100 | 104 | |
| 1/10th Current Regulation $V_{(ISP-ISN)}$ | | $V_{CTRL}$ = 0.35 V, $V_{ISP}$ = 12 V | | 8 | 10 | 12 | mV |
| | | $V_{CTRL}$ = 0.35 V, $V_{ISP}$ = 0 V | | 8 | 10 | 12 | |
| ISMON Monitor Output $V_{ISMON}$ | | $V_{(ISP-ISN)}$ = 100 mV, $V_{ISP}$ = 12 V/0 V | −40°C ≤ $T_J$ ≤ 125°C | 1.20 | 1.25 | 1.30 | V |
| | | $V_{(ISP-ISN)}$ = 10 mV, $V_{ISP}$ = 12 V/0 V | −40°C ≤ $T_J$ ≤ 125°C | 0.30 | 0.35 | 0.40 | |

(Specifications are at $T_A$ = 25°C (Note 2). $V_{IN}$ = 12 V, $V_{EN/UVLO}$ = 1.5 V, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS/COMMENTS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| | | $V_{(ISP-ISN)}$ = 0 mV, $V_{ISP}$ = 12 V/0 V | −40°C ≤ $T_J$ ≤ 125°C | 0.20 | 0.25 | 0.30 | |
| ISP/ISN Input Common Mode Range | | −40°C ≤ $T_J$ ≤ 125°C | | 0 | | 55 | V |
| ISP/ISN Low Side to High Side Switchover Voltage | | $V_{ISP}$ = $V_{ISN}$ | | | 1.8 | | V |
| ISP/ISN High Side to Low Side Switchover Voltage | | $V_{ISP}$ = $V_{ISN}$ | | | 1.7 | | V |
| ISP Input Bias Current | | $V_{ISP}$ = $V_{ISN}$ = 12 V | | | 23 | | µA |
| | | $V_{ISP}$ = $V_{ISN}$ = 0 V | | | −10 | | |
| | | $V_{EN/UVLO}$ = 0 V, $V_{ISP}$ = $V_{ISN}$ = 12 V or 0 V | | | 0 | | |
| ISN Input Bias Current | | $V_{ISP}$ = $V_{ISN}$ = 12 V | | | 23 | | µA |
| | | $V_{ISP}$ = $V_{ISN}$ = 0 V | | | −10 | | |
| | | $V_{EN/UVLO}$ = 0 V, $V_{ISP}$ = $V_{ISN}$ = 12 V or 0 V | | | 0 | | |
| ISP/ISN Current Regulation Amplifier $g_m$ | | | | | 2000 | | µs |
| FB Regulation Voltage | | $V_C$ = 1.2V | −40°C ≤ $T_J$ ≤ 125°C | 0.98 | 1.00 | 1.02 | V |
| FB Line Regulation | | $V_{IN}$ = 4 V to 55 V | | | 0.2 | | % |
| FB Load Regulation | | | | | 02 | | % |
| FB Voltage Regulation Amplifier $g_m$ | | | | | 660 | | µS |
| FB Input Bias Current | | FB in Regulation, Current Out of Pin | | | 10 | | nA |
| $V_C$ Output Impedance | | | | | 10 | | MΩ |

(Specifications are at $T_A$ = 25°C (Note 2). $V_{IN}$ = 12 V, $V_{EN/UVLO}$ = 1.5 V, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS/COMMENTS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **Current Comparator** | | | | | | | |
| Maximum Current Sense Threshold $V_{(LSP-LSN)}$ | | Buck, $V_{FB}$ = 0.8 V | −40°C ≤ $T_J$ ≤ 125°C | 34 | 50 | 65 | mV |
| | | Boost, $V_{FB}$ = 0.8 V | −40°C ≤ $T_J$ ≤ 125°C | 38 | 50 | 60 | |
| LSP Pin Bias Current | | $V_{LSP}$ = $V_{LSN}$ = 12 V | | | 60 | | µA |
| LSN Pin Bias Current | | $V_{LSP}$ = $V_{LSN}$ = 12 V | | | 60 | | µA |
| **Fault** | | | | | | | |
| FB Overvoltage Threshold ($V_{FB}$) | | Rising | | 1.08 | 1.1 | 1.12 | V |
| FB Overvoltage Hysteresis | | | | 35 | 50 | 65 | mV |
| FB Short Threshold ($V_{FB}$) | | Falling | | | 0.25 | | V |
| FB Short Hysteresis | | Hysteresis | | 35 | 50 | 65 | mV |
| ISP/ISN Over Current Threshold $V_{(ISP-ISN)}$ | | $V_{ISP}$ = 12 V | | | 750 | | mV |
| $\overline{PGOOD}$ Upper Threshold Offset from $V_{FB}$ | | Rising | | 8 | 10 | 12 | % |
| $\overline{PGOOD}$ Lower Threshold Offset from $V_{FB}$ | | Falling | | −12 | −10 | −8 | % |
| $\overline{PGOOD}$ Pull-Down Resistance | | | | | 100 | 200 | Ω |
| SS Hard Pull-Down Resistance | | $V_{EN/UVLO}$ = 1.1 V | | | 100 | 200 | Ω |
| SS Pull-Up Current | | $V_{FB}$ = 0.4 V, $V_{SS}$ = 0 V | | 7.5 | 12.5 | 17.5 | µA |
| SS Pull-Down Current | | $V_{FB}$ = 0.1 V, $V_{SS}$ = 2 V | | 0.75 | 1.25 | 1.75 | µA |

(Specifications are at $T_A$ = 25°C (Note 2). $V_{IN}$ = 12 V, $V_{EN/UVLO}$ = 1.5 V, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS/COMMENTS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| SS Fault Latch-Off Threshold | | | | 1.7 | | V |
| SS Fault Reset Threshold | | | | 0.2 | | V |
| **Oscillator** | | | | | | |
| Switching Frequency | | $V_{SYNC/SPRD}$ = 0 V, $R_T$ = 226 kΩ | | 685 | | kHz |
| | | $V_{SYNC/SPRD}$ = 0 V, $R_T$ = 97.6 kΩ | | 1400 | | |
| SYNC Frequency | | | 600 | | 1400 | kHz |
| SYNC/SPRD Input Bias Current | | $V_{SYNC/SPRD}$ = 5 V | −0.1 | 0 | 0.1 | µA |
| SYNC/SPRD Threshold Voltage | | | 0.4 | | 1.5 | V |
| Highest Spread Spectrum Above Oscillator Frequency | | $V_{SYNC/SPRD}$ = 5 V | 21 | 23 | 25 | % |
| **NMOS Drivers** | | | | | | |
| TG1, TG2 Gate Driver On-Resistance<br>Gate Pull-Up | | $V_{(BST-SW)}$ = 5 V | | 2.6 | | Ω |
| TG1, TG2 Gate Driver On-Resistance<br>Gate Pull-Down | | $V_{(BST-SW)}$ = 5 V | | 1.4 | | Ω |
| BG1, BG2 Gate Driver On-Resistance<br>Gate Pull-Up | | $V_{INTVCC}$ = 5 V | | 3.2 | | Ω |
| BG1, BG2 Gate Driver On-Resistance<br>Gate Pull-Down | | $V_{INTVCC}$ = 5 V | | 1.2 | | Ω |

[1] The ADPL76030 is specified over the −40°C to 125°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Note the maximum ambient temperature consistent with these

specifications is determined by specific operating conditions in conjunction with the board layout, rated package thermal impedance, and other environmental factors.

[2] The ADPL76030 includes overtemperature protection to protect the device during momentary overload conditions. Junction temperature exceeds 125°C when overtemperature protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability.

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C, unless otherwise specified.

**Table 2. Absolute Maximum Ratings**

| PARAMETER | RATING |
|---|---|
| $V_{IN}$, EN/UVLO, $V_{OUT}$, ISP, ISN | 58V |
| (ISP-ISN) | −1V to 1V |
| BST1, BST2 | 66V |
| SW1, SW2, LSP, LSN | −6V to 60V |
| $INTV_{CC}$, (BST1-SW1), (BST2-SW2) | 6V |
| (BST1-LSP), (BST1-LSN) | 6V |
| FB, SYNC/SPRD, CTRL, $\overline{PGOOD}$ | 6V |
| Storage Temperature Range | −65°C to 150°C |
| Operating Junction Temperature Range | −40°C to 125°C |

Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## Thermal Resistance

Thermal performance is directly linked to PCB design and operating environment. Close attention to PCB thermal design is required.

## Electrostatic Discharge (ESD)

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only. Human body model (HBM) per ANSI/ESDA/JEDEC JS-001. Field-induced charged device model (FICDM) and charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

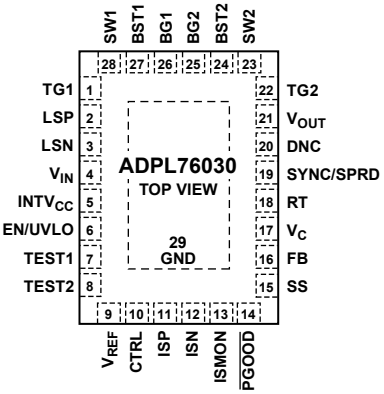
**Table 3. ADPL76030, 28-Lead Plastic QFN**

| ESD Model | Withstand Threshold (V) | Class |
|---|---|---|
| FICDM | ±1250 | C2 |
| HBM | ±3000 | 2 |

## ESD Caution

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS




NOTES
1. $\theta_{JA}$ = 43°C/W, $\theta_{JC}$ = 3.4°C/W.
2. EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB.

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*Figure 3. PIN CONFIGURATION*

**Table 4. Pin Descriptions**

| PIN | NAME | DESCRIPTION |
|---|---|---|
| 1 | TG1 | Buck Side Top Gate Drive. Drives the gate of buck side top N-channel MOSFET with a voltage swing from SW1 to BST1. |
| 2 | LSP | Positive Terminal of the Buck Side Inductor Current-Sense Resistor ($R_{SENSE}$). Ensure accurate current sense with Kelvin connection. |
| 3 | LSN | Negative Terminal of the Buck Side Inductor Current-Sense Resistor ($R_{SENSE}$). Ensure accurate current sense with Kelvin connection. |
| 4 | $V_{IN}$ | Input Supply. The $V_{IN}$ pin must be tied to the power input to determine the buck, buck-boost, or boost operation regions. Locally bypass this pin to ground with a minimum 1 µF ceramic capacitor. |
| 5 | $INTV_{CC}$ | Internal 5 V Linear Regulator Output. The $INTV_{CC}$ linear regulator is supplied from the $V_{IN}$ pin, and powers the internal control circuitry and gate drivers. Locally bypass this pin to ground with a minimum 4.7 µF ceramic capacitor. |
| 6 | EN/UVLO | Enable and Undervoltage Lockout. Force the pin below 0.3 V to shut down the part and reduce $V_{IN}$ quiescent current below 2 µA. Force the pin above 1.233 V for normal operation. The accurate 1.220 V falling threshold can be used to program an undervoltage lockout (UVLO) threshold with a resistor divider from $V_{IN}$ to ground. An accurate 2.5 µA pull-down current allows the programming of $V_{IN}$ UVLO hysteresis. If neither function is used, tie this pin directly to $V_{IN}$. |
| 7 | TEST1 | Factory Test Pin. This pin is used for testing purpose only and must be directly connected to ground for the part to operate properly. |
| 8 | TEST2 | Factory Test Pin. This pin is used for testing purposes only and must be tied to $V_{REF}$ for the part to operate properly. |

| | | |
|---|---|---|
| 9 | $V_{REF}$ | Voltage Reference Output. The $V_{REF}$ pin provides an accurate 2 V reference capable of supplying 1 mA current. Locally bypass this pin to ground with a 0.47 µF ceramic capacitor |
| 10 | CTRL | Control Input for ISP/ISN Current-Sense Threshold. The CTRL pin is used to program the ISP/ISN current limit: $$I_{IS(MAX)} = \frac{Min(V_{CTRL} - 0.25\ V, 1\ V)}{10 \times R_{IS}}$$ The $V_{CTRL}$ can be set by an external voltage reference or a resistor divider from $V_{REF}$ to ground. For 0.3 V ≤ $V_{CTRL}$ ≤ 1.15 V, the current-sense threshold linearly goes up from 5 mV to 90 mV. For $V_{CTRL}$ ≥ 1.35 V, the current-sense threshold is constant at 100 mV full scale value. For 1.15 V ≤ $V_{CTRL}$ ≤ 1.35 V, the current-sense threshold smoothly transitions from the linear function of $V_{CTRL}$ to the 100 mV constant value. Tie CTRL to $V_{REF}$ for the 100 mV full scale threshold. Force the pin below 0.3 V to stop switching. |
| 11 | ISP | Positive Terminal of the ISP/ISN Current-Sense Resistor ($R_{IS}$). Ensure accurate current sense with Kelvin connection. |
| 12 | ISN | Negative Terminal of the ISP/ISN Current-Sense Resistor ($R_{IS}$). Ensure accurate current sense with Kelvin connection. |
| 13 | ISMON | ISP/ISN Current-Sense Monitor Output. The ISMON pin generates a voltage equal to ten times $V_{(ISP-ISN)}$ plus 0.25 V offset voltage. For parallel applications, tie the master ADPL76030 ISMON pin to the slave ADPL76030 CTRL pin. |
| 14 | $\overline{PGOOD}$ | Power Good Open Drain Output. The $\overline{PGOOD}$ pin is pulled low when the FB pin is within ±10% of the final regulation voltage. To function, the pin requires an external pull-up resistor. |
| 15 | SS | Soft-Start Timer Setting. The SS pin is used to set the soft-start timer by connecting a capacitor to ground. An internal 12.5 µA pull-up current charging the external SS capacitor gradually ramps up FB regulation voltage. A 22 nF capacitor is recommended on this pin. Any UVLO or thermal shutdown immediately pulls the SS pin to ground and stops switching. Using a single resistor from SS to $V_{REF}$, the ADPL76030 can be set in three different fault protection modes during output short-circuit condition: hiccup (no resistor), latch-off (499 kΩ), and keep-running (100 kΩ). See more details in the *Applications Information* section. |
| 16 | FB | Voltage Loop Feedback Input. The FB pin is used for constant-voltage regulation and output fault protection. The internal error amplifier with its output $V_C$ regulates $V_{FB}$ to 1.00 V through the DC/DC converter. During output short-circuit ($V_{FB}$ < 0.25 V) condition, the part gets into one fault mode per customer setting. During an overvoltage ($V_{FB}$ > 1.1V) condition, the part turns off all TG1, BG1, TG2, and BG2. |
| 17 | $V_C$ | Error Amplifier Output to Set Inductor Current Comparator Threshold. The $V_C$ pin is used to compensate the control loop with an external RC network. |
| 18 | RT | Switching Frequency Setting. Connect a resistor from this pin to ground to set the internal oscillator frequency from 600 kHz to 1.4 MHz. |
| 19 | SYNC/SPRD | Switching Frequency Synchronization or Spread Spectrum. Ground this pin for switching at internal oscillator frequency. Apply a clock signal for external frequency |

| | | |
|---|---|---|
| | | synchronization. Tie to $INTV_{CC}$ for 25% triangle spread spectrum above internal oscillator frequency |
| 20 | DNC | Do not Connect. This pin must be left floating for the part to operate properly. |
| 21 | $V_{OUT}$ | Output Supply. The $V_{OUT}$ pin must be tied to the power output to determine the buck, buck-boost, or boost operation regions. Locally bypass this pin to ground with a minimum 1 µF ceramic capacitor. |
| 22 | TG2 | Boost Side Top Gate Drive. Drives the gate of boost side top N-Channel MOSFET with a voltage swing from SW2 to BST2. |
| 23 | SW2 | Boost Side Switch Node. The SW2 pin swings from a Schottky diode voltage drop below ground to $V_{OUT}$. |
| 24 | BST2 | Boost Side Bootstrap Floating Driver Supply. The BST2 pin has an integrated bootstrap Schottky diode from the $INTV_{CC}$ pin and requires an external bootstrap capacitor to the SW2 pin. The BST2 pin swings from a diode voltage drop below $INTV_{CC}$ to ($V_{OUT}$ + $INTV_{CC}$). |
| 25 | BG2 | Boost Side Bottom Gate Drive. Drives the gate of boost side bottom N-channel MOSFET with a voltage swing from ground to $INTV_{CC}$. |
| 26 | GND (Exposed Pad) | Ground. Solder the exposed pad directly to the ground plane. |
| 27 | BG1 | Buck Side Bottom Gate Drive. Drives the gate of buck side bottom N-channel MOSFET with a voltage swing from ground to $INTV_{CC}$. |
| 28 | BST1 | Buck Side Bootstrap Floating Driver Supply. The BST1 pin has an integrated bootstrap Schottky diode from the $INTV_{CC}$ pin and requires an external bootstrap capacitor to the SW1 pin. The BST1 pin swings from a diode voltage drop below $INTV_{CC}$ to ($V_{IN}$ + $INTV_{CC}$). |
| 29 | SW1 | Buck Side Switch Node. The SW1 pin swings from a Schottky diode voltage drop below ground up to $V_{IN}$. |

## BLOCK DIAGRAM

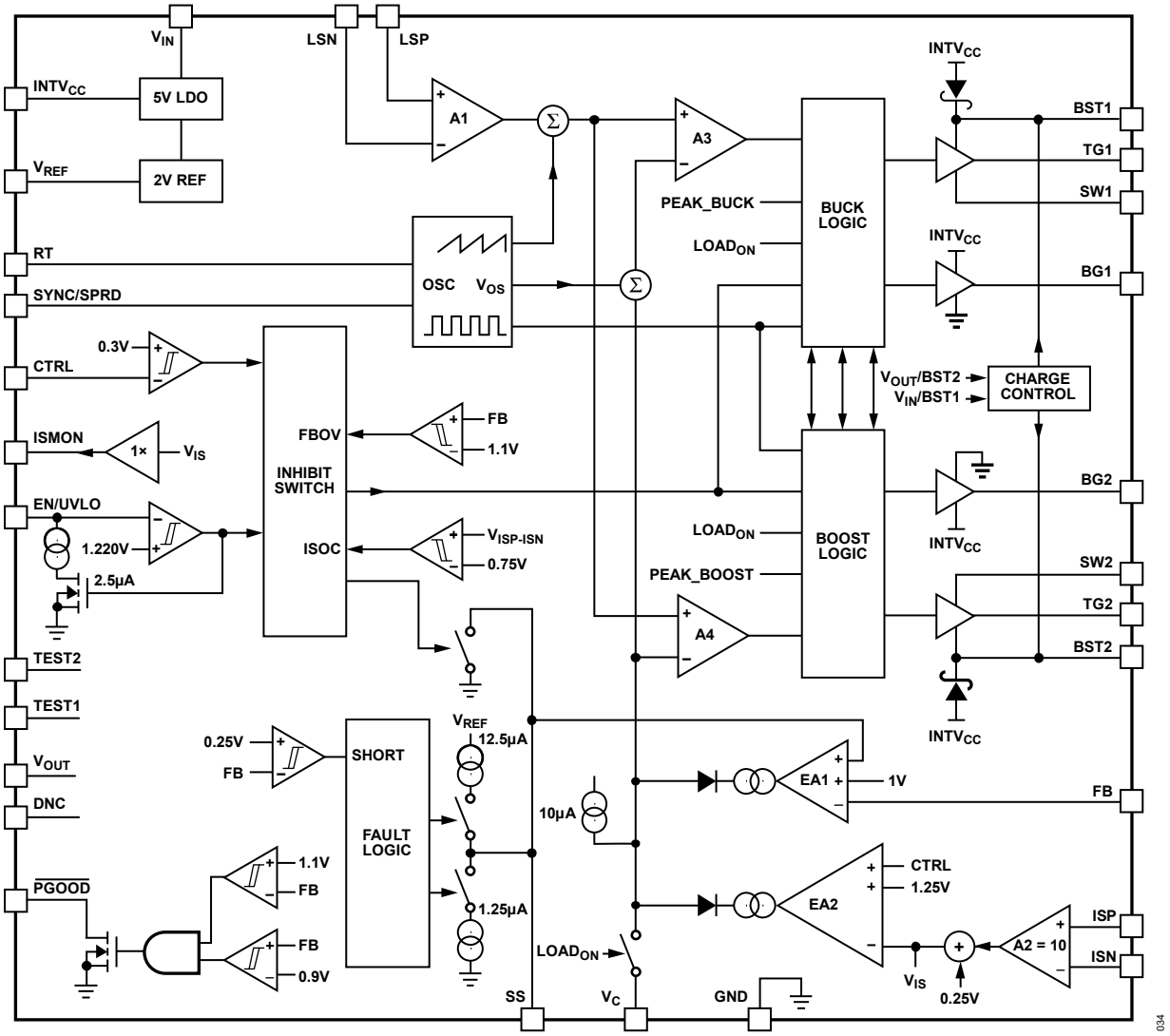



*Figure 4. BLOCK DIAGRAM*

## TYPICAL PERFORMANCE CHARACTERISTICS

$T_A$ = 25°C, unless otherwise noted.

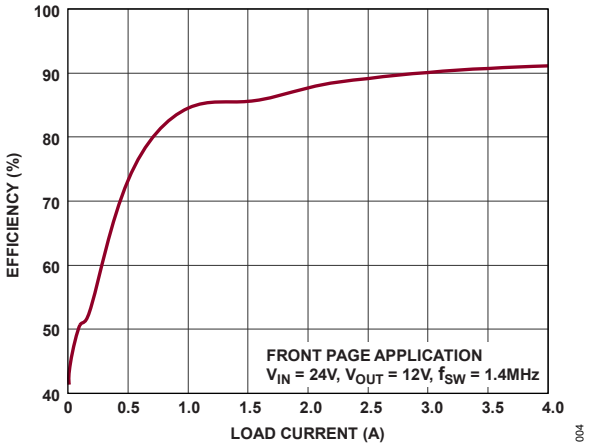



*Figure 5. Efficiency vs. Load Current (Buck Region)*

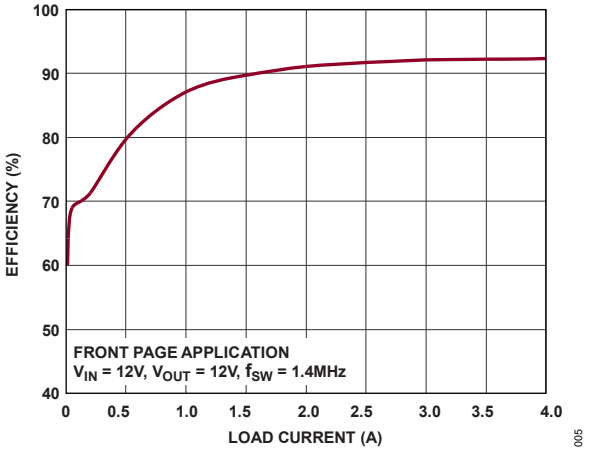



*Figure 6. Efficiency vs. Load Current (Buck Region)*

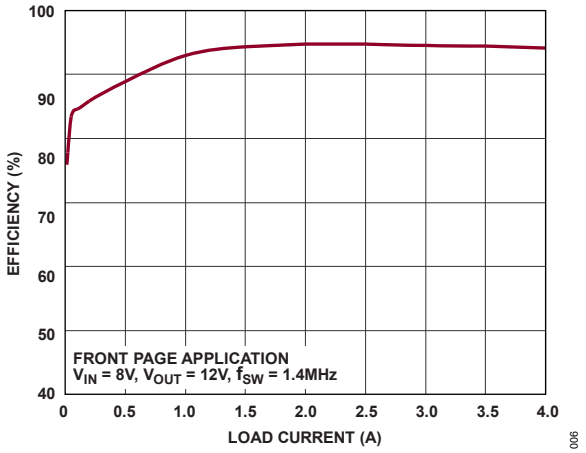



*Figure 7. Efficiency vs. Load Current (Boost Region)*

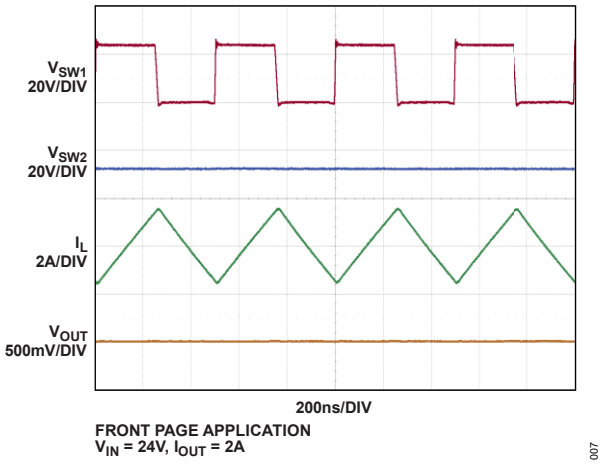



*Figure 8. Switching Waveforms (Buck Region)*

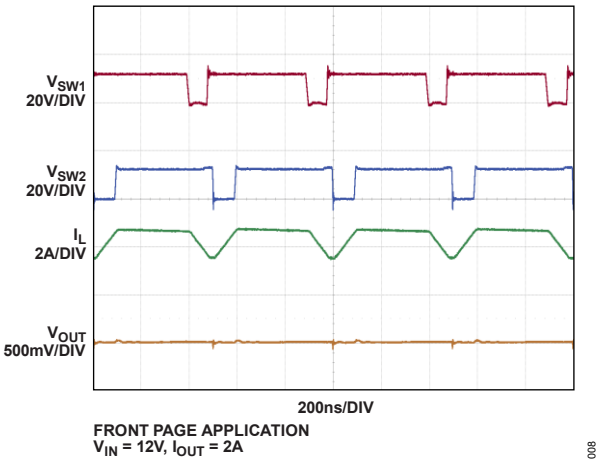



*Figure 9. Switching Waveforms (Buck-Boost Region)*

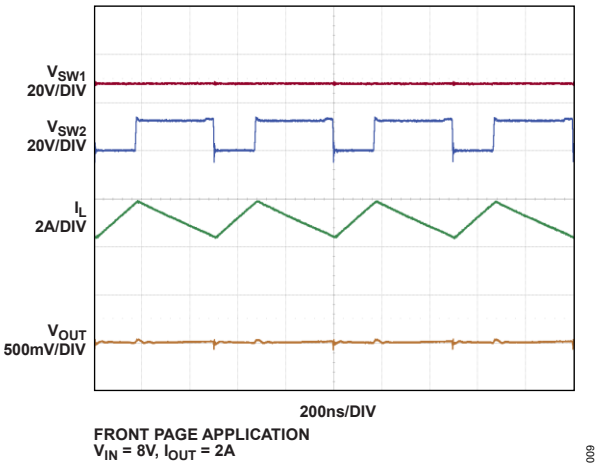



*Figure 10. Switching Waveforms (Boost Region)*

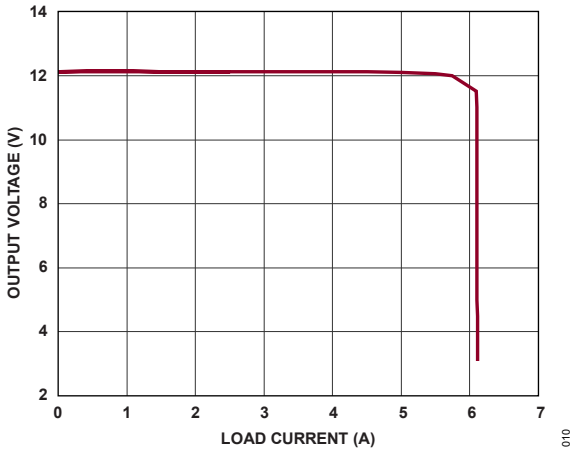



*Figure 11. $V_{OUT}$ vs. $I_{OUT}$ (CV/CC)*

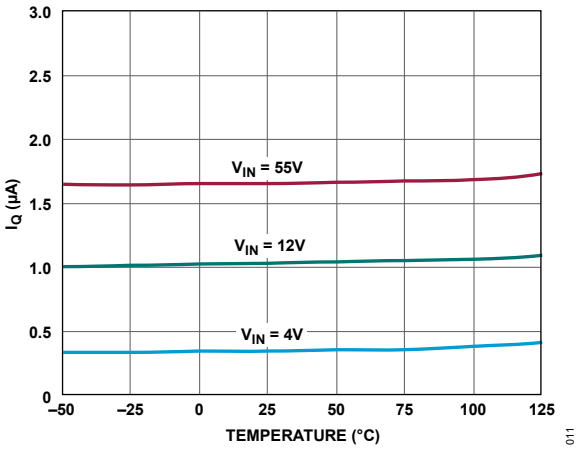



*Figure 12. $V_{IN}$ Shutdown Current*

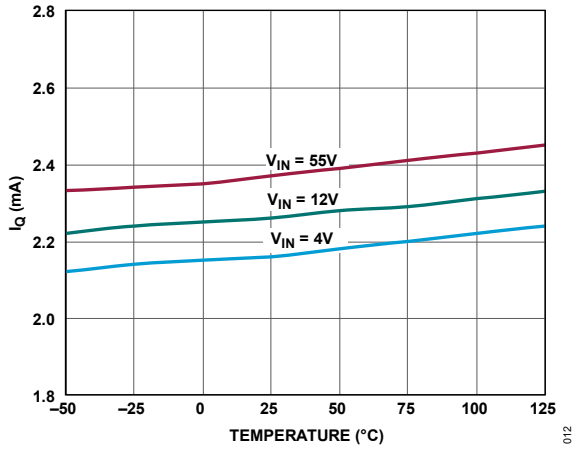



*Figure 13. $V_{IN}$ Quiescent Current*

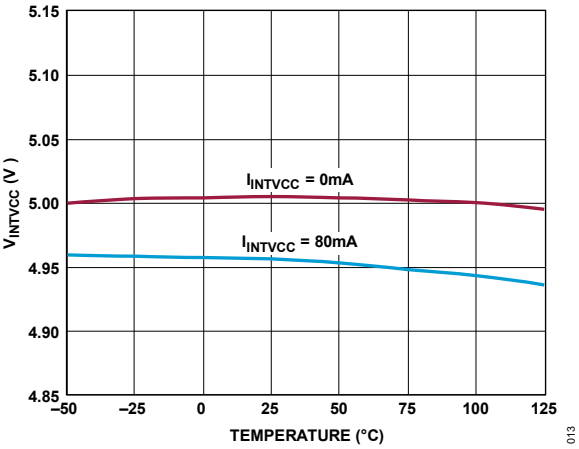



*Figure 14. $INTV_{CC}$ Voltage vs. Temperature*

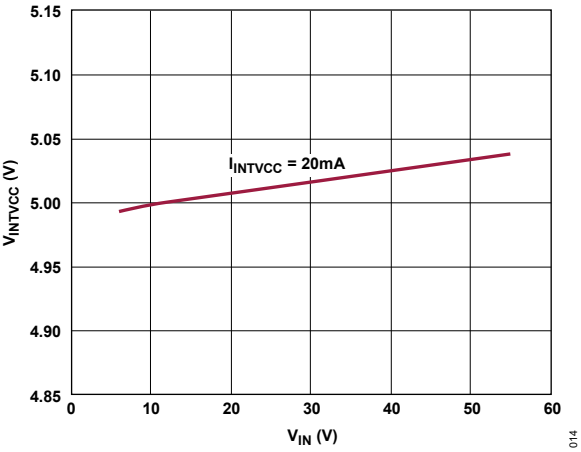



*Figure 15. $INTV_{CC}$ Voltage vs. $V_{IN}$*

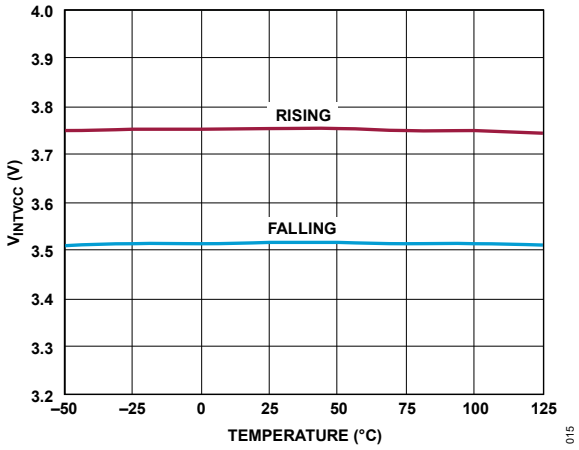



*Figure 16. $INTV_{CC}$ UVLO Threshold*

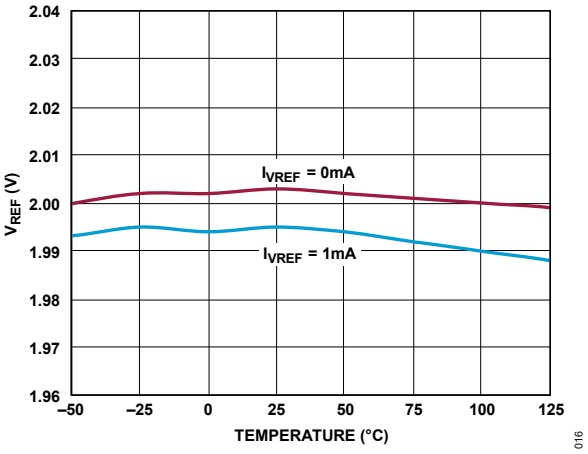



*Figure 17. $V_{REF}$ Voltage vs. Temperature*

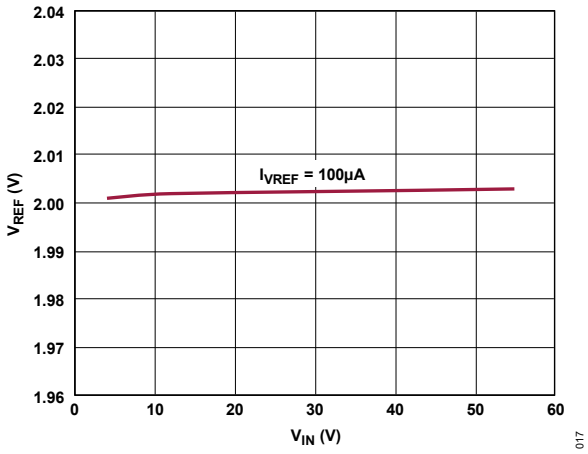



*Figure 18. $V_{REF}$ Voltage vs. $V_{IN}$*

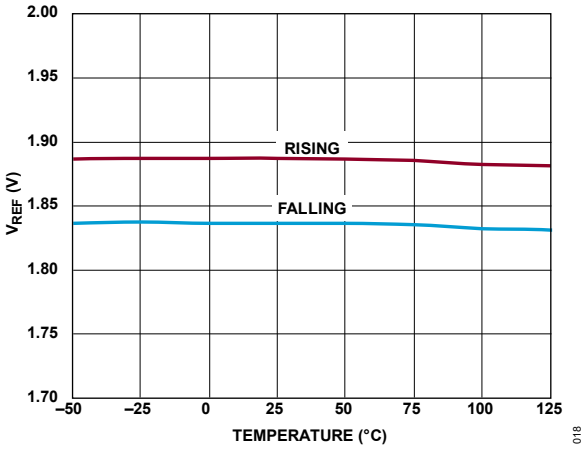



*Figure 19. $V_{REF}$ UVLO Threshold*

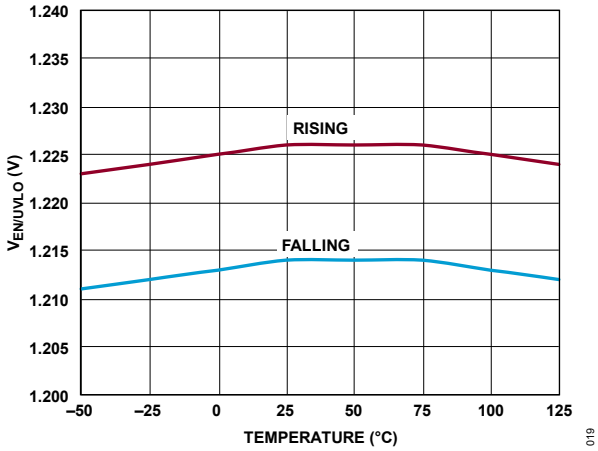



*Figure 20. EN/UVLO Enable Threshold*

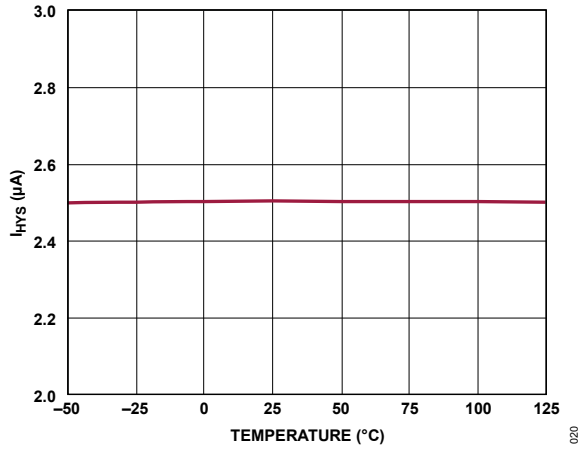



*Figure 21. EN/UVLO Hysteresis Current*

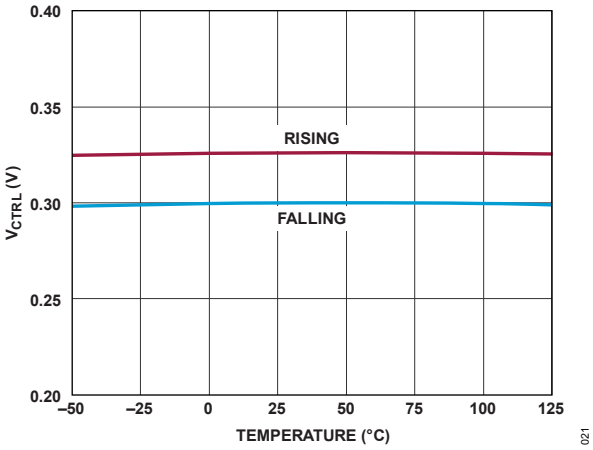



*Figure 22. CTRL Latch-Off Threshold*

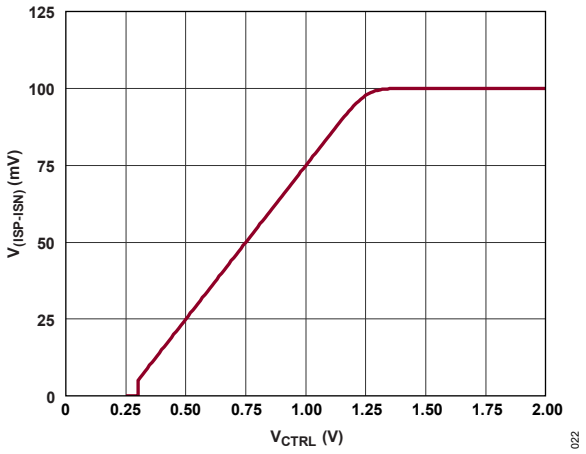



Figure 23. $V_{(ISP-ISN)}$ Regulation vs. $V_{CTRL}$

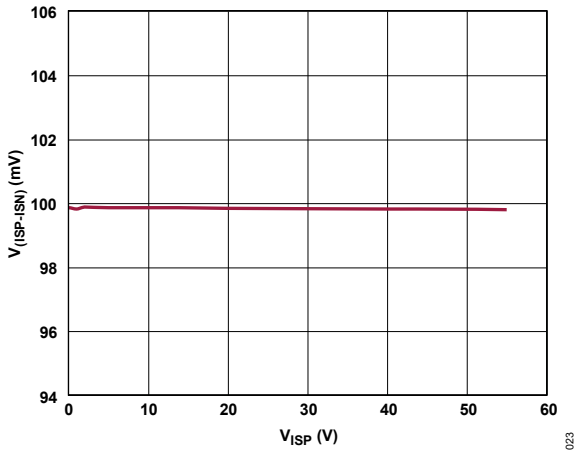



Figure 24. $V_{(ISP-ISN)}$ Regulation vs. $V_{ISP}$

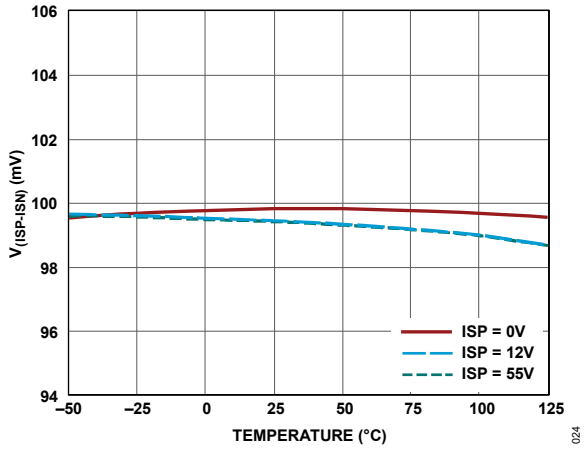



Figure 25. $V_{(ISP-ISN)}$ Regulation vs. Temperature

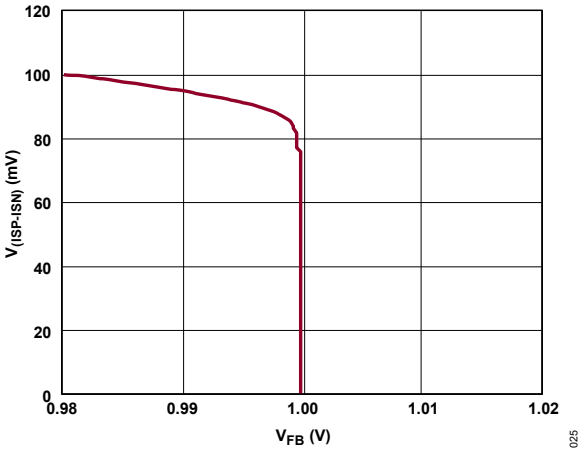



Figure 26. $V_{(ISP-ISN)}$ Regulation vs. $V_{FB}$

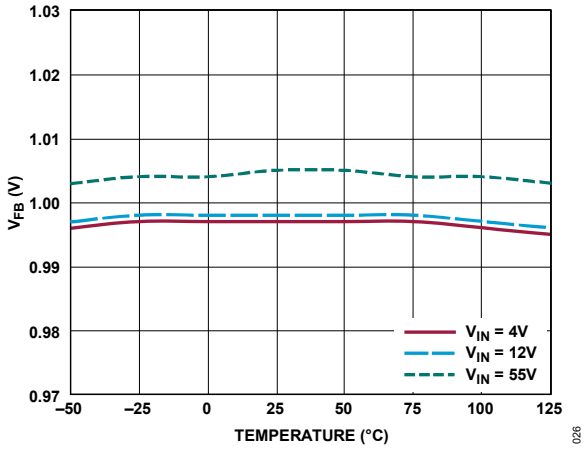



Figure 27. FB Regulation vs. Temperature

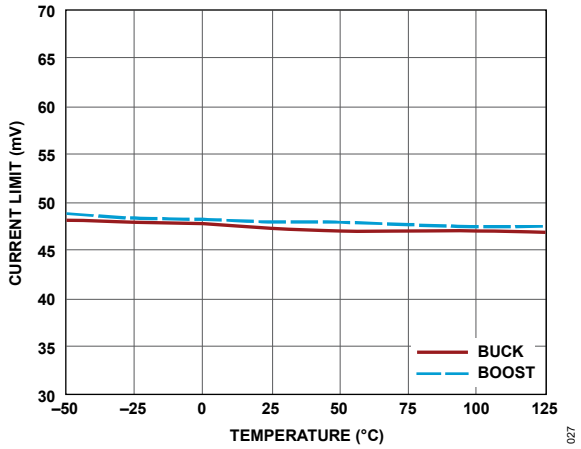



Figure 28. Maximum Current Sense vs. Temperature

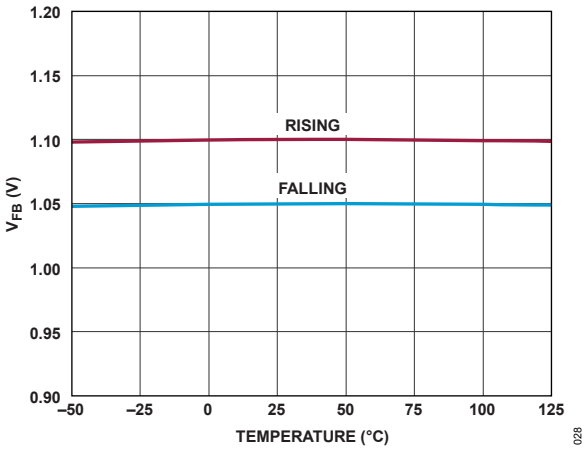



*Figure 29. FB Overvoltage Threshold*

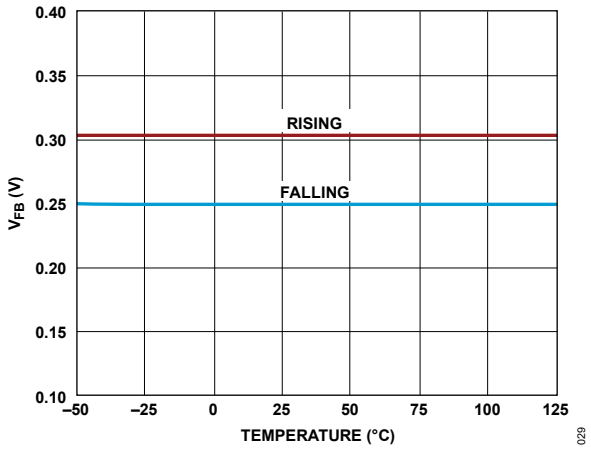



*Figure 30. FB Short Threshold*

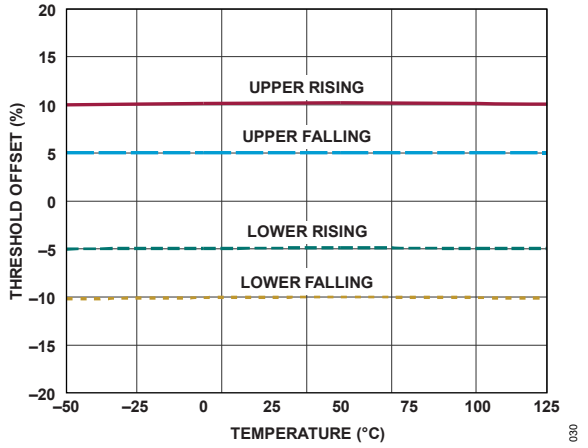



*Figure 31. $\overline{PGOOD}$ Thresholds*

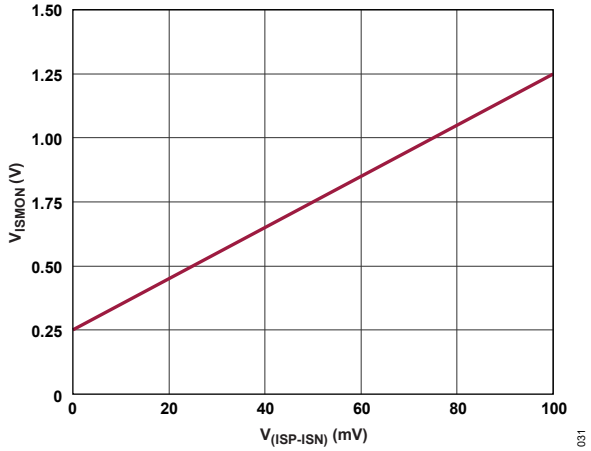



*Figure 32. ISMON Voltage vs. $V_{(ISP-ISN)}$*

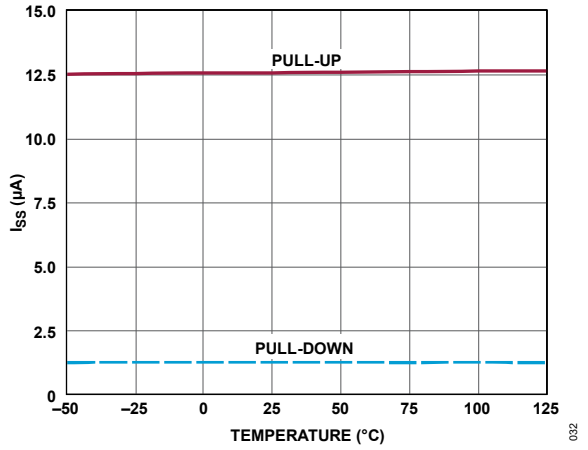



*Figure 33. SS Current vs. Temperature*

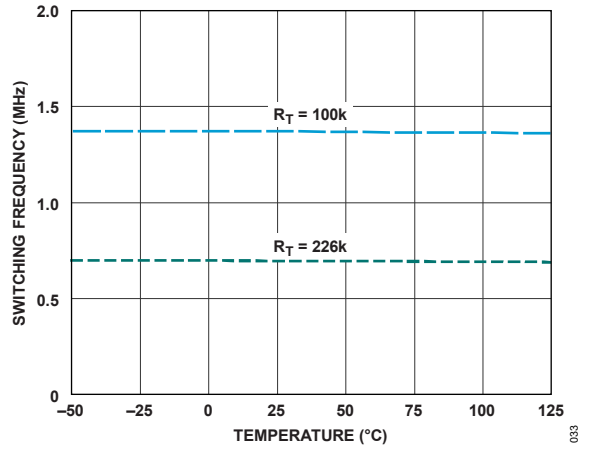



*Figure 34. Oscillator Frequency vs. Temperature*

# THEORY OF OPERATION

The ADPL76030 is a current-mode DC/DC controller that can regulate output voltage, and input or output current from input voltage above, below, or equal to the output voltage. The ADI proprietary peak-buck, peak-boost current-mode control scheme uses a single inductor current-sense resistor and provides smooth transition between buck region, buck-boost region, and boost region. Its operation is best understood by seeing the *BLOCK DIAGRAM*.

## Power Switch Control

*Figure 35* shows a simplified diagram of how the four power switches A, B, C, and D are connected to the inductor L, the current-sense resistor $R_{SENSE}$, power input $V_{IN}$, power output $V_{OUT}$, and ground. The current-sense resistor $R_{SENSE}$, connected to the LSP and LSN pins, provides inductor current information for both peak current-mode control and reverse current detection in buck region, buck-boost region, and boost region. *Figure 36* shows the current-mode control as a function of $V_{IN}/V_{OUT}$ ratio, and *Figure 37* shows the operation region as a function of $V_{IN}/ V_{OUT}$ ratio. The power switches are properly controlled to smoothly transition between modes and regions. Hysteresis is added to prevent chattering between modes and regions.

There are four states:

(1) Peak-buck current-mode control in buck region.

(2) Peak-buck current-mode control in buck-boost region.

(3) Peak-boost current-mode control in buck-boost region.

(4) Peak-boost current-mode control in boost region.

The following sections give detailed description for each state with waveforms, in which the shoot-through protection dead time between switches A and B, and between switches C and D are ignored for simplification.

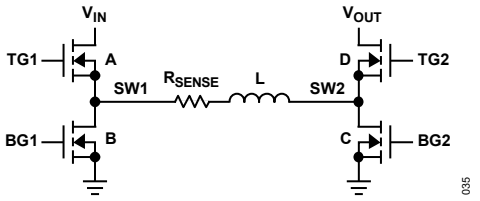



***Figure 35. Simplified Diagram of the Power Switches***

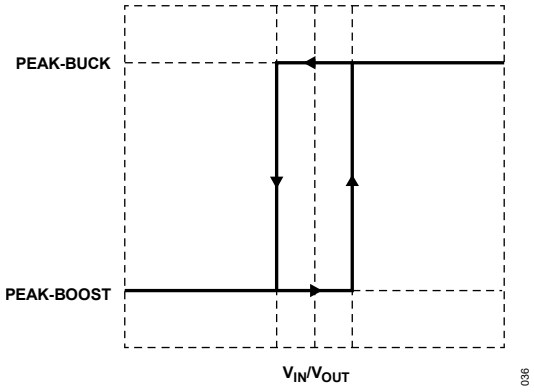



***Figure 36. Current Mode vs. $V_{IN}/V_{OUT}$ Ratio***

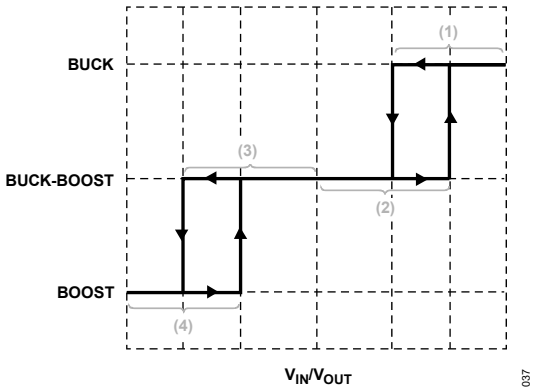



*Figure 37. Operation Region vs. $V_{IN}/V_{OUT}$ Ratio*

## (1) Peak-Buck in Buck Region ($V_{IN}$ >> $V_{OUT}$)

When $V_{IN}$ is much higher than $V_{OUT}$, the ADPL76030 uses peak-buck current-mode control in buck region (*Figure 38*). Switch C is always off and switch D is always on. At the beginning of every cycle, switch A is turned on and the inductor current ramps up. When the remainder of the peak buck current threshold commanded by $V_C$ voltage at buck current comparator A3 during (A + D) phase, switch A is turned off and switch B is turned on for the rest of the cycle. Switches A and B alternate, behaving like a typical synchronous buck regulator.

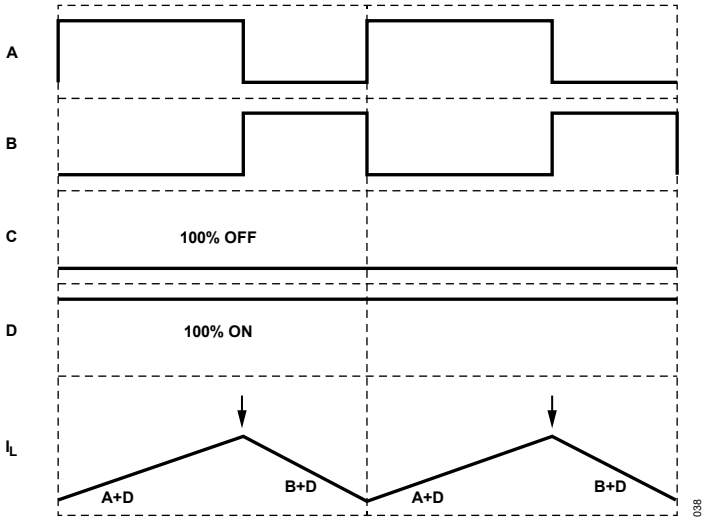



*Figure 38. Peak-Buck in Buck Region ($V_{IN}$ >> $V_{OUT}$)*

## (2) Peak-Buck in Buck-Boost Region ($V_{IN}$ ~> $V_{OUT}$)

When $V_{IN}$ is slightly higher than $V_{OUT}$, the ADPL76030 uses peak-buck current-mode control in buck-boost region (*Figure 39*). Switch C is always turned on for the beginning of the cycle and switch D is always turned on for the remainder of the cycle. At the beginning of every cycle, switches A and C are turned on and the inductor current ramps up. After the ramp completes, switch C is turned off and switch D is turned on, and the inductor keeps ramping up. When the inductor current hits the peak buck current threshold commanded by VC voltage at buck current comparator A3 during (A + D) phase, switch A is turned off and switch B is turned on for the rest of the cycle.

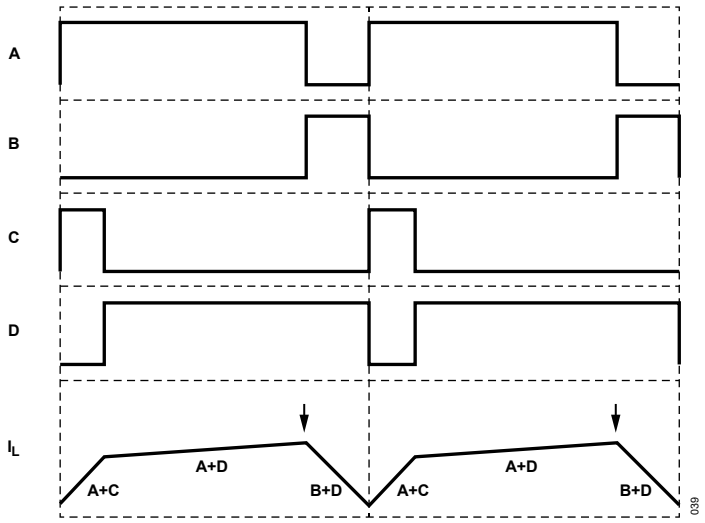



*Figure 39. Peak-Buck in Buck-Boost Region ($V_{IN}$ ~> $V_{OUT}$)*

## (3) Peak-Boost in Buck-Boost Region ($V_{IN}$)<~$V_{OUT}$

When $V_{IN}$ is slightly lower than $V_{OUT}$, the ADPL76030 uses peak-boost current-mode control in buck-boost region (*Figure 40*). Switch A is always turned on for the beginning of the cycle and switch B is always turned on for the remainder of the cycle. At the beginning of every cycle, switches A and C are turned on and the inductor current ramps up. When the inductor current hits the peak boost current threshold commanded by $V_C$ voltage at boost current comparator A4 during (A + C) phase, switch C is turned off and switch D is turned on for the rest of the cycle.

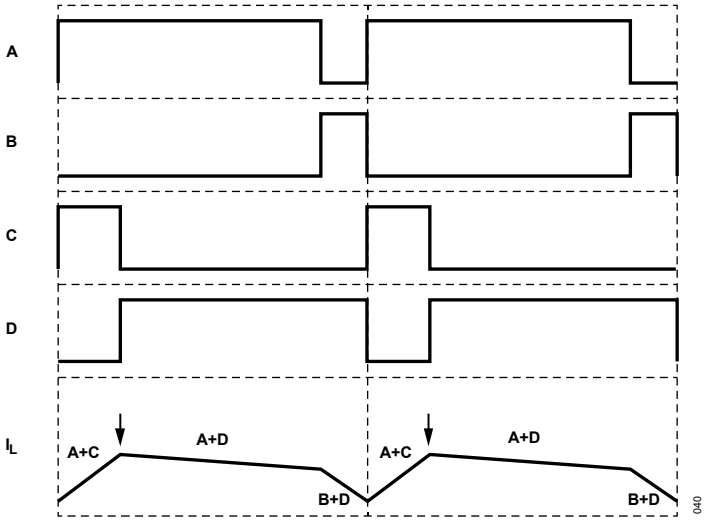



*Figure 40. Peak-Boost in Buck-Boost Region ($V_{IN}$<<$V_{OUT}$)*

## (4) Peak-Boost in Boost Region ($V_{IN}$ << $V_{OUT}$)

When $V_{IN}$ is much lower than $V_{OUT}$, the ADPL76030 uses peak-boost current-mode control in boost region (*Figure 41*). Switch A is always on and switch B is always off. At the beginning of every cycle, switch C is turned on and the inductor current ramps up. When the inductor current hits the peak boost current threshold commanded by $V_C$ voltage at boost current comparator A4 during (A+C) phase, switch C is turned off and switch D is turned on for the rest of the cycle. Switches C and D alternate, behaving like a typical synchronous boost regulator.

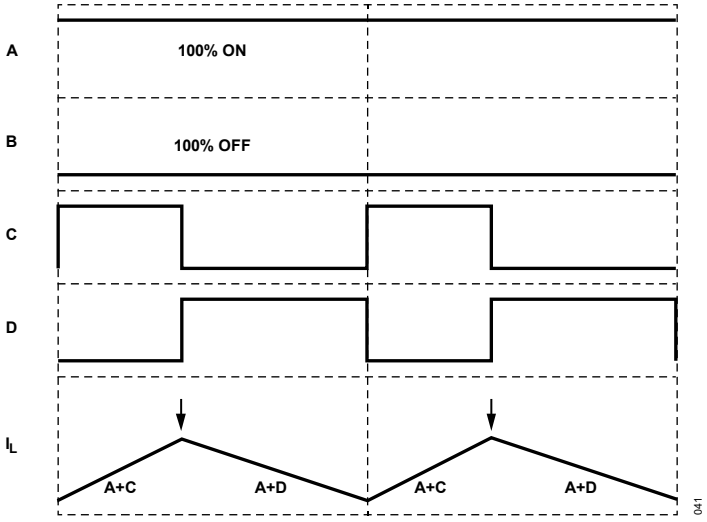



*Figure 41. Peak-Boost in Boost Region ($V_{IN}$ << $V_{OUT}$)*

## Main Control Loop

The ADPL76030 is a fixed frequency current-mode controller. The inductor current is sensed through the inductor sense resistor between the LSP and LSN pins. The current-sense voltage is gained up by amplifier A1 and added to a slope compensation ramp signal from the internal oscillator. The summing signal is then fed into the positive terminals of the buck current comparator A3 and boost current comparator A4. The negative terminals of A3 and A4 are controlled by the voltage on the $V_C$ pin, which is the diode-OR of error amplifiers EA1 and EA2.

Depending on the state of the peak-buck, peak-boost current-mode control, either the buck logic or the boost logic controls the four power switches so that either the FB voltage is regulated to 1 V or the current-sense voltage between the ISP and ISN pins is regulated by the CTRL pin during normal operation. The gains of EA1 and EA2 are balanced to ensure smooth transition between constant-voltage and constant-current operation with the same compensation network.

## Light Load Current Operation

At light load, the ADPL76030 runs either at full switching frequency discontinuous conduction mode or pulse-skipping mode, where the switches are held off for multiple cycles (that is, skipping pulses) to maintain the regulation and improve the efficiency. Both the buck and boost reverse current-sense thresholds are set to 1 mV (typical) so that no reverse inductor current is allowed.

In the buck region, switch B is turned off whenever the buck reverse current threshold is triggered during (B + D) phase. In the boost region, switch D is turned off whenever the boost reverse current threshold is triggered during (A + D) phase. In the buck-boost region, switch D is turned off whenever the boost reverse current threshold is triggered during (A + D) phase, and both switches B and D are turned off whenever the buck reverse current threshold is triggered during (B + D) phase.

## Internal Charge Path

Each of the two top MOSFET drivers is biased from its floating bootstrap capacitor, which is normally recharged by $INTV_{CC}$ through both the external and internal bootstrap diodes when the top MOSFET is turned off. When the ADPL76030 operates exclusively in the buck or boost regions, one of the top MOSFETs is constantly on. An internal charge path, from $V_{OUT}$ and BST2 to BST1, or from $V_{IN}$ and BST1 to BST2, charges the bootstrap capacitor to 4.6 V so that the top MOSFET can be kept on.

## Shutdown and Power-On-Reset

The ADPL76030 enters shutdown mode and drains less than 2 µA quiescent current when the EN/UVLO pin is below its shutdown threshold (0.3 V minimum). Once the EN/UVLO pin is above its shutdown threshold (1 V maximum), the ADPL76030 wakes up start-up circuitry, generates bandgap reference, and powers up the internal $INTV_{CC}$ LDO. The $INTV_{CC}$ LDO supplies the internal control circuitry and gate drivers. Now the ADPL76030 enters undervoltage lockout (UVLO) mode with a hysteresis current (2.5 µA typical) pulled into the EN/UVLO pin. When the $INTV_{CC}$ pin is charged above its rising UVLO threshold (3.78 V typical), the EN/UVLO pin passes its rising enable threshold (1.233 V typical), and the junction temperature is less than its thermal shutdown (165°C typical), the ADPL76030 enters enable mode, in which the EN/UVLO hysteresis current is turned off and the voltage reference $V_{REF}$ is charged up from ground. From the time of entering enable mode to the time of $V_{REF}$ passing its rising UVLO threshold (1.89 V typical), the ADPL76030 is going through a power-on-reset (POR), waking up the entire internal control circuitry and settling to the right initial conditions.

## Start-Up and Fault Protection

*Figure 42* shows the start-up and fault sequence for the ADPL76030. During the POR state, the SS pin is hard pulled down with a 100 Ω to ground. In a pre-biased condition, the SS pin must be pulled below 0.2 V to enter the INIT state, where the ADPL76030 waits 10 µs so that the SS pin can be fully discharged to ground. After the 10 µs, the ADPL76030 enters the UP/PRE state. The LOADON high signal happens when the CTRL pin is above its rising latch-off thresholds (0.325 V typical).

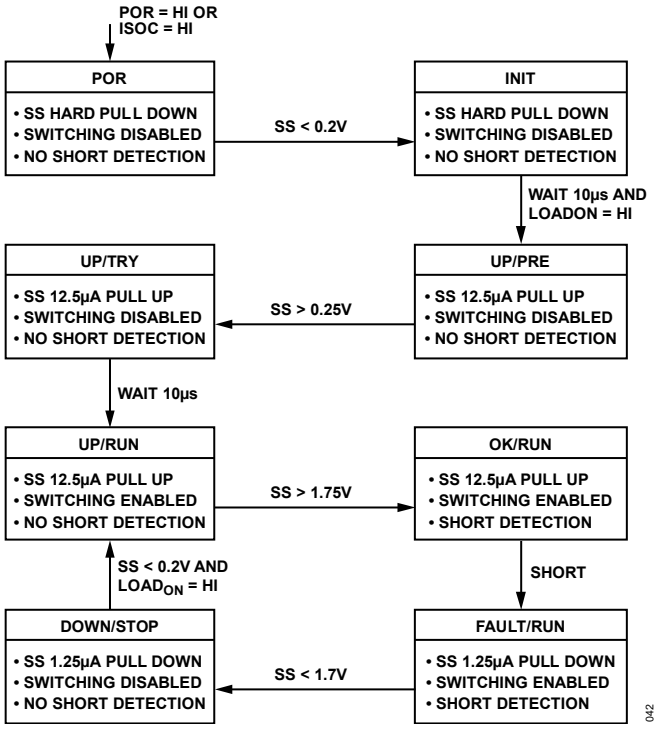



***Figure 42. Start-Up and Fault Sequence***

During the UP/PRE state, the SS pin is charged up by a 12.5 µA pull-up current while the switching is disabled. Once the SS pin is charged above 0.25 V, the ADPL76030 enters the UP/TRY state, while the switching is still disabled. If an excessive current flowing through the current-sense resistor triggers the ISP/ISN over current (ISOC) signal, it resets the ADPL76030 back into the POR state. After 10 µs in the UP/TRY state without triggering the ISOC signal, the ADPL76030 enters the UP/RUN state.

During the UP/RUN state, the switching is enabled and the start-up of the output voltage $V_{OUT}$ is controlled by the voltage on the SS pin. When the SS pin voltage is less than 1 V, the ADPL76030 regulates the FB pin voltage to the SS pin voltage instead of the 1 V reference. This allows the SS pin to be used to program soft-start by connecting an external capacitor from the SS pin to GND. The internal 12.5 µA pull-up current charges up the capacitor, creating a voltage ramp on the SS pin. As the SS pin voltage rises linearly from 0.25 V to 1 V (and beyond), the output voltage $V_{OUT}$ rises smoothly to its final regulation voltage.

Once the SS pin is charged above 1.75 V, the ADPL76030 enters the OK/RUN state, where the output short detection is activated. The output short means VFB < 0.25 V. When the output short happens, the ADPL76030 enters the FAULT/RUN state, where a 1.25 µA pull-down current slowly discharges the SS pin with the other conditions the same as the OK/RUN state. Once the SS pin is discharged below 1.7 V, the ADPL76030 enters the DOWN/STOP state, where the switching is disabled, and the short detection is deactivated with the previous fault latched. Once the SS pin is discharged below 0.2 V and the LOADON signal is still high, the ADPL76030 goes back to the UP/RUN state.

In an output short condition, the ADPL76030 can be set to hiccup, latch-off, or keep-running fault protection mode with a resistor between the SS and $V_{REF}$ pins. Without any resistor, the ADPL76030 hiccups between 0.2 V and 1.75 V, and goes around the UP/RUN, OK/RUN, FAULT/RUN, and DOWN/STOP states until the fault condition is cleared. With a 499 kΩ resistor, the ADPL76030 latches off until the EN/UVLO is toggled. With a 100 kΩ resistor, the ADPL76030 keeps running regardless of the fault.

# APPLICATIONS INFORMATION

*Figure 1* shows a typical ADPL76030 application circuit. This section serves as a guideline to select external components for typical applications. The examples and equations in this section assume continuous conduction mode, unless otherwise specified.

## Switching Frequency Selection

The ADPL76030 uses a constant frequency control scheme between 600 kHz and 1.4 MHz. Selection of the switching frequency is a trade-off between efficiency and component size. Low frequency operation improves efficiency by reducing MOSFET switching losses, but requires larger inductor and capacitor values. For high power applications, consider operating at lower frequencies to minimize MOSFET heating from switching losses. For low power applications, consider operating at higher frequencies to minimize the total solution size.

In addition, the specific application also plays an important role in switching frequency selection. In a noise-sensitive system, the switching frequency is usually selected to keep the switching noise out of a sensitive frequency band.

### Switching Frequency Setting

The switching frequency of the ADPL76030 can be set by the internal oscillator. With the SYNC/SPRD pin pulled to ground, the switching frequency is set by a resistor from the $R_T$ pin to ground. *Table 5* shows $R_T$ resistor values for common switching frequencies.

**Table 5. $R_T$ Resistor Values for Common Switching Frequencies**

| $f_{OSC}$ (MHz) | $R_T$ (k) |
|---|---|
| 0.6 | 267 |
| 0.8 | 191 |
| 1.0 | 147 |
| 1.2 | 118 |
| 1.4 | 97.6 |

### Spread Spectrum Frequency Modulation

Switching regulators can be particularly troublesome for applications where electromagnetic interference (EMI) is a concern. To improve the EMI performance, the ADPL76030 implements a triangle spread spectrum frequency modulation scheme. With the SYNC/SPRD pin tied to $INTV_{CC}$, the ADPL76030 starts to spread its switching frequency 25% above the internal oscillator frequency. *Figure 43* and *Figure 44* show the noise spectrum of the front-page application when spread spectrum is enabled.

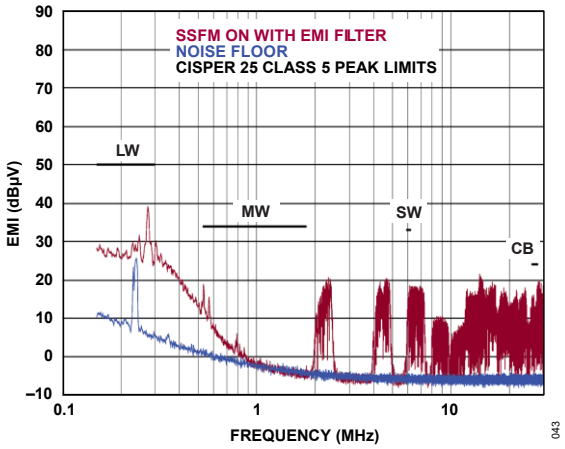



*Figure 43. Average Conducted EM*

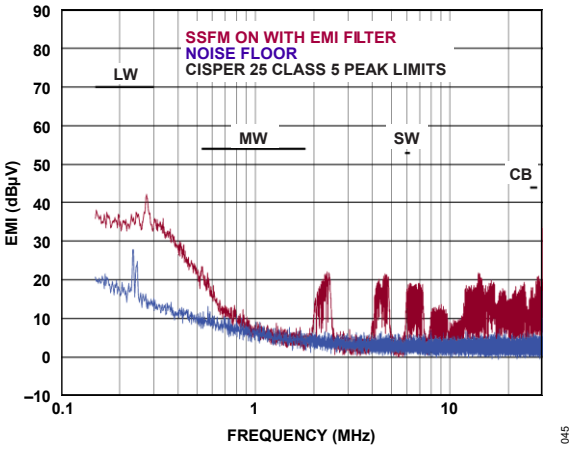



*Figure 44. Peak Conducted EMI*

### Frequency Synchronization

The ADPL76030 switching frequency can be synchronized to an external clock using the SYNC/SPRD pin. Driving the SYNC/SPRD with a 50% duty cycle waveform is always a good choice. Otherwise, maintain the duty cycle between 10% and 90%. Due to the use of a phase-locked loop (PLL) inside, there is no restriction between the synchronization frequency and internal oscillator frequency. The rising edge of the synchronization clock represents the beginning of a switching cycle, turning on switches A and C, or switches A and D.

## Inductor Selection

The switching frequency and inductor selection are interrelated in that higher switching frequencies allow the use of smaller inductor and capacitor values. The inductor value has a direct effect on ripple current. The highest current ripple $\Delta I_L\%$ happens in the buck region at $V_{IN(MAX)}$, and the lowest current ripple $\Delta I_L\%$ happens in the boost region at $V_{IN(MIN)}$. For any given ripple allowance set by customers, the minimum inductance can be calculated as:

$$L_{BUCK} > \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{f \times I_{OUT(MAX)} \times \Delta I_L\% \times V_{IN(MAX)}}$$

$$L_{BOOST} > \frac{{V_{IN(MIN)}}^2 \times (V_{OUT} - V_{IN(MIN)})}{f \times I_{OUT(MAX)} \times \Delta I_L\% \times {V_{OUT}}^2}$$

where:

$$\Delta I_L\% = \frac{\Delta I_L}{I_{L(AVG)}}$$

f is the switching frequency.

$V_{IN(MIN)}$ is the minimum input voltage.

$V_{IN(MAX)}$ is the maximum input voltage.

$V_{OUT}$ is the output voltage.

$I_{OUT(MAX)}$ is the maximum output current.

Slope compensation provides stability in constant frequency current-mode control by preventing subharmonic oscillations at certain duty cycles. The minimum inductance required for stability when duty cycles are larger than 50% can be calculated as:

$$L > \frac{10 \times V_{OUT} \times R_{SENSE}}{f}$$

For high efficiency, choose an inductor with low core loss, such as ferrite. Also, the inductor should have low DC resistance to reduce the $I^2R$ losses, and must be able to handle the peak inductor current without saturating. To minimize radiated noise, use a shielded inductor.

## $R_{SENSE}$ Selection and Maximum Output Current

$R_{SENSE}$ is chosen based on the required output current. The duty cycle independent maximum current-sense thresholds (50 mV in peak-buck and 50 mV in peak-boost) set the maximum inductor peak current in buck region, buck-boost region, and boost region.

In boost region, the lowest maximum average load current happens at $V_{IN(MIN)}$ and can be calculated as:

$$I_{OUT(MAX\_BOOST)} = \left(\frac{50\ mV}{R_{SENSE}} - \frac{\Delta I_{L(BOOST)}}{2}\right) \times \frac{V_{IN(MIN)}}{V_{OUT}}$$

where, $\Delta I_{L(BOOST)}$ is the peak-to-peak inductor ripple current in boost region, and can be calculated as:

$$\Delta I_{L(BOOST)} = \frac{V_{IN(MIN)} \times (V_{OUT} - V_{IN(MIN)})}{f \times L \times V_{OUT}}$$

In buck region, the lowest maximum average load current happens at $V_{IN(MAX)}$, and can be calculated as:

$$I_{OUT(MAX\_BUCK)} = \left(\frac{50\ mV}{R_{SENSE}} - \frac{\Delta I_{L(BUCK)}}{2}\right)$$

where, $\Delta I_{L(BUCK)}$ is peak-to-peak inductor ripple current in buck region and can be calculated as:

$$\Delta I_{L(BUCK)} = \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{f \times L \times V_{IN(MAX)}}$$

The maximum current sense $R_{SENSE}$ in the boost region is:

$$R_{SENSE(BOOST)} = \frac{2 \times 50\ mV \times V_{IN(MAX)}}{2 \times I_{OUT(MAX)} \times V_{OUT} + \Delta I_{L(BOOST)} \times V_{IN(MIN)}}$$

The maximum current sense $R_{SENSE}$ in the buck region is:

$$R_{SENSE(BUCK)} = \frac{2 \times 50\ mV}{2 \times I_{OUT(MAX)} + \Delta I_{L(BUCK)}}$$

The final $R_{SENSE}$ value should be lower than the calculated $R_{SENSE}$ in both the buck and boost regions. A 20% to 30% margin is usually recommended. Always choose a low ESL current-sense resistor.

## Power MOSFET Selection

The ADPL76030 requires four external N-channel power MOSFETs, two for the top switches (switches A and D in *Figure 35*) and two for the bottom switches (switches B and C in *Figure 35*). Important parameters for the power MOSFETs are the breakdown voltage $V_{BR(DSS)}$, threshold voltage $V_{GS(TH)}$, on-resistance $R_{DS(ON)}$, reverse transfer capacitance $C_{RSS}$, and maximum current $I_{DS(MAX)}$.

To achieve 1.4 MHz operation, the power MOSFET selection is critical. With typical 25 ns shoot-through protection deadtime, high performance power MOSFETs with low $Q_g$ and low $R_{DS(ON)}$ must be used.

Since the gate drive voltage is set by the 5 V $INTV_{CC}$ supply, logic-level threshold MOSFETs must be used in ADPL76030 applications. Switching four MOSFETs at higher frequency like 1.4 MHz, the substantial gate charge current from $INTV_{CC}$ can be estimated as:

$$I_{INTVCC} = f \times \left(Q_{gA} + Q_{gB} + Q_{gC} + Q_{gD}\right)$$

where:

f is the switching frequency.

$Q_{gA}$, $Q_{gB}$, $Q_{gC}$, $Q_{gD}$ are the total gate charges of MOSFETs A, B, C, D.

Make sure the total required $INTV_{CC}$ current does not exceed the $INTV_{CC}$ current limit in the data sheet. Typically, MOSFETs with less than 10 nC Qg are recommended. The ADPL76030 uses the $V_{IN}/V_{OUT}$ ratio to transition between modes and regions. Bigger IR drop in the power path caused by improper MOSFET and inductor selection may prevent the ADPL76030 from smooth transition. To ensure smooth transitions between buck, buck-boost, and boost modes of operation, choose low $R_{DS(ON)}$ MOSFETs and low DCR inductor to satisfy:

$$I_{OUT(MAX)} \leq \frac{0.025 \times V_{OUT}}{R_{A,B} + R_{C,D} + R_{SENSE} + R_L}$$

where:

$R_{A,B}$ is the maximum $R_{DS(ON)}$ of MOSFETs A or B at 25°C.

$R_{C,D}$ is the maximum $R_{DS(ON)}$ of MOSFETs C or D at 25°C.

$R_L$ is the maximum DCR resistor of inductor at 25°C.

The $R_{DS(ON)}$ and DCR increase at higher junction temperatures and the process variations are included in the calculation above.

To select the power MOSFETs, the power dissipated by the device must be known. For switch A, the maximum power dissipation happens in the boost region, when it remains on all the time. Its maximum power dissipation at maximum output current is given by:

$$P_{A(BOOST)} = \left(\frac{I_{OUT(MAX)} \times V_{OUT}}{V_{IN}}\right)^2 \times \rho T \times R_{DS(ON)}$$

Where, ρT is a normalization factor (unity at 25°C) accounting for the significant variation in on-resistance with temperature, typically 0.4%/°C, as shown in *Figure 45*. For a maximum junction temperature of 125°C, using a value of ρT = 1.5 is reasonable.

Switch B operates in the buck region as the synchronous rectifier. Its power dissipation at maximum output current is given by:

$$P_{B(BUCK)} = (\frac{V_{IN} - V_{OUT}}{V_{IN}}) \times {I_{OUT(MAX)}}^2 \times \rho T \times R_{DS(ON)}$$

Switch C operates in the boost region as the control switch. Its power dissipation at maximum current is given by:

$$P_{C(BOOST)} = \frac{(V_{OUT} - V_{IN}) \times V_{OUT}}{{V_{IN}}^2} \times {I_{OUT(MAX)}}^2 \times \rho T \times R_{DS(ON)} + k \times V_{OUT}\ 3 \times \frac{I_{OUT(MAX)}}{V_{IN}} \times C_{RSS} \times f$$

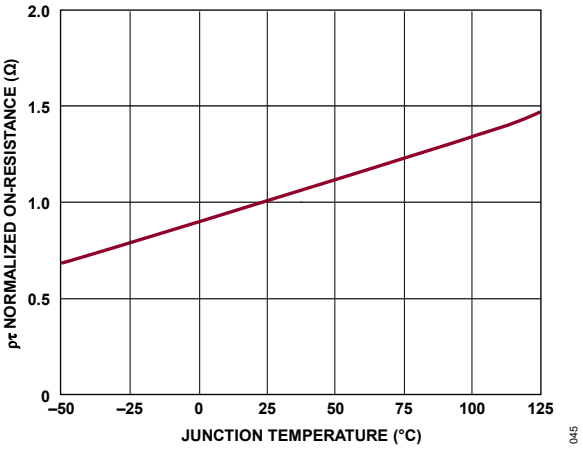



***Figure 45. Normalized $R_{DS(ON)}$ vs. Temperature***

where, $C_{RSS}$ is usually specified by the MOSFET manufacturers. The constant k, which accounts for the loss caused by reverse recovery current, is inversely proportional to the gate drive current and has an empirical value of 1.7.

For switch D, the maximum power dissipation happens in the boost region, when its duty cycle is higher than 50%. Its maximum power dissipation at maximum output current is given by:

$$P_{D(BOOST)} = \frac{V_{OUT}}{V_{IN}} \times {I_{OUT(MAX)}}^2 \times \rho T \times R_{DS(ON)}$$

For the same output voltage and current, switch A has the highest power dissipation and switch B has the lowest power dissipation, unless a short occurs at the output.

From a known power dissipated in the power MOSFET, its junction temperature can be obtained using the following formula:

$$T_J = T_A + P \times R_{TH(JA)}$$

The junction-to-ambient thermal resistance $R_{TH(JA)}$ includes the junction-to-case thermal resistance $R_{TH(JC)}$ and the case-to-ambient thermal resistance $R_{TH(CA)}$. This value of $T_J$ can then be compared to the original, assumed value used in the iterative calculation process.

## Optional Schottky Diode ($D_B$, $D_D$) Selection

The optional Schottky diodes $D_B$ (in parallel with switch B) and $D_D$ (in parallel with switch D) conduct during the dead time between the conduction of the power MOSFET switches. They are intended to prevent the body diode of synchronous switches B and D from turning on and storing charge during the dead time. In particular, $D_B$ significantly reduces reverse recovery current between switch B turn-off and switch A turn-on, and $D_D$ significantly reduces reverse recovery current between switch D turn-off and switch C turn-on. They improve converter efficiency and reduce switch voltage stress. For the diode to be effective, the inductance between it and the synchronous switch must be as small as possible, mandating that these components be placed adjacently.

## $C_{IN}$ and $C_{OUT}$ Selection

Input and output capacitance is necessary to suppress voltage ripple caused by discontinuous current moving in and out the regulator. A parallel combination of capacitors is typically used to achieve high capacitance and low equivalent series resistance (ESR). Dry tantalum, special polymer, aluminum electrolytic, and ceramic capacitors are all available in surface mount packages.

Capacitors with low ESR and high ripple current ratings, such as OS-CON and POSCAP are also available. Ceramic capacitors should be placed near the regulator input and output to suppress high frequency switching spikes. Ceramic capacitors, of at least 1µF, should also be placed from $V_{IN}$ to GND and $V_{OUT}$ to GND as close to the ADPL76030 pins as possible. Due to their excellent low ESR characteristics, ceramic capacitors can significantly reduce input ripple voltage and help reduce power loss in the higher ESR bulk capacitors. X5R or X7R dielectrics are preferred, as these materials retain their capacitance over wide voltage and temperature ranges. Many ceramic capacitors, particularly 0805 or 0603 case sizes, have greatly reduced capacitance at the desired operating voltage.

## Input Capacitance $C_{IN}$

Discontinuous input current is highest in the buck region due to the switch A toggling on and off. Make sure that the $C_{IN}$ capacitor network has low enough ESR and is sized to handle the maximum RMS current. In the buck region, the input RMS current is given by:

$$I_{RMS} \approx I_{OUT(MAX)} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

The formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT(MAX)}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief.

## Output Capacitance $C_{OUT}$

Discontinuous current shifts from the input to the output in the boost region. Make sure that the $C_{OUT}$ capacitor network is capable of reducing the output voltage ripple. The effects of ESR and the bulk capacitance must be considered when choosing the right capacitor for a given output ripple voltage. The maximum steady state ripple due to charging and discharging the bulk capacitance is given by:

$$\Delta V_{CAP(BOOST)} = \frac{I_{OUT(MAX)} \times (V_{OUT} - V_{IN(MIN)})}{C_{OUT} \times V_{OUT} \times f}$$

$$\Delta V_{CAP(BUCK)} = \frac{V_{OUT} \times \left(1 - \frac{V_{OUT}}{V_{IN(AX)}}\right)}{8 \times L \times f^2 \times C_{OUT}}$$

The maximum steady ripple due to the voltage drop across the ESR is given by:

$$\Delta V_{ESR(BOOST)} = \frac{V_{OUT} \times I_{OUT(MAX)}}{V_{IN(MIN)}} \times ESR$$

$$\Delta V_{ESR(BUCK)} = \frac{V_{OUT} \times \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)}{L \times f} \times ESR$$

## $INTV_{CC}$ Regulator

An internal P-channel low dropout regulator produces 5 V at the $INTV_{CC}$ pin from the $V_{IN}$ supply pin. The $INTV_{CC}$ powers the internal circuitry and gate drivers in the ADPL76030. The $INTV_{CC}$ regulator can supply an average current of 145 mA and must be bypassed to ground with a minimum of 4.7 µF ceramic capacitor. Good local bypass is necessary to supply the high transient current required by MOSFET gate drivers.

Higher input voltage applications with large MOSFETs being driven at higher switching frequencies may cause the maximum junction temperature rating for the ADPL76030 to be exceeded. The system supply current is normally dominated by the gate charge current. Additional external loading of the $INTV_{CC}$ also needs to be taken into account for the power dissipation calculation. The total ADPL76030 power dissipation in this case is $V_{IN} \times IINTV_{CC}$, and overall efficiency is lowered. The junction temperature can be estimated using the equation:

$T_J = T_A + P_D \times \theta_{JA}$

where, $\theta_{JA}$ (in °C/W) is the package thermal resistance.

To prevent maximum junction temperature from being exceeded, the input supply current must be checked operating in the continuous mode at maximum $V_{IN}$.

## Top Gate MOSFET Driver Supply ($C_{BST1}$, $C_{BST2}$)

The top MOSFET drivers, TG1 and TG2, are driven between their respective SW and BST pin voltages. The boost voltages are biased from floating bootstrap capacitors $C_{BST1}$ and $C_{BST2}$, which are normally recharged through both the external and internal bootstrap diodes when the respective top MOSFET is turned off. External bootstrap diodes are recommended because the internal bootstrap diodes are not always strong enough to refresh top MOSFETs at 1.4 MHz. Both capacitors are charged to the same voltage as the $INTV_{CC}$ voltage. The bootstrap capacitors $C_{BST1}$ and $C_{BST2}$ need to store about 100 times the gate charge required by the top switches A and D. In most applications, a 0.1 µF to 0.47 µF, X5R or X7R dielectric capacitor is adequate.

## Programming $V_{IN}$ UVLO

A resistor divider from $V_{IN}$ to the EN/UVLO pin implements $V_{IN}$ undervoltage lockout (UVLO). The EN/UVLO enable falling threshold is set at 1.220 V. In addition, the EN/UVLO pin sinks 2.5 µA when the voltage on the pin is below 1.220 V. This current provides user programmable hysteresis based on the value of R1. The programmable UVLO thresholds are:

$$V_{IN(ULVO+)} = 1.233\ V \times \frac{R1 + R2}{R2} + 2.5\ \mu A \times R1$$

$$V_{IN(ULVO-)} = 1.220\ V \times \frac{R1 + R2}{R2}$$

*Figure 46* shows the implementation of external shutdown control while still using the UVLO function. The NMOS grounds the EN/UVLO pin when turned on, and puts the ADPL76030 in shutdown with quiescent current less than 2 µA.

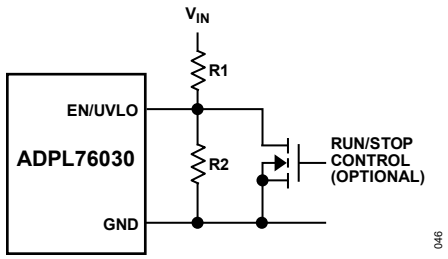



***Figure 46. $V_{IN}$ Undervoltage Lockout (UVLO)***

## Programming Input or Output Current Limit

The input or output current limit can be programmed by placing an appropriate value current-sense resistor, $R_{IS}$ in the input or output power path. The voltage drop across $R_{IS}$ is (Kelvin) sensed by the ISP and ISN pins. The CTRL pin should be tied to a voltage higher than 1.35 V to get the full-scale 100 mV (typical) threshold across the sense resistor. The CTRL pin can be used to reduce the current threshold to zero, although relative accuracy decreases with the decreasing sense threshold. When the CTRL pin voltage is between 0.3 V and 1.15 V, the current limit is:

$$I_{IS(MAX)} = \frac{V_{CTRL} - 0.25\ V}{10 \times R_{IS}}$$

When $V_{CTRL}$ is between 1.15 V and 1.35 V, the current limit varies with $V_{CTRL}$, but departs from the equation above by an increasing amount as $V_{CTRL}$ increases. Ultimately, when $V_{CTRL}$ is larger than 1.35 V, the current limit no longer varies. *Table 6* lists the typical $V_{(ISP-ISN)}$ threshold vs. $V_{CTRL}$.

**Table 6. $V_{(ISP-ISN)}$ Threshold vs. $V_{CTRL}$**

| $V_{CTRL}$ (V) | $V_{(ISP-ISN)}$ (mV) |
|---|---|
| 1.15 | 90 |
| 1.20 | 94.5 |
| 1.25 | 98 |
| 1.30 | 99.5 |
| 1.35 | 100 |

When $V_{CTRL}$ is larger than 1.35 V, the current threshold is regulated to:

$$I_{IS(MAX)} = \frac{100\ mV}{R_{IS}}$$

The CTRL pin should not be left open (tie to $V_{REF}$ if not used). The CTRL pin can also be used in conjunction with a thermistor to provide overtemperature protection for the output load, or with a resistor divider to $V_{IN}$ to reduce output power and switching current when $V_{IN}$ is low.

The presence of a time varying differential voltage ripple signal across the ISP and ISN pins at the switching frequency is expected. If the current-sense resistor $R_{IS}$ is placed between the power input and input bulk capacitor (*Figure 47*), or between the output bulk capacitor and system output (*Figure 49*), a filter is typically not necessary. If the $R_{IS}$ is placed between the input bulk capacitor and input decoupling capacitor (*Figure 48*), or between the output

decoupling capacitor and output bulk capacitor (*Figure 50*), a low pass filter formed by $R_F$ and $C_F$ is recommended to reduce the current ripple and stabilize the current loop. Since the bias currents of the ISP and ISN pins are matched, no offset is introduced by $R_F$. If input or output current limit is not used, the ISP and ISN pins should be shorted to $V_{IN}$, $V_{OUT}$, or ground.

## ISMON Current Monitor

The ISMON pin provides a buffered monitor output of the current flowing through the ISP/ISN current-sense resistor $R_{IS}$. The $V_{ISMON}$ voltage is calculated as $V_{(ISP-ISN)} \times 10 + 0.25$ V. Since the ISMON pin has the same 0.25 V offset as the CTRL pin, the master ADPL76030 ISMON pin can be directly tied to the slave ADPL76030 CTRL pin for equal current sharing in parallel applications.

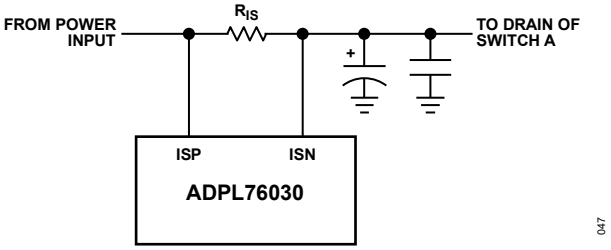



*Figure 47. Programming Input Current Limit(a)*

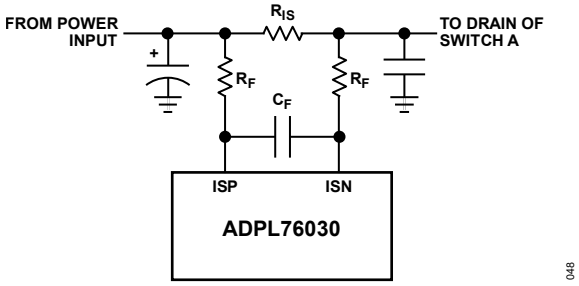



*Figure 48. Programming Input Current Limit(b)*

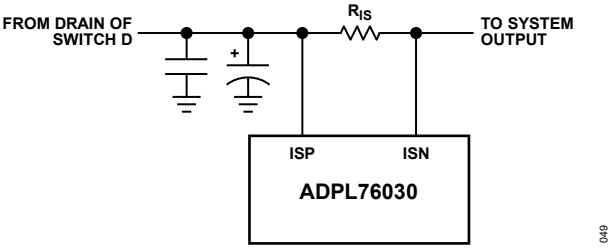



*Figure 49. Programming Output Current Limit(a)*

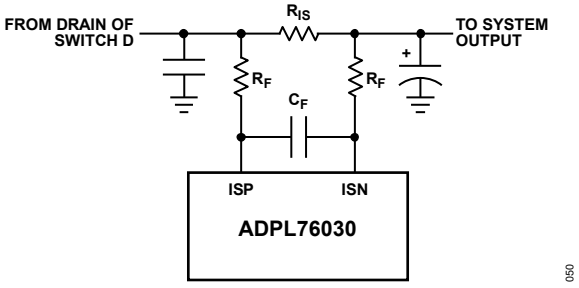



*Figure 50. Programming Output Current Limit(b)*

## Programming Output Voltage and Thresholds

The ADPL76030 has a voltage feedback pin FB that can be used to program a constant-voltage output. The output voltage can be set by selecting the values of R3 and R4 (*Figure 51*) according to the following equation:

$$V_{OUT} = 1\ V \times \frac{R3 + R4}{R4}$$

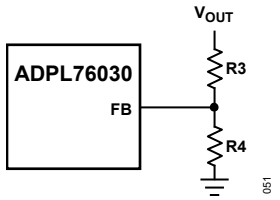



***Figure 51. Feedback Resistor Connection***

In addition, the FB pin also sets the output overvoltage threshold, output power good thresholds, and output short threshold. For an application with small output capacitors, the output voltage may overshoot a lot during load transient events. Once the FB pin hits its overvoltage threshold 1.1 V, the ADPL76030 stops switching by turning off TG1, BG1, TG2, and BG2. The output overvoltage threshold can be set as:

$$V_{OUT(OVP)} = 1.1\ V \times \frac{R3 + R4}{R4}$$

To provide the output short-circuit detection and protection, the output short falling threshold can be set as

$$V_{OUT(SHORT)} = 0.25\ V \times \frac{R3 + R4}{R4}$$

## Power GOOD ($\overline{PGOOD}$) Pin

The ADPL76030 provides an open-drain status pin, $\overline{PGOOD}$, which is pulled low when $V_{FB}$ is within ±10% of the 1.00 V regulation voltage. The $\overline{PGOOD}$ pin is allowed to be pulled up by an external resistor to $INTV_{CC}$ or an external voltage source of up to 6 V.

### Soft-Start and Short-Circuit Protection

As shown in *Figure 42* and explained in the *Theory of Operation* section, the SS pin can be used to program the output voltage soft-start by connecting an external capacitor from the SS pin to ground. The internal 12.5 µA pull-up current charges up the capacitor, creating a voltage ramp on the SS pin. As the SS pin voltage rises linearly from 0.25 V to 1 V (and beyond), the output voltage rises smoothly into its final voltage regulation. The soft-start time can be calculated as:

$$t_{SS} = 1\ V \times \frac{C_{SS}}{12.5\ \mu A}$$

Make sure the $C_{SS}$ is at least five to ten times larger than the compensation capacitor on the $V_C$ pin for a well-controlled output voltage soft-start. A 22 nF ceramic capacitor is a good starting point.

The SS pin is also used as a fault timer. Once an output short-circuit fault is detected, a 1.25 µA pull-down current source is activated. Using a single resistor from the SS pin to the $V_{REF}$ pin, the ADPL76030 can be set to three different fault protection modes: hiccup (no resistor), latch-off (499 k), and keep-running (100 k).

With a 100 k resistor in the keep-running mode, the ADPL76030 continues switching normally and regulates the current into ground. With a 499 k resistor in latch-off mode, the ADPL76030 stops switching until the EN/UVLO pin is pulled low and high to restart. With no resistor in the hiccup mode, the ADPL76030 enters low duty cycle auto-retry operation. The 1.25 µA pull-down current discharges the SS pin to 0.2 V and then 12.5 µA pull-up current charges the SS pin up. If the output short-circuit condition is not removed when the SS pin reaches 1.75 V, the 1.25 µA pull-down current turns on again, initiating a new hiccup cycle. This continues until the fault is removed. Once the output short-circuit condition is removed, the output has a smooth short-circuit recovery due to soft-start.

## Loop Compensation

The ADPL76030 uses an internal transconductance error amplifier, the output of which, $V_C$, compensates the control loop. The external inductor, output capacitor, and the compensation resistor and capacitor determine the loop stability.

The inductor and output capacitor are chosen based on performance, size, and cost. The compensation resistor and capacitor on the $V_C$ pin are set to optimize control loop response and stability. For a typical voltage regulator application, a 2.2 nF compensation capacitor on the $V_C$ pin is adequate, and a series resistor should always be used to increase the slew rate on the $V_C$ pin to maintain tighter output voltage regulation during fast transients on the input supply of the converter.

## Efficiency Considerations

The power efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change produces the most improvement. Although all dissipative elements in circuits produce losses, four main sources account for most losses in ADPL76030 circuits:

- DC $I^2R$ losses. These arise from the resistances of the MOSFETs, sensing resistor, inductor, and PC board traces, and cause the efficiency to drop at high output currents.
- Transition loss. This loss arises from the brief amount of time switch A or switch C spends in the saturated region during switch node transitions. It depends upon the input voltage, load current, driver strength, and MOSFET capacitance, among other factors.
- $INTV_{CC}$ current. This is the sum of the MOSFET driver and control currents.
- $C_{IN}$ and $C_{OUT}$ loss. The input capacitor has the difficult job of filtering the large RMS input current to the regulator in the buck region. The output capacitor has the difficult job of filtering the large RMS output current in the boost region. Both $C_{IN}$ and $C_{OUT}$ are required to have low ESR to minimize the AC $I^2R$ loss, and sufficient capacitance to prevent the RMS current from causing additional upstream losses in fuses or batteries.
- Other losses. Schottky diode $D_B$ and $D_D$ are responsible for conduction losses during dead time and light load conduction periods. Inductor core loss occurs predominately at light loads. Switch A causes reverse recovery current loss in the buck region, and switch C causes reverse recovery current loss in the boost region. When making adjustments to improve efficiency, the input current is the best indicator of changes in efficiency. If a change is made and the input current decreases, then the efficiency has increased. If there is no change in the input current, then there is no change in efficiency.

## PC Board Layout Checklist

The basic PC board layout requires a dedicated ground plane layer. Also, for high current, a multilayer board provides heat sinking for power components.

- The ground plane layer should not have any traces and it should be as close as possible to the layer with power MOSFETs.
- Place $C_{IN}$, switch A, switch B, and $D_B$ in one compact area. Place $C_{OUT}$, switch C, switch D, and $D_D$ in one compact area.
- Use immediate vias to connect the components to the ground plane. Use several large vias for each power component.
- Use planes for $V_{IN}$ and $V_{OUT}$ to maintain good voltage filtering and keep power losses low.
- Flood all unused areas on all layers with copper. Flooding with copper reduces the temperature rise of power components. Connect the copper areas to any DC net ($V_{IN}$ or GND).
- Separate the signal and power grounds. All small-signal components should return to the exposed GND pad from the bottom, which is then tied to the power GND close to the sources of switch B and switch C.
- Place switch A and switch C as close to the controller as possible, keeping the PGND, BG, and SW traces short.
- Keep the high dV/dT SW1, SW2, BST1, BST2, TG1, and TG2 nodes away from sensitive small-signal nodes.
- The path formed by switch A, switch B, $D_B$, and the $C_{IN}$ capacitor should have short leads and PCB trace lengths. The path formed by switch C, switch D, $D_D$, and the $C_{OUT}$ capacitor also should have short leads and PCB trace lengths.
- The output capacitor (–) terminals should be connected as close as possible to the (–) terminals of the input capacitor.
- Connect the top driver bootstrap capacitor $C_{BST1}$ closely to the BST1 and SW1 pins. Connect the top driver bootstrap capacitor $C_{BST2}$ closely to the BST2 and SW2 pins.
- Connect the input capacitors $C_{IN}$ and output capacitors $C_{OUT}$ closely to the power MOSFETs. These capacitors carry the MOSFET AC current.
- Route LSP and LSN traces together with minimum PCB trace spacing. Avoid sense lines pass through noisy areas, such as switch nodes. The filter capacitor between LSP and LSN should be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the $R_{SENSE}$ resistor. Low ESL sense resistor is recommended.
- Connect the $V_C$ pin compensation network close to the IC, between $V_C$ and the signal ground. The capacitor helps to filter the effects of PCB noise and output voltage ripple voltage from the compensation loop.
- Connect the $INTV_{CC}$ bypass capacitor, $CINTV_{CC}$, close to the IC, between the $INTV_{CC}$ and power ground. This capacitor carries the MOSFET drivers' current peaks.

## ORDERING INFORMATION

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING* | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|
| ADPL76030AUFD#PBF | ADPL76030AUFD#TRPBF | 76030 | 28-Lead (4 mm × 5 mm) Plastic QFN | –40°C to 125°C |

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

*Tape and reel specifications*. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown ADPL76030 are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific automotive reliability reports for these models

## TYPICAL APPLICATION

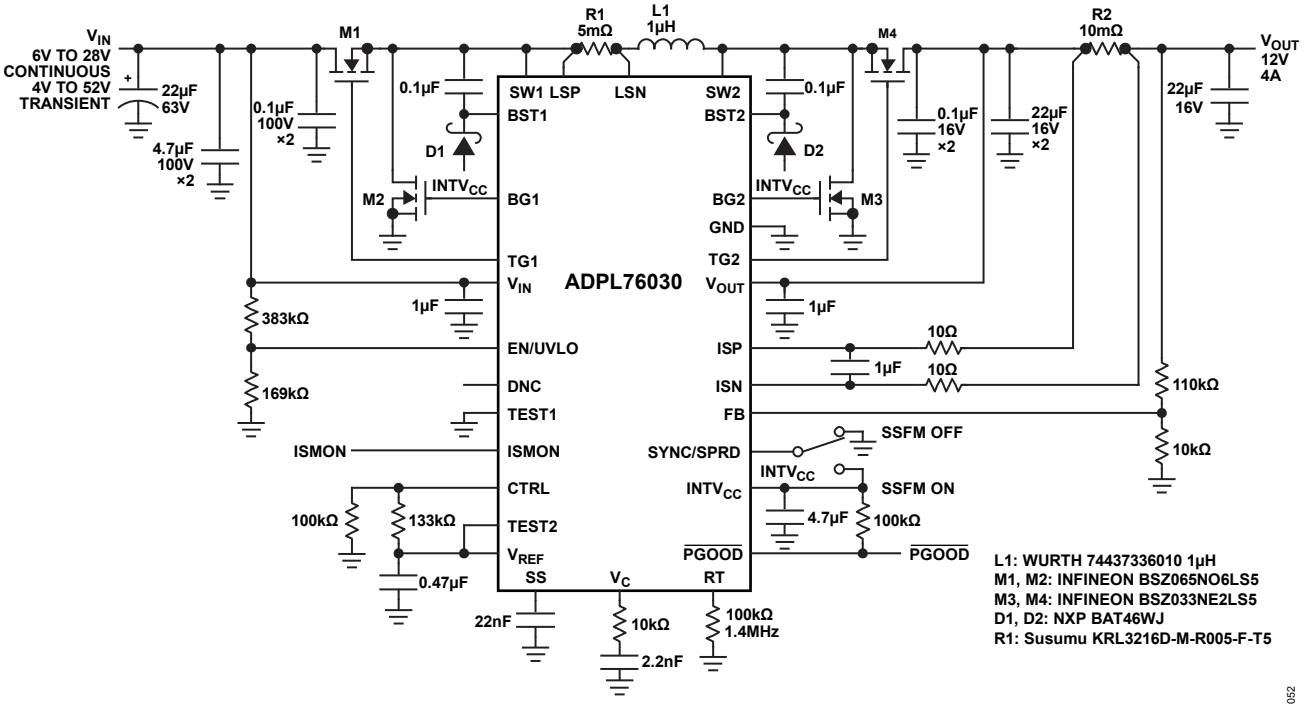
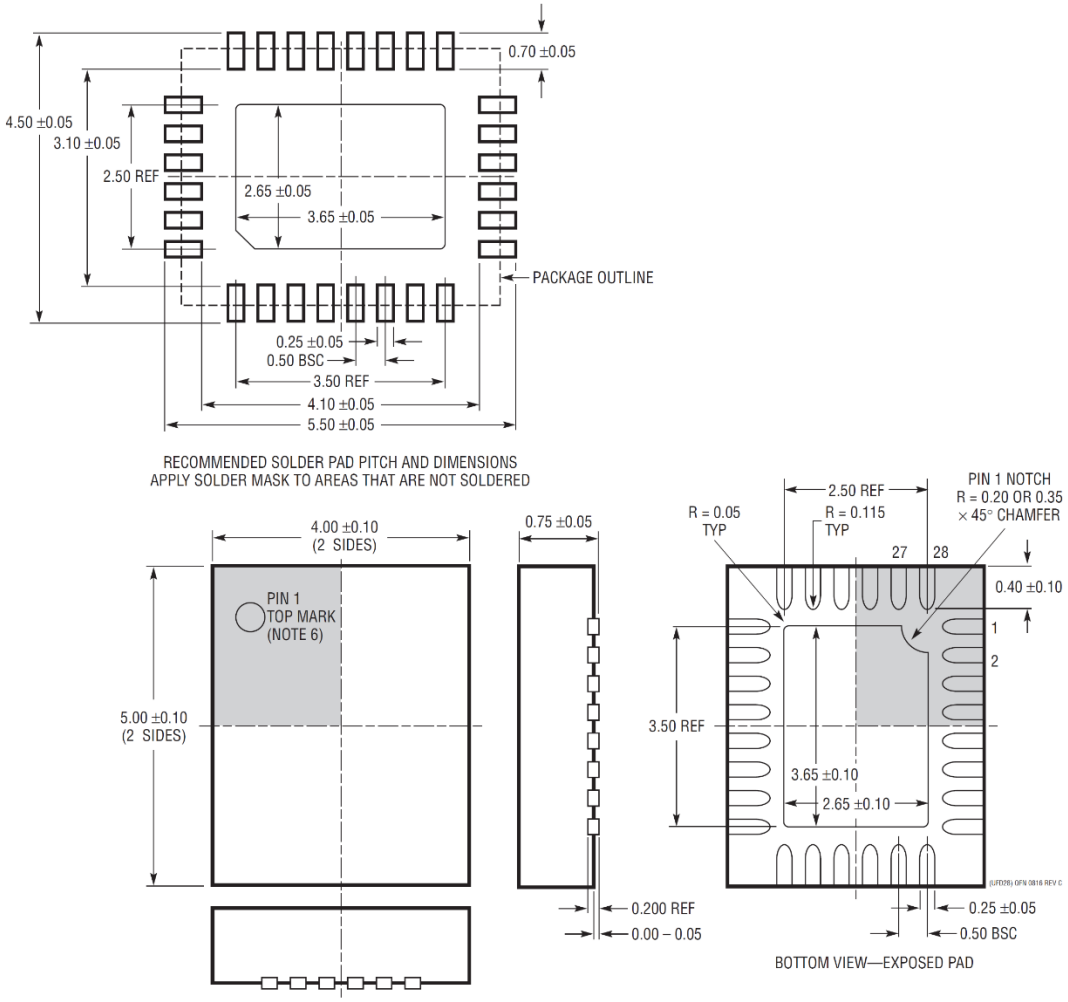



*Figure 52. 95% Efficient 48 W (12 V, 4 A), 1.4 MHz Buck-Boost Voltage Regulator*

# PACKAGE DESCRIPTION

**UFD Package**
**28-Lead Plastic QFN (4mm × 5mm)**
(Reference LTC DWG # 05-08-1712 Rev C)




NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGHD-3).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE