Data Sheet

ADPD7000

Multimodal Sensor Front End

FEATURES

- Multimodal analog front end
- Optical channel
  - 4 input channels with multiple operation modes for various sensor measurements
  - 4-channel processing with simultaneous sampling
  - 12 programmable time slots for synchronized sensor measurements
  - Flexible input multiplexing to support single-ended sensor measurements
  - 8 LED drivers, 2 of which can be driven simultaneously
  - Flexible sampling rate from 0.004 Hz to 9 kHz using internal oscillators
  - AC ambient light rejection: 78 dB up to 100 Hz
  - 400 mA total LED peak drive current
  - Individual ambient cancellation DAC at TIA input with 9-bit control up to 300 µA
  - Individual LED DC cancellation DAC at TIA input with 7-bit control up to 190 µA
- ECG channel
  - <1 µV RMS RTI noise at diagnosis bandwidth
  - High input impedance 20 GΩ
  - Accepts up to ±1.2 V of DC differential input range
  - CMRR: 115 dB
  - Flexible 4 electrode configurations to support various applications
  - Both AC lead off detection and DC lead off detection
  - Support always on, low power, lead on detection
- BIA channel
  - Low power, high accuracy excitation path
  - Configurable excitation frequency up to 250 kHz
  - Sine wave excitation with a 12-bit DAC
  - High accuracy with large imbalance contact impedance ≤20 kΩ
  - Configurable receive filters with low noise design
  - Complex impedance measurement engine
  - Integrated current-limit resistors
- EDA channel
  - Support both voltage excitation and current excitation
  - 10 kΩ to100 MΩ measurement range with 1 nS resolution
  - DFT and decimation for high accuracy measurement result
- SPI communications supported
- 704-byte FIFO

APPLICATIONS

- Wearable health and fitness monitors: heart rate, heart rate variability, saturation level of pulse oxygen, body impedance analysis, hydration analysis, and cuff-less noninvasive blood pressure
- Clinical patient monitors: small bed-side patient, home portable patient, and small remote patient
- Industrial monitoring: particle, aerosol, and gas detection
- Conductivity detection

GENERAL DESCRIPTION

The ADPD7000 is a highly integrated analog front end (AFE) designed for measuring various vital signals.

The optical channel is designed as an optical transceiver, stimulating up to eight light emitting diodes (LEDs) and measuring the return signal on up to four separate current inputs. The signal chain rejects signal offsets and corruption from asynchronous modulated interference, typically from ambient light, eliminating the need for optical filters or externally controlled DC cancellation circuitry.

The electrocardiography (ECG) signal acquisition is designed to support low noise, diagnostic level measurement in the presence of a variety of interferers. The ECG signal chain has a number of complementary features supporting ECG measurement, such as driven reference for common-mode rejection and lead off detection to identify a fallen electrode.

The body impedance analysis (BIA) signal chain is designed for body impedance measurement with a configurable excitation path and measurement path. A 12-bit digital-to-analog converter (DAC) is used in the excitation path to generate the sinusoid wave and high precision measurement, with configurable filters used to measure the body response of the stimulus.

The electrodermal activity (EDA) signal chain is designed for electrodermal activity. By multiplexing BIA and ECG peripheral circuits, the ADPD7000 supports high precision AC and DC measurement with 1 nS resolution.

The data output and functional configuration use a serial port interface (SPI) on the ADPD7000. The control circuitry includes flexible LED signaling and synchronous detection, digital filters, digital wave generators, and configurable filters.

The ADPD7000 is available in a 2.795 mm × 2.560 mm, 0.40 mm pitch, 36-ball WLCSP.

Rev. 0

TABLE OF CONTENTS

REVISION HISTORY

4/2023—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

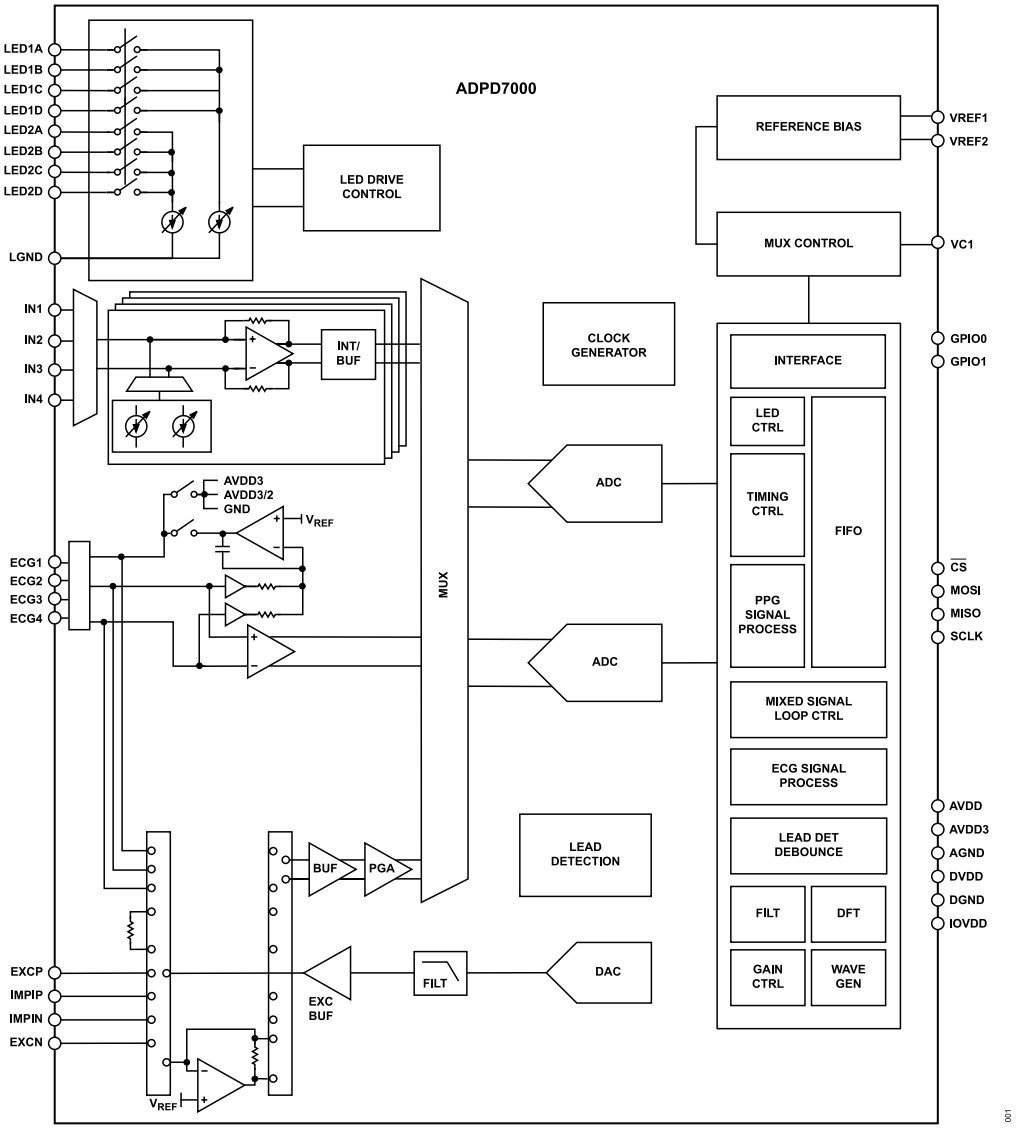

Figure 1. Functional Block Diagram

SPECIFICATIONS

TEMPERATURE AND POWER SPECIFICATIONS

Table 1. Temperature and Power Specifications

Parameter	Min	Typ	Max	Unit
TEMPERATURE RANGE				
Operating Range	−40		+85	°C
Storage Range	−65		+150	°C
POWER SUPPLY VOLTAGES				
AVDD	1.7	1.8	1.9	V
AVDD3	2.7	3.3	3.6	V
DVDD	1.7	1.8	1.9	V
IOVDD	1.7	1.8	3.6	V

PERFORMANCE SPECIFICATION

AVDD = DVDD = IOVDD = 1.8 V, AVDD3 = 3.3 V, and T_A = 25°C, unless otherwise noted.

Table 2. Performance Specifications

Parameter	Test Condition/Comments	Min	Typ	Max	Unit
DATA ACQUISTION					
Datapath Width				32	Bits
FIRST IN, FIRST OUT (FIFO) SIZE				704	Bytes
INTERNAL 960 kHz OSCILLATOR ACCURACY	Full temperature range (−40°C to +85°C)		±1		%
PHOTOPLETHYSMOGRAPHY (PPG) CHANNEL					
Transimpedance Amplifier (TIA) Gain		12.5		400	kΩ
DIGITAL INTEGRATION MODE					
Analog-to-Digital Converter (ADC) Resolution	TIA feedback resistor (R_F)				
	12.5 kΩ		5.84		nA/LSB
	25 kΩ		2.92		nA/LSB
	50 kΩ		1.46		nA/LSB
	100 kΩ		0.73		nA/LSB
	200 kΩ		0.365		nA/LSB
	400 kΩ		0.183		nA/LSB
ADC Saturation Level	TIA feedback resistor				
	12.5 kΩ		48		µA
	25 kΩ		24		µA
	50 kΩ		12		µA
	100 kΩ		6		µA
	200 kΩ		3		µA
	400 kΩ		1.5		µA
DC Ambient Light Rejection (ALR)					
ALR Range		0		300	µA
ALR Resolution			0.6		µA
LED DC Cancellation					
Range		0		190	µA
Resolution			1.48		µA
Dark Noise	Pulse = 1, ADC sample = 20				
	TIA gain = 12.5 kΩ		1590		pA RMS

SPECIFICATIONS

Table 2. Performance Specifications (Continued)

Parameter	Test Condition/Comments	Min	Typ	Max	Unit
	TIA gain = 25 kΩ		867		pA RMS
	TIA gain = 50 kΩ		425		pA RMS
	TIA gain = 100 kΩ		235		pA RMS
	TIA gain = 200 kΩ		140		pA RMS
	TIA gain = 400 kΩ		92		pA RMS
Signal-to-Noise Ratio (SNR)	White card reflection, pulse = 1, ADC sample = 20				
	TIA gain = 12.5 kΩ		90		dB
	TIA gain = 25 kΩ		90		dB
	TIA gain = 50 kΩ		88		dB
	TIA gain = 100 kΩ		87		dB
	TIA gain = 200 kΩ		85		dB
	TIA gain = 400 kΩ		82		dB
AC ALR	Up to 100 Hz		84		dB
DC Power Supply Rejection Ratio (PSRR)	At 75% full-scale (FS) input, optimal settings, all gains[1]		60		dB
LED DRIVER					
Peak Current per Driver	LED pulse enabled		200		mA
Peak Current, Total	Using multiple LED drivers simultaneously		400		mA
Current Step	High SNR mode		1.57		mA
	Low compliance mode		0.78		mA
Compliance Voltage	High SNR mode		400		mV
	Low compliance mode		200		mV
Power	AFE current only, 70% FS output data rate (ODR) = 25 Hz				
Standby	DVDD + AVDD		0.3		µA
Typical Heart Rate Monitor (HRM) Application	DVDD + AVDD		18.7		µA
SAMPLING RATE		0.004		9000	Hz
ECG CHANNEL	Resolution is 286 nV, unless otherwise noted				
Input Bias Current	ECG input pins, room temperature, lead off detection is off, measured at dc		22		pA
Input Impedance	ECG input pins, measured at dc		20		GΩ
Differential Input Range		−1.2		+1.2	V
Electrode Single-Ended Input Voltage Range		0.2		AVDD3 − 0.2	V
Input Common-Mode Range		0.4		AVDD3 − 0.4	V
−3 dB Monitor Bandwidth	Data rate = 250 SPS	40			Hz
−3 dB Diagnostic Bandwidth	Data rate = 500 SPS	150			Hz
Gain Flatness	DC to 5.3 Hz (data rate = 250 SPS)		±1		%
	DC to 19 Hz (data rate = 500 SPS)		±1.5		%
Gain Error		−2		+2	%
Resolution			286		nV/LSB
			572		nV/LSB
Input Referred Noise					
10 Sec Measurement Using Internal Shorted Mode, Measured at Room Temperature	Data rate = 250 SPS, monitoring filter bandwidth (40 Hz)		0.38		µV RMS
	Data rate = 500 SPS, diagnostic filter bandwidth (150 Hz)		0.86		µV RMS
10 Sec System Level Measurement with Proper Electrode Model and	Data rate = 250 SPS, monitoring filter bandwidth (40 Hz)		0.5		µV RMS
	Data rate = 500 SPS, diagnostic filter bandwidth (150 Hz)		0.937		µV RMS

SPECIFICATIONS

Table 2. Performance Specifications (Continued)

Parameter	Test Condition/Comments	Min	Typ	Max	Unit
All Functions Enabled (DC Lead Off (DCLO) and AC Lead Off (ACLO)					
Channel Common-Mode Rejection Ratio (CMRR)	Balanced mode, measured at 60 Hz		115		dB
Output Date Rate	Aligned with filter design	250		4000	Hz
ECG Channel Enable Time	Data rate of 500 SPS		15		ms
Overload Recovery Time			10		ms
ECG Channel Power	ODR = 500 Hz, ACLO and DCLO functions enabled, resolution = 286 nV/LSB		1.7		mW
DCLO DETECTION					
Drive Circuit					
Lead Off Current Range	Lead fail current is programmable over the specified range, programmed current magnitude setting applies across all electrode pins, current polarity is programmable on individual electrode basis	0		1.1	µA
Measure Circuit					
Right Leg Driver (RLD)[2] Lead Off Thresholds		AVDD3 − 0.8		AVDD3 − 0.2	V
High		AVDD3 − 0.8		AVDD3 − 0.2	V
Low		0.2		0.8	V
ACLO THRESHOLD					
Drive Circuit					
Excitation Frequency			4		kHz
Current		0		70	nA
Measure Circuit					
Threshold		0.04		2.33	nF
RLD					
Output Voltage		GND	AVDD3/2	AVDD3	V
Stable Load Capacitance				2.2	nF
BIA CHANNEL SYSTEM PERFORMANCE	For impedance (Z) = 1 kΩ (0.1% tolerant resistor), excitation frequency ($f_{EXCITATION}$) = 50 kHz, sine amplitude = 0.6 V p-p, TIA resistor (R_{TIA}) = 2 kΩ, TIA capacitor (C_{TIA}) = 7 pF, isolation capacitor = 470 nF, current-limiting resistor (R_{LIMIT}) = 1 kΩ				
Total System Accuracy					
Magnitude			0.26		%
Phase			1		Degrees
Body Impedance Magnitude Error	Contact resistor ≤1 kΩ		0.26		%
	Contact resistor ≤20 kΩ		5		%
Body Impedance Magnitude Repeatability	Room temperature, test 10 times, contact resistor <1 kΩ		0.1		%
Body Phase Angle Error			1		Degrees
TRANSMIT STAGE					
Output Frequency Range			50	250	kHz
Output Frequency Resolution			0.48		Hz
Output Voltage Range				800	mV
Output Voltage Resolution			0.39		mV
RECEIVE STAGE					
Input Leakage Current					
Input Capacitance	Toward ground for current sensing		10		pF
	Toward ground for voltage sensing		10		pF

SPECIFICATIONS

Table 2. Performance Specifications (Continued)

Parameter	Test Condition/Comments	Min	Typ	Max	Unit
ADC Saturation Level	Voltage		±0.8		V
	Current (TIA = 2 kΩ)		±400		µA
CALIBRATION RESISTOR					
Internal			2		kΩ
Power Consumption	ODR = 30 Hz, DFT = 1024, R_{TIA} = 2 kΩ, $V_{EXCITATION\ p-p}$ = 600 mV, contact resistor ($R_{CONTACT}$) = body resistor (R_{BODY}) = 1 kΩ, $f_{EXCITATION}$ = 50 kHz, 12× time slots		11.2		mW
EDA CHANNEL					
TIA Gain	TIA feedback resistor	1		1000	kΩ
Programmable Gain Amplifier (PGA) Gain			1.5		
			2		
			3		
			6		
Discrete Fourier Transform (DFT) Points		4		8192	
DC Current Range	For DC current mode	0.002		1.1	µA
DC Excitation Voltage	For DC voltage mode	0.5		1.3	V
AC Voltage Excitation	For AC voltage mode			800	mV
AC Voltage Frequency	For AC voltage mode			100	Hz
Impedance Measurement					
Range		0.01		100	MΩ
Resolution			1		nS
Error				5	%
Power Consumption	ODR = 1 Hz, sampling frequency (f_S) = 2.5 kΩ, DFT = 512, DCLO current (I_{DCLO}) = 6 nA, R_{TIA} = 1 MΩ, body impedance (Z_{BODY}) = 1 MΩ		0.78		mW

[1] DC PSRR = 20 × log((Signal(LSB)/NUM_INT_x/NUM_REPEAT_x × 0.146 mV/LSB)/V_{IN} (mV))

[2] The ECG signals, RLD, ECGIP, and ECGIN, can be routed to each one of the ECG1 to ECG4 pins, controlled by settings within the ECG_MATRIX register.

DIGITAL SPECIFICATIONS

IOVDD = 1.7 V to 3.6 V, unless otherwise noted.

Table 3. Digital Specifications

Parameter	Test Condition/Comments	Min	Typ	Max	Unit
LOGIC INPUTS					
Input Voltage Level					
GPIOx, MISO, MOSI, SCLK, and $\overline{CS}$					
High		0.7 × IOVDD		IOVDD + 0.3	V
Low		−0.3		+0.3 × IOVDD	V
Input Current Level	All logic inputs				
High				10	µA
Low		−10			µA
Input Capacitance			2		pF
LOGIC OUTPUTS					
Output Voltage Level					
GPIOx and MISO					
High	2 mA high level output current	IOVDD – 0.5			V
Low	2 mA low level output current			0.5	V

SPECIFICATIONS

TIMING SPECIFICATIONS

Table 4. Timing Specifications

Parameter	Symbol	Test Condition/Comments	Min	Typ	Max	Unit
SPI PORT						
SCLK						
Frequency	f_{SCLK}				10	MHz
Minimum Pulse Width						
High	$t_{SCLKPWH}$		15			ns
Low	$t_{SCLKPWL}$		15			ns
$\overline{CS}$						
Setup Time	t_{CSS}	$\overline{CS}$ setup to SCLK rising edge	11			ns
Hold Time	t_{CSH}	$\overline{CS}$ hold from SCLK rising edge	5			ns
Pulse Width High	t_{CSPWH}	$\overline{CS}$ pulse width high	15			ns
MOSI						
Setup Time	t_{MOSIS}	MOSI setup to SCLK rising edge	5			ns
Hold Time	t_{MOSIH}	MOSI hold from SCLK rising edge	5			ns
SWITCHING CHARACTERISTICS						
MISO Output Delay	t_{MISOD}	MISO valid output delay from SCLK falling edge				
		Register 0x057 = 0x0050 (default)			21.5	ns
		Register 0x057 = 0x005F (maximum slew rate, maximum drive strength for SPI)			14	ns

Timing Diagram

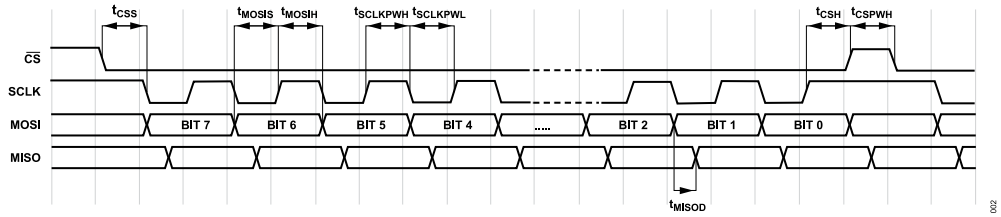

Figure 2. SPI Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 5. Absolute Maximum Ratings

Parameter	Rating
AVDD to AGND	−0.3 V to +2.2 V
AVDD3 to AGND	−0.3 V to +3.9 V
DVDD to DGND	−0.3 V to +2.2 V
IOVDD to IOGND	−0.3 V to +3.9 V
GPIOx, MOSI, MISO, SCLK, $\overline{CS}$ to DGND	−0.3 V to +3.9 V
LEDxx to LGND	−0.3 V to +3.9 V
Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure, and θ_{JC} is the junction to case thermal resistance.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CB-36-11[1]	42.15	0.98	°C/W

[1] The thermal resistance values are defined as per the JESD51-12 standard.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

Machine model (MM) per ANSI/ESD STM5.2. MM voltage values are for characterization only.

ESD Ratings for ADPD7000

Table 7. ADPD7000, 36-Ball WLCSP

ESD Model	Withstand Threshold (V)	Class
HBM	2500	2
CDM	1250	C3

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

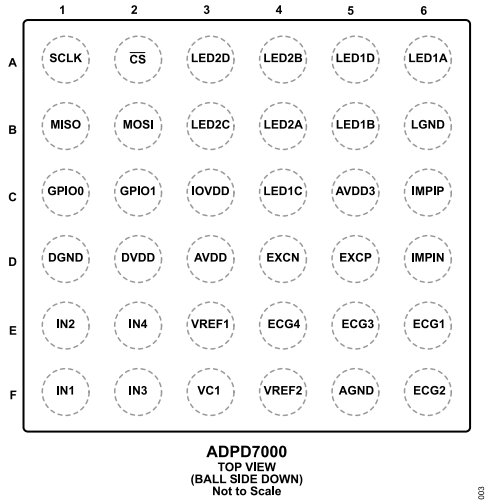

Figure 3. Pin Configuration, Top View

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
D3	AVDD	Power	1.8 V Analog Power Supply.
C5	AVDD3	Power	3.3 V Analog Power Supply.
F5	AGND	Power	Analog Ground.
D2	DVDD	Power	1.8 V Digital Power Supply.
D1	DGND	Power	Digital Ground.
C3	IOVDD	Power	Input and Output Power Supply.
B6	LGND	Power	LED Ground.
E3	VREF1	Analog	ADC 1 Reference.
F4	VREF2	Analog	ADC 2 Reference.
F3	VC1	Analog	Output Voltage Source 1 for Photodiode Common Cathode Bias or Other Sensor Stimulus.
F1	IN1	Analog	Current Input 1.
E1	IN2	Analog	Current Input 2.
F2	IN3	Analog	Current Input 3.
E2	IN4	Analog	Current Input 4.
A6	LED1A	Analog	LED Driver 1A.
B5	LED1B	Analog	LED Driver 1B.
C4	LED1C	Analog	LED Driver 1C.
A5	LED1D	Analog	LED Driver 1D.
B4	LED2A	Analog	LED Driver 2A.
A4	LED2B	Analog	LED Driver 2B.
B3	LED2C	Analog	LED Driver 2C.
A3	LED2D	Analog	LED Driver 2D.
E6	ECG1	Analog	ECG Electrode Pad 1.
F6	ECG2	Analog	ECG Electrode Pad 2.
E5	ECG3	Analog	ECG Electrode Pad 3.
E4	ECG4	Analog	ECG Electrode Pad 4.
C6	IMPIP	Analog	BIA Positive Input.
D6	IMPIN	Analog	BIA Negative Input.
D5	EXCP	Analog	BIA Excitation Positive Output.
D4	EXCN	Analog	BIA Excitation Negative Output.
A2	$\overline{CS}$	Digital	SPI Chip Select Input.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 8. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Type	Description
A1	SCLK	Digital	SPI Clock Input.
B1	MISO	Digital	SPI Controller Input and Target Output.
B2	MOSI	Digital	SPI Controller Output and Target Input.
C1	GPIO0	Digital	General-Purpose Input and Output 0.
C2	GPIO1	Digital	General-Purpose Input and Output 1.

TYPICAL PERFORMANCE CHARACTERISTICS

DVDD = AVDD = 1.8 V, AVDD3 = 3.3 V, LGND = DGND = AGND = 0 V, and T_A = 25°C, unless otherwise noted.

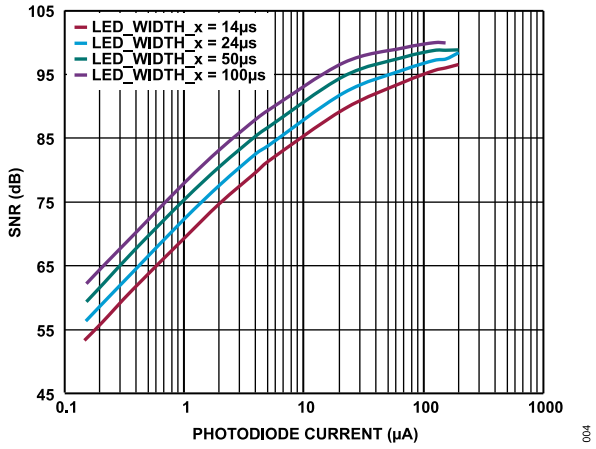

Figure 4. SNR vs. Photodiode Current, Number of Sequence Repeats = 1, TIA Gain = 100 kΩ

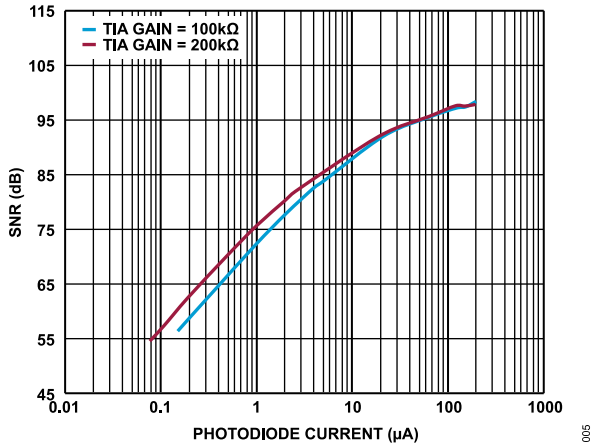

Figure 5. SNR vs. Photodiode Current, LED Width = 24 µs, Number of Sequence Repeats = 1

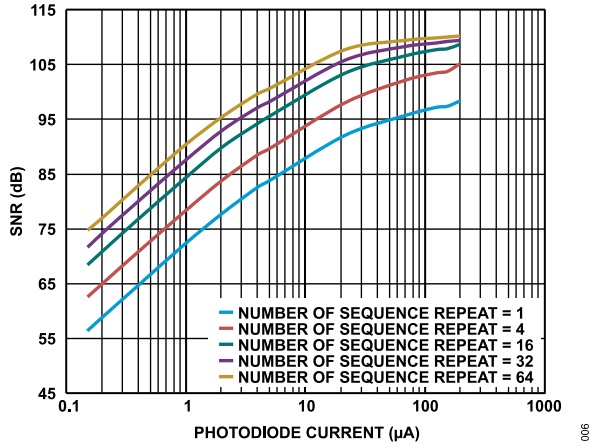

Figure 6. SNR vs. Photodiode Current, LED Width = 24 µs, TIA Gain = 100 kΩ

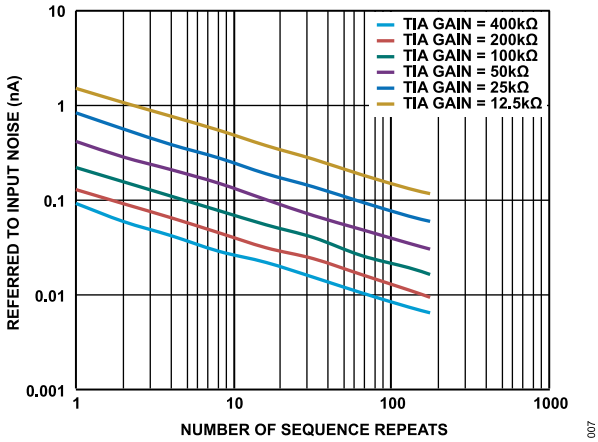

Figure 7. Referred to Input Noise vs. Number of Sequence Repeats

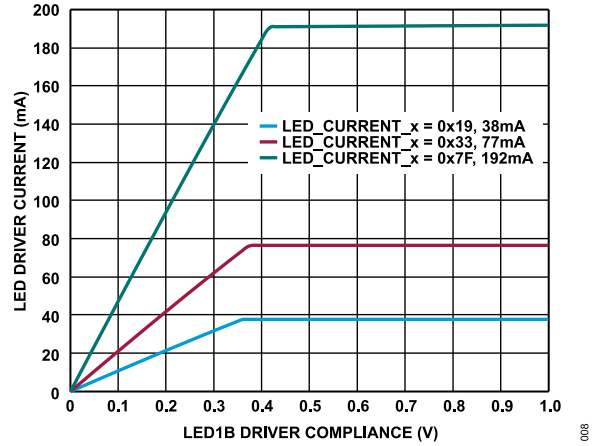

Figure 8. LED Driver Current vs. LED1B Driver Compliance, High SNR Mode

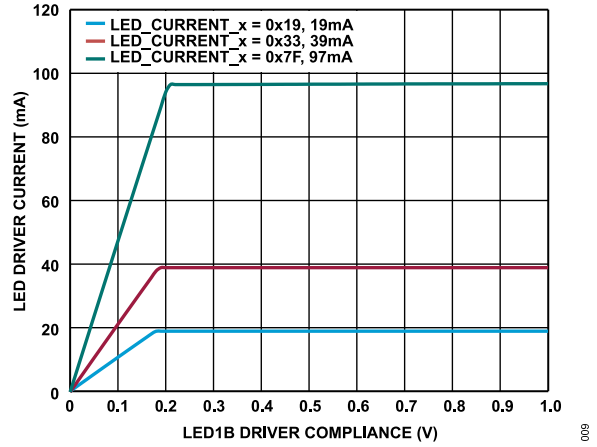

Figure 9. LED Driver Current vs. LED1B Driver Compliance, Low Compliance Mode

TYPICAL PERFORMANCE CHARACTERISTICS

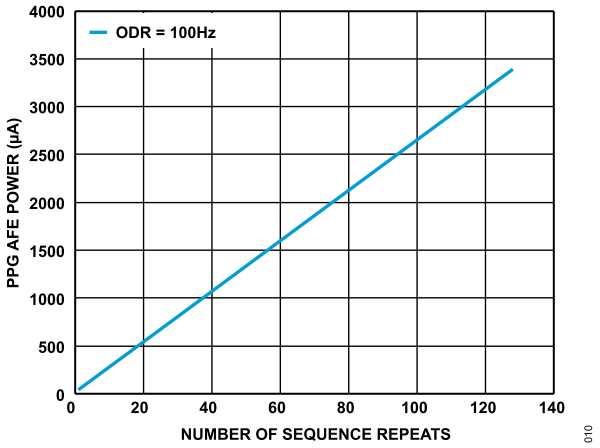

Figure 10. PPG AFE Power vs. Number of Sequence Repeats

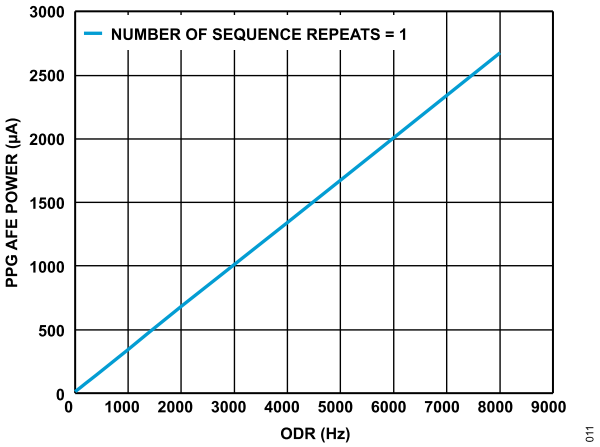

Figure 11. PPG AFE Power vs. ODR

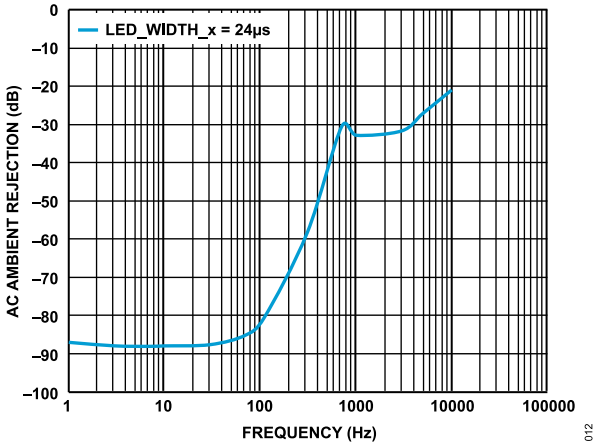

Figure 12. AC Ambient Rejection vs. Frequency

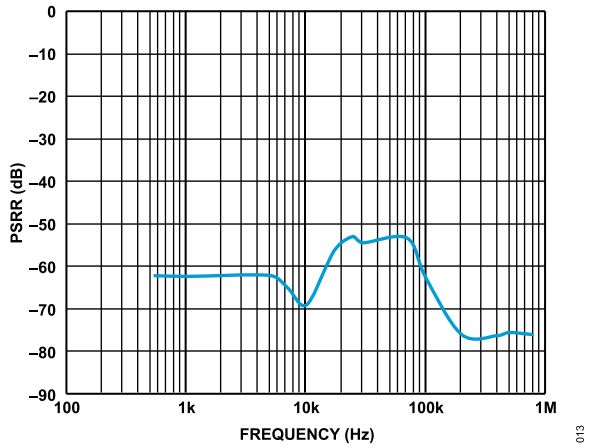

Figure 13. PSRR vs. Frequency, Photodiode Current = 8 µA

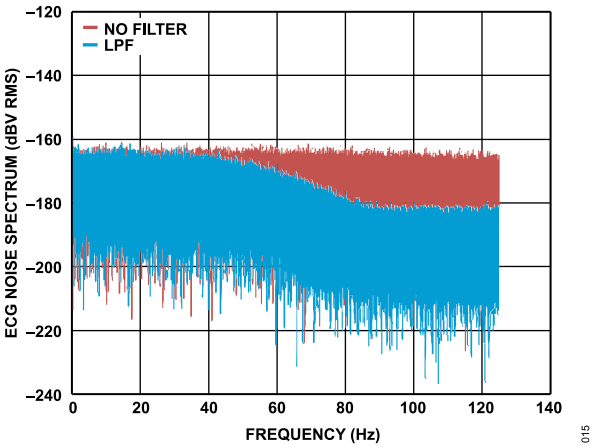

Figure 14. ECG Noise Spectrum vs. Frequency, Input Shorted to Common-Mode Voltage (V_{CM}), Resolution = 286 nV/LSB, Sample Rate = 250 Hz (LPF Is Low Pass Filter)

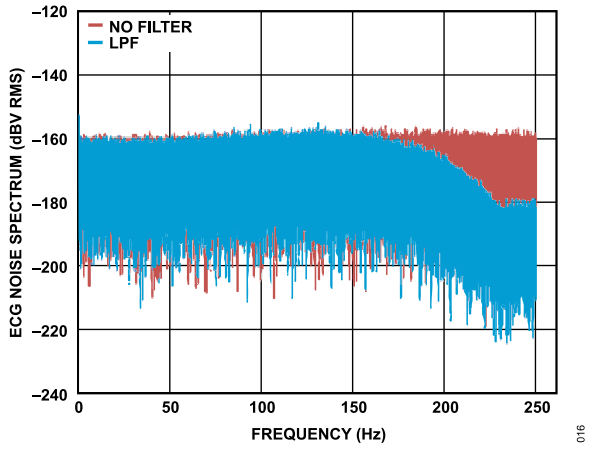

Figure 15. ECG Noise Spectrum vs. Frequency, Input Shorted to V_{CM}, Resolution = 286 nV/LSB, Sample Rate = 500 Hz

TYPICAL PERFORMANCE CHARACTERISTICS

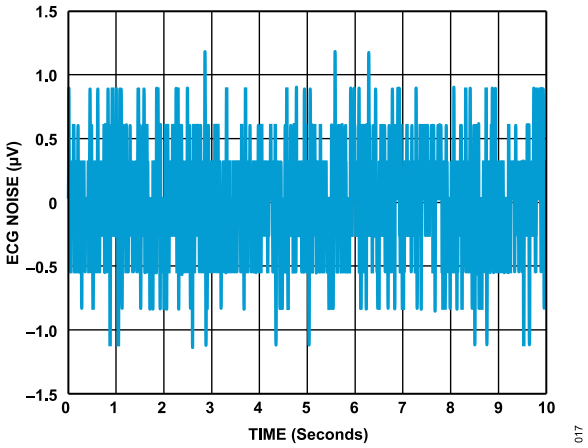

Figure 16. ECG Noise vs. Time, Input Shorted to V_{CM}, Resolution = 286 nV/LSB, Sample Rate = 250 Hz

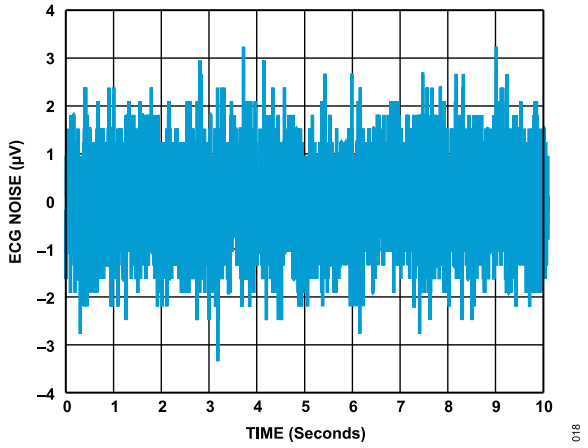

Figure 17. ECG Noise vs. Time, Input Shorted to V_{CM}, Resolution = 286 nV/LSB, Sample Rate = 500 Hz

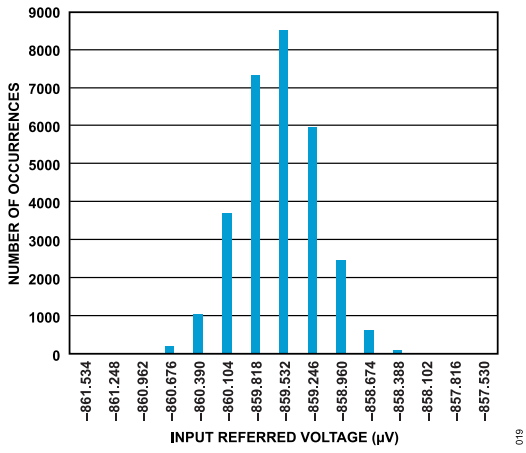

Figure 18. ECG Noise Histogram, Input Shorted to V_{CM}, Resolution = 286 nV/LSB, Sample Rate = 250 Hz

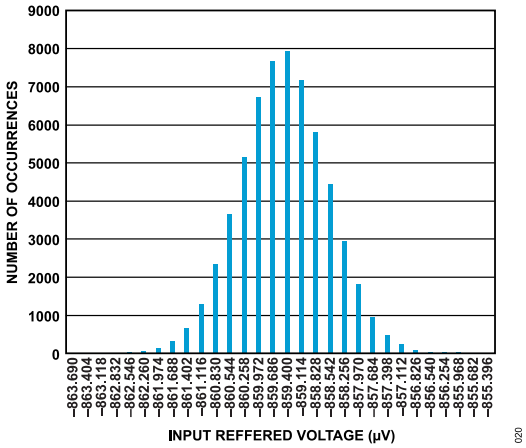

Figure 19. ECG Noise Histogram, Input Shorted to V_{CM}, Resolution = 286 nV/LSB, Sample Rate = 500 Hz

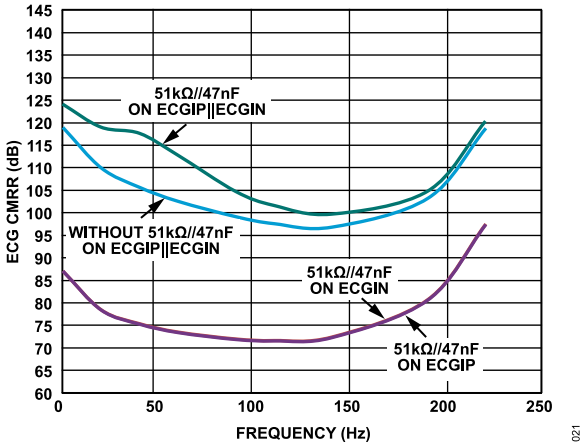

Figure 20. ECG CMRR vs. Frequency, Resolution = 286 nV/LSB, Sample Rate = 500 Hz

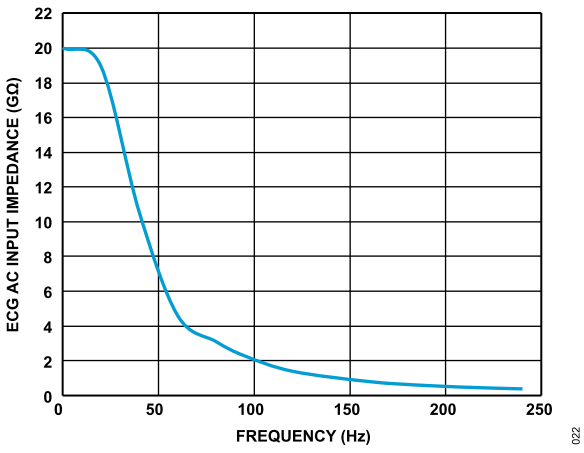

Figure 21. ECG AC Input Impedance vs. Frequency, Resolution = 286 nV/LSB, Sample Rate = 500 Hz

TYPICAL PERFORMANCE CHARACTERISTICS

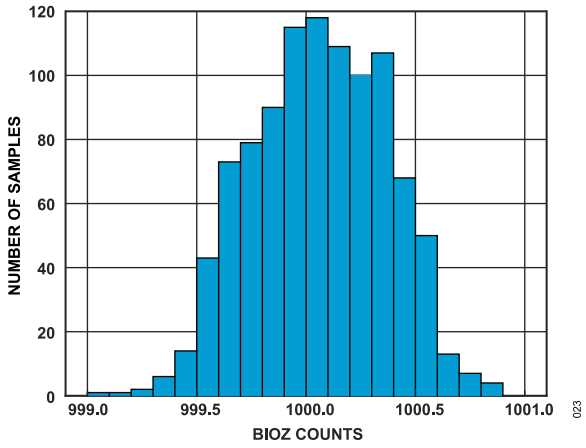

Figure 22. Bioimpedance (BIOZ) Noise Histogram ($f_{EXCITATION}$ = 50 kHz, TIA GAIN = 2 kΩ, DFT = 1024, $Z_{CONTACT}$ = 1 kΩ, Z_{BODY} = 1 kΩ)

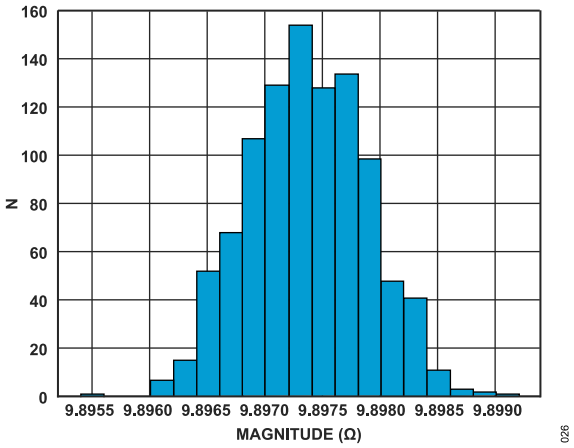

Figure 25. EDA Noise Histogram, f_S = 2.5 kΩ, DFT = 1024, PGA = 1.5, and ODR = 100 Hz

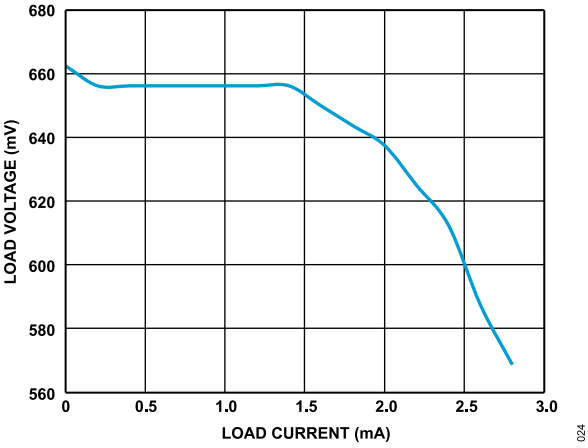

Figure 23. BIOZ Drive Capability

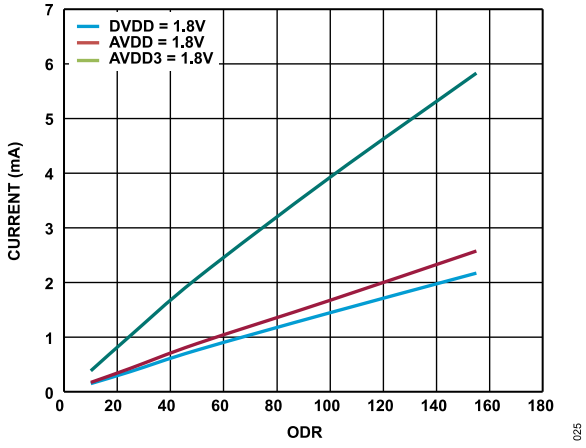

Figure 24. Power Consumption vs. ODR (12 Time Slots, DFT = 1024)

THEORY OF OPERATION

INTRODUCTION

The ADPD7000 is a multimodal, vital signal monitoring AFE that comprises four high performance signal chains: an optical measurement path (PPG), ECG measurement path, BIA measurement path, and EDA measurement path.

The PPG measurement path works as a transceiver that supports up to eight LEDs and four photodiode inputs. The current on the LEDs is programmable from two 7-bit LED drivers. The receiver path provides two high performance readout channels that can sample simultaneously and can be configured separately. Two high performance current DACs (IDACs) are implemented in each channel to provide first class ambient light suppression and large dynamic range in different application scenarios.

The ECG measurement path offers a high input impedance, low noise, high dynamic range solution to allow high quality ECG signal acquisition in wearable devices. Both DCLO detection and ACLO detection are integrated to guarantee proper detectability.

The stimulus in the BIA path offers a sine wave with various options for frequency, amplitude, and phase to make the ADPD7000 suitable for measurement in different scenarios. A low noise TIA, PGA, filter, and ADC are integrated in the receiver channel to provide high performance impedance measurement. Direct digital synthesis (DDS) and DFT engines are also integrated in this path.

The EDA measurement path offers different modes, including AC voltage measurement, DC voltage measurement, and DC current measurement, which provide low noise, high measure accuracy in EDA application.

An internal state machine allows flexible control of these three measurement paths. The acquisition data can be stored in a 704-byte FIFO.

TIME SLOT OPERATION

An internal configurable controller handles the operation of the ADPD7000. This controller generates the timing needed to generate sampling regions comprising combinations of the three measurement paths and sleep periods. To facilitate the use of multiple signal chains, multiple time slots handle the access to different transmitters or receivers.

The system is characterized by the ODR, which determines the repetition periodicity of each enabled time slot. The enabled time slots are repeated at the time slot rate configured by the TIMESLOT_PERIOD_x bits.

There are 31 time slots in the ADPD7000, as shown in Figure 26.

Each enabled PPG and BIA time slot is repeated at the time slot rate, followed by an ultra-low power sleep period.

ECG_TS is the ECG time slot. The operation of the ECG signal chain is not in time slot fashion. After the ECG time slot turns on, the ECG signal chain runs until the system stops. However, the ECG signal chain output data is synchronized to the FIFO with this time slot rate.

Following the ECG time slot, there are 12 PPG time slots (PPG_TSA to PPG_TSL). Each PPG time slot allows the creation of one or more LED pulses and modulate pulses, as well as the acquisition of the photodiode or other device current based on that stimulus. The operating parameters for each time slot are highly configurable.

The last 18 time slots are the BIA time slots (BIA/EDA_TSA to BIA/EDA_TSR), which is shared with the EDA time slots. Each BIA time slot allows the excitation voltages, frequencies, and receiver configurations to facilitate accurate body impedance measurement.

Equation 1 determines the sampling rate (time slot rate), as follows:

$$\text{Sampling Rate} = \text{Timer Clock Frequency (Hz)} / \text{TIMESLOT\_PERIODx} \quad (1)$$

Table 9. Sources of Low Frequency Clock (LFCLK) and Timer Clock[1]

LFCLK	Timer Clock	ALT_CLOCKS	TM_CLK_GPIO_SEL
960 kHz Internal	960 kHz internal	0	N/A
960 kHz External	960 kHz external	1	N/A
960 kHz Internal	960 kHz internal	2	N/A
1 MHz External (Divided from 32 MHz)	1 MHz external (divided from 32 MHz)	3	N/A
960 kHz Internal	960 kHz external	4	1
960 kHz Internal	32 kHz external	4	0

[1] N/A means not applicable.

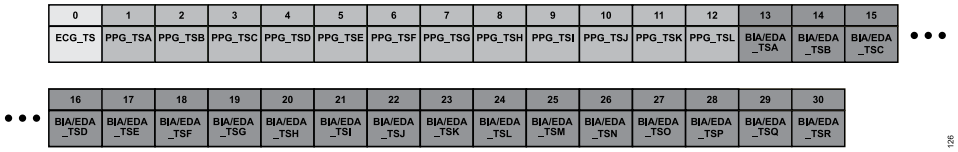

Figure 26. Time Slot Allocation

THEORY OF OPERATION

LEAD-ON DETECTION

The lead-on detection feature on the ADPD7000 delivers an ultra-low power mode by setting the LEAD_ON_MODE bit (Register 00F, Bit 11) to 1 when the operating mode is set to stand by or PPG only mode. When the operating mode is set to go with any ECG or BIOZ time slot enabled, some of the lead-on detection circuits are controlled by the ECG and/or BIOZ time slot operation; therefore, the lead-on detection mode is ignored.

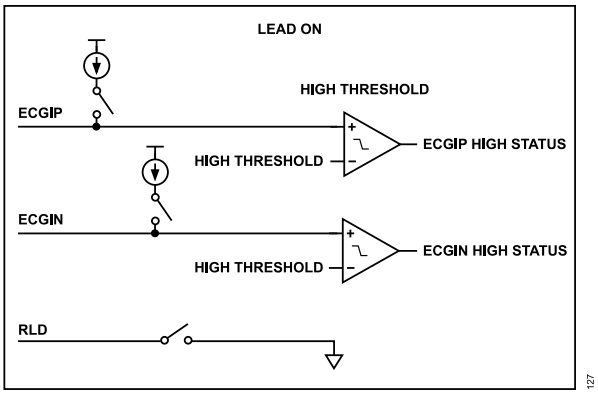

Figure 27. Lead-On Detection

OPTICAL SIGNAL CHAIN

The optical signal path stimulates up to eight LEDs and measures the return signal on up to four separate current inputs. Twelve optical time slots enable 12 separate optical measurements per sampling period.

The analog inputs can be driven single-ended or in differential pairs. The four analog inputs can be multiplexed into a single channel or two independent channels, enabling simultaneous sampling of two sensors.

The optical signal chain consists of a TIA, an integrator that can also be configured as a buffer depending on the register setting, and an ADC. The digital block provides multiple operating modes, programmable timing, and block averaging.

Two independent LED drivers are provided that can each drive up to 200 mA. Two LED drivers can be enabled in any time slot and can be programmed from 1.57 mA to 200 mA monotonically, with a 7-bit register setting. The LED drivers enabled in any time slot can provide a combined maximum LED current of 400 mA.

When making optical measurements, ambient light rejection is automatic without the need of external control loops, dc current subtraction, or digital algorithms.

The LED driver is a current sink and is independent from the LED supply voltage and the LED type. The optical measurement path produces a high SNR for relatively low LED power, while greatly reducing the effect of ambient light on the measured signal.

Analog Signal Path

The analog signal path of the optical signal chain consists of four current inputs that can be configured as single-ended or differential pairs into one of four independent channels. The four channels can be sampled simultaneously for applications that require instantaneous sampling of four sensors.

Analog Input Multiplexer

The optical signal chain supports four analog input pins. Each input can be used as a single-ended input or as part of a differential pair. Figure 28 shows a single representation of the input switch matrix, which allows a programmable connection to the four optical channels. Each pair of inputs has a duplicate of this multiplexer: IN1 and IN2, and IN3 and IN4. The connections are programmable per time slot.

The PAIR12 and PAIR34 bits select whether the matching input pair is used as two single-ended inputs or as a differential pair. This selection is valid for all active time slots. The INP12_x and INP34_x bits specify whether the input pair is enabled during the corresponding time slot and, if enabled, which input is connected to which optical channel. Note that Channel 1 and Channel 2 support single-ended or differential inputs, while Channel 3 and Channel 4 only support a single-ended input.

The sleep conditions are used for any inputs that are not enabled. Sleep conditions are determined by the INP_SLEEP_12 and INP_SLEEP_34 bits, which specify the state for the input pairs during sleep and when the inputs are not active. Inputs are only considered active during the precondition and pulse regions for time slots where they are enabled.

Preconditioning of the sensor connected to the input is provided to set the operating point at the input before sampling. There are several different options for preconditioning determined by the PRECON_x bits. The PRECON_x bits are provided for each time slot to specify the precondition for enabled inputs or input pairs during the corresponding time slot. Preconditioning options include floating the inputs, VC1, an internal voltage reference signal for the TIA (TIA_VREF), a TIA input, and shorting the input pair. The preconditioning time at the start of each time slot is programmable using the PRE_WIDTH_x bits. The default preconditioning period is 4 µs.

The block diagram in Figure 28 shows the bias levels that can be switched into the input connections during sleep and preconditioning. These connections are not available during the sampling phase of a time slot in which the input is selected.

THEORY OF OPERATION

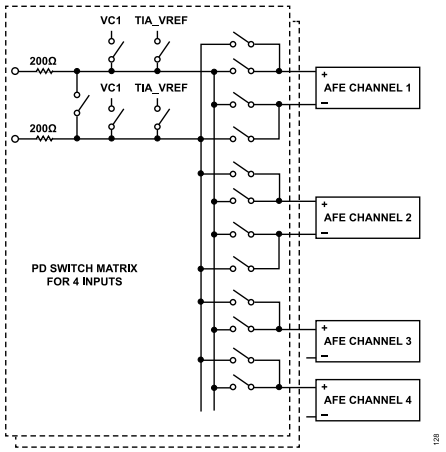

Figure 28. Switch Matrix Block Diagram

Ambient Light Cancellation

The ADPD7000 has three modes to perform ambient light cancellation, as follows:

- Coarse tuning only
- Coarse and fine tuning loop
- External microcontroller unit (MCU) control

Coarse tuning only mode and coarse and fine tuning loop mode are automatically controlled by the ADPD7000 without any software assistance. External MCU control mode allows tuning the ambient light rejection through an external algorithm.

Use the AMBIENT_CANCELLATION_x bits to choose the mode.

Coarse tuning mode works at the beginning of each PPG time slot. This mode measures the ambient light level and sets the ambient DAC code. This circuitry needs 48 µs to complete these activities and determine the baseline of the ambient DAC. Afterward, the PPG channel can start normal operation–for example, if in digital integration mode, the PPG receiver channel can start to take dark samples. This ambient baseline is used in the time slot if coarse tuning only mode is enabled.

If coarse and fine tuning loop mode is enabled, the coarse tuning circuit works the same way as in coarse tuning mode. However, the ambient DAC code updates after each dark sample measurement.

Select these two modes with the AMBIENT_CANCELLATION_x bits for system level design flexibility.

Coarse loop mode makes the measurement to find the accurate value of the ambient current. Then, the ambient DAC subtracts the ambient current at the beginning of the signal chain so that it does not corrupt the PPG signal measurement.

Both analog integration mode and digital integration mode can perform coarse loop ambient rejection.

The fine tuning loop updates the ambient information after each dark sample measurement. This feature is available only in digital integration mode.

The MCU mode allows the user to subtract the ambient current. The DAC_AMBIENT_CH1_x and DAC_AMBIENT_CH2_x bits are designed to allow the user to fill in the current ambient value, and the AFE then subtracts that value from the signal chain. DAC_AMBIENT_CH1_x and DAC_AMBIENT_CH2_x are 9-bit fields, with each LSB representing a 0.6 µA step in a 0 µA to 300 µA range.

LED DC Cancellation

Besides the ambient DAC, there is another IDAC at the input of each signal chain. This IDAC is used to subtract the unwanted dc component in the reflected LED to increase the dynamic range of the receiver channel.

These two IDACs are controlled by the MCU only. The DAC_LED_DC_CH1_x and DAC_LED_DC_CH2_x bits control the LED dc canceling, 7-bit IDAC with full scale.

The LED dc subtraction feature is available only for digital integration mode.

A certain amount of dc current can be subtracted from the AFE based on the top level optical and system design. DAC_LED_DC_CH1_x and DAC_LED_DC_CH2_x are 7-bit fields, with each LSB representing a 1.5 µA step in a 0 µA to 190 µA range.

LED Drivers

The optical path has two LED drivers, each of which is brought out to four LED driver outputs, providing a total of eight LED output drivers. The device can drive up to two LEDs simultaneously, one from each driver pair. The LED output driver is a current sink. Figure 29 shows an example of a single LED driver output pair.

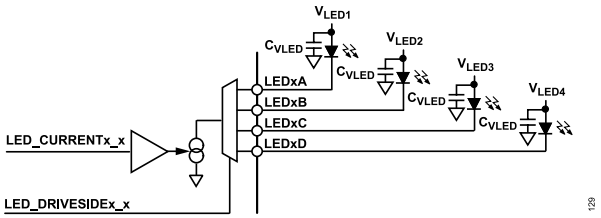

Figure 29. LED Driver Output Pair (C_{VLED} Are the Bypass Capacitors)

The LED driver output pins (LED1A, LED2A, LED1B, LED2B, LED1C, LED2C, LED1D, and LED2D) have a maximum allowable pin voltage of 3.6 V. Any voltage exposure over this rating affects the reliability of the device operation and, in certain circumstances, causes the device to cease proper operation. The voltage of the LED driver output pins must not be confused with the supply voltages of the LEDs. V_{LEDx} is the voltage applied to the anode of the external LED, whereas the LED output driver pins are connected to the cathode of the external LEDs. The compliance voltage is

THEORY OF OPERATION

the amount of headroom voltage at the LED driver pins, measured with respect to ground, required to maintain the programmed LED current levels. The compliance voltage is a function of the current required.

ECG SIGNAL CHAIN

The ECG channel measures the differential voltage across two electrodes to create a lead measurement. The output of this channel is a 24-bit digital word representing the measured ECG voltage. The maximum input differential signal is ±1.2 V, and the LSB size is 286 nV. The output data rate can be 250 SPS, 500 SPS, 1 kSPS, 2 kSPS, or 4 kSPS. This filter selection affects the digital processing but not the analog processing. Additionally, a 4 kHz AC lead off signal is converted by the analog ECG path and extracted in the digital domain.

The ECG channel has a dedicated ADC path with feedback arrangement to remove the DC offset presented by the ECG electrodes. The ECG channel is designed to provide a high quality ECG signal process while suppressing the large DC offset that is caused by the complex system design.

Both DC and AC lead off detection and DC lead on detection are integrated to accommodate different complex lead contact conditions to provide reliable lead information.

The RLD signal is designed to better bias the human body potential to avoid interference.

ECGIP and ECGIN are the signal inputs for the ECG channel, and these inputs must be connected to the input leads. The RLD signal must be connected to the reference lead.

The ECG signals (RLD, ECGIP, and ECGIN) can be routed to each one of the ECG1 to ECG4 pins, controlled by settings within the ECG_MATRIX register.

ECG Main Signal Chain

Figure 30 shows the ECG main signal chain diagram.

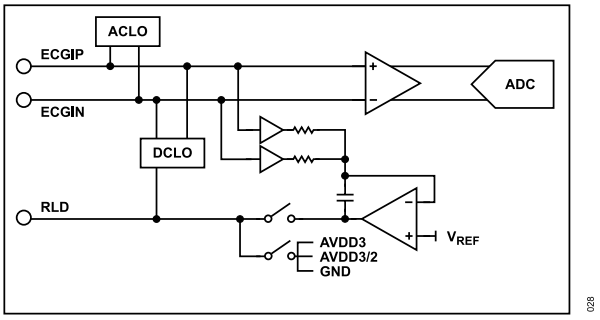

Figure 30. ECG Main Signal Chain Diagram

DC Lead Off (DCLO) Detection

The DCLO circuit injects a small programmable DC current into each input electrode and monitors the resulting electrode voltage. Figure 31 shows the DCLO detection diagram.

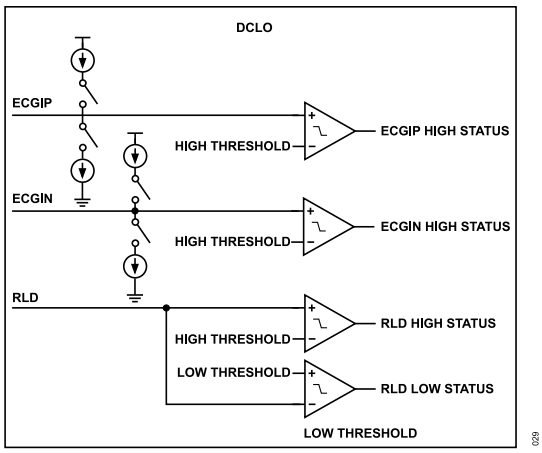

Figure 31. DCLO Detection Diagram

When both the ECGIP and ECGIN signals are properly connected, the current flow from one of the ECG inputs through the patient and into the other ECG input produces a minimal voltage shift. The fail current magnitude is common across all ECG electrodes and programmable from 0 nA to 1.1 µA.

The polarity of the fail current is independent for each electrode and programmed using the ECG_DCLO_POLARITY_IN and ECG_DCLO_POLARITY_IP bits (see Register 0x101). When an electrode connection degrades or falls off, the signal voltage of that electrode is pulled high or low depending on the programmed fail current polarity.

The detection circuit is based on each individual electrode input (ECGIP and ECGIN). The detection circuit uses comparators based with independent programmable threshold levels for ECG inputs.

For each input lead (ECGIP and ECGIN), there is only one comparator with a high-side threshold. For the RLD signal, there are two comparators with a high-side threshold and low-side threshold.

These threshold limits are chosen such that all the threshold voltages cover the expected signal range. The window comparator compares the electrode input voltage with the corresponding threshold voltages. When the voltage change on a particular electrode exceeds one of the programmed threshold voltages for that fail current, the DC resistance of the electrode contact can flag a lead off.

AC Lead Off (ACLO) Detection

The ECG path has an ACLO detection circuit that can be used for lead off detection with the DCLO detection circuit to deal with different types of lead. Figure 32 shows the ACLO detection diagram.

THEORY OF OPERATION

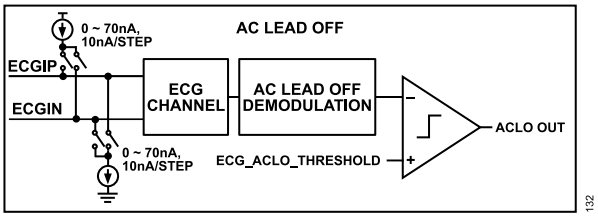

Figure 32. ACLO Detection Diagram

The ACLO method of sensing if the electrodes are connected to the patient is based on injecting AC currents into each ECG electrode and measuring the amplitudes of the resulting voltages through the ECG channel. The ECG channel must be enabled to use the ACLO function.

The magnitude of the ACLO current is programmable through the ECG_ACLO_MAG bits. The AC current is driven out onto the ECG input paths and establishes a voltage between the ECG channel inputs where it is measured. The measured voltage is synchronously demodulated and sent through a comparator. The user can set the threshold though the ECG_ACLO_THRESHOLD bits.

The ACLO detection functions only on the ECG input pins (ECGIP and ECGIN) and is not supported for the RLD signal. A properly connected electrode has a small signal because the drive current flows into the right leg (RL). An improperly connected or dried out electrode has a larger signal as determined by a capacitive voltage divider.

Right Leg Driver (RLD)

The use of a driven reference benefits overall performance by improving common-mode rejection of noise and interference from external sources, such as power line interference (50 Hz or 60 Hz) or other patient connected instruments. The drive stage also acts to absorb lead fail currents injected into the ECG electrodes.

The reference electrode drive circuit senses the V_{CM} of the patient and drives an inverted version back to the body, creating a negative feedback loop around the patient. The RLD amplifier uses V_{CM} = AVDD3/2, which centers the electrode voltages in the middle of the ADC input range. Each electrode input is buffered and fed to the RLD amplifier through a switch.

The amount of capacitance on the RLD signal affects the RLD amplifier. For best performance, the capacitance on this node must be less than 2.2 nF. In normal operation, the RLD amplifier output is applied to the RL electrode via the RLD signal and associated protection network.

The RLD amplifier can be turned off and the user can drive the RLD signal by selecting a voltage in the ECG_RLD_OUT_SEL bits.

BIA SIGNAL CHAIN

The BIA signal chain is designed for body impedance measurement. The signal chain consists of a high frequency precision excitation loop and a measurement channel, which enables a wide capability of measurement of the different bioimpedance configurations.

The excitation loop consists of a 12-bit DAC, referred to as the high speed DAC. This DAC is capable of generating high frequency excitation signals up to 250 kHz.

The measurement channel features an ADC with input buffers, a built-in antialias filter, and a PGA.

An ultralow leakage, programmable switch matrix connects the sensor to the internal analog excitation and measurement blocks. This matrix provides an interface for connecting external bioimpedance and calibration resistors. Figure 33 shows the block diagram of this BIA signal chain.

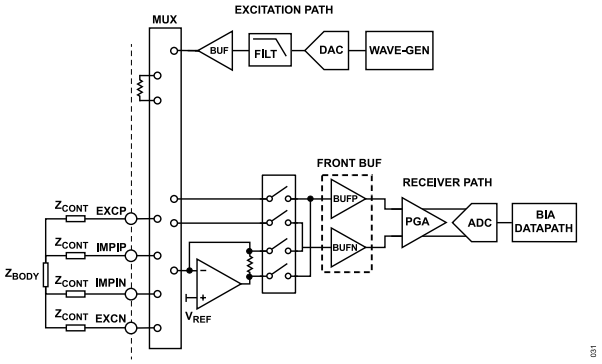

Figure 33. BIA Channel Block Diagram (Z_{CONT} Is Contact Impedance)

The input multiplexer (mux) of the excitation loop is controlled by the BIOZ_TSW_x, BIOZ_DSW_x, and BIOZ_RINT_SW_x bits. The input mux for the measurement path is controlled by the BIOZ_NCHAN_x and BIOZ_PCHAN_x. Table 10 shows the connections of the input mux with the related bit setting. The flexible design of the BIA channel allows different configurations of the measurement.

Table 10. TIA Connections in the BIA Channel

Bit Name	Setting	Connection
BIOZ_TSW_x	0001	IMPIP
	0010	IMPIN
	0100	EXCP
	1000	EXCN
BIOZ_RINT_SW_x, Bits[1:0]	1	The internal resistor (R_{INT}) that connects to the external buffer (EXCBUF) and the high power TIA (HPTIA) blocks
	0	R_{INT} no connection
BIOZ_DSW_x	0001	IMPIP
	0010	IMPIN
	0100	EXCP
	1000	EXCN
BIOZ_NCHAN_x	000	HPTIA_n[1]
	001	IMPIN

THEORY OF OPERATION

Table 10. TIA Connections in the BIA Channel (Continued)

Bit Name	Setting	Connection
	010	EXCP
	011	R_{INT_SN}[2]
	100	IMPIP
	101	EXCN
	110	ECG RLD (EDA only)
	111	ECGIP (EDA only)
BIOZ_PCHAN_x	000	HPTIA_p[1]
	001	IMPIP
	010	EXCN
	011	R_{INT_SP}[2]
	100	IMPIN
	101	EXCP
	110	ECGIN (EDA only)
	111	ECGIP (EDA only)

[1] HPTIA_n and HPTIA_p refer to the two terminals of the TIA resistor.

[2] R_{INT_SN} and R_{IN_SP} refer to the two terminals of the internal resistor.

The frequency of the generated sine wave is controlled by the BIOZ_SINEFCW_x_x bits, whereas the amplitude of the sine wave is controlled by the BIOZ_SINEAMPLITUDE_x bits. The BIOZ_SINE_PHASE_OFFSET_x bits are used to control the sine wave phase.

Use the following equations to set the voltage output (V_{OUT}) amplitude and sine wave frequency with these bits, respectively, as follows:

$$V_{OUT} = 0.8 \times \frac{BIOZ\_SINEAMPLITUDE\_x}{2^{11}} \text{ V p-p} \quad (2)$$

$$Frequency = \frac{32M \times BIOZ\_SINEFCW\_x\_x}{2^{26}} \text{ Hz} \quad (3)$$

The TIA gain can be accessed through the BIOZ_TIA_RGAIN_x bits.

After digitizing the measurement, the ADC output is sent to the datapath of the BIA channel, which includes filters, gain controls, and DFT. The DFT result is I data and Q data of the received sine wave, and the data format is 3 bytes or 4 bytes and is controlled by the BIOZ_DATA_SIZE_x bit.

When the chain turns on, the DFT path can wait before performing the DFT. The waiting time is controlled by the BIOZ_ADC_CONV_DLY_x registers.

For accurate measurement, the chip must perform ratio measurement. That is, the chip must measure the known internal resistor at R_{INT}, and then measure the unknown resistor. Use the ratio method to calculate the resistor under test.

EDA SIGNAL PATH

EDA, also known as galvanic skin response (GSR), measures the electrical activity conducted through sweat glands in the skin, which indicates the intensity of an emotion experienced.

The ADPD7000 supports three measurement modes: AC voltage, DC voltage, and DC current. To calculate the unknown impedance, measure the current (I) flow into the unknown impedance and also measure the voltage across the unknown impedance ($V_{Z_{UNKNOWN}}$). Use the following equation to calculate the unknown impedance:

$$|Z| = \frac{V_{Z_{UNKNOWN}}}{I} \quad (4)$$

Typically, the use of two electrodes can measure the EDA (see Figure 34). The excitation signal is a low frequency excitation, and the measurement result is the combination of the skin impedance and the electrode contact impedance.

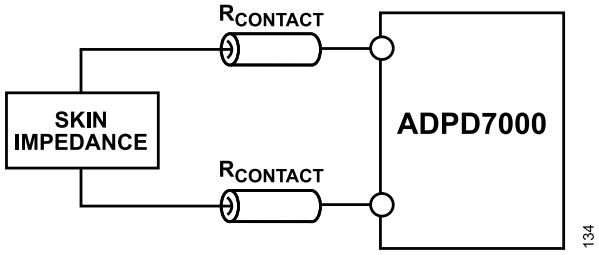

Figure 34. EDA Measurement Method

FIFO

The FIFO is never written with partial packets of data. If there is not enough room for the data that is written to the FIFO for all enabled time slots and any selected status bytes, no data is written from any of the time slots during that period and the INT_FIFO_OFLOW status bit is set.

The order of samples written to the FIFO (if selected) is dark data followed by lit data. Table 11 shows the byte order for multibyte words.

Table 11. Byte Order for FIFO Writes

Size	Byte Order (After Shift)
8	[7:0]
16	[15:8], [7:0]
24	[23:16], [15:8], [7:0]
32	[31:24], [23:16], [15:8], [7:0]

The FIFO size is 704 bytes. When the FIFO is empty, a read operation returns 0xFF, and the INT_FIFO_UFLOW status bit is set.

ECG Data Format

The data in the ECG is channel is 24-bit unsigned data with a status byte as a header. Figure 35 shows the data in the ECG channel.

THEORY OF OPERATION

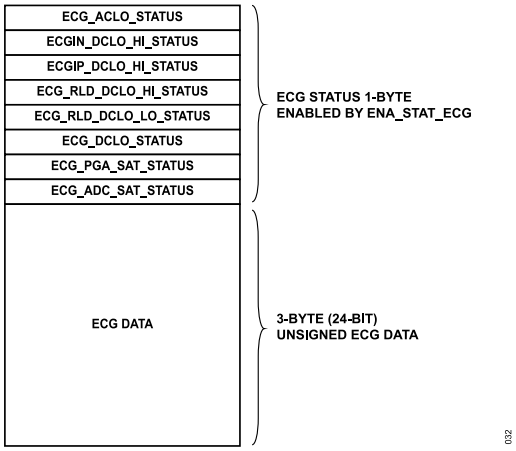

Figure 35. ECG Data Format

If ENA_STAT_ECG is set to 1, the ECG output data is a 4-byte structure, where the highest byte is the ECG related status information. If ENA_STAT_ECG is set to 0, the ECG output data is a 3-byte structure with only ECG channel output data.

PPG Data Format

At the end of each time slot, the selected data is written to the FIFO. The packet can include 0-, 8-, 16-, 24-, or 32-bit data for each of the dark data, signal data, or lit data values. The bit alignment of the data written to the FIFO is selectable with a shift of 0 bits to 31 bits, with saturation provided. Lower bits are ignored. The DARK_SIZE_x, LIT_SIZE_x and SIGNAL_SIZE_x bits select the number of bytes of each field to be written from 0 bytes to 4 bytes. When set to 0, no data is written for that data type. The DARK_SHIFT_x, LIT_SHIFT_x, and SIGNAL_SHIFT_x bits select the number bits to shift the output data to the right before writing the FIFO. If there are any significant bits at more significant bit positions than those selected, the data written to the FIFO is saturated.

The order of samples written to the FIFO (if selected) is signal data followed by dark data and then lit data. If both channels are enabled, all selected Channel 1 data values are written to the FIFO first, followed by the Channel 2 data.

For example, in modes that use dark data, the eight upper bits of the dark data can be stored with 24 appropriately selected bits from the signal data for each time slot. This method detects whether the ambient light is becoming large, while limiting the size of the amount of data transferred.

Figure 36 shows the PPG data format in the FIFO.

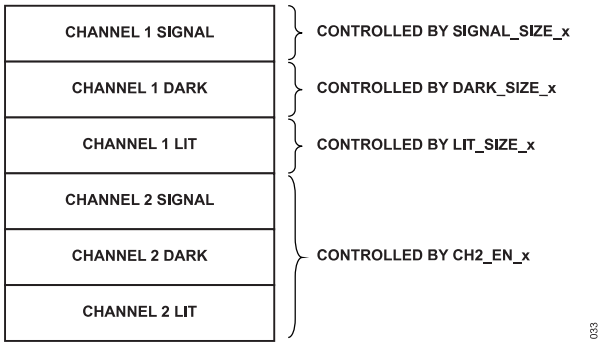

Figure 36. PPG Data Format

BIA/EDA Data Format

The BIA/EDA data format is 3-byte or 4-byte I data followed by 3-byte or 4 byte Q data. Figure 37 shows the BIA data format in the FIFO.

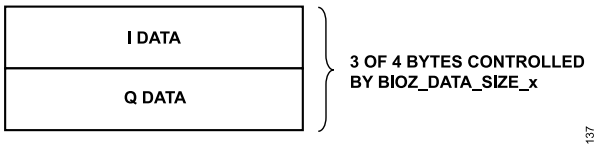

Figure 37. BIA/EDA Data Format

Data Arrangement in the FIFO

The data in the FIFO is arranged according to the enabled time slots and follow the same sequence.

For example, Figure 38 shows the data in the FIFO if one ECG time slot, three PPG time slots, and two BIA time slots are enabled.

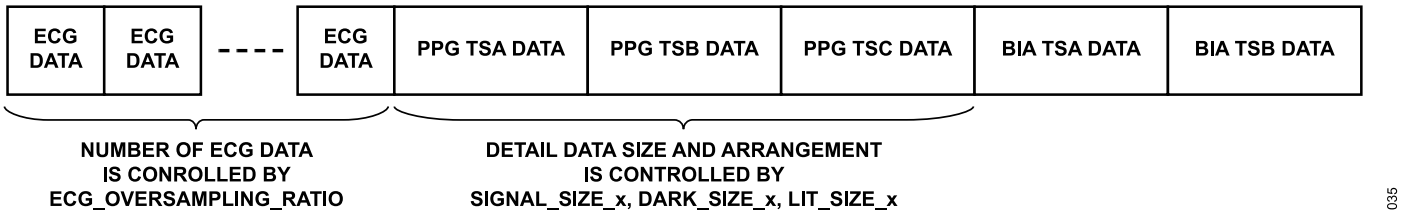

Figure 38. Example of Data Arrangement in the FIFO (TSA Is Time Slot A, TSB Is Time Slot B, and TSC Is Time Slot C)

THEORY OF OPERATION

CLOCKING

Low Frequency Oscillator

A low frequency oscillator clocks the low speed state machine, which sets the time base used to control the sample timing, wake-up states, and overall operation. There are three options for low frequency oscillator generation. The first option is an internal 960 kHz oscillator. The second option is for the host to provide a low frequency oscillator externally. Finally, the low frequency oscillator can be generated by a divide by 32 of an external high frequency clock source at 32 MHz. When powering up the device, it is expected that the low frequency oscillator be enabled and left running continuously.

To operate with the on-chip low frequency oscillator, use the following writes. Set the OSC_960K_EN bit to 1 to turn on the internal oscillator. The internal 960 kHz clock frequency is set using the 10-bit OSC_960K_FREQ_ADJ bits.

If higher timing precision is required than can be provided by the on-chip low frequency oscillator, the low frequency oscillator can be driven directly from an external source provided on a GPIOx input. To enable an external low frequency clock, use the following writes. Enable one of the GPIOx inputs using the GPIO_PIN_CFGx bits. Next, use the ALT_CLK_GPIO bits to choose the enabled GPIOx input to be used for the external low frequency oscillator. Set the ALT_CLOCKS bits to 0x1 to select an external low frequency oscillator.

In a third method, an external 32 MHz clock is used for both the high frequency clock and to be divided down to generate the low frequency clock. To use this method, follow the previous instructions for an external low frequency clock but set the ALT_CLOCKS bits to 0x3, and a divide by 32 used to generate the low frequency clock so that a 1 MHz clock is generated from the external 32 MHz clock.

For this low frequency, after power-on, the 960 kHz trim code in fuse of the ADPD7000 automatically loads, resulting in this 960 kHz clock being highly accurate. This operation is automatically handled by the chip, and the user must not take any additional steps.

High Frequency Oscillator

A 32 MHz high frequency oscillator is generated internally or can be provided externally. This high frequency clock clocks the high speed state machine, which controls the AFE operations during the time slots, such as LED timing, integration times, and BIA excitation frequency.

The high frequency oscillator can be internally generated by setting the ALT_CLOCKS bits to 0x0 or 0x1. When selected, the internal 32 MHz oscillator is enabled automatically by the low speed state machine during the appropriate wake-up time or during the 32 MHz oscillator calibration routine.

The high frequency oscillator can also be driven from an external source. To provide an external 32 MHz high frequency oscillator, enable one of the GPIO inputs using the GPIO_PIN_CFGx bits. Then, use the ALT_CLK_GPIO bits to choose the enabled GPIOx input for the external high frequency oscillator. Finally, write 0x2 or 0x3 to the ALT_CLOCKS bits to select an external high frequency oscillator. Writing 0x2 provides only the high frequency oscillator from the external source, whereas writing 0x3 generates both the low frequency oscillator and high frequency oscillator from the external 32 MHz source. When using an external 32 MHz oscillator, it must be kept running continuously for proper device operation.

TIME STAMP OPERATION

The time stamp feature is useful for calibrating the low frequency oscillator as well as providing the host with timing information during time slot operation. Timestamping is supported by the use of any GPIO as a time stamp request input, the CAPTURE_TIMESTAMP bit to enable capture of the time stamp trigger, a time counter running in the low frequency oscillator domain, and two output registers. The output bits include TIMESTAMP_COUNT_x, which holds the number of low frequency oscillator cycles between time stamp triggers, and TIMESTAMP_SLOT_DELTA, which holds the number of low frequency oscillator cycles remaining to the next time slot start.

The setup for using the time stamp operation is as follows:

1. Set OSC_CAL_ENABLE = 1 to enable the oscillator calibration circuitry.
2. Configure a GPIO to support the time stamp input using the appropriate GPIO_PIN_CFG_x bits. Select the matching GPIOx to provide the time stamp using the TIMESTAMP_ GPIO bits.
3. Configure the ADPD7000 for operation and enable the low frequency oscillator.
4. If the TIMESTAMP_SLOT_DELTA function is desired, start the time slot operation by placing the device in go mode using the OP_MODE bit (see Table 12). For low frequency oscillator calibration, it is only required that the low frequency oscillator is enabled. The device does not have to be in go mode for low frequency oscillator calibration.

Use the following procedure to capture the time stamp:

1. Set the CAPTURE_TIMESTAMP bit to 1 to enable the capture of the time stamp on the next rising edge of the selected GPIOx input.
2. The host provides the initial time stamp trigger on the selected GPIOx at an appropriate time.
3. The CAPTURE_TIMESTAMP bit is cleared when the timestamp signal is captured unless the TIMESTAMP_ ALWAYS_EN bit is set, in which case, the capture of the time stamp is always enabled. Reenable the capture if necessary.
4. The host provides a subsequent time stamp trigger on the selected GPIO at an appropriate time.

THEORY OF OPERATION

5. The number of low frequency oscillator cycles that occurred between time stamp triggers can be read from the TIMESTAMP_COUNT_x bits.

The host must continue to handle the FIFO data normally during time stamp processing.

If using a dedicated pin for a time stamp that does not have transitions other than the time stamp, set the TIMESTAMP_ ALWAYS_EN bit to avoid automatic clearing of the CAPTURE_ TIMESTAMP bit. This setting removes the need to enable the time stamp capture each time.

The host can also use TIMESTAMP_SLOT_DELTA to determine when the next time slot occurs. TIMESTAMP_SLOT_DELTA can determine the arrival time of the samples currently in the FIFO.

The time stamp trigger is edge sensitive and can be set to either trigger on the rising edge (default) or falling edge using TIMESTAMP_INV.

Low Frequency Oscillator Calibration

The time stamp circuitry can calibrate the 960 kHz low frequency oscillator circuit by adjusting the frequency to match the timing of the time stamp triggers. Simply compare the TIMESTAMP_COUNT_x value in low frequency oscillator cycles to the actual time stamp trigger period and adjust the OSC_960K_FREQ_ADJ value accordingly.

High Frequency Oscillator Calibration

The high frequency oscillator is calibrated by comparing multiples of its cycles with multiple cycles of the low frequency oscillator, which is calibrated to the system time. Calibration of the low frequency oscillator precedes calibration of the high frequency oscillator. The method for calibrating the high frequency oscillator is as follows:

1. Set OSC_CAL_ENABLE = 1 to enable the oscillator calibration circuitry.
2. Write 1 to the OSC_32M_CAL_START bit.
3. The ADPD7000 automatically powers up the high frequency oscillator.
4. The device automatically waits for the high frequency oscillator to be stable.
5. An internal counter automatically counts the number of 32 MHz high frequency oscillations that occur during 128 cycles of the 960 kHz low frequency oscillator.
6. The OSC_32M_CAL_COUNT bits update with the final count.
7. The 32 MHz oscillator automatically powers down following calibration unless time slots are active.
8. The device resets the OSC_32M_CAL_START bit indicating the count has updated.

The OSC_32M_FREQ_ADJ bits adjust the frequency of the 32 MHz oscillator to the desired frequency. When using an external low frequency oscillator, the 32 MHz oscillator calibration is performed with respect to the externally provided low frequency oscillator.

When the calibrations of the low frequency and high frequency oscillators are complete, set CLK_CAL_ENA = 0 to disable the clocking of the oscillator calibration circuitry to reduce the power consumption. CLK_CAL_ENA defaults to 0 so that the calibration circuitry is disabled by default.

EXECUTION MODES

A state machine in the low frequency oscillator clock domain controls sleep times, wake-up cycles, and the start of time slot operations. The low frequency oscillator serves as the time base for all time slot operations, controls the sample rates, and clocks the low frequency state machine. This state machine controls all operations and is controlled by the OP_MODE bit.

Table 12. OP_MODE Bit Setting Descriptions

OP_MODE Setting	Mode	Description
000	Standby	All operations stopped. Time slot actions reset. Low power standby state.
001	Go	Transitioning to this state from standby mode starts time slot operations.
011	ADC test mode	This mode goes through the normal wake-up sequence and then does continuous ADC cycles based on the PPG Time Slot A setting
101	Repeat selected time slots without sleep	This mode does one normal wake-up sequence and then cycles through the enabled time slot sequences without going to sleep between.
111	DAC test mode	This mode goes through the normal wake-up sequence and then does continuous DAC cycles based on the BIOZ Time Slot A settings. BIOZ Time Slot A must be enabled before starting DAC test mode.

At power-up and following any subsequent reset operations, the ADPD7000 is in standby mode. The user can write 0 to the OP_MODE bit to immediately stop operations and return to standby mode.

The time slots are enabled by the ECG_TIMESLOT_EN, PPG_TIMESLOT_EN, and BIOZ_TIMESLOT_EN bits in the OPMODE register (see Register 0x010 in Table 23).

Set ECG_TIMESLOT_EN to 1 enable the ECG time slot. Set the BIOZ_TIMESLOT_MODE bit to 1 and BIOZ_TIMESLOT_EN to a certain value to enable the corresponding EDA time slots. Set BIOZ_TIMESLOT_MODE to 0 and BIOZ_TIMESLOT_EN to a certain value to enable the corresponding BIA time slots. Set PPG_TIMESLOT_EN to a certain value to enable the corresponding PPG time slot.

After enabling the desired time slots, set the OP_MODE bit to 1 to start the chip operation.

THEORY OF OPERATION

Register writes that affect operating modes cannot occur during go mode. The user must enter standby mode before changing the control registers. Standby mode resets the digital portion of the ADC, all of the pulse generators, and the state machine.

When OP_MODE is set to 1, the device immediately starts the first wake-up sequence and time slot operations unless using an external synchronization trigger. If using an external synchronization trigger, the device enters the sleep state before the first wake-up and time slot regions begin.

HOST INTERFACE

The ADPD7000 uses an SPI to communicate with other devices. The device also provides numerous FIFO, error, and threshold status bits, each of which can be provided by an interrupt function from a GPIO, read from status registers, or appended as optional status bytes at the end of a FIFO packet.

Interrupt Status Bits

FIFO Threshold Interrupt

The FIFO threshold interrupt status bit, INT_FIFO_TH, is set when the number of bytes in the FIFO exceeds the value stored in the FIFO_TH register. The INT_FIFO_TH bit is cleared automatically when a FIFO read reduces the number of bytes below the value in the FIFO_TH register, which allows the user to set an appropriate data size for their host needs.

The INT_FIFO_TH bit does not trigger if the FIFO byte count exceeds the threshold in the middle of any write of complete data. Instead, the INT_FIFO_TH bit is set at the next write to the FIFO. For example, if only PPG TSA is running, it only writes 4-byte lit data to the FIFO. Figure 39 shows the data in the FIFO.

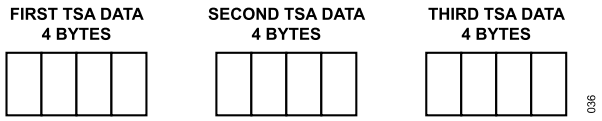

Figure 39. FIFO Threshold Interrupt Example

If the threshold is set as 4, the interrupt triggers at the beginning of the second TSA data write to the FIFO. If the threshold is set as 5, 6, or 7, the INT_FIFO_TH bit does not trigger until the write of the third TSA data. This method can help prevent any partial data read from the FIFO.

Clearing Interrupt Status Bits

All status bits are set regardless of whether the status bit is routed to one of the interrupt outputs, Interrupt X or Interrupt Y. The status bits are independent of the interrupt enable bits. The status bits are always set by the corresponding event. The interrupt bits stay set until they are either manually or automatically cleared.

The user can manually clear a given interrupt by writing a 1 to the matching interrupt status bit. In addition, the data interrupt status bits can be configured to clear automatically. When the INT_ACLEAR_FIFO bit is set, the appropriate interrupt status bit is automatically cleared when any matching FIFO register is read. Automatic clearing of the interrupt status bits removes the need to manually clear these interrupts.

Optional Status Bytes

There is an option to append each data packet with status bits. This option is useful for hosts that cannot spare an interrupt channel to service. The status bytes can each be individually selected in the FIFO_STATUS_BYTES register. Each bit in the FIFO_ STATUS_BYTES register enables a status byte that is appended to the data packet in the FIFO. If any bit in the FIFO_STATUS_ BYTES register is set to 1, the byte that is appended to the data packet contains the status bits.

The 4-bit sequence number cycles from 0 to 15 and is incremented with a wraparound every time the time slot sequence completes. This sequence number can also be made available bitwise on the GPIOx pins.

Interrupt Outputs, Interrupt X and Interrupt Y

The ADPD7000 supports two separate interrupt outputs, Interrupt X and Interrupt Y. Each interrupt has the option to be driven to any of the two GPIOx pins. The two different interrupt outputs can be generated for a host processor if desired. For example, the FIFO threshold interrupt, INT_FIFO_TH, can be routed to Interrupt X and used to drive the direct memory access (DMA) channel of the host, while the INT_FIFO_OFLOW and INT_FIFO_UFLOW interrupts can be routed to Interrupt Y and used to drive an additional host interrupt pin.

For each interrupt, there is an associated Interrupt X and Interrupt Y enable bit. See Table 24 for a full list of available interrupts that can be brought out on Interrupt X and Interrupt Y. The logic for the Interrupt X and Interrupt Y function is a logic AND of the status bit with its matching enable bit. All enabled status bits are then logically OR'ed to create the interrupt function. The enable bits do not affect the status bits.

General-Purpose I/Os

The ADPD7000 provides two general-purpose I/O pins: GPIO0 and GPIO1. These GPIOs can be used as previously described in the Interrupt Outputs, Interrupt X and Interrupt Y section for interrupt outputs or for providing external clock signals to the device. The GPIOs can also be used for many different control signals, as synchronization controls to external devices, as well as test signals that are useful during system debugging. All of the available signals that can be brought out on a GPIOx pin are listed in Table 24.

IOVDD Supply Voltage Consideration

The ADPD7000 can operate with IOVDD as low as 1.7 V and as high as 3.6 V. LOW_IOVDD_EN in Register 0x0057 is set to 0x1 for

THEORY OF OPERATION

IOVDD lower than 3 V. 0x1 is the default value for this bit because the typical IOVDD value is 1.8 V.

If 3 V or higher is supplied for IOVDD, the LOW_IOVDD_EN bit must be set to 0x0 for proper operation.

SPI

The ADPD7000 contains an SPI port that operates synchronously with its input clocks.

The ADPD7000 has an internal power-on reset circuit that sets the device into a known idle state during the initial power-up. After the power-on reset is released, approximately 2 µs to 6 µs after the DVDD supply is active, there is an initialization state that sets the register default values. This initialization state lasts approximately 15 µs to 20 µs. The device can then be read and written through the SPI.

The registers are accessed using addresses within a 15-bit address space. Each address references a 15-bit register with one address reserved for the FIFO read accesses. For SPIs, reads and writes auto-increment to the next register if additional words are accessed as part of the same access sequence. This automatic address increment occurs for all addresses except the FIFO address, one less than the FIFO address and the last used address, which is 0x351. Reads from the FIFO address continue to access the next byte from the FIFO.

SPI Operations

The SPI single register write operation is shown in Figure 40. The first two bytes contain the 15-bit register address and specify that a write is requested. The remaining two bytes are the 16 data bits to write to the register. The register write occurs only when all 16 bits are shifted in prior to deassertion of the $\overline{CS}$ signal.

In addition, multiple registers can be written if additional 16-bit data is shifted in before deassertion of the $\overline{CS}$ signal. The register address automatically increments to the next register after each 16 bits of data.

The SPI single register read operation is shown in Figure 41. The first two bytes contain the 15-bit register address and specify that a read is requested. Register bits are shifted out starting with the MSB. In addition, multiple registers can be read if additional 16-bit data is shifted out prior to deassertion of the $\overline{CS}$ signal.

It is recommended that reading from the FIFO is performed byte wise. There is no requirement to read multiples of 16 bits.

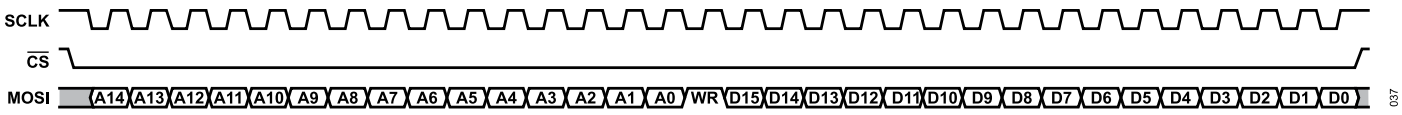

Figure 40. SPI Write Operation

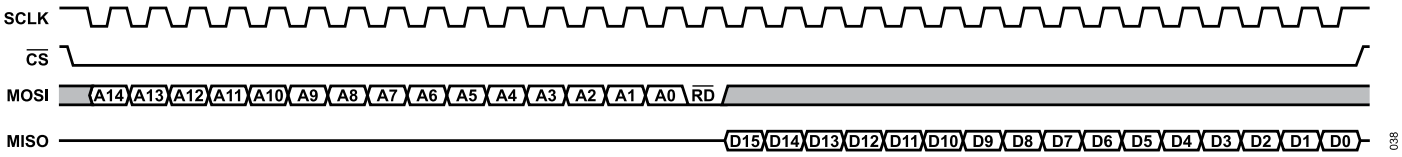

Figure 41. SPI Read Operation

APPLICATIONS INFORMATION

LEAD-ON APPLICATION

The ADPD7000 lead-on detection mode can be enabled in standby or PPG only operation mode. When the lead-on detection mode triggers, the lead-on status signals can be routed out from any GPIOs, which can be used as an interrupt signal to inform host.

In real-world application, for example, a smart watch detects the lead-on status from two electrodes attached to the wrist, that is, ECGIP and RLD or ECGIN and RLD. For ECGIN and RLD, for example, when the electrodes contact the human body, there is a path between ECGIN and RLD that makes the input of the lead-on comparator lower than the threshold, resulting in the lead-on status being set.

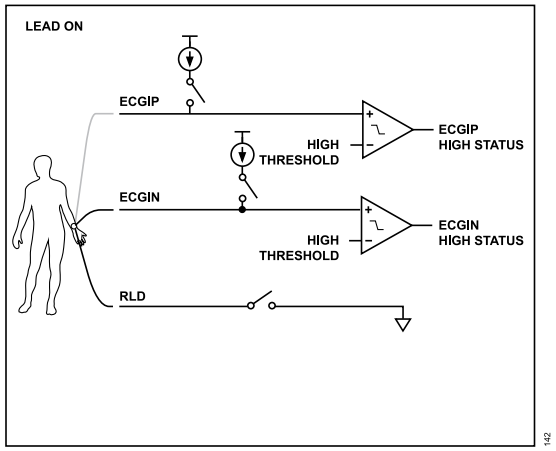

Figure 42. Lead-On Detection Application Block

Table 13. Registers for Lead-On Mode

Register, Bit Number	Name	Description
0x00F, Bit 11	LEAD_ON_MODE	Set to 1 to enable lead-on detection mode.
0x005, Bit 11	ECG_RLD_LEADON_HI_STATUS	ECG RLD lead-on high status bit. Write 1 to this bit to clear this status.
0x005, Bit 10	ECG_RLD_LEADON_LO_STATUS	ECG RLD lead-on low status bit. Write 1 to this bit to clear this status.
0x005, Bit 9	ECGIN_LEADON_HI_STATUS	ECGIN lead-on high status bit. Write 1 to this bit to clear this status.
0x005, Bit 8	ECGIP_LEADON_HI_STATUS	ECGIP lead-on high status bit. Write 1 to this bit to clear this status.

OPTICAL PATH

Digital Integration Mode

The ADPD7000 supports a digital integration mode in the optical path to accommodate sensors that require longer pulses. Digital integration mode allows the system to use a larger LED duty cycle, which can result in the highest achievable SNR levels.

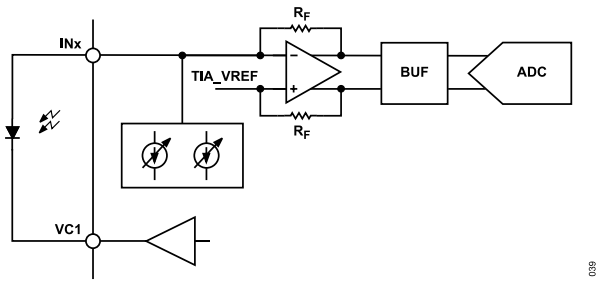

Figure 43. Signal Path for Digital Integration Mode

In digital integration mode, the integrator is configured as a buffer, resulting in the signal path shown in Figure 43. Digital integration regions are configured by the user and separated into lit and dark regions. The LED is pulsed in the lit region, and the LED is off in the dark region. ADC samples are taken at 1 µs intervals within the lit and dark regions and are then digitally integrated. The integration of the ADC samples from the dark region is subtracted from the integration of the ADC samples from the lit region, and the result is written into the relevant FIFO. Both signal and dark values can be written to the FIFO.

The ADPD7000 supports one-region and two-region digital integration modes. In one-region digital integration mode, an equal number of dark and lit samples are taken where all of the dark samples are taken in the dark region just before the lit region. One-region digital integration mode is shown in the timing diagram in Figure 44.

In two-region digital integration mode, an equal number of dark and lit samples are taken. However, the dark region is split such that half of the samples are taken in the dark region before the lit region, and the other half is taken in the dark region following the lit region. The two-region digital integration mode results in higher ambient light rejection than the one-region digital integration mode in situations with a varying ambient light level. A timing diagram for two-region digital integration mode is shown in Figure 45.

The signal data for one-region digital integration mode that reads from the FIFO follows:

$$Signal = (I_{PD} \times R_{TIA} \times TIA\_CONFIG \times BUF\_GAIN \times NUM\_INT\_x \times NUM\_REPEAT\_x)/(146\ \mu V/LSB) \quad (5)$$

where:
I_{PD} is the PD current.
TIA_CONFIG is the TIA configuration. BUF_*GAIN* is the buffer gain.

The signal data for two-region digital integration mode that reads from the FIFO follows:

$$Signal = ((I_{PD} \times R_{TIA} \times TIA\_CONFIG \times BUF\_GAIN \times NUM\_INT\_x \times NUM\_REPEAT\_x)/(146\ \mu V/LSB)) \times 2 \quad (6)$$

APPLICATIONS INFORMATION

The AFE_PATH_CFG_x, TIA_GAIN_CHx_x, AFE_BUFFER_GAIN_x, and AFE_BUFFER_CAP_x bits must follow a certain combination in digital integration mode (both one-region mode and two-region mode). Table 14 shows the recommended settings of these bits. The TIA gain setting is independent of these settings.

Table 14. Bit Settings for AFE Path in Digital Integration Mode

Bit Name	Recommended Setting
AFE_PATH_CFG_x	0x28
TIA_GAIN_CHx_x	0x3
AFE_BUFFER_GAIN_x	0x3
AFE_BUFFER_CAP_x	0x1

The result of the configurations of the bits in Table 14 is the 1× TIA configuration with a buffer gain = 2.

Table 15 shows the relevant register settings for the digital integration modes of operation. The MIN_PERIOD_x bits must be set manually with the proper period because the minimum period is not automatically calculated in digital integration mode.

The recommended MIN_PERIOD_x setting for one-region digital integration mode is as follows:

$$MIN\_PERIOD\_x = NUM\_INT\_x \times 2 + (2 + t_D) \times 2$$

The recommended MIN_PERIOD_x setting for two-region digital integration mode is as follows:

$$MIN\_PERIOD\_x = NUM\_INT\_x \times 4 + t_D \times 2 + 6\ \mu s$$

The t_D value is the response time of the optical device. The 6 µs time is essential for the ambient fine loop update.

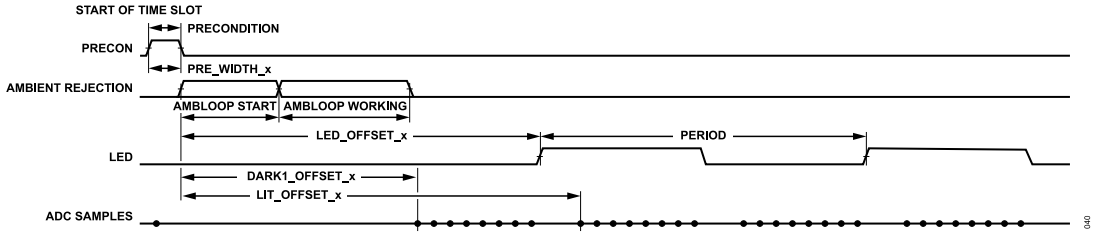

Figure 44. One-Region Digital Integration Mode Timing Diagram

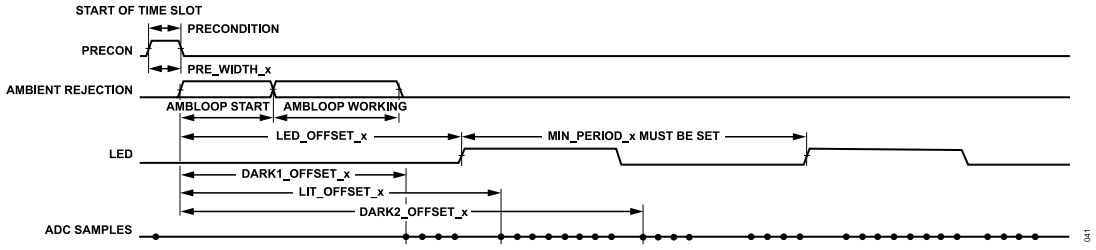

Figure 45. Two-Region Digital Integration Mode Timing Diagram

Table 15. Relevant Settings for Digital Integration Modes, for Example, for Time Slot A

Group	Time Slot A Register Address	Bit Field Name	Description
Signal Path Setup	0x0120, Bits[13:11]	SAMPLE_TYPE_A	Set to 0x2 for one-region digital integration mode. Set to 0x3 for two-region digital integration mode.
	0x0121, Bits[6:0]	AFE_PATH_CFG_A	Set to 0x28 for TIA, buffer, and ADC. Use 1x TIA configuration.
	0x0122, Bits[7:0]	INPxx_A	Enable desired inputs.
	0x0123, Bits[14:12]	PRECON_A	Set to 0x5 to precondition anode of photodiode to TIA_VREF.
	0x0123, Bits[1:0]	VC1_SELECT_A	Set to 0x2 to set ~215 mV reverse bias across photodiode.
	0x0124, Bits[5:0]	TIA_GAIN_CHx_A	Select TIA gain.
	0x0124, Bits[9:8]	AFE_TRIM_VREF_A	Set to 0x2 to set TIA_VREF = 0.8855 V.
	0x0124, Bits[12:11]	AFE_BUFFER_GAIN_A	Buffer gain selection. Set to 2 to select buffer gain = 2.
	0x125, Bits[13:12]	AFE_BUFFER_CAP_A	Buffer feedback capacitor selection. Set to 0x1 to 12.6 pF.
Timing	0x012A, Bits[15:8]	NUM_INT_A	Set to the number of desired ADC conversions in the dark and lit regions.
	0x012A, Bits[7:0]	NUM_REPEAT_A	Number of sequence repeats.
	0x012B, Bits[9:0]	MIN_PERIOD_A	Set the period. Automatic period calculation is not supported in digital integration mode.
	0x0138, Bits[8:0]	LIT_OFFSET_A	Set to the time of the first ADC conversion in the lit region.

APPLICATIONS INFORMATION

Table 15. Relevant Settings for Digital Integration Modes, for Example, for Time Slot A (Continued)

Group	Time Slot A Register Address	Bit Field Name	Description
	0x0139, Bits[6:0]	DARK1_OFFSET_A	Set to the time of the first ADC conversion in the Dark 1 region.
	0x0139, Bits[15:7]	DARK2_OFFSET_A	Set to the time of the first ADC conversion in the Dark 2 region. Only used in two-region digital integration mode.
LED Settings	0x0129, Bits[1:0]	LED_MODEx_A	Select LED mode.
	0x0129, Bits[7:4]	LED_DRIVESIDEx_A	Select LED for time slot used.
	0x0128, Bits[14:8], Bits[6:0]	LED_CURRENTx_A	Set LED current for selected LED.
	0x012C, Bits[7:0]	LED_OFFSET_A	Sets start time of first LED pulse in 1 µs increments.
	0x012C, Bits[15:8]	LED_WIDTH_A	Sets width of LED pulse in 1 µs increments.

Timing Recommendations for Digital Integration Mode

When setting the timing for digital integration mode, it is important to place the ADC samples such that the signal being sampled is given time to settle before the sample being taken. Photodiode capacitance and the TIA settling time affect the settling time of the input signal.

If automatic ambient light rejection is on (AMBIENT_CANCELLATION_x is set to either 1 (01) or 2 (10) decimal), time is needed at the beginning of each time slot to enable the ambient rejection loop. The start-up time of this loop is 18 µs, and the working time of this loop is 30 µs.

The TIA_SAT_DET internal block must be turned on to speed up the TIA settling. Speeding up the TIA settling can help the TIA enter a normal working state quickly to make the automatic ambient rejection loop more accurate.

After the ambient loop completes, the first ADC sample of dark data can be enabled. The DARK1_OFFSET_x setting must be equal or larger than the ambient loop working time (48 µs).

Figure 46 shows an example of the proper placement of the ADC sampling edges.

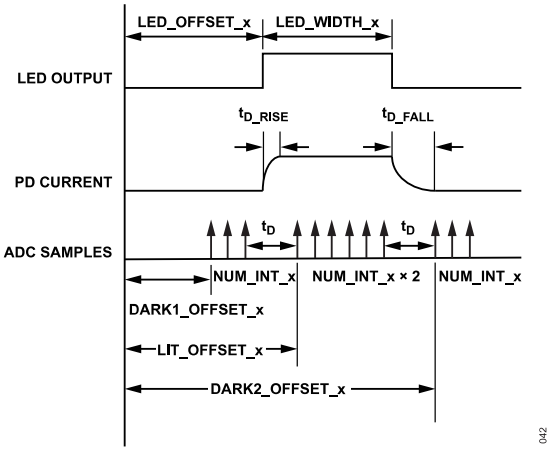

Figure 46. Proper Placement of ADC Sampling Edges in Digital Integration Mode

The recommended DARK1_OFFSET_x setting after the automatic ambient loop completes is 48 µs, or 10 µs if automatic ambient rejection is not turned on.

As shown in Figure 46, different optical devices, including the LED and photodiode, have different response times. t_{D_RISE} is the rising time of the photodiode current, and t_{D_FALL} is the falling time of the photodiode current. t_D is either t_{D_RISE} or t_{D_FALL}, depending on which one is bigger.

See the following equations to calculate the timing:

$$LED\_OFFSET\_x = DARK1\_OFFSET\_x + (NUM\_INT\_x + t_D - t_{D\_RISE}) \quad (7)$$

$$LIT\_OFFSET\_x = LED\_OFFSET\_x + t_{D\_RISE} \quad (8)$$

$$DARK2\_OFFSET\_x = LED\_OFFSET\_x + LED\_WIDTH\_x + t_D \quad (9)$$

These values must be characterized in the final application. These settings only apply to two-region digital integration mode.

Table 16. Empirical Values for Two-Region Digital Integration Mode

Optical Device	Green (µs)	Red (µs)	Infrared (µs)
LED_WIDTH_x	24	24	36
PERIOD_x	58	60	138
NUM_INT_x	10	9	13
LED_OFFSET_x	60	59	91
LIT_OFFSET_x	64	65	101
DARK1_OFFSET_x	48	48	48
DARK2_OFFSET_x	90	91	167
t_{D_RISE}	4	6	10
t_{D_FALL}	6	8	40

Optimizing Sampling Sequence

If the empirical value is not appropriate for the measurement, optimize the sampling sequence.

See the following reference method for sweeping the curve (this example is based on TSA Channel 1 in a dark environment):

1. Enable the following settings:
   - One-region digital integration mode
   - 1× TIA configuration

APPLICATIONS INFORMATION

- AFE_TRIM_VREF_A = 3
- AMBIENT_CANCELLATION_A = 0
- NUM_INT_A = 1
- NUM_REPEAT_A = 1
- DARK1_OFFSET_A = 10
- LED_OFFSET_A = 20
- LED_WIDTH_A = 80
- LIT_OFFSET_A = 130
- MIN_PERIOD_A = 160

2. Power on the optical devices and enable TSA Channel 1.
3. Collect about 100 lit data values (remove the first 10 data values) and calculate the mean value.
4. Sweep the LIT_OFFSET_A bit from 130 to 10 and reproduce the result from Step 3.
5. Plot the mean value of the lit data and LIT_OFFSET_A. The response time of the optical device (for example, OSRAM FIREFLY® CT DBLP31.12) is shown in Figure 47.

When collecting the lit data with the LIT_OFFSET_A bit changing, the data is lower than 16384 (unsaturated).

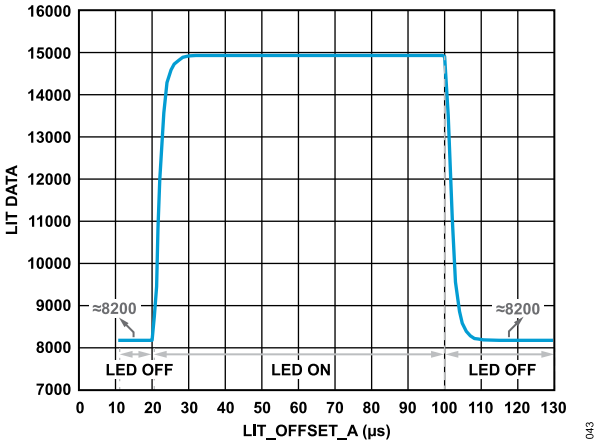

Figure 47. Timing of OSRAM FIREFLY CT DBLP31.12 (Green LED)

ECG PATH

The ADPD7000 has four ECG electrode pads (ECG1, ECG2, ECG3, and ECG4) and ECG signals can be routed to most of the four pads via register configuration (see Table 17). This architecture is quite flexible and suited for a variety of customer applications, which eases design and results in time savings.

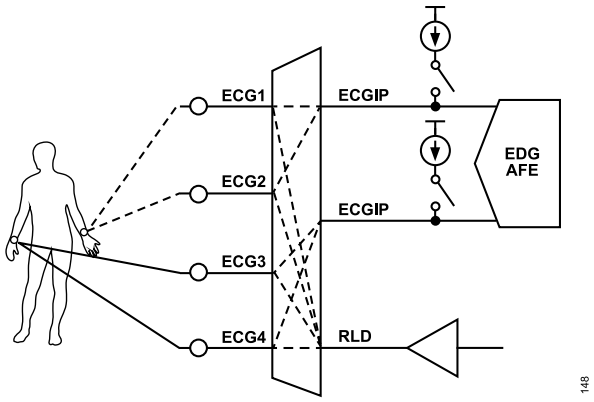

Figure 48. ECG Path Matrix

Figure 49 shows a typical connection diagram for the three-electrode ECG application. Figure 49 captures the external components required around the ADPD7000, including current limitation resistors for the ECG channel. These component values were designed by users considering the maximum current of every channel. For example, using 51 kΩ, 51 kΩ, and 330 kΩ on the ECGIP, ECGIN, and RLD channels, respectively, for reference is suggested.

The signal data for ECG measurement that is read from the FIFO follows:

$$Signal = \frac{V_{IN}(V)}{Resolution} + 8,388,608\ (LSB) \quad (10)$$

Note that 8,388,608 is the center code of the ADC.

Table 17 shows the relevant register settings for the basic ECG measurement.

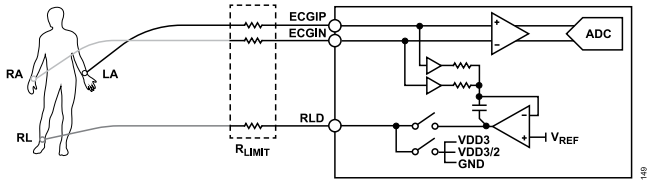

Figure 49. System Overview of ECG Circuit Showing ECG Channel Protection and External Components Requirements

Table 17. Relevant Settings for Basic ECG Measurement

Group	Register Address	Bit Field Name	Description
ECG_ANA_CTRL	0x0100, Bit 12	ECG_SHORT_IN_RLD	Set to 1 to short ECGIN to RLD internally.
	0x0100, Bit 11	ECG_SHORT_IP_RLD	Set to 1 to short ECGIP to RLD internally.
	0x0100, Bit 9	ECG_CGA_PREBUF_ALWAYSON	Set to 1 to keep CGA prebuffers always on.
	0x0100, Bit 8	ECG_CGA_GAIN	Set to 0 to select a gain = 32 and set to 1 to select a gain = 16.
	0x0100, Bit 7	ECG_RLD_VCM_EN	Set to 1 to enable the V_{CM} (AVDD3/2) generator in the RLD circuit.

APPLICATIONS INFORMATION

Table 17. Relevant Settings for Basic ECG Measurement (Continued)

Group	Register Address	Bit Field Name	Description
	0x0100, Bit 6	ECG_RLD_OUT_DISCONNECTED	Set to 1 to disconnect the RLD output.
	0x0100, Bits[5:4]	ECG_RLD_OUT_SEL	Select the RLD output.
	0x0100, Bit 3	ECG_RLD_SAT_EN	Set to 1 to enable the DCLO for the RLD.
	0x0100, Bits[2:1]	ECG_RLD_SAT_THRESHOLD	DCLO threshold selection for the RLD.
	0x0100, Bit 0	ECG_RLD_EN	Set to 1 to enable the RLD amplifier.
ECG_LEADOFF_CTRL	0x0101, Bit 15	ECG_ACLO_EN	Set to 1 to enable the ACLO detector for the ECG inputs.
	0x0101, Bits[14:12]	ECG_ACLO_MAG	Select the ACLO excite current magnitude.
	0x0101, Bits[11:9]	ECG_ACLO_THRESHOLD	Select ACLO threshold for the ECG inputs.
	0x0101, Bit 8	ECG_DCLO_L_EN	Set to 1 to enable the low range DCLO detector for the ECG inputs.
	0x0101, Bits[7:4]	ECG_DCLO_MAG	Select the DCLO excite current magnitude.
	0x0101, Bit 3	ECG_DCLO_POLARITY_IN	Select DCLO output current polarity at ECGIN.
	0x0101, Bit 2	ECG_DCLO_POLARITY_IP	Select DCLO output current polarity at ECGIP.
	0x0101, Bits[1:0]	ECG_DCLO_THRESHOLD	Select DCLO threshold for the ECG inputs.
ECG_DIG_CTRL_1	0x0102, Bits[8:3]	ECG_OVERSAMPLE_RATIO	For ECG only mode, keep the default value. For multimodal, refer to the register description.
	0x0102, Bits[2:0]	ECG_ODR_SEL	Select the ECG ODR.
ECG_DIG_CTRL_2	0x103, Bit 15	ECG_DCLO_H_EN	Enables high-range DCLO current.
	0x0103, Bits[14:11]	ECG_DCLO_H_MAG	High-range DCLO excite current magnitude.
	0x0103, Bit 10	ECG_DCLO_IP_EN	Enables the DCLO current output at ECGIP.
	0x0103, Bit 9	ECG_DCLO_IN_EN	Enables the DCLO current output at ECGIN.
	0x0103, Bit 8	ECG_DCLO_DET_IN_EN	Enables the DCLO detection comparator at ECGIN.
	0x0103, Bit 7	ECG_DCLO_DET_IP_EN	Enables the DCLO detection comparator at ECGIP.
	0x0103, Bit 6	ECG_DCLO_M_EN	Enables the DC mode of the ACLO current circuit.
	0x0103, Bits[3:0]	ECG_CAL_GAIN	Calibrated gain ECG.
ECG_MATRIX	0x104, Bit 9	ECG_SWAP_POLARITY	Set to 1 to swap the ECG signal path polarity.
	0x104, Bit 8	ECG_PINS_CON_BIOZ	Set to 1 to connect the selected ECGx pins to the BIOZ path
	0x104, Bit 7	ECG_E1_CON_ECGIP	Set to 1 to connect ECG1 pin to ECGIP.
	0x104, Bit 6	ECG_E1_CON_RLD	Set to 1 to connect ECG1 pin to RLD.
	0x104, Bit 5	ECG_E2_CON_ECGIP	Set to 1 to connect ECG2 pin to ECGIP.
	0x104, Bit 4	ECG_E2_CON_RLD	Set to 1 to connect ECG2 pin to RLD.
	0x104, Bit 3	ECG_E3_CON_ECGIN	Set to 1 to connect ECG3 pin to ECGIN.
	0x104, Bit 2	ECG_E3_CON_RLD	Set to 1 to connect ECG3 pin to RLD.
	0x104, Bit 1	ECG_E4_CON_ECGIN	Set to 1 to connect ECG4 pin to ECGIN.
	0x104, Bit 0	ECG_E4_CON_RLD	Set to 1 to connect ECG4 pin to RLD.

APPLICATIONS INFORMATION

Lead Off

DCLO detection uses the ECG_STATUS register to identify the lead connection status. Figure 50 shows an example of DCLO detection. In the case, R1, R2, and R3 are the contact impedances at ECGIP, ECGIN, and RLD, respectively.

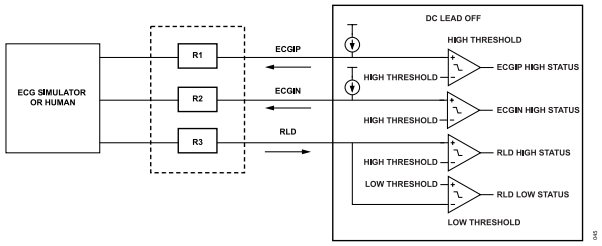

Figure 50. DCLO Detection Example

When using source current at ECGIP and ECGIN, the dc excitation current setting (ECG_DCLO_MAG) follows Equation 11:

If R1 = R2 = R3 = 3R,

$$(DCLO\ \ Current\ \ Magnitude > High\ \ Threshold\ \ Voltage)/3R \quad (11)$$

Generally, the DCLO current magnitude setting is rounded up to nearest register value.

Table 18 is the ECG DCLO status truth table.

ACLO threshold selection depends on the particular cable, electrode, or protection scheme because these parameters are typically unique for the specific use case. Identifying the appropriate threshold can start with a high threshold and ratchet it down until a lead off is detected, then increase the threshold by some safety margin.

Table 19 shows the low threshold of electrode difference capacitance for ACLO detection.

Table 18. ECG DCLO Status Truth Table

Status	ECGIN_DCLO_HI_STATUS	ECGIP_DCLO_HI_STATUS	ECG_DCLO_STATUS
All Leads Failed	1	1	1
No Lead Failed	0	0	0
RLD Failed	1	1	1
ECGIN Right Arm (RA) Failed	0	1	1
ECGIP Left Arm (LA) Failed	1	0	1

Table 19. Low Threshold of Electrode Difference Capacitance for ACLO Detection

	ECG_ACLO_MAG						
ECG_ACLO_THRESHOLD	0x1	0x2	0x3	0x4	0x5	0x6	0x7
0x0	0.04 nF	0.08 nF	0.13 nF	0.17 nF	0.21 nF	0.25 nF	0.29 nF
0x1	0.05 nF	0.1 nF	0.14 nF	0.19 nF	0.24 nF	0.29 nF	0.33 nF
0x2	0.06 nF	0.11 nF	0.17 nF	0.22 nF	0.28 nF	0.33 nF	0.39 nF
0x3	0.07 nF	0.13 nF	0.2 nF	0.27 nF	0.33 nF	0.4 nF	0.47 nF
0x4	0.08 nF	0.17 nF	0.25 nF	0.33 nF	0.42 nF	0.5 nF	0.58 nF
0x5	0.11 nF	0.22 nF	0.33 nF	0.44 nF	0.56 nF	0.67 nF	0.78 nF
0x6	0.17 nF	0.33 nF	0.5 nF	0.67 nF	0.83 nF	1 nF	1.17 nF
0x7	0.33 nF	0.67 nF	1 nF	1.33 nF	1.67 nF	2 nF	2.33 nF

APPLICATIONS INFORMATION

BIA PATH

The BIA path in the ADPD7000 can be used to perform 4-wire impedance measurement on the body. This approach uses a high precision, AC voltage source to excite a sensor with a known AC voltage (V_{AC}). To calculate the impedance, measure the current (I) that flows from the unknown impedance (Z_{UNKOWN}) and the voltage across the unknown impedance ($V_{Z_{UNKNOWN}}$). Use the following equation to calculate the impedance:

$$|Z_{UNKNOWN}| = \frac{V_{Z_{UNKNOWN}}}{I} \quad (12)$$

In real-world applications, medical devices must conform to the IEC 60601 standard, which limits the amount of DC and AC voltage that can be applied to the human body.

In Figure 51, there are discrete isolation capacitors (C_{ISO1}, C_{ISO2}, C_{ISO3}, and C_{ISO4}) that ensure no DC voltage occurs across the body. R_{LIMIT} limits the current provided to the sensor to conform to the IEC 60601 standard.

$R_{CONTACTx}$ represents the resistances of the electrodes connecting to the unknown impedance.

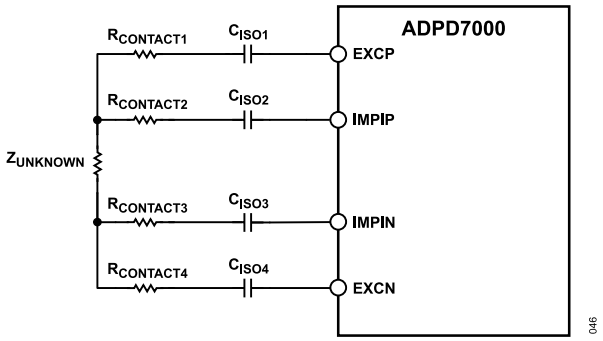

Figure 51. BIA Path Diagram

As shown in Figure 51, a 4-wire bioimpedance solution requires a precision AC voltage source, a high precision current meter, and a precision differential voltage meter.

The ADPD7000 uses a high speed DAC and waveform generator to generate the precision AC voltage. The device uses a high speed, high precision TIA for converting current from the sensor into a voltage measured by the ADC. The TIA channel measures the response current.

The ADC converts the current measurement with a 1 MSPS speed. A DFT is performed on the data. The DFT is implemented on the ADPD7000. The number of DFT points is configurable up to 8192. The ADPD7000 calculates the real and imaginary parts, and the host microcontroller calculates the unknown impedance of the sensor.

There are a number of discrete components needed in the system to guarantee safety and accuracy.

To conform to IEC 60601 standards, limit the amount of AC current entering the human body. The maximum allowable AC current is 500 µA at 50 kHz and 600 µA at 60 kHz. When calculating the R_{LIMIT} resistor value, the maximum output voltage from the ADPD7000 is 0.8 V p-p (0.2828 V RMS). Set the maximum allowable AC current to 80% of maximum, or 400 µA RMS. The following equation is the result of these values:

$$R_{LIMIT} = \frac{0.2828\ \text{V RMS}}{400\ \mu\text{A}} = 707\ \Omega \quad (13)$$

As such, a ~1 kΩ R_{LIMIT} is selected and connected to the EXCP pin on the ADPD7000. This calculation ignores C_{ISOx} because of its small size.

However, to reduce cost and complexity for customers, the ADPD7000 integrates R_{LIMIT} internally, and its value is configurable by the BIOZ_CURRENT_LIMIT_x bits. Three values are available for customer use: 0 Ω, 650 Ω, and 1.3 kΩ.

To conform to IEC 60601 standards, a 10 µA maximum DC current is allowed to enter the human body. In this application, the DC current is guaranteed to be zero due to the addition of isolation capacitors. A value of 0.47 µF is selected for the isolation capacitors because 0.47 µF is a sufficiently large capacitance that is also available in small packages suitable for wearable electronics.

The ADPD7000 runs the BIA time slot and fills the FIFO with the DFT real and imaginary results for both the voltage and current measurements (four data points in total). The host microcontroller reads the data FIFO and uses the real and imaginary DFT results to calculate the unknown impedance. Calculate the impedance of the sensor by using the following equations:

$$\text{Volage Measurement Magnitude} = \sqrt{r^2 + i^2} \quad (14)$$

$$\text{Voltage Measurement Phase} = tan^{-1}\frac{i}{r} \quad (15)$$

To calculate the impedance, use Ohm's law by dividing the voltage magnitude by the current magnitude. Convert the current measurement value into a voltage using R_{TIA}. This gain must be taken into account. Therefore, the equation to determine the unknown impedance is as follows:

$$|Z_{UNKNOWN}| = \frac{Voltage\ \ Magnitude}{Current\ \ Magnitude} \times R_{TIA} \quad (16)$$

EDA PATH

The EDA path of the ADPD7000 is flexible, and its signals can be routed to either the BIA pads or the ECGx pads, which are controlled by the BIOZ_EXCBUF_ECG_x, BIOZ_TIA_ECG_x, BIOZ_NCHAN_x, and BIOZ_PCHAN_x registers. Table 20 shows the detail connections of the input mux matrix with the related register settings.

APPLICATIONS INFORMATION

Table 20. EDA Channel Connections

Register	Setting	Connection
BIOZ_TIA_ECG_x	001	TIA connected to ECGIN
	010	TIA connected to ECGIP
	100	TIA connected to ECG RLD
BIOZ_EXCBUF_ECG_x	0001	EXC_BUF connected to ECGIN
	0010	EXC_BUF connected to ECGIP
	0100	EXC_BUF connected to ECG RLD

Table 21. Front Buffer Connected

Register	Setting	Connect to
BIOZ_NCHAN_x	001	IMPIN
	010	EXCP
	100	IMPIP
	101	EXCN
	110	ECG RLD
	111	ECGIP
BIOZ_PCHAN_x	001	IMPIP
	010	EXCN
	100	IMPIN
	101	EXCP
	110	ECGIN
	111	ECGIP

Frequency, magnitude of generated sine wave, TIA gain, and DFT points are almost the same as the BIA operation. For DC current mode, set the BIOZ_DCLO_IP_EN_x and BIOZ_DCLO_IN_x bits to 1 to choose the current injected into ECGIP and ECGIN. The current magnitude can be configured by the BIOZ_DCLO_I_MAG_x, BIOZ_DCLO_M_MAG_x, and BIOZ_DCLO_H_MAG_x bits, and the current range is from 2 nA to 1.1 µA.

APPLICATIONS INFORMATION

MULTIMODAL

Figure 52 shows the basic design reference schematic for PPG, ECG, and BIA multimodal applications.

As one multimodal analog front end, the ADPD7000 can also support a single PPG, ECG, and BIA function or a combination of PPG, ECG, and BIA functions.

For example, for a PPG and BIA application, Figure 53 shows the basic application reference schematic.

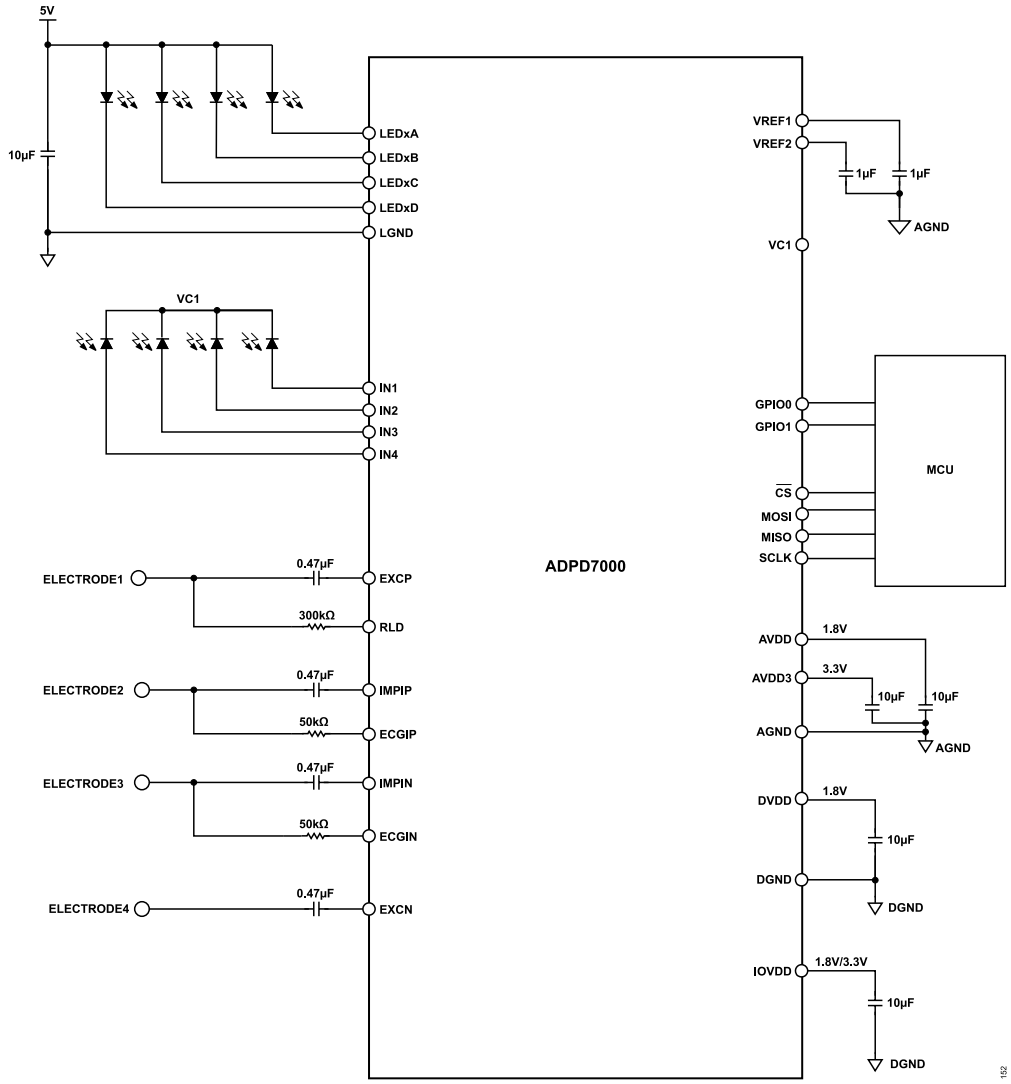

Figure 52. Multimodal Application Reference Schematic

APPLICATIONS INFORMATION

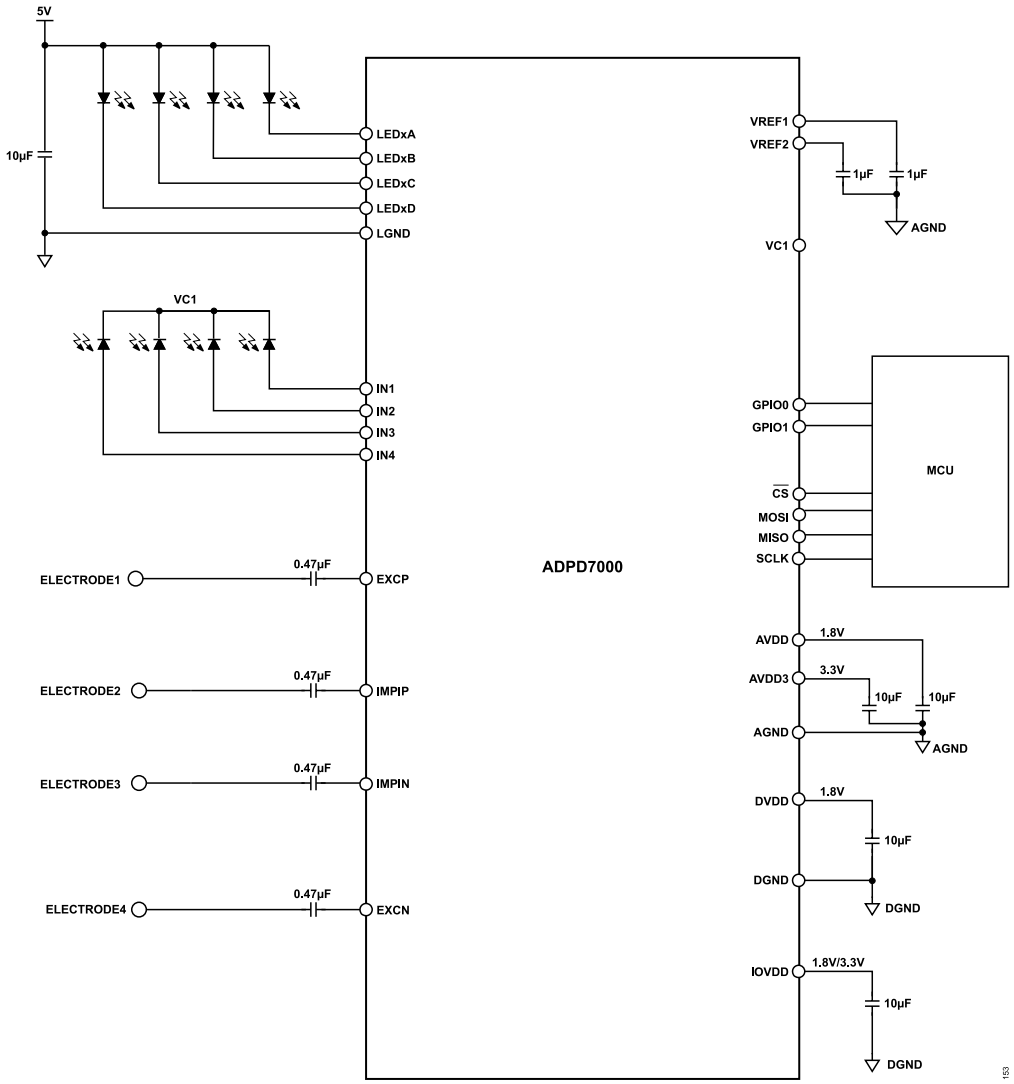

Figure 53. ADPD7000 PPG and BIA Application Reference Schematic

Power-Up Sequencing

Note that a power-up sequence is not needed.

FIFO Data Structure

Table 22 shows the data structure in the FIFO for the recommended multimodal measurement configuration. There are 52 bytes for every data pattern.

Table 22. Data Structure in FIFO

Byte Order in FIFO	Description
Byte 0 to Byte 19	ECG data: 20 bytes
Byte 20 to Byte 23	PPG_A data: 4 bytes
Byte 24 to Byte 27	PPG_B data: 4 bytes
Byte 28 to Byte 33	BIOZ_A data: 6 bytes
Byte 34 to Byte 39	BIOZ_B data: 6 bytes
Byte 40 to Byte 45	BIOZ_C data: 6 bytes
Byte 46 to Byte 51	BIOZ_D data: 6 bytes

DESIGN GUIDE

The ADPD7000 is a multimodal, vital sign monitoring AFE. The performance of the device can be adversely impacted by the PCB layout, especially for the analog input interfaces.

Power Rails

For the power supply, decouple the AVDD, AVDD3, DVDD, and IOVDD pins with a 0.1 µF or larger ceramic chip capacitor to the PCB ground plane placed near the power pins. It is recommended that all decoupling capacitors use individual vias to the PCB ground plane to avoid mutual impedance coupling between decoupled supplies when sharing vias.

APPLICATIONS INFORMATION

Optical Channel

For the PPG channel, decouple the VREF1 pin and VREF2 pin to the PCB ground plane with a 1.0 µF ceramic capacitor. The voltage on the VREF1 pin and VREF2 pin is nominally 1.2 V. Therefore, a 6.3 V rated ceramic capacitor is adequate for this purpose. The most critical aspect of the PCB layout of the ADPD7000 is the handling of the IN1, IN2, IN3, and IN4 nodes. Because photodiode input is sensitive to noise, and any parasitic capacitive coupling to the pin can result in additional noise, it is recommended that the photodiode input trace in the layout be as short as possible and fully guarded by the ground plane.

For example, for a 6-layer stack design, place the chip in the top layer with the optical components in the bottom layer. Therefore, it is recommended to make the IN1, IN2, IN3, and IN4 trace length in the top short to avoid parasitic effects. In the bottom layer, the IN1, IN2, IN3, and IN4 traces and the photodiode anode are fully guarded with the ground shape and trace. VC1 and the photodiode cathode are also guarded with the ground plane. Layer 5 is filled with a ground plane for reference. Keep the analog input signals away from other digital or noisy signals.

ECG Channel

For the ECG channel, both traces of ECGIP and ECGIN must match to achieve high CMRR performance. Use a differential pair layout for ECGIP and ECGIN and shorten the length of the traces.

BIA and EDA Channel

For the BIA and EDA channel, minimize the resistance of the PCB trace to guarantee measurement accuracy.

REGISTER SUMMARY

Table 23. Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x000	FIFO_STATUS	[15:8]	CLEAR_FIFO	INT_FIFO_UFLOW	INT_FIFO_OFLOW	INT_FIFO_TH	FIFO_INIT_DONE_STATUS	FIFO_BYTE_COUNT[10:8]			0x0000	R/W
		[7:0]	FIFO_BYTE_COUNT[7:0]									
0x001	INT_STATUS_TS1	[15:8]	RESERVED				INT_PPG_LEV0_L	INT_PPG_LEV0_K	INT_PPG_LEV0_J	INT_PPG_LEV0_I	0x0000	R/W
		[7:0]	INT_PPG_LEV0_H	INT_PPG_LEV0_G	INT_PPG_LEV0_F	INT_PPG_LEV0_E	INT_PPG_LEV0_D	INT_PPG_LEV0_C	INT_PPG_LEV0_B	INT_PPG_LEV0_A		
0x002	INT_STATUS_TS2	[15:8]	RESERVED				INT_PPG_LEV1_L	INT_PPG_LEV1_K	INT_PPG_LEV1_J	INT_PPG_LEV1_I	0x0000	R/W
		[7:0]	INT_PPG_LEV1_H	INT_PPG_LEV1_G	INT_PPG_LEV1_F	INT_PPG_LEV1_E	INT_PPG_LEV1_D	INT_PPG_LEV1_C	INT_PPG_LEV1_B	INT_PPG_LEV1_A		
0x003	INT_STATUS_BIOZ	[15:8]	INT_BIOZ_SAT_P	INT_BIOZ_SAT_O	INT_BIOZ_SAT_N	INT_BIOZ_SAT_M	INT_BIOZ_SAT_L	INT_BIOZ_SAT_K	INT_BIOZ_SAT_J	INT_BIOZ_SAT_I	0x0000	R/W
		[7:0]	INT_BIOZ_SAT_H	INT_BIOZ_SAT_G	INT_BIOZ_SAT_F	INT_BIOZ_SAT_E	INT_BIOZ_SAT_D	INT_BIOZ_SAT_C	INT_BIOZ_SAT_B	INT_BIOZ_SAT_A		
0x004	ECG_STATUS	[15:8]	INT_BIOZ_SAT_R	INT_BIOZ_SAT_Q	RESERVED						0x00FC	R/W
		[7:0]	ECG_ACLO_STATUS	ECGIN_DCLO_HI_STATUS	ECGIP_DCLO_HI_STATUS	ECG_RLD_DCLO_HI_STATUS	ECG_RLD_DCLO_LO_STATUS	ECG_DCLO_STATUS	ECG_PGA_SAT_STATUS	ECG_ADC_SAT_STATUS		
0x005	GLOBAL_STATUS	[15:8]	RESERVED				ECG_RLD_LEADON_HI_STATUS	ECG_RLD_LEADON_LO_STATUS	ECGIN_LEADON_HI_STATUS	ECGIP_LEADON_HI_STATUS	0x0000	R/W
		[7:0]	RESERVED							INVALID_CFG_STATUS		
0x006	FIFO_TH	[15:8]	RESERVED						FIFO_TH[9:8]		0x000C	R/W
		[7:0]	FIFO_TH[7:0]									
0x007	INT_ACLEAR	[15:8]	INT_ACLEAR_FIFO	RESERVED							0x8000	R/W
		[7:0]	RESERVED									
0x008	CHIP_ID	[15:8]	VERSION								0x00C6	R
		[7:0]	CHIP_ID									
0x009	OSC32M	[15:8]	RESERVED							OSC_32M_EFUSE_CTRL	0x0080	R/W
		[7:0]	OSC_32M_FREQ_ADJ									
0x00A	OSC32M_CAL	[15:8]	OSC_32M_CAL_START	OSC_32M_CAL_COUNT[14:8]							0x0000	R/W
		[7:0]	OSC_32M_CAL_COUNT[7:0]									
0x00B	OSC960K	[15:8]	CAPTURE_TIMESTAMP	RESERVED			OSC_960K_EFUSE_CTRL	OSC_CAL_ENABLE	OSC_960K_FREQ_ADJ[9:8]		0x0AB2	R/W
		[7:0]	OSC_960K_FREQ_ADJ[7:0]									
0x00D	TS_FREQ	[15:8]	TIMESLOT_PERIOD_L[15:8]								0x2580	R/W
		[7:0]	TIMESLOT_PERIOD_L[7:0]									
0x00E	TS_FREQH	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED	TIMESLOT_PERIOD_H								

REGISTER SUMMARY

Table 23. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x00F	SYS_CTL	[15:8]	SW_RESET	RESERVED			LEAD_ON_MODE	ALT_CLOCKS			0x0000	R/W
		[7:0]	ALT_CLK_GPIO		LP_MODE_SLEEP	GO_SLEEP	RANDOM_SLEEP	TM_CLK_GPIO_SEL	OSC_960K_EN	LOWPOWER_BIAS_EN		
0x010	OPMODE	[15:8]	ECG_TIMESLOT_EN	RESERVED	BIOZ_TIMESLOT_MODE	BIOZ_TIMESLOT_EN					0x0000	R/W
		[7:0]	PPG_TIMESLOT_EN				RESERVED	OP_MODE				
0x011	STAMP_L	[15:8]	TIMESTAMP_COUNT_L[15:8]								0x0000	R
		[7:0]	TIMESTAMP_COUNT_L[7:0]									
0x012	STAMP_H	[15:8]	TIMESTAMP_COUNT_H[15:8]								0x0000	R
		[7:0]	TIMESTAMP_COUNT_H[7:0]									
0x013	STAMPDELTA	[15:8]	TIMESTAMP_SLOT_DELTA[15:8]								0x0000	R
		[7:0]	TIMESTAMP_SLOT_DELTA[7:0]									
0x014	INT_ENABLE_XD	[15:8]	INTX_EN_FIFO_TH	INTX_EN_FIFO_UFLOW	INTX_EN_FIFO_OFLOW	RESERVED					0x0000	R/W
		[7:0]	RESERVED									
0x015	INT_ENABLE_YD	[15:8]	INTY_EN_FIFO_TH	INTY_EN_FIFO_UFLOW	INTY_EN_FIFO_OFLOW	RESERVED					0x0000	R/W
		[7:0]	RESERVED									
0x01E	FIFO_STATUS_BYTES	[15:8]	RESERVED						ENA_STAT_ECG	ENA_STAT_LEVX	0x0200	R/W
		[7:0]	ENA_STAT_LEV1	ENA_STAT_LEV0	ENA_SEQ_NUM	RESERVED						
0x020	INPUT_SLEEP	[15:8]	RESERVED								0x0000	R/W
		[7:0]	INP_SLEEP_34				INP_SLEEP_12					
0x021	INPUT_CFG	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED		VC1_SLEEP		RESERVED		PAIR34	PAIR12		
0x022	GPIO_CFG	[15:8]	GPIO_SLEW		GPIO_DRV		RESERVED			GPIO_PIN_CFG2, Bit 2	0x0000	R/W
		[7:0]	GPIO_PIN_CFG2[1:0]		GPIO_PIN_CFG1			GPIO_PIN_CFG0				
0x023	GPIO01	[15:8]	GPIOOUT1								0x0000	R/W
		[7:0]	GPIOOUT0									
0x025	GPIO_IN	[15:8]	RESERVED								0x0000	R
		[7:0]	RESERVED				GPIO_INPUT					
0x026	GPIO_EXT	[15:8]	RESERVED							GOUT_SLEEP	0x0000	R/W
		[7:0]	TIMESTAMP_INV	TIMESTAMP_ALWAYS_EN	TIMESTAMP_GPIO		RESERVED	EXT_SYNC_EN	EXT_SYNC_GPIO			
0x02F	FIFO_DATA	[15:8]	FIFO_DATA[15:8]								0x0000	R
		[7:0]	FIFO_DATA[7:0]									
0x044	EFUSE	[15:8]	EFUSE_REFRESH	RESERVED							0x0005	R/W

REGISTER SUMMARY

Table 23. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
		[7:0]	RESERVED					EFUSE_EN		EFUSE_REG_EN		
0x057	IO_ADJUST	[15:8]	RESERVED								0x0050	R/W
		[7:0]	RESERVED	LOW_IOVDD_EN	RESERVED		SPI_SLEW		SPI_DRV			
0x100	ECG_ANA_CTRL	[15:8]	RESERVED			ECG_SHORT_IN_RLD	ECG_SHORT_IP_RLD	RESERVED	ECG_CGA_PREBUF_ALWAYSON	ECG_CGA_GAIN	0x0070	R/W
		[7:0]	ECG_RLD_VCM_EN	ECG_RLD_OUT_DISCONNECT	ECG_RLD_OUT_SEL		ECG_RLD_SAT_EN	ECG_RLD_SAT_THRESHOLD		ECG_RLD_EN		
0x101	ECG_LEADOFF_CTRL	[15:8]	ECG_ACLO_EN	ECG_ACLO_MAG			ECG_ACLO_THRESHOLD			ECG_DCLO_L_EN	0x0004	R/W
		[7:0]	ECG_DCLO_MAG				ECG_DCLO_POLARITY_IN	ECG_DCLO_POLARITY_IP	ECG_DCLO_THRESHOLD			
0x102	ECG_DIG_CTRL1	[15:8]	RESERVED					ECG_DEBOUNCER_INIT	ECG_DEBOUNCER_SEL	ECG_OVERSAMPLING_RATIO[5]	0x0018	R/W
		[7:0]	ECG_OVERSAMPLING_RATIO[4:0]					ECG_ODR_SEL				
0x103	ECG_DIG_CTRL2	[15:8]	ECG_DCLO_H_EN	ECG_DCLO_H_MAG				ECG_DCLO_IP_EN	ECG_DCLO_IN_EN	ECG_DCLO_DET_IN_EN	0x0000	R/W
		[7:0]	ECG_DCLO_DET_IP_EN	ECG_DCLO_M_EN	ECG_ACLO_INV	ECG_BYPASS_EQLZR	ECG_CAL_GAIN					
0x104	ECG_MATRIX	[15:8]	RESERVED						ECG_SWAP_POLARITY	ECG_PINS_CON_BIOZ	0x0000	R/W
		[7:0]	ECG_E1_CON_ECGIP	ECG_E1_CON_RLD	ECG_E2_CON_ECGIP	ECG_E2_CON_RLD	ECG_E3_CON_ECGIN	ECG_E3_CON_RLD	ECG_E4_CON_ECGIN	ECG_E4_CON_RLD		
0x120	TS_CTRL_A	[15:8]	RESERVED		SAMPLE_TYPE_A			RESERVED	TIMESLOT_OFFSET_A[9:8]		0x1000	R/W
		[7:0]	TIMESLOT_OFFSET_A[7:0]									
0x121	TS_PATH_A	[15:8]	PRE_WIDTH_A				AMBIENT_CANCELLATION_A		GOUT_A	RESERVED	0x4020	R/W
		[7:0]	RESERVED	AFE_PATH_CFG_A								
0x122	INPUTS_A	[15:8]	INP4_SEL_A		INP3_SEL_A		INP2_SEL_A		INP1_SEL_A		0x0000	R/W
		[7:0]	INP34_A				INP12_A					
0x123	CATHODE_A	[15:8]	RESERVED	PRECON_A			RESERVED		AFE_VREF_AMB_SEL_A		0x0200	R/W
		[7:0]	VC1_AMB_SEL_A		VC1_PULSE_A		VC1_ALT_A		VC1_SEL_A			
0x124	AFE_TRIM1_A	[15:8]	AFE_TIA_SAT_DETECT_EN_A	RESERVED		AFE_BUFFER_GAIN_A		VREF_PULSE_A	AFE_TRIM_VREF_A		0x02C9	R/W
		[7:0]	VREF_PULSE_VAL_A		TIA_GAIN_CH2_A			TIA_GAIN_CH1_A				
0x125	AFE_TRIM2_A	[15:8]	RESERVED			AFE_BUFFER_CAP_A	RESERVED				0x0000	R/W

REGISTER SUMMARY

Table 23. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
		[7:0]	RESERVED		TIA_GAIN_CH4_A			TIA_GAIN_CH3_A				
0x126	AFE_DAC1_A	[15:8]	DAC_AMBIENT_CH1_A[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH1_A, Bit 0	DAC_LED_DC_CH1_A								
0x127	AFE_DAC2_A	[15:8]	DAC_AMBIENT_CH2_A[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH2_A, Bit 0	DAC_LED_DC_CH2_A								
0x128	LED_POW12_A	[15:8]	RESERVED	LED_CURRENT2_A							0x0000	R/W
		[7:0]	RESERVED	LED_CURRENT1_A								
0x129	LED_MODE_A	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LED_DRIVESIDE2_A		LED_DRIVESIDE1_A		RESERVED		LED_MODE2_A	LED_MODE1_A		
0x12A	COUNTS_A	[15:8]	NUM_INT_A								0x0101	R/W
		[7:0]	NUM_REPEAT_A									
0x12B	PERIOD_A	[15:8]	RESERVED	COARSE_LOOP_WIDTH_A	MOD_TYPE_A		RESERVED		MIN_PERIOD_A[9:8]		0x0000	R/W
		[7:0]	MIN_PERIOD_A[7:0]									
0x12C	LED_PULSE1_A	[15:8]	LED_WIDTH_A								0x0210	R/W
		[7:0]	LED_OFFSET_A									
0x12D	AFE_DAC3_A	[15:8]	DAC_AMBIENT_CH3_A[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH3_A, Bit 0	DAC_LED_DC_CH3_A								
0x12E	AFE_DAC4_A	[15:8]	DAC_AMBIENT_CH4_A[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH4_A, Bit 0	DAC_LED_DC_CH4_A								
0x12F	THRESH0_A	[15:8]	RESERVED			THRESH0_SHIFT_A					0x0000	R/W
		[7:0]	THRESH0_VALUE_A									
0x130	MOD_PULSE_A	[15:8]	MOD_WIDTH_A								0x0001	R/W
		[7:0]	MOD_OFFSET_A									
0x131	PATTERN1_A	[15:8]	LED_DISABLE_A				MOD_DISABLE_A				0x0000	R/W
		[7:0]	SUBTRACT_A				AFE_SWAP_A					
0x132	THRESH_CFG_A	[15:8]	RESERVED					THRESH1_DIR_A	THRESH1_TYPE_A		0x0000	R/W
		[7:0]	RESERVED					THRESH0_DIR_A	THRESH0_TYPE_A			

REGISTER SUMMARY

Table 23. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x133	ADC_OFF1_A	[15:8]	RESERVED		CH1_ADC_ADJUST_A[13:8]						0x0000	R/W
		[7:0]	CH1_ADC_ADJUST_A[7:0]									
0x134	ADC_OFF2_A	[15:8]	RESERVED		CH2_ADC_ADJUST_A[13:8]						0x0000	R/W
		[7:0]	CH2_ADC_ADJUST_A[7:0]									
0x135	DATA1_A	[15:8]	DARK_SHIFT_A					DARK_SIZE_A			0x0003	R/W
		[7:0]	SIGNAL_SHIFT_A					SIGNAL_SIZE_A				
0x136	DATA2_A	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LIT_SHIFT_A					LIT_SIZE_A				
0x137	DECIMATE_A	[15:8]	CHANNEL_EN_A		RESERVED			SUBSAMPLE_RATIO_A[6:4]			0x0010	R/W
		[7:0]	SUBSAMPLE_RATIO_A[3:0]				RESERVED					
0x138	DIGINT_LIT_A	[15:8]	RESERVED							LIT_OFFSET_A, Bit 8	0x0026	R/W
		[7:0]	LIT_OFFSET_A[7:0]									
0x139	DIGINT_DARK_A	[15:8]	DARK2_OFFSET_A[8:1]								0x0086	R/W
		[7:0]	DARK2_OFFSET_A, Bit 0	DARK1_OFFSET_A								
0x13A	ADC_OFF3_A	[15:8]	RESERVED		CH3_ADC_ADJUST_A[13:8]						0x0000	R/W
		[7:0]	CH3_ADC_ADJUST_A[7:0]									
0x13B	ADC_OFF4_A	[15:8]	RESERVED		CH4_ADC_ADJUST_A[13:8]						0x0000	R/W
		[7:0]	CH4_ADC_ADJUST_A[7:0]									
0x13C	THRESH1_A	[15:8]	RESERVED			THRESH1_SHIFT_A					0x0000	R/W
		[7:0]	THRESH1_VALUE_A									
0x140	TS_CTRL_B	[15:8]	RESERVED		SAMPLE_TYPE_B			RESERVED	TIMESLOT_OFFSET_B[9:8]		0x1000	R/W
		[7:0]	TIMESLOT_OFFSET_B[7:0]									
0x141	TS_PATH_B	[15:8]	PRE_WIDTH_B				AMBIENT_CANCELLATION_B		GOUT_B	RESERVED	0x4020	R/W
		[7:0]	RESERVED	AFE_PATH_CFG_B								
0x142	INPUTS_B	[15:8]	INP4_SEL_B		INP3_SEL_B		INP2_SEL_B		INP1_SEL_B		0x0000	R/W
		[7:0]	INP34_B				INP12_B					
0x143	CATHODE_B	[15:8]	RESERVED	PRECON_B			RESERVED		AFE_VREF_AMB_SEL_B		0x0200	R/W
		[7:0]	VC1_AMB_SEL_B		VC1_PULSE_B		VC1_ALT_B		VC1_SEL_B			
0x144	AFE_TRIM1_B	[15:8]	AFE_TIA_SAT_DETECT_EN_B	RESERVED		AFE_BUFFER_GAIN_B		VREF_PULSE_B	AFE_TRIM_VREF_B		0x02C9	R/W
		[7:0]	VREF_PULSE_VAL_B		TIA_GAIN_CH2_B			TIA_GAIN_CH1_B				
0x145	AFE_TRIM2_B	[15:8]	RESERVED			AFE_BUFFER_CAP_B	RESERVED				0x0000	R/W
		[7:0]	RESERVED		TIA_GAIN_CH4_B			TIA_GAIN_CH3_B				

REGISTER SUMMARY

Table 23. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x146	AFE_DAC 1_B	[15:8]	DAC_AMBIENT_CH1_B[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH1_B, Bit 0	DAC_LED_DC_CH1_B								
0x147	AFE_DAC 2_B	[15:8]	DAC_AMBIENT_CH2_B[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH2_B, Bit 0	DAC_LED_DC_CH2_B								
0x148	LED_POW 12_B	[15:8]	RESERVED	LED_CURRENT2_B							0x0000	R/W
		[7:0]	RESERVED	LED_CURRENT1_B								
0x149	LED_MOD E_B	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LED_DRIVESIDE2_B		LED_DRIVESIDE1_B		RESERVED		LED_MODE 2_B	LED_MODE 1_B		
0x14A	COUNTS_ B	[15:8]	NUM_INT_B								0x0101	R/W
		[7:0]	NUM_REPEAT_B									
0x14B	PERIOD_ B	[15:8]	RESERVED	COARSE_LOOP_WIDTH_B	MOD_TYPE_B		RESERVED		MIN_PERIOD_B[9:8]		0x0000	R/W
		[7:0]	MIN_PERIOD_B[7:0]									
0x14C	LED_PUL SE1_B	[15:8]	LED_WIDTH_B								0x0210	R/W
		[7:0]	LED_OFFSET_B									
0x14D	AFE_DAC 3_B	[15:8]	DAC_AMBIENT_CH3_B[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH3_B, Bit 0	DAC_LED_DC_CH3_B								
0x14E	AFE_DAC 4_B	[15:8]	DAC_AMBIENT_CH4_B[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH4_B, Bit 0	DAC_LED_DC_CH4_B								
0x14F	THRESH0 _B	[15:8]	RESERVED			THRESH0_SHIFT_B					0x0000	R/W
		[7:0]	THRESH0_VALUE_B									
0x150	MOD_PUL SE_B	[15:8]	MOD_WIDTH_B								0x0001	R/W
		[7:0]	MOD_OFFSET_B									
0x151	PATTERN 1_B	[15:8]	LED_DISABLE_B				MOD_DISABLE_B				0x0000	R/W
		[7:0]	SUBTRACT_B				AFE_SWAP_B					
0x152	THRESH_ CFG_B	[15:8]	RESERVED					THRESH1_DIR_B	THRESH1_TYPE_B		0x0000	R/W
		[7:0]	RESERVED					THRESH0_DIR_B	THRESH0_TYPE_B			

REGISTER SUMMARY

Table 23. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x153	ADC_OFF1_B	[15:8]	RESERVED		CH1_ADC_ADJUST_B[13:8]						0x0000	R/W
		[7:0]	CH1_ADC_ADJUST_B[7:0]									
0x154	ADC_OFF2_B	[15:8]	RESERVED		CH2_ADC_ADJUST_B[13:8]						0x0000	R/W
		[7:0]	CH2_ADC_ADJUST_B[7:0]									
0x155	DATA1_B	[15:8]	DARK_SHIFT_B					DARK_SIZE_B			0x0003	R/W
		[7:0]	SIGNAL_SHIFT_B					SIGNAL_SIZE_B				
0x156	DATA2_B	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LIT_SHIFT_B					LIT_SIZE_B				
0x157	DECIMATE_B	[15:8]	CHANNEL_EN_B		RESERVED			SUBSAMPLE_RATIO_B[6:4]			0x0010	R/W
		[7:0]	SUBSAMPLE_RATIO_B[3:0]				RESERVED					
0x158	DIGINT_LIT_B	[15:8]	RESERVED							LIT_OFFSET_B, Bit 8	0x0026	R/W
		[7:0]	LIT_OFFSET_B[7:0]									
0x159	DIGINT_DARK_B	[15:8]	DARK2_OFFSET_B[8:1]								0x0086	R/W
		[7:0]	DARK2_OFFSET_B, Bit 0	DARK1_OFFSET_B								
0x15A	ADC_OFF3_B	[15:8]	RESERVED		CH3_ADC_ADJUST_B[13:8]						0x0000	R/W
		[7:0]	CH3_ADC_ADJUST_B[7:0]									
0x15B	ADC_OFF4_B	[15:8]	RESERVED		CH4_ADC_ADJUST_B[13:8]						0x0000	R/W
		[7:0]	CH4_ADC_ADJUST_B[7:0]									
0x15C	THRESH1_B	[15:8]	RESERVED			THRESH1_SHIFT_B					0x0000	R/W
		[7:0]	THRESH1_VALUE_B									
0x160	TS_CTRL_C	[15:8]	RESERVED		SAMPLE_TYPE_C			RESERVED	TIMESLOT_OFFSET_C[9:8]		0x1000	R/W
		[7:0]	TIMESLOT_OFFSET_C[7:0]									
0x161	TS_PATH_C	[15:8]	PRE_WIDTH_C				AMBIENT_CANCELLATION_C		GOUT_C	RESERVED	0x4020	R/W
		[7:0]	RESERVED	AFE_PATH_CFG_C								
0x162	INPUTS_C	[15:8]	INP4_SEL_C		INP3_SEL_C		INP2_SEL_C		INP1_SEL_C		0x0000	R/W
		[7:0]	INP34_C				INP12_C					
0x163	CATHODE_C	[15:8]	RESERVED	PRECON_C			RESERVED		AFE_VREF_AMB_SEL_C		0x0200	R/W
		[7:0]	VC1_AMB_SEL_C		VC1_PULSE_C		VC1_ALT_C		VC1_SEL_C			
0x164	AFE_TRIM1_C	[15:8]	AFE_TIA_SAT_DETECT_EN_C	RESERVED		AFE_BUFFER_GAIN_C		VREF_PULSE_C	AFE_TRIM_VREF_C		0x02C9	R/W
		[7:0]	VREF_PULSE_VAL_C		TIA_GAIN_CH2_C			TIA_GAIN_CH1_C				
0x165	AFE_TRIM2_C	[15:8]	RESERVED			AFE_BUFFER_CAP_C	RESERVED				0x0000	R/W
		[7:0]	RESERVED		TIA_GAIN_CH4_C			TIA_GAIN_CH3_C				

REGISTER SUMMARY

Table 23. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x166	AFE_DAC 1_C	[15:8]	DAC_AMBIENT_CH1_C[8:1]								0x0000	R/W
		[7:0]	DAC_AMB IENT_CH1 _C, Bit 0	DAC_LED_DC_CH1_C								
0x167	AFE_DAC 2_C	[15:8]	DAC_AMBIENT_CH2_C[8:1]								0x0000	R/W
		[7:0]	DAC_AMB IENT_CH2 _C, Bit 0	DAC_LED_DC_CH2_C								
0x168	LED_POW 12_C	[15:8]	RESERVE D	LED_CURRENT2_C							0x0000	R/W
		[7:0]	RESERVE D	LED_CURRENT1_C								
0x169	LED_MOD E_C	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LED_DRIVESIDE2_C		LED_DRIVESIDE1_C		RESERVED		LED_MODE 2_C	LED_MODE 1_C		
0x16A	COUNTS_ C	[15:8]	NUM_INT_C								0x0101	R/W
		[7:0]	NUM_REPEAT_C									
0x16B	PERIOD_ C	[15:8]	RESERVE D	COARSE_L OOP_WIDT H_C	MOD_TYPE_C		RESERVED		MIN_PERIOD_C[9:8]		0x0000	R/W
		[7:0]	MIN_PERIOD_C[7:0]									
0x16C	LED_PUL SE1_C	[15:8]	LED_WIDTH_C								0x0210	R/W
		[7:0]	LED_OFFSET_C									
0x16D	AFE_DAC 3_C	[15:8]	DAC_AMBIENT_CH3_C[8:1]								0x0000	R/W
		[7:0]	DAC_AMB IENT_CH3 _C, Bit 0	DAC_LED_DC_CH3_C								
0x16E	AFE_DAC 4_C	[15:8]	DAC_AMBIENT_CH4_C[8:1]								0x0000	R/W
		[7:0]	DAC_AMB IENT_CH4 _C, Bit 0	DAC_LED_DC_CH4_C								
0x16F	THRESH0 _C	[15:8]	RESERVED			THRESH0_SHIFT_C					0x0000	R/W
		[7:0]	THRESH0_VALUE_C									
0x170	MOD_PUL SE_C	[15:8]	MOD_WIDTH_C								0x0001	R/W
		[7:0]	MOD_OFFSET_C									
0x171	PATTERN 1_C	[15:8]	LED_DISABLE_C				MOD_DISABLE_C				0x0000	R/W
		[7:0]	SUBTRACT_C				AFE_SWAP_C					
0x172	THRESH_ CFG_C	[15:8]	RESERVED					THRESH1_ DIR_C	THRESH1_TYPE_C		0x0000	R/W
		[7:0]	RESERVED					THRESH0_ DIR_C	THRESH0_TYPE_C			

REGISTER SUMMARY

Table 23. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x173	ADC_OFF1_C	[15:8]	RESERVED		CH1_ADC_ADJUST_C[13:8]						0x0000	R/W
		[7:0]	CH1_ADC_ADJUST_C[7:0]									
0x174	ADC_OFF2_C	[15:8]	RESERVED		CH2_ADC_ADJUST_C[13:8]						0x0000	R/W
		[7:0]	CH2_ADC_ADJUST_C[7:0]									
0x175	DATA1_C	[15:8]	DARK_SHIFT_C					DARK_SIZE_C			0x0003	R/W
		[7:0]	SIGNAL_SHIFT_C					SIGNAL_SIZE_C				
0x176	DATA2_C	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LIT_SHIFT_C					LIT_SIZE_C				
0x177	DECIMATE_C	[15:8]	CHANNEL_EN_C		RESERVED			SUBSAMPLE_RATIO_C[6:4]			0x0010	R/W
		[7:0]	SUBSAMPLE_RATIO_C[3:0]				RESERVED					
0x178	DIGINT_LIT_C	[15:8]	RESERVED							LIT_OFFSET_C, Bit 8	0x0026	R/W
		[7:0]	LIT_OFFSET_C[7:0]									
0x179	DIGINT_DARK_C	[15:8]	DARK2_OFFSET_C[8:1]								0x0086	R/W
		[7:0]	DARK2_OFFSET_C, Bit 0	DARK1_OFFSET_C								
0x17A	ADC_OFF3_C	[15:8]	RESERVED		CH3_ADC_ADJUST_C[13:8]						0x0000	R/W
		[7:0]	CH3_ADC_ADJUST_C[7:0]									
0x17B	ADC_OFF4_C	[15:8]	RESERVED		CH4_ADC_ADJUST_C[13:8]						0x0000	R/W
		[7:0]	CH4_ADC_ADJUST_C[7:0]									
0x17C	THRESH1_C	[15:8]	RESERVED			THRESH1_SHIFT_C					0x0000	R/W
		[7:0]	THRESH1_VALUE_C									
0x180	TS_CTRL_D	[15:8]	RESERVED		SAMPLE_TYPE_D			RESERVED	TIMESLOT_OFFSET_D[9:8]		0x1000	R/W
		[7:0]	TIMESLOT_OFFSET_D[7:0]									
0x181	TS_PATH_D	[15:8]	PRE_WIDTH_D				AMBIENT_CANCELLATION_D		GOUT_D	RESERVED	0x4020	R/W
		[7:0]	RESERVED	AFE_PATH_CFG_D								
0x182	INPUTS_D	[15:8]	INP4_SEL_D		INP3_SEL_D		INP2_SEL_D		INP1_SEL_D		0x0000	R/W
		[7:0]	INP34_D				INP12_D					
0x183	CATHODE_D	[15:8]	RESERVED	PRECON_D			RESERVED		AFE_VREF_AMB_SEL_D		0x0200	R/W
		[7:0]	VC1_AMB_SEL_D		VC1_PULSE_D		VC1_ALT_D		VC1_SEL_D			
0x184	AFE_TRIM1_D	[15:8]	AFE_TIA_SAT_DETECT_EN_D	RESERVED		AFE_BUFFER_GAIN_D		VREF_PULSE_D	AFE_TRIM_VREF_D		0x02C9	R/W
		[7:0]	VREF_PULSE_VAL_D		TIA_GAIN_CH2_D			TIA_GAIN_CH1_D				
0x185	AFE_TRIM2_D	[15:8]	RESERVED			AFE_BUFFER_CAP_D	RESERVED				0x0000	R/W
		[7:0]	RESERVED		TIA_GAIN_CH4_D			TIA_GAIN_CH3_D				

REGISTER SUMMARY

Table 23. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x186	AFE_DAC 1_D	[15:8]	DAC_AMBIENT_CH1_D[8:1]								0x0000	R/W
		[7:0]	DAC_AMB IENT_CH1 _D, Bit 0	DAC_LED_DC_CH1_D								
0x187	AFE_DAC 2_D	[15:8]	DAC_AMBIENT_CH2_D[8:1]								0x0000	R/W
		[7:0]	DAC_AMB IENT_CH2 _D, Bit 0	DAC_LED_DC_CH2_D								
0x188	LED_POW 12_D	[15:8]	RESERVE D	LED_CURRENT2_D							0x0000	R/W
		[7:0]	RESERVE D	LED_CURRENT1_D								
0x189	LED_MOD E_D	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LED_DRIVESIDE2_D		LED_DRIVESIDE1_D		RESERVED		LED_MODE 2_D	LED_MODE 1_D		
0x18A	COUNTS_ D	[15:8]	NUM_INT_D								0x0101	R/W
		[7:0]	NUM_REPEAT_D									
0x18B	PERIOD_ D	[15:8]	RESERVE D	COARSE_L OOP_WIDT H_D	MOD_TYPE_D		RESERVED		MIN_PERIOD_D[9:8]		0x0000	R/W
		[7:0]	MIN_PERIOD_D[7:0]									
0x18C	LED_PUL SE1_D	[15:8]	LED_WIDTH_D								0x0210	R/W
		[7:0]	LED_OFFSET_D									
0x18D	AFE_DAC 3_D	[15:8]	DAC_AMBIENT_CH3_D[8:1]								0x0000	R/W
		[7:0]	DAC_AMB IENT_CH3 _D, Bit 0	DAC_LED_DC_CH3_D								
0x18E	AFE_DAC 4_D	[15:8]	DAC_AMBIENT_CH4_D[8:1]								0x0000	R/W
		[7:0]	DAC_AMB IENT_CH4 _D, Bit 0	DAC_LED_DC_CH4_D								
0x18F	THRESH0 _D	[15:8]	RESERVED			THRESH0_SHIFT_D					0x0000	R/W
		[7:0]	THRESH0_VALUE_D									
0x190	MOD_PUL SE_D	[15:8]	MOD_WIDTH_D								0x0001	R/W
		[7:0]	MOD_OFFSET_D									
0x191	PATTERN 1_D	[15:8]	LED_DISABLE_D				MOD_DISABLE_D				0x0000	R/W
		[7:0]	SUBTRACT_D				AFE_SWAP_D					
0x192	THRESH_ CFG_D	[15:8]	RESERVED					THRESH1_ DIR_D	THRESH1_TYPE_D		0x0000	R/W
		[7:0]	RESERVED					THRESH0_ DIR_D	THRESH0_TYPE_D			

REGISTER SUMMARY

Table 23. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x193	ADC_OFF1_D	[15:8]	RESERVED		CH1_ADC_ADJUST_D[13:8]						0x0000	R/W
		[7:0]	CH1_ADC_ADJUST_D[7:0]									
0x194	ADC_OFF2_D	[15:8]	RESERVED		CH2_ADC_ADJUST_D[13:8]						0x0000	R/W
		[7:0]	CH2_ADC_ADJUST_D[7:0]									
0x195	DATA1_D	[15:8]	DARK_SHIFT_D					DARK_SIZE_D			0x0003	R/W
		[7:0]	SIGNAL_SHIFT_D					SIGNAL_SIZE_D				
0x196	DATA2_D	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LIT_SHIFT_D					LIT_SIZE_D				
0x197	DECIMATE_D	[15:8]	CHANNEL_EN_D		RESERVED			SUBSAMPLE_RATIO_D[6:4]			0x0010	R/W
		[7:0]	SUBSAMPLE_RATIO_D[3:0]				RESERVED					
0x198	DIGINT_LIT_D	[15:8]	RESERVED							LIT_OFFSET_D, Bit 8	0x0026	R/W
		[7:0]	LIT_OFFSET_D[7:0]									
0x199	DIGINT_DARK_D	[15:8]	DARK2_OFFSET_D[8:1]								0x0086	R/W
		[7:0]	DARK2_OFFSET_D, Bit 0	DARK1_OFFSET_D								
0x19A	ADC_OFF3_D	[15:8]	RESERVED		CH3_ADC_ADJUST_D[13:8]						0x0000	R/W
		[7:0]	CH3_ADC_ADJUST_D[7:0]									
0x19B	ADC_OFF4_D	[15:8]	RESERVED		CH4_ADC_ADJUST_D[13:8]						0x0000	R/W
		[7:0]	CH4_ADC_ADJUST_D[7:0]									
0x19C	THRESH1_D	[15:8]	RESERVED			THRESH1_SHIFT_D					0x0000	R/W
		[7:0]	THRESH1_VALUE_D									
0x1A0	TS_CTRL_E	[15:8]	RESERVED		SAMPLE_TYPE_E			RESERVED	TIMESLOT_OFFSET_E[9:8]		0x1000	R/W
		[7:0]	TIMESLOT_OFFSET_E[7:0]									
0x1A1	TS_PATH_E	[15:8]	PRE_WIDTH_E				AMBIENT_CANCELLATION_E		GOUT_E	RESERVED	0x4020	R/W
		[7:0]	RESERVED	AFE_PATH_CFG_E								
0x1A2	INPUTS_E	[15:8]	INP4_SEL_E		INP3_SEL_E		INP2_SEL_E		INP1_SEL_E		0x0000	R/W
		[7:0]	INP34_E				INP12_E					
0x1A3	CATHODE_E	[15:8]	RESERVED	PRECON_E			RESERVED		AFE_VREF_AMB_SEL_E		0x0200	R/W
		[7:0]	VC1_AMB_SEL_E		VC1_PULSE_E		VC1_ALT_E		VC1_SEL_E			
0x1A4	AFE_TRIM1_E	[15:8]	AFE_TIA_SAT_DETECT_EN_E	RESERVED		AFE_BUFFER_GAIN_E		VREF_PULSE_E	AFE_TRIM_VREF_E		0x02C9	R/W
		[7:0]	VREF_PULSE_VAL_E		TIA_GAIN_CH2_E			TIA_GAIN_CH1_E				
0x1A5	AFE_TRIM2_E	[15:8]	RESERVED			AFE_BUFFER_CAP_E	RESERVED				0x0000	R/W
		[7:0]	RESERVED		TIA_GAIN_CH4_E			TIA_GAIN_CH3_E				

REGISTER SUMMARY

Table 23. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x1A6	AFE_DAC1_E	[15:8]	DAC_AMBIENT_CH1_E[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH1_E, Bit 0	DAC_LED_DC_CH1_E								
0x1A7	AFE_DAC2_E	[15:8]	DAC_AMBIENT_CH2_E[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH2_E, Bit 0	DAC_LED_DC_CH2_E								
0x1A8	LED_POW12_E	[15:8]	RESERVED	LED_CURRENT2_E							0x0000	R/W
		[7:0]	RESERVED	LED_CURRENT1_E								
0x1A9	LED_MODE_E	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LED_DRIVESIDE2_E		LED_DRIVESIDE1_E		RESERVED		LED_MODE2_E	LED_MODE1_E		
0x1AA	COUNTS_E	[15:8]	NUM_INT_E								0x0101	R/W
		[7:0]	NUM_REPEAT_E									
0x1AB	PERIOD_E	[15:8]	RESERVED	COARSE_LOOP_WIDTH_E	MOD_TYPE_E		RESERVED		MIN_PERIOD_E[9:8]		0x0000	R/W
		[7:0]	MIN_PERIOD_E[7:0]									
0x1AC	LED_PULSE1_E	[15:8]	LED_WIDTH_E								0x0210	R/W
		[7:0]	LED_OFFSET_E									
0x1AD	AFE_DAC3_E	[15:8]	DAC_AMBIENT_CH3_E[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH3_E, Bit 0	DAC_LED_DC_CH3_E								
0x1AE	AFE_DAC4_E	[15:8]	DAC_AMBIENT_CH4_E[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH4_E, Bit 0	DAC_LED_DC_CH4_E								
0x1AF	THRESH0_E	[15:8]	RESERVED			THRESH0_SHIFT_E					0x0000	R/W
		[7:0]	THRESH0_VALUE_E									
0x1B0	MOD_PULSE_E	[15:8]	MOD_WIDTH_E								0x0001	R/W
		[7:0]	MOD_OFFSET_E									
0x1B1	PATTERN1_E	[15:8]	LED_DISABLE_E				MOD_DISABLE_E				0x0000	R/W
		[7:0]	SUBTRACT_E				AFE_SWAP_E					
0x1B2	THRESH_CFG_E	[15:8]	RESERVED					THRESH1_DIR_E	THRESH1_TYPE_E		0x0000	R/W
		[7:0]	RESERVED					THRESH0_DIR_E	THRESH0_TYPE_E			

REGISTER SUMMARY

Table 23. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x1B3	ADC_OFF1_E	[15:8]	RESERVED		CH1_ADC_ADJUST_E[13:8]						0x0000	R/W
		[7:0]	CH1_ADC_ADJUST_E[7:0]									
0x1B4	ADC_OFF2_E	[15:8]	RESERVED		CH2_ADC_ADJUST_E[13:8]						0x0000	R/W
		[7:0]	CH2_ADC_ADJUST_E[7:0]									
0x1B5	DATA1_E	[15:8]	DARK_SHIFT_E					DARK_SIZE_E			0x0003	R/W
		[7:0]	SIGNAL_SHIFT_E					SIGNAL_SIZE_E				
0x1B6	DATA2_E	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LIT_SHIFT_E					LIT_SIZE_E				
0x1B7	DECIMATE_E	[15:8]	CHANNEL_EN_E		RESERVED			SUBSAMPLE_RATIO_E[6:4]			0x0010	R/W
		[7:0]	SUBSAMPLE_RATIO_E[3:0]				RESERVED					
0x1B8	DIGINT_LIT_E	[15:8]	RESERVED							LIT_OFFSET_E, Bit 8	0x0026	R/W
		[7:0]	LIT_OFFSET_E[7:0]									
0x1B9	DIGINT_DARK_E	[15:8]	DARK2_OFFSET_E[8:1]								0x0086	R/W
		[7:0]	DARK2_OFFSET_E, Bit 0	DARK1_OFFSET_E								
0x1BA	ADC_OFF3_E	[15:8]	RESERVED		CH3_ADC_ADJUST_E[13:8]						0x0000	R/W
		[7:0]	CH3_ADC_ADJUST_E[7:0]									
0x1BB	ADC_OFF4_E	[15:8]	RESERVED		CH4_ADC_ADJUST_E[13:8]						0x0000	R/W
		[7:0]	CH4_ADC_ADJUST_E[7:0]									
0x1BC	THRESH1_E	[15:8]	RESERVED			THRESH1_SHIFT_E					0x0000	R/W
		[7:0]	THRESH1_VALUE_E									
0x1C0	TS_CTRL_F	[15:8]	RESERVED		SAMPLE_TYPE_F			RESERVED	TIMESLOT_OFFSET_F[9:8]		0x1000	R/W
		[7:0]	TIMESLOT_OFFSET_F[7:0]									
0x1C1	TS_PATH_F	[15:8]	PRE_WIDTH_F				AMBIENT_CANCELLATION_F		GOUT_F	RESERVED	0x4020	R/W
		[7:0]	RESERVED	AFE_PATH_CFG_F								
0x1C2	INPUTS_F	[15:8]	INP4_SEL_F		INP3_SEL_F		INP2_SEL_F		INP1_SEL_F		0x0000	R/W
		[7:0]	INP34_F				INP12_F					
0x1C3	CATHODE_F	[15:8]	RESERVED	PRECON_F			RESERVED		AFE_VREF_AMB_SEL_F		0x0200	R/W
		[7:0]	VC1_AMB_SEL_F		VC1_PULSE_F		VC1_ALT_F		VC1_SEL_F			
0x1C4	AFE_TRIM1_F	[15:8]	AFE_TIA_SAT_DETECT_EN_F	RESERVED		AFE_BUFFER_GAIN_F		VREF_PULSE_F	AFE_TRIM_VREF_F		0x02C9	R/W
		[7:0]	VREF_PULSE_VAL_F		TIA_GAIN_CH2_F			TIA_GAIN_CH1_F				
0x1C5	AFE_TRIM2_F	[15:8]	RESERVED			AFE_BUFFER_CAP_F	RESERVED				0x0000	R/W
		[7:0]	RESERVED		TIA_GAIN_CH4_F			TIA_GAIN_CH3_F				

REGISTER SUMMARY

Table 23. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x1C6	AFE_DAC1_F	[15:8]	DAC_AMBIENT_CH1_F[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH1_F, Bit 0	DAC_LED_DC_CH1_F								
0x1C7	AFE_DAC2_F	[15:8]	DAC_AMBIENT_CH2_F[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH2_F, Bit 0	DAC_LED_DC_CH2_F								
0x1C8	LED_POW12_F	[15:8]	RESERVED	LED_CURRENT2_F							0x0000	R/W
		[7:0]	RESERVED	LED_CURRENT1_F								
0x1C9	LED_MODE_F	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LED_DRIVESIDE2_F		LED_DRIVESIDE1_F		RESERVED		LED_MODE2_F	LED_MODE1_F		
0x1CA	COUNTS_F	[15:8]	NUM_INT_F								0x0101	R/W
		[7:0]	NUM_REPEAT_F									
0x1CB	PERIOD_F	[15:8]	RESERVED	COARSE_LOOP_WIDTH_F	MOD_TYPE_F		RESERVED		MIN_PERIOD_F[9:8]		0x0000	R/W
		[7:0]	MIN_PERIOD_F[7:0]									
0x1CC	LED_PULSE1_F	[15:8]	LED_WIDTH_F								0x0210	R/W
		[7:0]	LED_OFFSET_F									
0x1CD	AFE_DAC3_F	[15:8]	DAC_AMBIENT_CH3_F[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH3_F, Bit 0	DAC_LED_DC_CH3_F								
0x1CE	AFE_DAC4_F	[15:8]	DAC_AMBIENT_CH4_F[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH4_F, Bit 0	DAC_LED_DC_CH4_F								
0x1CF	THRESH0_F	[15:8]	RESERVED			THRESH0_SHIFT_F					0x0000	R/W
		[7:0]	THRESH0_VALUE_F									
0x1D0	MOD_PULSE_F	[15:8]	MOD_WIDTH_F								0x0001	R/W
		[7:0]	MOD_OFFSET_F									
0x1D1	PATTERN1_F	[15:8]	LED_DISABLE_F				MOD_DISABLE_F				0x0000	R/W
		[7:0]	SUBTRACT_F				AFE_SWAP_F					
0x1D2	THRESH_CFG_F	[15:8]	RESERVED					THRESH1_DIR_F	THRESH1_TYPE_F		0x0000	R/W
		[7:0]	RESERVED					THRESH0_DIR_F	THRESH0_TYPE_F			

REGISTER SUMMARY

Table 23. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x1D3	ADC_OFF1_F	[15:8]	RESERVED		CH1_ADC_ADJUST_F[13:8]						0x0000	R/W
		[7:0]	CH1_ADC_ADJUST_F[7:0]									
0x1D4	ADC_OFF2_F	[15:8]	RESERVED		CH2_ADC_ADJUST_F[13:8]						0x0000	R/W
		[7:0]	CH2_ADC_ADJUST_F[7:0]									
0x1D5	DATA1_F	[15:8]	DARK_SHIFT_F					DARK_SIZE_F			0x0003	R/W
		[7:0]	SIGNAL_SHIFT_F					SIGNAL_SIZE_F				
0x1D6	DATA2_F	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LIT_SHIFT_F					LIT_SIZE_F				
0x1D7	DECIMATE_F	[15:8]	CHANNEL_EN_F		RESERVED			SUBSAMPLE_RATIO_F[6:4]			0x0010	R/W
		[7:0]	SUBSAMPLE_RATIO_F[3:0]				RESERVED					
0x1D8	DIGINT_LIT_F	[15:8]	RESERVED							LIT_OFFSET_F, Bit 8	0x0026	R/W
		[7:0]	LIT_OFFSET_F[7:0]									
0x1D9	DIGINT_DARK_F	[15:8]	DARK2_OFFSET_F[8:1]								0x0086	R/W
		[7:0]	DARK2_OFFSET_F, Bit 0	DARK1_OFFSET_F								
0x1DA	ADC_OFF3_F	[15:8]	RESERVED		CH3_ADC_ADJUST_F[13:8]						0x0000	R/W
		[7:0]	CH3_ADC_ADJUST_F[7:0]									
0x1DB	ADC_OFF4_F	[15:8]	RESERVED		CH4_ADC_ADJUST_F[13:8]						0x0000	R/W
		[7:0]	CH4_ADC_ADJUST_F[7:0]									
0x1DC	THRESH1_F	[15:8]	RESERVED			THRESH1_SHIFT_F					0x0000	R/W
		[7:0]	THRESH1_VALUE_F									
0x1E0	TS_CTRL_G	[15:8]	RESERVED		SAMPLE_TYPE_G			RESERVED	TIMESLOT_OFFSET_G[9:8]		0x1000	R/W
		[7:0]	TIMESLOT_OFFSET_G[7:0]									
0x1E1	TS_PATH_G	[15:8]	PRE_WIDTH_G				AMBIENT_CANCELLATION_G		GOUT_G	RESERVED	0x4020	R/W
		[7:0]	RESERVED	AFE_PATH_CFG_G								
0x1E2	INPUTS_G	[15:8]	INP4_SEL_G		INP3_SEL_G		INP2_SEL_G		INP1_SEL_G		0x0000	R/W
		[7:0]	INP34_G				INP12_G					
0x1E3	CATHODE_G	[15:8]	RESERVED	PRECON_G			RESERVED		AFE_VREF_AMB_SEL_G		0x0200	R/W
		[7:0]	VC1_AMB_SEL_G		VC1_PULSE_G		VC1_ALT_G		VC1_SEL_G			
0x1E4	AFE_TRIM1_G	[15:8]	AFE_TIA_SAT_DETECT_EN_G	RESERVED		AFE_BUFFER_GAIN_G		VREF_PULSE_G	AFE_TRIM_VREF_G		0x02C9	R/W
		[7:0]	VREF_PULSE_VAL_G		TIA_GAIN_CH2_G			TIA_GAIN_CH1_G				
0x1E5	AFE_TRIM2_G	[15:8]	RESERVED			AFE_BUFFER_CAP_G	RESERVED				0x0000	R/W
		[7:0]	RESERVED		TIA_GAIN_CH4_G			TIA_GAIN_CH3_G				

REGISTER SUMMARY

Table 23. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x1E6	AFE_DAC1_G	[15:8]	DAC_AMBIENT_CH1_G[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH1_G, Bit 0	DAC_LED_DC_CH1_G								
0x1E7	AFE_DAC2_G	[15:8]	DAC_AMBIENT_CH2_G[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH2_G, Bit 0	DAC_LED_DC_CH2_G								
0x1E8	LED_POW12_G	[15:8]	RESERVED	LED_CURRENT2_G							0x0000	R/W
		[7:0]	RESERVED	LED_CURRENT1_G								
0x1E9	LED_MODE_G	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LED_DRIVESIDE2_G		LED_DRIVESIDE1_G		RESERVED		LED_MODE2_G	LED_MODE1_G		
0x1EA	COUNTS_G	[15:8]	NUM_INT_G								0x0101	R/W
		[7:0]	NUM_REPEAT_G									
0x1EB	PERIOD_G	[15:8]	RESERVED	COARSE_LOOP_WIDTH_G	MOD_TYPE_G		RESERVED		MIN_PERIOD_G[9:8]		0x0000	R/W
		[7:0]	MIN_PERIOD_G[7:0]									
0x1EC	LED_PULSE1_G	[15:8]	LED_WIDTH_G								0x0210	R/W
		[7:0]	LED_OFFSET_G									
0x1ED	AFE_DAC3_G	[15:8]	DAC_AMBIENT_CH3_G[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH3_G, Bit 0	DAC_LED_DC_CH3_G								
0x1EE	AFE_DAC4_G	[15:8]	DAC_AMBIENT_CH4_G[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH4_G, Bit 0	DAC_LED_DC_CH4_G								
0x1EF	THRESH0_G	[15:8]	RESERVED			THRESH0_SHIFT_G					0x0000	R/W
		[7:0]	THRESH0_VALUE_G									
0x1F0	MOD_PULSE_G	[15:8]	MOD_WIDTH_G								0x0001	R/W
		[7:0]	MOD_OFFSET_G									
0x1F1	PATTERN1_G	[15:8]	LED_DISABLE_G				MOD_DISABLE_G				0x0000	R/W
		[7:0]	SUBTRACT_G				AFE_SWAP_G					
0x1F2	THRESH_CFG_G	[15:8]	RESERVED					THRESH1_DIR_G	THRESH1_TYPE_G		0x0000	R/W
		[7:0]	RESERVED					THRESH0_DIR_G	THRESH0_TYPE_G			

REGISTER SUMMARY

Table 23. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x1F3	ADC_OFF1_G	[15:8]	RESERVED		CH1_ADC_ADJUST_G[13:8]						0x0000	R/W
		[7:0]	CH1_ADC_ADJUST_G[7:0]									
0x1F4	ADC_OFF2_G	[15:8]	RESERVED		CH2_ADC_ADJUST_G[13:8]						0x0000	R/W
		[7:0]	CH2_ADC_ADJUST_G[7:0]									
0x1F5	DATA1_G	[15:8]	DARK_SHIFT_G					DARK_SIZE_G			0x0003	R/W
		[7:0]	SIGNAL_SHIFT_G					SIGNAL_SIZE_G				
0x1F6	DATA2_G	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LIT_SHIFT_G					LIT_SIZE_G				
0x1F7	DECIMATE_G	[15:8]	CHANNEL_EN_G		RESERVED			SUBSAMPLE_RATIO_G[6:4]			0x0010	R/W
		[7:0]	SUBSAMPLE_RATIO_G[3:0]				RESERVED					
0x1F8	DIGINT_LIT_G	[15:8]	RESERVED							LIT_OFFSET_G, Bit 8	0x0026	R/W
		[7:0]	LIT_OFFSET_G[7:0]									
0x1F9	DIGINT_DARK_G	[15:8]	DARK2_OFFSET_G[8:1]								0x0086	R/W
		[7:0]	DARK2_OFFSET_G, Bit 0	DARK1_OFFSET_G								
0x1FA	ADC_OFF3_G	[15:8]	RESERVED		CH3_ADC_ADJUST_G[13:8]						0x0000	R/W
		[7:0]	CH3_ADC_ADJUST_G[7:0]									
0x1FB	ADC_OFF4_G	[15:8]	RESERVED		CH4_ADC_ADJUST_G[13:8]						0x0000	R/W
		[7:0]	CH4_ADC_ADJUST_G[7:0]									
0x1FC	THRESH1_G	[15:8]	RESERVED			THRESH1_SHIFT_G					0x0000	R/W
		[7:0]	THRESH1_VALUE_G									
0x200	TS_CTRL_H	[15:8]	RESERVED		SAMPLE_TYPE_H			RESERVED	TIMESLOT_OFFSET_H[9:8]		0x1000	R/W
		[7:0]	TIMESLOT_OFFSET_H[7:0]									
0x201	TS_PATH_H	[15:8]	PRE_WIDTH_H				AMBIENT_CANCELLATION_H		GOUT_H	RESERVED	0x4020	R/W
		[7:0]	RESERVED	AFE_PATH_CFG_H								
0x202	INPUTS_H	[15:8]	INP4_SEL_H		INP3_SEL_H		INP2_SEL_H		INP1_SEL_H		0x0000	R/W
		[7:0]	INP34_H				INP12_H					
0x203	CATHODE_H	[15:8]	RESERVED	PRECON_H			RESERVED		AFE_VREF_AMB_SEL_H		0x0200	R/W
		[7:0]	VC1_AMB_SEL_H		VC1_PULSE_H		VC1_ALT_H		VC1_SEL_H			
0x204	AFE_TRIM1_H	[15:8]	AFE_TIA_SAT_DETECT_EN_H	RESERVED		AFE_BUFFER_GAIN_H		VREF_PULSE_H	AFE_TRIM_VREF_H		0x02C9	R/W
		[7:0]	VREF_PULSE_VAL_H		TIA_GAIN_CH2_H			TIA_GAIN_CH1_H				
0x205	AFE_TRIM2_H	[15:8]	RESERVED			AFE_BUFFER_CAP_H	RESERVED				0x0000	R/W
		[7:0]	RESERVED		TIA_GAIN_CH4_H			TIA_GAIN_CH3_H				

REGISTER SUMMARY

Table 23. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x206	AFE_DAC1_H	[15:8]	DAC_AMBIENT_CH1_H[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH1_H, Bit 0	DAC_LED_DC_CH1_H								
0x207	AFE_DAC2_H	[15:8]	DAC_AMBIENT_CH2_H[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH2_H, Bit 0	DAC_LED_DC_CH2_H								
0x208	LED_POW12_H	[15:8]	RESERVED	LED_CURRENT2_H							0x0000	R/W
		[7:0]	RESERVED	LED_CURRENT1_H								
0x209	LED_MODE_H	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LED_DRIVESIDE2_H		LED_DRIVESIDE1_H		RESERVED		LED_MODE2_H	LED_MODE1_H		
0x20A	COUNTS_H	[15:8]	NUM_INT_H								0x0101	R/W
		[7:0]	NUM_REPEAT_H									
0x20B	PERIOD_H	[15:8]	RESERVED	COARSE_LOOP_WIDTH_H	MOD_TYPE_H		RESERVED		MIN_PERIOD_H[9:8]		0x0000	R/W
		[7:0]	MIN_PERIOD_H[7:0]									
0x20C	LED_PULSE1_H	[15:8]	LED_WIDTH_H								0x0210	R/W
		[7:0]	LED_OFFSET_H									
0x20D	AFE_DAC3_H	[15:8]	DAC_AMBIENT_CH3_H[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH3_H, Bit 0	DAC_LED_DC_CH3_H								
0x20E	AFE_DAC4_H	[15:8]	DAC_AMBIENT_CH4_H[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH4_H, Bit 0	DAC_LED_DC_CH4_H								
0x20F	THRESH0_H	[15:8]	RESERVED			THRESH0_SHIFT_H					0x0000	R/W
		[7:0]	THRESH0_VALUE_H									
0x210	MOD_PULSE_H	[15:8]	MOD_WIDTH_H								0x0001	R/W
		[7:0]	MOD_OFFSET_H									
0x211	PATTERN1_H	[15:8]	LED_DISABLE_H				MOD_DISABLE_H				0x0000	R/W
		[7:0]	SUBTRACT_H				AFE_SWAP_H					
0x212	THRESH_CFG_H	[15:8]	RESERVED					THRESH1_DIR_H	THRESH1_TYPE_H		0x0000	R/W
		[7:0]	RESERVED					THRESH0_DIR_H	THRESH0_TYPE_H			

REGISTER SUMMARY

Table 23. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x213	ADC_OFF 1_H	[15:8]	RESERVED		CH1_ADC_ADJUST_H[13:8]						0x0000	R/W
		[7:0]	CH1_ADC_ADJUST_H[7:0]									
0x214	ADC_OFF 2_H	[15:8]	RESERVED		CH2_ADC_ADJUST_H[13:8]						0x0000	R/W
		[7:0]	CH2_ADC_ADJUST_H[7:0]									
0x215	DATA1_H	[15:8]	DARK_SHIFT_H					DARK_SIZE_H			0x0003	R/W
		[7:0]	SIGNAL_SHIFT_H					SIGNAL_SIZE_H				
0x216	DATA2_H	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LIT_SHIFT_H					LIT_SIZE_H				
0x217	DECIMAT E_H	[15:8]	CHANNEL_EN_H		RESERVED			SUBSAMPLE_RATIO_H[6:4]			0x0010	R/W
		[7:0]	SUBSAMPLE_RATIO_H[3:0]				RESERVED					
0x218	DIGINT_LI T_H	[15:8]	RESERVED							LIT_OFFSE T_H, Bit 8	0x0026	R/W
		[7:0]	LIT_OFFSET_H[7:0]									
0x219	DIGINT_D ARK_H	[15:8]	DARK2_OFFSET_H[8:1]								0x0086	R/W
		[7:0]	DARK2_O FFSET_H, Bit 0	DARK1_OFFSET_H								
0x21A	ADC_OFF 3_H	[15:8]	RESERVED		CH3_ADC_ADJUST_H[13:8]						0x0000	R/W
		[7:0]	CH3_ADC_ADJUST_H[7:0]									
0x21B	ADC_OFF 4_H	[15:8]	RESERVED		CH4_ADC_ADJUST_H[13:8]						0x0000	R/W
		[7:0]	CH4_ADC_ADJUST_H[7:0]									
0x21C	THRESH1 _H	[15:8]	RESERVED			THRESH1_SHIFT_H					0x0000	R/W
		[7:0]	THRESH1_VALUE_H									
0x220	TS_CTRL_ I	[15:8]	RESERVED		SAMPLE_TYPE_I			RESERVED	TIMESLOT_OFFSET_I[9:8]		0x1000	R/W
		[7:0]	TIMESLOT_OFFSET_I[7:0]									
0x221	TS_PATH_ I	[15:8]	PRE_WIDTH_I				AMBIENT_CANCELLATIO N_I		GOUT_I	RESERVED	0x4020	R/W
		[7:0]	RESERVE D	AFE_PATH_CFG_I								
0x222	INPUTS_I	[15:8]	INP4_SEL_I		INP3_SEL_I		INP2_SEL_I		INP1_SEL_I		0x0000	R/W
		[7:0]	INP34_I				INP12_I					
0x223	CATHODE _I	[15:8]	RESERVE D	PRECON_I			RESERVED		AFE_VREF_AMB_SEL_I		0x0200	R/W
		[7:0]	VC1_AMB_SEL_I		VC1_PULSE_I		VC1_ALT_I		VC1_SEL_I			
0x224	AFE_TRIM 1_I	[15:8]	AFE_TIA_ SAT_DET ECT_EN_I	RESERVED		AFE_BUFFER_GAIN_I		VREF_PUL SE_I	AFE_TRIM_VREF_I		0x02C9	R/W
		[7:0]	VREF_PULSE_VAL_I		TIA_GAIN_CH2_I			TIA_GAIN_CH1_I				
0x225	AFE_TRIM 2_I	[15:8]	RESERVED			AFE_BUFF ER_CAP_I	RESERVED				0x0000	R/W
		[7:0]	RESERVED		TIA_GAIN_CH4_I			TIA_GAIN_CH3_I				

REGISTER SUMMARY

Table 23. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x226	AFE_DAC1_I	[15:8]	DAC_AMBIENT_CH1_I[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH1_I, Bit 0	DAC_LED_DC_CH1_I								
0x227	AFE_DAC2_I	[15:8]	DAC_AMBIENT_CH2_I[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH2_I, Bit 0	DAC_LED_DC_CH2_I								
0x228	LED_POW12_I	[15:8]	RESERVED	LED_CURRENT2_I							0x0000	R/W
		[7:0]	RESERVED	LED_CURRENT1_I								
0x229	LED_MODE_I	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LED_DRIVESIDE2_I		LED_DRIVESIDE1_I		RESERVED		LED_MODE2_I	LED_MODE1_I		
0x22A	COUNTS_I	[15:8]	NUM_INT_I								0x0101	R/W
		[7:0]	NUM_REPEAT_I									
0x22B	PERIOD_I	[15:8]	RESERVED	COARSE_LOOP_WIDTH_I	MOD_TYPE_I		RESERVED		MIN_PERIOD_I[9:8]		0x0000	R/W
		[7:0]	MIN_PERIOD_I[7:0]									
0x22C	LED_PULSE1_I	[15:8]	LED_WIDTH_I								0x0210	R/W
		[7:0]	LED_OFFSET_I									
0x22D	AFE_DAC3_I	[15:8]	DAC_AMBIENT_CH3_I[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH3_I, Bit 0	DAC_LED_DC_CH3_I								
0x22E	AFE_DAC4_I	[15:8]	DAC_AMBIENT_CH4_I[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH4_I, Bit 0	DAC_LED_DC_CH4_I								
0x22F	THRESH0_I	[15:8]	RESERVED			THRESH0_SHIFT_I					0x0000	R/W
		[7:0]	THRESH0_VALUE_I									
0x230	MOD_PULSE_I	[15:8]	MOD_WIDTH_I								0x0001	R/W
		[7:0]	MOD_OFFSET_I									
0x231	PATTERN1_I	[15:8]	LED_DISABLE_I				MOD_DISABLE_I				0x0000	R/W
		[7:0]	SUBTRACT_I				AFE_SWAP_I					
0x232	THRESH_CFG_I	[15:8]	RESERVED					THRESH1_DIR_I	THRESH1_TYPE_I		0x0000	R/W
		[7:0]	RESERVED					THRESH0_DIR_I	THRESH0_TYPE_I			

REGISTER SUMMARY

Table 23. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x233	ADC_OFF1_I	[15:8]	RESERVED		CH1_ADC_ADJUST_I[13:8]						0x0000	R/W
		[7:0]	CH1_ADC_ADJUST_I[7:0]									
0x234	ADC_OFF2_I	[15:8]	RESERVED		CH2_ADC_ADJUST_I[13:8]						0x0000	R/W
		[7:0]	CH2_ADC_ADJUST_I[7:0]									
0x235	DATA1_I	[15:8]	DARK_SHIFT_I					DARK_SIZE_I			0x0003	R/W
		[7:0]	SIGNAL_SHIFT_I					SIGNAL_SIZE_I				
0x236	DATA2_I	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LIT_SHIFT_I					LIT_SIZE_I				
0x237	DECIMATE_I	[15:8]	CHANNEL_EN_I		RESERVED			SUBSAMPLE_RATIO_I[6:4]			0x0010	R/W
		[7:0]	SUBSAMPLE_RATIO_I[3:0]				RESERVED					
0x238	DIGINT_LIT_I	[15:8]	RESERVED							LIT_OFFSET_I, Bit 8	0x0026	R/W
		[7:0]	LIT_OFFSET_I[7:0]									
0x239	DIGINT_DARK_I	[15:8]	DARK2_OFFSET_I[8:1]								0x0086	R/W
		[7:0]	DARK2_OFFSET_I, Bit 0	DARK1_OFFSET_I								
0x23A	ADC_OFF3_I	[15:8]	RESERVED		CH3_ADC_ADJUST_I[13:8]						0x0000	R/W
		[7:0]	CH3_ADC_ADJUST_I[7:0]									
0x23B	ADC_OFF4_I	[15:8]	RESERVED		CH4_ADC_ADJUST_I[13:8]						0x0000	R/W
		[7:0]	CH4_ADC_ADJUST_I[7:0]									
0x23C	THRESH1_I	[15:8]	RESERVED			THRESH1_SHIFT_I					0x0000	R/W
		[7:0]	THRESH1_VALUE_I									
0x240	TS_CTRL_J	[15:8]	RESERVED		SAMPLE_TYPE_J			RESERVED	TIMESLOT_OFFSET_J[9:8]		0x1000	R/W
		[7:0]	TIMESLOT_OFFSET_J[7:0]									
0x241	TS_PATH_J	[15:8]	PRE_WIDTH_J				AMBIENT_CANCELLATION_J		GOUT_J	RESERVED	0x4020	R/W
		[7:0]	RESERVED	AFE_PATH_CFG_J								
0x242	INPUTS_J	[15:8]	INP4_SEL_J		INP3_SEL_J		INP2_SEL_J		INP1_SEL_J		0x0000	R/W
		[7:0]	INP34_J				INP12_J					
0x243	CATHODE_J	[15:8]	RESERVED	PRECON_J			RESERVED		AFE_VREF_AMB_SEL_J		0x0200	R/W
		[7:0]	VC1_AMB_SEL_J		VC1_PULSE_J		VC1_ALT_J		VC1_SEL_J			
0x244	AFE_TRIM1_J	[15:8]	AFE_TIA_SAT_DETECT_EN_J	RESERVED		AFE_BUFFER_GAIN_J		VREF_PULSE_J	AFE_TRIM_VREF_J		0x02C9	R/W
		[7:0]	VREF_PULSE_VAL_J		TIA_GAIN_CH2_J			TIA_GAIN_CH1_J				
0x245	AFE_TRIM2_J	[15:8]	RESERVED			AFE_BUFFER_CAP_J	RESERVED				0x0000	R/W
		[7:0]	RESERVED		TIA_GAIN_CH4_J			TIA_GAIN_CH3_J				

REGISTER SUMMARY

Table 23. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x246	AFE_DAC1_J	[15:8]	DAC_AMBIENT_CH1_J[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH1_J, Bit 0	DAC_LED_DC_CH1_J								
0x247	AFE_DAC2_J	[15:8]	DAC_AMBIENT_CH2_J[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH2_J, Bit 0	DAC_LED_DC_CH2_J								
0x248	LED_POW12_J	[15:8]	RESERVED	LED_CURRENT2_J							0x0000	R/W
		[7:0]	RESERVED	LED_CURRENT1_J								
0x249	LED_MODE_J	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LED_DRIVESIDE2_J		LED_DRIVESIDE1_J		RESERVED		LED_MODE2_J	LED_MODE1_J		
0x24A	COUNTS_J	[15:8]	NUM_INT_J								0x0101	R/W
		[7:0]	NUM_REPEAT_J									
0x24B	PERIOD_J	[15:8]	RESERVED	COARSE_LOOP_WIDTH_J	MOD_TYPE_J		RESERVED		MIN_PERIOD_J[9:8]		0x0000	R/W
		[7:0]	MIN_PERIOD_J[7:0]									
0x24C	LED_PULSE1_J	[15:8]	LED_WIDTH_J								0x0210	R/W
		[7:0]	LED_OFFSET_J									
0x24D	AFE_DAC3_J	[15:8]	DAC_AMBIENT_CH3_J[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH3_J, Bit 0	DAC_LED_DC_CH3_J								
0x24E	AFE_DAC4_J	[15:8]	DAC_AMBIENT_CH4_J[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH4_J, Bit 0	DAC_LED_DC_CH4_J								
0x24F	THRESH0_J	[15:8]	RESERVED			THRESH0_SHIFT_J					0x0000	R/W
		[7:0]	THRESH0_VALUE_J									
0x250	MOD_PULSE_J	[15:8]	MOD_WIDTH_J								0x0001	R/W
		[7:0]	MOD_OFFSET_J									
0x251	PATTERN1_J	[15:8]	LED_DISABLE_J				MOD_DISABLE_J				0x0000	R/W
		[7:0]	SUBTRACT_J				AFE_SWAP_J					
0x252	THRESH_CFG_J	[15:8]	RESERVED					THRESH1_DIR_J	THRESH1_TYPE_J		0x0000	R/W
		[7:0]	RESERVED					THRESH0_DIR_J	THRESH0_TYPE_J			

REGISTER SUMMARY

Table 23. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x253	ADC_OFF1_J	[15:8]	RESERVED		CH1_ADC_ADJUST_J[13:8]						0x0000	R/W
		[7:0]	CH1_ADC_ADJUST_J[7:0]									
0x254	ADC_OFF2_J	[15:8]	RESERVED		CH2_ADC_ADJUST_J[13:8]						0x0000	R/W
		[7:0]	CH2_ADC_ADJUST_J[7:0]									
0x255	DATA1_J	[15:8]	DARK_SHIFT_J					DARK_SIZE_J			0x0003	R/W
		[7:0]	SIGNAL_SHIFT_J					SIGNAL_SIZE_J				
0x256	DATA2_J	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LIT_SHIFT_J					LIT_SIZE_J				
0x257	DECIMATE_J	[15:8]	CHANNEL_EN_J		RESERVED			SUBSAMPLE_RATIO_J[6:4]			0x0010	R/W
		[7:0]	SUBSAMPLE_RATIO_J[3:0]				RESERVED					
0x258	DIGINT_LIT_J	[15:8]	RESERVED							LIT_OFFSET_J, Bit 8	0x0026	R/W
		[7:0]	LIT_OFFSET_J[7:0]									
0x259	DIGINT_DARK_J	[15:8]	DARK2_OFFSET_J[8:1]								0x0086	R/W
		[7:0]	DARK2_OFFSET_J, Bit 0	DARK1_OFFSET_J								
0x25A	ADC_OFF3_J	[15:8]	RESERVED		CH3_ADC_ADJUST_J[13:8]						0x0000	R/W
		[7:0]	CH3_ADC_ADJUST_J[7:0]									
0x25B	ADC_OFF4_J	[15:8]	RESERVED		CH4_ADC_ADJUST_J[13:8]						0x0000	R/W
		[7:0]	CH4_ADC_ADJUST_J[7:0]									
0x25C	THRESH1_J	[15:8]	RESERVED			THRESH1_SHIFT_J					0x0000	R/W
		[7:0]	THRESH1_VALUE_J									
0x260	TS_CTRL_K	[15:8]	RESERVED		SAMPLE_TYPE_K			RESERVED	TIMESLOT_OFFSET_K[9:8]		0x1000	R/W
		[7:0]	TIMESLOT_OFFSET_K[7:0]									
0x261	TS_PATH_K	[15:8]	PRE_WIDTH_K				AMBIENT_CANCELLATION_K		GOUT_K	RESERVED	0x4020	R/W
		[7:0]	RESERVED	AFE_PATH_CFG_K								
0x262	INPUTS_K	[15:8]	INP4_SEL_K		INP3_SEL_K		INP2_SEL_K		INP1_SEL_K		0x0000	R/W
		[7:0]	INP34_K				INP12_K					
0x263	CATHODE_K	[15:8]	RESERVED	PRECON_K			RESERVED		AFE_VREF_AMB_SEL_K		0x0200	R/W
		[7:0]	VC1_AMB_SEL_K		VC1_PULSE_K		VC1_ALT_K		VC1_SEL_K			
0x264	AFE_TRIM1_K	[15:8]	AFE_TIA_SAT_DETECT_EN_K	RESERVED		AFE_BUFFER_GAIN_K		VREF_PULSE_K	AFE_TRIM_VREF_K		0x02C9	R/W
		[7:0]	VREF_PULSE_VAL_K		TIA_GAIN_CH2_K			TIA_GAIN_CH1_K				
0x265	AFE_TRIM2_K	[15:8]	RESERVED			AFE_BUFFER_CAP_K	RESERVED				0x0000	R/W
		[7:0]	RESERVED		TIA_GAIN_CH4_K			TIA_GAIN_CH3_K				

REGISTER SUMMARY

Table 23. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x266	AFE_DAC1_K	[15:8]	DAC_AMBIENT_CH1_K[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH1_K, Bit 0	DAC_LED_DC_CH1_K								
0x267	AFE_DAC2_K	[15:8]	DAC_AMBIENT_CH2_K[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH2_K, Bit 0	DAC_LED_DC_CH2_K								
0x268	LED_POW12_K	[15:8]	RESERVED	LED_CURRENT2_K							0x0000	R/W
		[7:0]	RESERVED	LED_CURRENT1_K								
0x269	LED_MODE_K	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LED_DRIVESIDE2_K		LED_DRIVESIDE1_K		RESERVED		LED_MODE2_K	LED_MODE1_K		
0x26A	COUNTS_K	[15:8]	NUM_INT_K								0x0101	R/W
		[7:0]	NUM_REPEAT_K									
0x26B	PERIOD_K	[15:8]	RESERVED	COARSE_LOOP_WIDTH_K	MOD_TYPE_K		RESERVED		MIN_PERIOD_K[9:8]		0x0000	R/W
		[7:0]	MIN_PERIOD_K[7:0]									
0x26C	LED_PULSE1_K	[15:8]	LED_WIDTH_K								0x0210	R/W
		[7:0]	LED_OFFSET_K									
0x26D	AFE_DAC3_K	[15:8]	DAC_AMBIENT_CH3_K[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH3_K, Bit 0	DAC_LED_DC_CH3_K								
0x26E	AFE_DAC4_K	[15:8]	DAC_AMBIENT_CH4_K[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH4_K, Bit 0	DAC_LED_DC_CH4_K								
0x26F	THRESH0_K	[15:8]	RESERVED			THRESH0_SHIFT_K					0x0000	R/W
		[7:0]	THRESH0_VALUE_K									
0x270	MOD_PULSE_K	[15:8]	MOD_WIDTH_K								0x0001	R/W
		[7:0]	MOD_OFFSET_K									
0x271	PATTERN1_K	[15:8]	LED_DISABLE_K				MOD_DISABLE_K				0x0000	R/W
		[7:0]	SUBTRACT_K				AFE_SWAP_K					
0x272	THRESH_CFG_K	[15:8]	RESERVED					THRESH1_DIR_K	THRESH1_TYPE_K		0x0000	R/W
		[7:0]	RESERVED					THRESH0_DIR_K	THRESH0_TYPE_K			

REGISTER SUMMARY

Table 23. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x273	ADC_OFF1_K	[15:8]	RESERVED		CH1_ADC_ADJUST_K[13:8]						0x0000	R/W
		[7:0]	CH1_ADC_ADJUST_K[7:0]									
0x274	ADC_OFF2_K	[15:8]	RESERVED		CH2_ADC_ADJUST_K[13:8]						0x0000	R/W
		[7:0]	CH2_ADC_ADJUST_K[7:0]									
0x275	DATA1_K	[15:8]	DARK_SHIFT_K					DARK_SIZE_K			0x0003	R/W
		[7:0]	SIGNAL_SHIFT_K					SIGNAL_SIZE_K				
0x276	DATA2_K	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LIT_SHIFT_K					LIT_SIZE_K				
0x277	DECIMATE_K	[15:8]	CHANNEL_EN_K		RESERVED			SUBSAMPLE_RATIO_K[6:4]			0x0010	R/W
		[7:0]	SUBSAMPLE_RATIO_K[3:0]				RESERVED					
0x278	DIGINT_LIT_K	[15:8]	RESERVED							LIT_OFFSET_K, Bit 8	0x0026	R/W
		[7:0]	LIT_OFFSET_K[7:0]									
0x279	DIGINT_DARK_K	[15:8]	DARK2_OFFSET_K[8:1]								0x0086	R/W
		[7:0]	DARK2_OFFSET_K, Bit 0	DARK1_OFFSET_K								
0x27A	ADC_OFF3_K	[15:8]	RESERVED		CH3_ADC_ADJUST_K[13:8]						0x0000	R/W
		[7:0]	CH3_ADC_ADJUST_K[7:0]									
0x27B	ADC_OFF4_K	[15:8]	RESERVED		CH4_ADC_ADJUST_K[13:8]						0x0000	R/W
		[7:0]	CH4_ADC_ADJUST_K[7:0]									
0x27C	THRESH1_K	[15:8]	RESERVED			THRESH1_SHIFT_K					0x0000	R/W
		[7:0]	THRESH1_VALUE_K									
0x280	TS_CTRL_L	[15:8]	RESERVED		SAMPLE_TYPE_L			RESERVED	TIMESLOT_OFFSET_L[9:8]		0x1000	R/W
		[7:0]	TIMESLOT_OFFSET_L[7:0]									
0x281	TS_PATH_L	[15:8]	PRE_WIDTH_L				AMBIENT_CANCELLATION_L		GOUT_L	RESERVED	0x4020	R/W
		[7:0]	RESERVED	AFE_PATH_CFG_L								
0x282	INPUTS_L	[15:8]	INP4_SEL_L		INP3_SEL_L		INP2_SEL_L		INP1_SEL_L		0x0000	R/W
		[7:0]	INP34_L				INP12_L					
0x283	CATHODE_L	[15:8]	RESERVED	PRECON_L			RESERVED		AFE_VREF_AMB_SEL_L		0x0200	R/W
		[7:0]	VC1_AMB_SEL_L		VC1_PULSE_L		VC1_ALT_L		VC1_SEL_L			
0x284	AFE_TRIM1_L	[15:8]	AFE_TIA_SAT_DETECT_EN_L	RESERVED		AFE_BUFFER_GAIN_L		VREF_PULSE_L	AFE_TRIM_VREF_L		0x02C9	R/W
		[7:0]	VREF_PULSE_VAL_L		TIA_GAIN_CH2_L			TIA_GAIN_CH1_L				
0x285	AFE_TRIM2_L	[15:8]	RESERVED			AFE_BUFFER_CAP_L	RESERVED				0x0000	R/W
		[7:0]	RESERVED		TIA_GAIN_CH4_L			TIA_GAIN_CH3_L				

REGISTER SUMMARY

Table 23. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x286	AFE_DAC 1_L	[15:8]	DAC_AMBIENT_CH1_L[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH1_L, Bit 0	DAC_LED_DC_CH1_L								
0x287	AFE_DAC 2_L	[15:8]	DAC_AMBIENT_CH2_L[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH2_L, Bit 0	DAC_LED_DC_CH2_L								
0x288	LED_POW 12_L	[15:8]	RESERVED	LED_CURRENT2_L							0x0000	R/W
		[7:0]	RESERVED	LED_CURRENT1_L								
0x289	LED_MOD E_L	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LED_DRIVESIDE2_L		LED_DRIVESIDE1_L		RESERVED		LED_MODE 2_L	LED_MODE 1_L		
0x28A	COUNTS_ L	[15:8]	NUM_INT_L								0x0101	R/W
		[7:0]	NUM_REPEAT_L									
0x28B	PERIOD_L	[15:8]	RESERVED	COARSE_LOOP_WIDTH_L	MOD_TYPE_L		RESERVED		MIN_PERIOD_L[9:8]		0x0000	R/W
		[7:0]	MIN_PERIOD_L[7:0]									
0x28C	LED_PUL SE1_L	[15:8]	LED_WIDTH_L								0x0210	R/W
		[7:0]	LED_OFFSET_L									
0x28D	AFE_DAC 3_L	[15:8]	DAC_AMBIENT_CH3_L[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH3_L, Bit 0	DAC_LED_DC_CH3_L								
0x28E	AFE_DAC 4_L	[15:8]	DAC_AMBIENT_CH4_L[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH4_L, Bit 0	DAC_LED_DC_CH4_L								
0x28F	THRESH0 _L	[15:8]	RESERVED			THRESH0_SHIFT_L					0x0000	R/W
		[7:0]	THRESH0_VALUE_L									
0x290	MOD_PUL SE_L	[15:8]	MOD_WIDTH_L								0x0001	R/W
		[7:0]	MOD_OFFSET_L									
0x291	PATTERN 1_L	[15:8]	LED_DISABLE_L				MOD_DISABLE_L				0x0000	R/W
		[7:0]	SUBTRACT_L				AFE_SWAP_L					
0x292	THRESH_ CFG_L	[15:8]	RESERVED					THRESH1_DIR_L	THRESH1_TYPE_L		0x0000	R/W
		[7:0]	RESERVED					THRESH0_DIR_L	THRESH0_TYPE_L			

REGISTER SUMMARY

Table 23. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x293	ADC_OFF1_L	[15:8]	RESERVED		CH1_ADC_ADJUST_L[13:8]						0x0000	R/W
		[7:0]	CH1_ADC_ADJUST_L[7:0]									
0x294	ADC_OFF2_L	[15:8]	RESERVED		CH2_ADC_ADJUST_L[13:8]						0x0000	R/W
		[7:0]	CH2_ADC_ADJUST_L[7:0]									
0x295	DATA1_L	[15:8]	DARK_SHIFT_L					DARK_SIZE_L			0x0003	R/W
		[7:0]	SIGNAL_SHIFT_L					SIGNAL_SIZE_L				
0x296	DATA2_L	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LIT_SHIFT_L					LIT_SIZE_L				
0x297	DECIMATE_L	[15:8]	CHANNEL_EN_L		RESERVED			SUBSAMPLE_RATIO_L[6:4]			0x0010	R/W
		[7:0]	SUBSAMPLE_RATIO_L[3:0]				RESERVED					
0x298	DIGINT_LIT_L	[15:8]	RESERVED							LIT_OFFSET_L, Bit 8	0x0026	R/W
		[7:0]	LIT_OFFSET_L[7:0]									
0x299	DIGINT_DARK_L	[15:8]	DARK2_OFFSET_L[8:1]								0x0086	R/W
		[7:0]	DARK2_OFFSET_L, Bit 0	DARK1_OFFSET_L								
0x29A	ADC_OFF3_L	[15:8]	RESERVED		CH3_ADC_ADJUST_L[13:8]						0x0000	R/W
		[7:0]	CH3_ADC_ADJUST_L[7:0]									
0x29B	ADC_OFF4_L	[15:8]	RESERVED		CH4_ADC_ADJUST_L[13:8]						0x0000	R/W
		[7:0]	CH4_ADC_ADJUST_L[7:0]									
0x29C	THRESH1_L	[15:8]	RESERVED			THRESH1_SHIFT_L					0x0000	R/W
		[7:0]	THRESH1_VALUE_L									
0x2A0	BIOZ_AFECON_A	[15:8]	RESERVED		BIOZ_DACREF_LPMODE_A	BIOZ_REFNORM_A	BIOZ_TIMESLOT_OFFSET_A[9:6]				0x0000	R/W
		[7:0]	BIOZ_TIMESLOT_OFFSET_A[5:0]						BIOZ_TIAEN_A	BIOZ_EXCITATION_TYPE_A		
0x2A1	BIOZ_WGFCW_LOW_A	[15:8]	BIOZ_SINEFCW_L_A[15:8]								0x0000	R/W
		[7:0]	BIOZ_SINEFCW_L_A[7:0]									
0x2A2	BIOZ_WGFCW_HI_A	[15:8]	BIOZ_DATA_SELECTION_A	BIOZ_NCHAN_ALT_A			BIOZ_PCHAN_ALT_A			RESERVED	0x0000	R/W
		[7:0]	RESERVED				BIOZ_SINEFCW_H_A					
0x2A3	BIOZ_WGPHASE_A	[15:8]	BIOZ_SINE_PHASE_OFFSET_A[15:8]								0x0000	R/W
		[7:0]	BIOZ_SINE_PHASE_OFFSET_A[7:0]									
0x2A4	BIOZ_DFTPHASE_A	[15:8]	BIOZ_DFT_PHASE_OFFSET_A[15:8]								0x0000	R/W
		[7:0]	BIOZ_DFT_PHASE_OFFSET_A[7:0]									

REGISTER SUMMARY

Table 23. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x2A5	BIOZ_WG OFFSET_ A	[15:8]	RESERVED				BIOZ_SINE_OFFSET_A[11:8]				0x0000	R/W
		[7:0]	BIOZ_SINE_OFFSET_A[7:0]									
0x2A6	BIOZ_WG AMPLITU DE_A	[15:8]	RESERVED					BIOZ_SINEAMPLITUDE_A[10:8]			0x0600	R/W
		[7:0]	BIOZ_SINEAMPLITUDE_A[7:0]									
0x2A7	BIOZ_DAC CON_A	[15:8]	RESERVED		BIOZ_EXBU FEN_A	BIOZ_DACBUFBW_A			BIOZ_BW20 0KEN_A	BIOZ_BW50 KEN_A	0x120D	R/W
		[7:0]	BIOZ_RATE_DIV_A									
0x2A8	BIOZ_ADC _LEVEL_A	[15:8]	BIOZ_ADC_LEVEL_H_A								0xFF00	R/W
		[7:0]	BIOZ_ADC_LEVEL_L_A									
0x2A9	BIOZ_DC_ EXCITATI ON_A	[15:8]	BIOZ_DCL O_POLARI TY_IP_A	BIOZ_DCLO _POLARITY _IN_A	BIOZ_DCLO _L_EN_A	BIOZ_DCLO_L_MAG_A				BIOZ_DCLO _M_EN_A	0x0000	R/W
		[7:0]	BIOZ_DCLO_M_MAG_A			BIOZ_DCLO _H_EN_A	BIOZ_DCLO_H_MAG_A					
0x2AA	BIOZ_ANA _CTRL1_A	[15:8]	BIOZ_TIA_RGAIN_A				BIOZ_TIA_CGAIN_A				0x1730	R/W
		[7:0]	BIOZ_EXCBUF_LPMODE _A		BIOZ_CHOP_OFF_IN_A		BIOZ_TIA_LPMODE_A		BIOZ_RX_L PMODE_A	BIOZ_DAC_ RCF_LOWB W_EN_A		
0x2AB	BIOZ_ANA _CTRL2_A	[15:8]	BIOZ_TIA_ VREF_SE L_A	BIOZ_CM_S W_A	BIOZ_NCHAN_A			BIOZ_PCHAN_A			0x0000	R/W
		[7:0]	BIOZ_TSW_A				BIOZ_DSW_A					
0x2AC	BIOZ_ANA _CTRL3_A	[15:8]	BIOZ_CHOP_OFF_EXC_ A		BIOZ_PGA_GAIN_A		BIOZ_TIA_ECG_A			BIOZ_EXCB UF_ECG_A, Bit 2	0xC000	R/W
		[7:0]	BIOZ_EXCBUF_ECG_A[1 :0]		BIOZ_DCLO _IP_EN_A	BIOZ_DCLO _IN_EN_A	BIOZ_CURRENT_LIMIT_A		BIOZ_RINT_SW_A			
0x2AD	BIOZ_ADC FILTERCO N_A	[15:8]	RESERVED				BIOZ_ADC_PERIOD_A[5:2]				0x0004	R/W
		[7:0]	BIOZ_ADC_PERIOD_A[1: 0]		BIOZ_AVRGNUM_A		BIOZ_AVRG EN_A	BIOZ_SINC 3BYP_A	BIOZ_SINC3OSR_A			
0x2AE	BIOZ_DFT CON_A	[15:8]	RESERVED								0x0009	R/W
		[7:0]	BIOZ_DAT A_SIZE_A	BIOZ_DFT_ TYPE_A	BIOZ_WG_ DFT_DIFF_ PHASE_EN _A	BIOZ_HANN INGEN_A	BIOZ_DFTNUM_A					
0x2AF	BIOZ_ADC _CONV_D LY_A	[15:8]	BIOZ_PRE_WIDTH_A			BIOZ_PRECON_SEL_A		BIOZ_SUBSAMPLE_RATIO_A[6:4]			0x0011	R/W
		[7:0]	BIOZ_SUBSAMPLE_RATIO_A[3:0]				BIOZ_PREC ON_RES_A	BIOZ_ADC_CONV_DLY_A				
0x2B0	BIOZ_AFE CON_B	[15:8]	RESERVED		BIOZ_DACR EF_LPMOD E_B	BIOZ_REFN ORM_B	BIOZ_TIMESLOT_OFFSET_B[9:6]				0x0000	R/W

REGISTER SUMMARY

Table 23. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
		[7:0]	BIOZ_TIMESLOT_OFFSET_B[5:0]						BIOZ_TIAEN_B	BIOZ_EXCITATION_TYPE_B		
0x2B1	BIOZ_WGFCW_LOW_B	[15:8]	BIOZ_SINEFCW_L_B[15:8]								0x0000	R/W
		[7:0]	BIOZ_SINEFCW_L_B[7:0]									
0x2B2	BIOZ_WGFCW_HI_B	[15:8]	BIOZ_DATA_SELECTION_B	BIOZ_NCHAN_ALT_B			BIOZ_PCHAN_ALT_B			RESERVED	0x0000	R/W
		[7:0]	RESERVED				BIOZ_SINEFCW_H_B					
0x2B3	BIOZ_WGPHASE_B	[15:8]	BIOZ_SINE_PHASE_OFFSET_B[15:8]								0x0000	R/W
		[7:0]	BIOZ_SINE_PHASE_OFFSET_B[7:0]									
0x2B4	BIOZ_DFTPHASE_B	[15:8]	BIOZ_DFT_PHASE_OFFSET_B[15:8]								0x0000	R/W
		[7:0]	BIOZ_DFT_PHASE_OFFSET_B[7:0]									
0x2B5	BIOZ_WGOFFSET_B	[15:8]	RESERVED				BIOZ_SINE_OFFSET_B[11:8]				0x0000	R/W
		[7:0]	BIOZ_SINE_OFFSET_B[7:0]									
0x2B6	BIOZ_WGAMPLITUDE_B	[15:8]	RESERVED					BIOZ_SINEAMPLITUDE_B[10:8]			0x0600	R/W
		[7:0]	BIOZ_SINEAMPLITUDE_B[7:0]									
0x2B7	BIOZ_DACCON_B	[15:8]	RESERVED		BIOZ_EXBUFEN_B	BIOZ_DACBUFBW_B			BIOZ_BW200KEN_B	BIOZ_BW50KEN_B	0x120D	R/W
		[7:0]	BIOZ_RATE_DIV_B									
0x2B8	BIOZ_ADC_LEVEL_B	[15:8]	BIOZ_ADC_LEVEL_H_B								0xFF00	R/W
		[7:0]	BIOZ_ADC_LEVEL_L_B									
0x2B9	BIOZ_DC_EXCITATION_B	[15:8]	BIOZ_DCLO_POLARITY_IP_B	BIOZ_DCLO_POLARITY_IN_B	BIOZ_DCLO_L_EN_B	BIOZ_DCLO_L_MAG_B				BIOZ_DCLO_M_EN_B	0x0000	R/W
		[7:0]	BIOZ_DCLO_M_MAG_B			BIOZ_DCLO_H_EN_B	BIOZ_DCLO_H_MAG_B					
0x2BA	BIOZ_ANA_CTRL1_B	[15:8]	BIOZ_TIA_RGAIN_B				BIOZ_TIA_CGAIN_B				0x1730	R/W
		[7:0]	BIOZ_EXCBUF_LPMODE_B		BIOZ_CHOP_OFF_IN_B		BIOZ_TIA_LPMODE_B		BIOZ_RX_LPMODE_B	BIOZ_DAC_RCF_LOWBW_EN_B		
0x2BB	BIOZ_ANA_CTRL2_B	[15:8]	BIOZ_TIA_VREF_SEL_B	BIOZ_CM_SW_B	BIOZ_NCHAN_B			BIOZ_PCHAN_B			0x0000	R/W
		[7:0]	BIOZ_TSW_B				BIOZ_DSW_B					
0x2BC	BIOZ_ANA_CTRL3_B	[15:8]	BIOZ_CHOP_OFF_EXC_B		BIOZ_PGA_GAIN_B		BIOZ_TIA_ECG_B			BIOZ_EXCBUF_ECG_B, Bit 2	0xC000	R/W
		[7:0]	BIOZ_EXCBUF_ECG_B[1:0]		BIOZ_DCLO_IP_EN_B	BIOZ_DCLO_IN_EN_B	BIOZ_CURRENT_LIMIT_B		BIOZ_RINT_SW_B			

REGISTER SUMMARY

Table 23. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x2BD	BIOZ_ADC FILTERCO N_B	[15:8]	RESERVED				BIOZ_ADC_PERIOD_B[5:2]				0x0004	R/W
		[7:0]	BIOZ_ADC_PERIOD_B[1: 0]		BIOZ_AVRGNUM_B		BIOZ_AVRG EN_B	BIOZ_SINC 3BYP_B	BIOZ_SINC3OSR_B			
0x2BE	BIOZ_DFT CON_B	[15:8]	RESERVED								0x0009	R/W
		[7:0]	BIOZ_DAT A_SIZE_B	BIOZ_DFT_ TYPE_B	BIOZ_WG_ DFT_DIFF_ PHASE_EN _B	BIOZ_HANN INGEN_B	BIOZ_DFTNUM_B					
0x2BF	BIOZ_ADC _CONV_D LY_B	[15:8]	BIOZ_PRE_WIDTH_B			BIOZ_PRECON_SEL_B		BIOZ_SUBSAMPLE_RATIO_B[6:4]			0x0011	R/W
		[7:0]	BIOZ_SUBSAMPLE_RATIO_B[3:0]				BIOZ_PREC ON_RES_B	BIOZ_ADC_CONV_DLY_B				
0x2C0	BIOZ_AFE CON_C	[15:8]	RESERVED		BIOZ_DACR EF_LPMOD E_C	BIOZ_REFN ORM_C	BIOZ_TIMESLOT_OFFSET_C[9:6]				0x0000	R/W
		[7:0]	BIOZ_TIMESLOT_OFFSET_C[5:0]						BIOZ_TIAE N_C	BIOZ_EXCI TATION_TY PE_C		
0x2C1	BIOZ_WG FCW_LO W_C	[15:8]	BIOZ_SINEFCW_L_C[15:8]								0x0000	R/W
		[7:0]	BIOZ_SINEFCW_L_C[7:0]									
0x2C2	BIOZ_WG FCW_HI_ C	[15:8]	BIOZ_DAT A_SELEC TION_C	BIOZ_NCHAN_ALT_C			BIOZ_PCHAN_ALT_C			RESERVED	0x0000	R/W
		[7:0]	RESERVED				BIOZ_SINEFCW_H_C					
0x2C3	BIOZ_WG PHASE_C	[15:8]	BIOZ_SINE_PHASE_OFFSET_C[15:8]								0x0000	R/W
		[7:0]	BIOZ_SINE_PHASE_OFFSET_C[7:0]									
0x2C4	BIOZ_DFT PHASE_C	[15:8]	BIOZ_DFT_PHASE_OFFSET_C[15:8]								0x0000	R/W
		[7:0]	BIOZ_DFT_PHASE_OFFSET_C[7:0]									
0x2C5	BIOZ_WG OFFSET_ C	[15:8]	RESERVED				BIOZ_SINE_OFFSET_C[11:8]				0x0000	R/W
		[7:0]	BIOZ_SINE_OFFSET_C[7:0]									
0x2C6	BIOZ_WG AMPLITU DE_C	[15:8]	RESERVED					BIOZ_SINEAMPLITUDE_C[10:8]			0x0600	R/W
		[7:0]	BIOZ_SINEAMPLITUDE_C[7:0]									
0x2C7	BIOZ_DAC CON_C	[15:8]	RESERVED		BIOZ_EXBU FEN_C	BIOZ_DACBUFBW_C			BIOZ_BW20 0KEN_C	BIOZ_BW50 KEN_C	0x120D	R/W
		[7:0]	BIOZ_RATE_DIV_C									
0x2C8	BIOZ_ADC _LEVEL_C	[15:8]	BIOZ_ADC_LEVEL_H_C								0xFF00	R/W
		[7:0]	BIOZ_ADC_LEVEL_L_C									

REGISTER SUMMARY

Table 23. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x2C9	BIOZ_DC_EXCITATION_C	[15:8]	BIOZ_DCLO_POLARITY_IP_C	BIOZ_DCLO_POLARITY_IN_C	BIOZ_DCLO_L_EN_C	BIOZ_DCLO_L_MAG_C				BIOZ_DCLO_M_EN_C	0x0000	R/W
		[7:0]	BIOZ_DCLO_M_MAG_C			BIOZ_DCLO_H_EN_C	BIOZ_DCLO_H_MAG_C					
0x2CA	BIOZ_ANA_CTRL1_C	[15:8]	BIOZ_TIA_RGAIN_C				BIOZ_TIA_CGAIN_C				0x1730	R/W
		[7:0]	BIOZ_EXCBUF_LPMODE_C		BIOZ_CHOP_OFF_IN_C		BIOZ_TIA_LPMODE_C		BIOZ_RX_LPMODE_C	BIOZ_DAC_RCF_LOWBW_EN_C		
0x2CB	BIOZ_ANA_CTRL2_C	[15:8]	BIOZ_TIA_VREF_SEL_C	BIOZ_CM_SW_C	BIOZ_NCHAN_C		BIOZ_PCHAN_C				0x0000	R/W
		[7:0]	BIOZ_TSW_C				BIOZ_DSW_C					
0x2CC	BIOZ_ANA_CTRL3_C	[15:8]	BIOZ_CHOP_OFF_EXC_C		BIOZ_PGA_GAIN_C		BIOZ_TIA_ECG_C			BIOZ_EXCBUF_ECG_C, Bit 2	0xC000	R/W
		[7:0]	BIOZ_EXCBUF_ECG_C[1:0]		BIOZ_DCLO_IP_EN_C	BIOZ_DCLO_IN_EN_C	BIOZ_CURRENT_LIMIT_C		BIOZ_RINT_SW_C			
0x2CD	BIOZ_ADCFILTERCON_C	[15:8]	RESERVED				BIOZ_ADC_PERIOD_C[5:2]				0x0004	R/W
		[7:0]	BIOZ_ADC_PERIOD_C[1:0]		BIOZ_AVRGNUM_C		BIOZ_AVRGEN_C	BIOZ_SINC3BYP_C	BIOZ_SINC3OSR_C			
0x2CE	BIOZ_DFTCON_C	[15:8]	RESERVED								0x0009	R/W
		[7:0]	BIOZ_DATA_SIZE_C	BIOZ_DFT_TYPE_C	BIOZ_WG_DFT_DIFF_PHASE_EN_C	BIOZ_HANNINGEN_C	BIOZ_DFTNUM_C					
0x2CF	BIOZ_ADC_CONV_DLY_C	[15:8]	BIOZ_PRE_WIDTH_C			BIOZ_PRECON_SEL_C	BIOZ_SUBSAMPLE_RATIO_C[6:4]				0x0011	R/W
		[7:0]	BIOZ_SUBSAMPLE_RATIO_C[3:0]				BIOZ_PRECON_RES_C	BIOZ_ADC_CONV_DLY_C				
0x2D0	BIOZ_AFECON_D	[15:8]	RESERVED		BIOZ_DACREF_LPMODE_D	BIOZ_REFNORM_D	BIOZ_TIMESLOT_OFFSET_D[9:6]				0x0000	R/W
		[7:0]	BIOZ_TIMESLOT_OFFSET_D[5:0]						BIOZ_TIAEN_D	BIOZ_EXCITATION_TYPE_D		
0x2D1	BIOZ_WGFCW_LOW_D	[15:8]	BIOZ_SINEFCW_L_D[15:8]								0x0000	R/W
		[7:0]	BIOZ_SINEFCW_L_D[7:0]									
0x2D2	BIOZ_WGFCW_HI_D	[15:8]	BIOZ_DATA_SELECTION_D	BIOZ_NCHAN_ALT_D			BIOZ_PCHAN_ALT_D			RESERVED	0x0000	R/W
		[7:0]	RESERVED				BIOZ_SINEFCW_H_D					
0x2D3	BIOZ_WGPHASE_D	[15:8]	BIOZ_SINE_PHASE_OFFSET_D[15:8]								0x0000	R/W
		[7:0]	BIOZ_SINE_PHASE_OFFSET_D[7:0]									

REGISTER SUMMARY

Table 23. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x2D4	BIOZ_DFT PHASE_D	[15:8]	BIOZ_DFT_PHASE_OFFSET_D[15:8]								0x0000	R/W
		[7:0]	BIOZ_DFT_PHASE_OFFSET_D[7:0]									
0x2D5	BIOZ_WG OFFSET_ D	[15:8]	RESERVED				BIOZ_SINE_OFFSET_D[11:8]				0x0000	R/W
		[7:0]	BIOZ_SINE_OFFSET_D[7:0]									
0x2D6	BIOZ_WG AMPLITU DE_D	[15:8]	RESERVED					BIOZ_SINEAMPLITUDE_D[10:8]			0x0600	R/W
		[7:0]	BIOZ_SINEAMPLITUDE_D[7:0]									
0x2D7	BIOZ_DAC CON_D	[15:8]	RESERVED		BIOZ_EXBU FEN_D	BIOZ_DACBUFBW_D			BIOZ_BW20 0KEN_D	BIOZ_BW50 KEN_D	0x120D	R/W
		[7:0]	BIOZ_RATE_DIV_D									
0x2D8	BIOZ_ADC _LEVEL_D	[15:8]	BIOZ_ADC_LEVEL_H_D								0xFF00	R/W
		[7:0]	BIOZ_ADC_LEVEL_L_D									
0x2D9	BIOZ_DC_ EXCITATI ON_D	[15:8]	BIOZ_DCLO_POLARI TY_IP_D	BIOZ_DCLO _POLARITY _IN_D	BIOZ_DCLO _L_EN_D	BIOZ_DCLO_L_MAG_D				BIOZ_DCLO _M_EN_D	0x0000	R/W
		[7:0]	BIOZ_DCLO_M_MAG_D			BIOZ_DCLO _H_EN_D	BIOZ_DCLO_H_MAG_D					
0x2DA	BIOZ_ANA _CTRL1_D	[15:8]	BIOZ_TIA_RGAIN_D				BIOZ_TIA_CGAIN_D				0x1730	R/W
		[7:0]	BIOZ_EXCBUF_LPMODE _D		BIOZ_CHOP_OFF_IN_D		BIOZ_TIA_LPMODE_D		BIOZ_RX_L PMODE_D	BIOZ_DAC_ RCF_LOWB W_EN_D		
0x2DB	BIOZ_ANA _CTRL2_D	[15:8]	BIOZ_TIA_ VREF_SE L_D	BIOZ_CM_S W_D	BIOZ_NCHAN_D			BIOZ_PCHAN_D			0x0000	R/W
		[7:0]	BIOZ_TSW_D				BIOZ_DSW_D					
0x2DC	BIOZ_ANA _CTRL3_D	[15:8]	BIOZ_CHOP_OFF_EXC_ D		BIOZ_PGA_GAIN_D		BIOZ_TIA_ECG_D			BIOZ_EXCB UF_ECG_D[2]	0xC000	R/W
		[7:0]	BIOZ_EXCBUF_ECG_D[1 :0]		BIOZ_DCLO _IP_EN_D	BIOZ_DCLO _IN_EN_D	BIOZ_CURRENT_LIMIT_D		BIOZ_RINT_SW_D			
0x2DD	BIOZ_ADC FILTERCO N_D	[15:8]	RESERVED				BIOZ_ADC_PERIOD_D[5:2]				0x0004	R/W
		[7:0]	BIOZ_ADC_PERIOD_D[1: 0]		BIOZ_AVRGNUM_D		BIOZ_AVRG EN_D	BIOZ_SINC 3BYP_D	BIOZ_SINC3OSR_D			
0x2DE	BIOZ_DFT CON_D	[15:8]	RESERVED								0x0009	R/W
		[7:0]	BIOZ_DAT A_SIZE_D	BIOZ_DFT_ TYPE_D	BIOZ_WG_ DFT_DIFF_ PHASE_EN _D	BIOZ_HANN INGEN_D	BIOZ_DFTNUM_D					
0x2DF	BIOZ_ADC _CONV_D LY_D	[15:8]	BIOZ_PRE_WIDTH_D			BIOZ_PRECON_SEL_D		BIOZ_SUBSAMPLE_RATIO_D[6:4]			0x0011	R/W
		[7:0]	BIOZ_SUBSAMPLE_RATIO_D[3:0]				BIOZ_PREC ON_RES_D	BIOZ_ADC_CONV_DLY_D				

REGISTER SUMMARY

Table 23. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x2E0	BIOZ_AFECON_E	[15:8]	RESERVED		BIOZ_DACREF_LPMODE_E	BIOZ_REFNORM_E	BIOZ_TIMESLOT_OFFSET_E[9:6]				0x0000	R/W
		[7:0]	BIOZ_TIMESLOT_OFFSET_E[5:0]						BIOZ_TIAEN_E	BIOZ_EXCITATION_TYPE_E		
0x2E1	BIOZ_WGFCW_LOW_E	[15:8]	BIOZ_SINEFCW_L_E[15:8]								0x0000	R/W
		[7:0]	BIOZ_SINEFCW_L_E[7:0]									
0x2E2	BIOZ_WGFCW_HI_E	[15:8]	BIOZ_DATA_SELECTION_E	BIOZ_NCHAN_ALT_E			BIOZ_PCHAN_ALT_E			RESERVED	0x0000	R/W
		[7:0]	RESERVED				BIOZ_SINEFCW_H_E					
0x2E3	BIOZ_WGPHASE_E	[15:8]	BIOZ_SINE_PHASE_OFFSET_E[15:8]								0x0000	R/W
		[7:0]	BIOZ_SINE_PHASE_OFFSET_E[7:0]									
0x2E4	BIOZ_DFTPHASE_E	[15:8]	BIOZ_DFT_PHASE_OFFSET_E[15:8]								0x0000	R/W
		[7:0]	BIOZ_DFT_PHASE_OFFSET_E[7:0]									
0x2E5	BIOZ_WGOFFSET_E	[15:8]	RESERVED				BIOZ_SINE_OFFSET_E[11:8]				0x0000	R/W
		[7:0]	BIOZ_SINE_OFFSET_E[7:0]									
0x2E6	BIOZ_WGAMPLITUDE_E	[15:8]	RESERVED					BIOZ_SINEAMPLITUDE_E[10:8]			0x0600	R/W
		[7:0]	BIOZ_SINEAMPLITUDE_E[7:0]									
0x2E7	BIOZ_DACCON_E	[15:8]	RESERVED		BIOZ_EXBUFEN_E	BIOZ_DACBUFBW_E			BIOZ_BW200KEN_E	BIOZ_BW50KEN_E	0x120D	R/W
		[7:0]	BIOZ_RATE_DIV_E									
0x2E8	BIOZ_ADC_LEVEL_E	[15:8]	BIOZ_ADC_LEVEL_H_E								0xFF00	R/W
		[7:0]	BIOZ_ADC_LEVEL_L_E									
0x2E9	BIOZ_DC_EXCITATION_E	[15:8]	BIOZ_DCLO_POLARITY_IP_E	BIOZ_DCLO_POLARITY_IN_E	BIOZ_DCLO_L_EN_E	BIOZ_DCLO_L_MAG_E				BIOZ_DCLO_M_EN_E	0x0000	R/W
		[7:0]	BIOZ_DCLO_M_MAG_E			BIOZ_DCLO_H_EN_E	BIOZ_DCLO_H_MAG_E					
0x2EA	BIOZ_ANA_CTRL1_E	[15:8]	BIOZ_TIA_RGAIN_E				BIOZ_TIA_CGAIN_E				0x1730	R/W
		[7:0]	BIOZ_EXCBUF_LPMODE_E		BIOZ_CHOP_OFF_IN_E		BIOZ_TIA_LPMODE_E		BIOZ_RX_LPMODE_E	BIOZ_DAC_RCF_LOWBW_EN_E		
0x2EB	BIOZ_ANA_CTRL2_E	[15:8]	BIOZ_TIA_VREF_SEL_E	BIOZ_CM_SW_E	BIOZ_NCHAN_E			BIOZ_PCHAN_E			0x0000	R/W
		[7:0]	BIOZ_TSW_E				BIOZ_DSW_E					
0x2EC	BIOZ_ANA_CTRL3_E	[15:8]	BIOZ_CHOP_OFF_EXC_E		BIOZ_PGA_GAIN_E		BIOZ_TIA_ECG_E			BIOZ_EXCBUF_ECG_E, Bit 2	0xC000	R/W

REGISTER SUMMARY

Table 23. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
		[7:0]	BIOZ_EXCBUF_ECG_E[1:0]		BIOZ_DCLO_IP_EN_E	BIOZ_DCLO_IN_EN_E	BIOZ_CURRENT_LIMIT_E		BIOZ_RINT_SW_E			
0x2ED	BIOZ_ADCFILTERCON_E	[15:8]	RESERVED				BIOZ_ADC_PERIOD_E[5:2]				0x0004	R/W
		[7:0]	BIOZ_ADC_PERIOD_E[1:0]		BIOZ_AVRGNUM_E		BIOZ_AVRGEN_E	BIOZ_SINC3BYP_E	BIOZ_SINC3OSR_E			
0x2EE	BIOZ_DFTCON_E	[15:8]	RESERVED								0x0009	R/W
		[7:0]	BIOZ_DATA_SIZE_E	BIOZ_DFT_TYPE_E	BIOZ_WG_DFT_DIFF_PHASE_EN_E	BIOZ_HANNINGEN_E	BIOZ_DFTNUM_E					
0x2EF	BIOZ_ADC_CONV_DLY_E	[15:8]	BIOZ_PRE_WIDTH_E			BIOZ_PRECON_SEL_E	BIOZ_SUBSAMPLE_RATIO_E[6:4]				0x0011	R/W
		[7:0]	BIOZ_SUBSAMPLE_RATIO_E[3:0]				BIOZ_PRECON_RES_E	BIOZ_ADC_CONV_DLY_E				
0x2F0	BIOZ_AFECON_F	[15:8]	RESERVED		BIOZ_DACREF_LPMODE_F	BIOZ_REFNORM_F	BIOZ_TIMESLOT_OFFSET_F[9:6]				0x0000	R/W
		[7:0]	BIOZ_TIMESLOT_OFFSET_F[5:0]						BIOZ_TIAEN_F	BIOZ_EXCITATION_TYPE_F		
0x2F1	BIOZ_WGFCW_LOW_F	[15:8]	BIOZ_SINEFCW_L_F[15:8]								0x0000	R/W
		[7:0]	BIOZ_SINEFCW_L_F[7:0]									
0x2F2	BIOZ_WGFCW_HI_F	[15:8]	BIOZ_DATA_SELECTION_F	BIOZ_NCHAN_ALT_F			BIOZ_PCHAN_ALT_F			RESERVED	0x0000	R/W
		[7:0]	RESERVED				BIOZ_SINEFCW_H_F					
0x2F3	BIOZ_WGPHASE_F	[15:8]	BIOZ_SINE_PHASE_OFFSET_F[15:8]								0x0000	R/W
		[7:0]	BIOZ_SINE_PHASE_OFFSET_F[7:0]									
0x2F4	BIOZ_DFTPHASE_F	[15:8]	BIOZ_DFT_PHASE_OFFSET_F[15:8]								0x0000	R/W
		[7:0]	BIOZ_DFT_PHASE_OFFSET_F[7:0]									
0x2F5	BIOZ_WGOFFSET_F	[15:8]	RESERVED				BIOZ_SINE_OFFSET_F[11:8]				0x0000	R/W
		[7:0]	BIOZ_SINE_OFFSET_F[7:0]									
0x2F6	BIOZ_WGAMPLITUDE_F	[15:8]	RESERVED					BIOZ_SINEAMPLITUDE_F[10:8]			0x0600	R/W
		[7:0]	BIOZ_SINEAMPLITUDE_F[7:0]									
0x2F7	BIOZ_DACCON_F	[15:8]	RESERVED		BIOZ_EXBUFEN_F	BIOZ_DACBUFBW_F			BIOZ_BW200KEN_F	BIOZ_BW50KEN_F	0x120D	R/W
		[7:0]	BIOZ_RATE_DIV_F									
0x2F8	BIOZ_ADC_LEVEL_F	[15:8]	BIOZ_ADC_LEVEL_H_F								0xFF00	R/W
		[7:0]	BIOZ_ADC_LEVEL_L_F									

REGISTER SUMMARY

Table 23. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x2F9	BIOZ_DC_EXCITATION_F	[15:8]	BIOZ_DCLO_POLARITY_IP_F	BIOZ_DCLO_POLARITY_IN_F	BIOZ_DCLO_L_EN_F	BIOZ_DCLO_L_MAG_F				BIOZ_DCLO_M_EN_F	0x0000	R/W
		[7:0]	BIOZ_DCLO_M_MAG_F			BIOZ_DCLO_H_EN_F	BIOZ_DCLO_H_MAG_F					
0x2FA	BIOZ_ANA_CTRL1_F	[15:8]	BIOZ_TIA_RGAIN_F				BIOZ_TIA_CGAIN_F				0x1730	R/W
		[7:0]	BIOZ_EXCBUF_LPMODE_F		BIOZ_CHOP_OFF_IN_F		BIOZ_TIA_LPMODE_F		BIOZ_RX_LPMODE_F	BIOZ_DAC_RCF_LOWBW_EN_F		
0x2FB	BIOZ_ANA_CTRL2_F	[15:8]	BIOZ_TIA_VREF_SEL_F	BIOZ_CM_SW_F	BIOZ_NCHAN_F			BIOZ_PCHAN_F			0x0000	R/W
		[7:0]	BIOZ_TSW_F				BIOZ_DSW_F					
0x2FC	BIOZ_ANA_CTRL3_F	[15:8]	BIOZ_CHOP_OFF_EXC_F		BIOZ_PGA_GAIN_F		BIOZ_TIA_ECG_F			BIOZ_EXCBUF_ECG_F, Bit 2	0xC000	R/W
		[7:0]	BIOZ_EXCBUF_ECG_F[1:0]		BIOZ_DCLO_IP_EN_F	BIOZ_DCLO_IN_EN_F	BIOZ_CURRENT_LIMIT_F		BIOZ_RINT_SW_F			
0x2FD	BIOZ_ADCFILTERCON_F	[15:8]	RESERVED				BIOZ_ADC_PERIOD_F[5:2]				0x0004	R/W
		[7:0]	BIOZ_ADC_PERIOD_F[1:0]		BIOZ_AVRGNUM_F		BIOZ_AVRGEN_F	BIOZ_SINC3BYP_F	BIOZ_SINC3OSR_F			
0x2FE	BIOZ_DFTCON_F	[15:8]	RESERVED								0x0009	R/W
		[7:0]	BIOZ_DATA_SIZE_F	BIOZ_DFT_TYPE_F	BIOZ_WG_DFT_DIFF_PHASE_EN_F	BIOZ_HANNINGEN_F	BIOZ_DFTNUM_F					
0x2FF	BIOZ_ADC_CONV_DLY_F	[15:8]	BIOZ_PRE_WIDTH_F			BIOZ_PRECON_SEL_F		BIOZ_SUBSAMPLE_RATIO_F[6:4]			0x0011	R/W
		[7:0]	BIOZ_SUBSAMPLE_RATIO_F[3:0]				BIOZ_PRECON_RES_F	BIOZ_ADC_CONV_DLY_F				
0x300	BIOZ_AFECON_G	[15:8]	RESERVED		BIOZ_DACREF_LPMODE_G	BIOZ_REFNORM_G	BIOZ_TIMESLOT_OFFSET_G[9:6]				0x0000	R/W
		[7:0]	BIOZ_TIMESLOT_OFFSET_G[5:0]						BIOZ_TIAEN_G	BIOZ_EXCITATION_TYPE_G		
0x301	BIOZ_WGFCW_LOW_G	[15:8]	BIOZ_SINEFCW_L_G[15:8]								0x0000	R/W
		[7:0]	BIOZ_SINEFCW_L_G[7:0]									
0x302	BIOZ_WGFCW_HI_G	[15:8]	BIOZ_DATA_SELECTION_G	BIOZ_NCHAN_ALT_G			BIOZ_PCHAN_ALT_G			RESERVED	0x0000	R/W
		[7:0]	RESERVED				BIOZ_SINEFCW_H_G					
0x303	BIOZ_WGPHASE_G	[15:8]	BIOZ_SINE_PHASE_OFFSET_G[15:8]								0x0000	R/W
		[7:0]	BIOZ_SINE_PHASE_OFFSET_G[7:0]									

REGISTER SUMMARY

Table 23. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x304	BIOZ_DFT PHASE_G	[15:8]	BIOZ_DFT_PHASE_OFFSET_G[15:8]								0x0000	R/W
		[7:0]	BIOZ_DFT_PHASE_OFFSET_G[7:0]									
0x305	BIOZ_WG OFFSET_ G	[15:8]	RESERVED				BIOZ_SINE_OFFSET_G[11:8]				0x0000	R/W
		[7:0]	BIOZ_SINE_OFFSET_G[7:0]									
0x306	BIOZ_WG AMPLITU DE_G	[15:8]	RESERVED					BIOZ_SINEAMPLITUDE_G[10:8]			0x0600	R/W
		[7:0]	BIOZ_SINEAMPLITUDE_G[7:0]									
0x307	BIOZ_DAC CON_G	[15:8]	RESERVED		BIOZ_EXBU FEN_G	BIOZ_DACBUFBW_G			BIOZ_BW20 0KEN_G	BIOZ_BW50 KEN_G	0x120D	R/W
		[7:0]	BIOZ_RATE_DIV_G									
0x308	BIOZ_ADC _LEVEL_G	[15:8]	BIOZ_ADC_LEVEL_H_G								0xFF00	R/W
		[7:0]	BIOZ_ADC_LEVEL_L_G									
0x309	BIOZ_DC_ EXCITATI ON_G	[15:8]	BIOZ_DCLO_POLARI TY_IP_G	BIOZ_DCLO _POLARITY _IN_G	BIOZ_DCLO _L_EN_G	BIOZ_DCLO_L_MAG_G				BIOZ_DCLO _M_EN_G	0x0000	R/W
		[7:0]	BIOZ_DCLO_M_MAG_G			BIOZ_DCLO _H_EN_G	BIOZ_DCLO_H_MAG_G					
0x30A	BIOZ_ANA _CTRL1_ G	[15:8]	BIOZ_TIA_RGAIN_G				BIOZ_TIA_CGAIN_G				0x1730	R/W
		[7:0]	BIOZ_EXCBUF_LPMODE _G		BIOZ_CHOP_OFF_IN_G		BIOZ_TIA_LPMODE_G		BIOZ_RX_L PMODE_G	BIOZ_DAC_ RCF_LOWB W_EN_G		
0x30B	BIOZ_ANA _CTRL2_ G	[15:8]	BIOZ_TIA_ VREF_SE L_G	BIOZ_CM_S W_G	BIOZ_NCHAN_G			BIOZ_PCHAN_G			0x0000	R/W
		[7:0]	BIOZ_TSW_G				BIOZ_DSW_G					
0x30C	BIOZ_ANA _CTRL3_ G	[15:8]	BIOZ_CHOP_OFF_EXC_ G		BIOZ_PGA_GAIN_G		BIOZ_TIA_ECG_G			BIOZ_EXCB UF_ECG_G, Bit 2	0xC000	R/W
		[7:0]	BIOZ_EXCBUF_ECG_G[1:0]		BIOZ_DCLO _IP_EN_G	BIOZ_DCLO _IN_EN_G	BIOZ_CURRENT_LIMIT_G		BIOZ_RINT_SW_G			
0x30D	BIOZ_ADC FILTERCO N_G	[15:8]	RESERVED				BIOZ_ADC_PERIOD_G[5:2]				0x0004	R/W
		[7:0]	BIOZ_ADC_PERIOD_G[1 :0]		BIOZ_AVRGNUM_G		BIOZ_AVRG EN_G	BIOZ_SINC 3BYP_G	BIOZ_SINC3OSR_G			
0x30E	BIOZ_DFT CON_G	[15:8]	RESERVED								0x0009	R/W
		[7:0]	BIOZ_DAT A_SIZE_G	BIOZ_DFT_ TYPE_G	BIOZ_WG_ DFT_DIFF_ PHASE_EN _G	BIOZ_HANN INGEN_G	BIOZ_DFTNUM_G					
0x30F	BIOZ_ADC _CONV_D LY_G	[15:8]	BIOZ_PRE_WIDTH_G			BIOZ_PRECON_SEL_G		BIOZ_SUBSAMPLE_RATIO_G[6:4]			0x0011	R/W

REGISTER SUMMARY

Table 23. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
		[7:0]	BIOZ_SUBSAMPLE_RATIO_G[3:0]				BIOZ_PRECON_RES_G	BIOZ_ADC_CONV_DLY_G				
0x310	BIOZ_AFECON_H	[15:8]	RESERVED		BIOZ_DACREF_LPMODE_H	BIOZ_REFNORM_H	BIOZ_TIMESLOT_OFFSET_H[9:6]				0x0000	R/W
		[7:0]	BIOZ_TIMESLOT_OFFSET_H[5:0]						BIOZ_TIAEN_H	BIOZ_EXCITATION_TYPE_H		
0x311	BIOZ_WGFCW_LOW_H	[15:8]	BIOZ_SINEFCW_L_H[15:8]								0x0000	R/W
		[7:0]	BIOZ_SINEFCW_L_H[7:0]									
0x312	BIOZ_WGFCW_HI_H	[15:8]	BIOZ_DATA_SELECTION_H	BIOZ_NCHAN_ALT_H			BIOZ_PCHAN_ALT_H			RESERVED	0x0000	R/W
		[7:0]	RESERVED				BIOZ_SINEFCW_H_H					
0x313	BIOZ_WGPHASE_H	[15:8]	BIOZ_SINE_PHASE_OFFSET_H[15:8]								0x0000	R/W
		[7:0]	BIOZ_SINE_PHASE_OFFSET_H[7:0]									
0x314	BIOZ_DFTPHASE_H	[15:8]	BIOZ_DFT_PHASE_OFFSET_H[15:8]								0x0000	R/W
		[7:0]	BIOZ_DFT_PHASE_OFFSET_H[7:0]									
0x315	BIOZ_WGOFFSET_H	[15:8]	RESERVED				BIOZ_SINE_OFFSET_H[11:8]				0x0000	R/W
		[7:0]	BIOZ_SINE_OFFSET_H[7:0]									
0x316	BIOZ_WGAMPLITUDE_H	[15:8]	RESERVED					BIOZ_SINEAMPLITUDE_H[10:8]			0x0600	R/W
		[7:0]	BIOZ_SINEAMPLITUDE_H[7:0]									
0x317	BIOZ_DACCON_H	[15:8]	RESERVED		BIOZ_EXBUFEN_H	BIOZ_DACBUFBW_H			BIOZ_BW200KEN_H	BIOZ_BW50KEN_H	0x120D	R/W
		[7:0]	BIOZ_RATE_DIV_H									
0x318	BIOZ_ADC_LEVEL_H	[15:8]	BIOZ_ADC_LEVEL_H_H								0xFF00	R/W
		[7:0]	BIOZ_ADC_LEVEL_L_H									
0x319	BIOZ_DC_EXCITATION_H	[15:8]	BIOZ_DCLO_POLARITY_IP_H	BIOZ_DCLO_POLARITY_IN_H	BIOZ_DCLO_L_EN_H	BIOZ_DCLO_L_MAG_H				BIOZ_DCLO_M_EN_H	0x0000	R/W
		[7:0]	BIOZ_DCLO_M_MAG_H			BIOZ_DCLO_H_EN_H	BIOZ_DCLO_H_MAG_H					
0x31A	BIOZ_ANA_CTRL1_H	[15:8]	BIOZ_TIA_RGAIN_H				BIOZ_TIA_CGAIN_H				0x1730	R/W
		[7:0]	BIOZ_EXCBUF_LPMODE_H		BIOZ_CHOP_OFF_IN_H		BIOZ_TIA_LPMODE_H		BIOZ_RX_LPMODE_H	BIOZ_DAC_RCF_LOWBW_EN_H		
0x31B	BIOZ_ANA_CTRL2_H	[15:8]	BIOZ_TIA_VREF_SEL_H	BIOZ_CM_SW_H	BIOZ_NCHAN_H			BIOZ_PCHAN_H			0x0000	R/W
		[7:0]	BIOZ_TSW_H				BIOZ_DSW_H					

REGISTER SUMMARY

Table 23. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x31C	BIOZ_ANA_CTRL3_H	[15:8]	BIOZ_CHOP_OFF_EXC_H		BIOZ_PGA_GAIN_H		BIOZ_TIA_ECG_H			BIOZ_EXCBUF_ECG_H, Bit 2	0xC000	R/W
		[7:0]	BIOZ_EXCBUF_ECG_H[1:0]		BIOZ_DCLO_IP_EN_H	BIOZ_DCLO_IN_EN_H	BIOZ_CURRENT_LIMIT_H		BIOZ_RINT_SW_H			
0x31D	BIOZ_ADCFILTERCON_H	[15:8]	RESERVED				BIOZ_ADC_PERIOD_H[5:2]				0x0004	R/W
		[7:0]	BIOZ_ADC_PERIOD_H[1:0]		BIOZ_AVRGNUM_H		BIOZ_AVRGEN_H	BIOZ_SINC3BYP_H	BIOZ_SINC3OSR_H			
0x31E	BIOZ_DFTCON_H	[15:8]	RESERVED								0x0009	R/W
		[7:0]	BIOZ_DATA_SIZE_H	BIOZ_DFT_TYPE_H	BIOZ_WG_DFT_DIFF_PHASE_EN_H	BIOZ_HANNINGEN_H	BIOZ_DFTNUM_H					
0x31F	BIOZ_ADC_CONV_DLY_H	[15:8]	BIOZ_PRE_WIDTH_H			BIOZ_PRECON_SEL_H	BIOZ_SUBSAMPLE_RATIO_H[6:4]				0x0011	R/W
		[7:0]	BIOZ_SUBSAMPLE_RATIO_H[3:0]				BIOZ_PRECON_RES_H	BIOZ_ADC_CONV_DLY_H				
0x320	BIOZ_AFECON_I	[15:8]	RESERVED		BIOZ_DACREF_LPMODE_I	BIOZ_REFNORM_I	BIOZ_TIMESLOT_OFFSET_I[9:6]				0x0000	R/W
		[7:0]	BIOZ_TIMESLOT_OFFSET_I[5:0]						BIOZ_TIAEN_I	BIOZ_EXCITATION_TYPE_I		
0x321	BIOZ_WGFCW_LOW_I	[15:8]	BIOZ_SINEFCW_L_I[15:8]								0x0000	R/W
		[7:0]	BIOZ_SINEFCW_L_I[7:0]									
0x322	BIOZ_WGFCW_HI_I	[15:8]	BIOZ_DATA_SELECTION_I	BIOZ_NCHAN_ALT_I			BIOZ_PCHAN_ALT_I			RESERVED	0x0000	R/W
		[7:0]	RESERVED				BIOZ_SINEFCW_H_I					
0x323	BIOZ_WGPHASE_I	[15:8]	BIOZ_SINE_PHASE_OFFSET_I[15:8]								0x0000	R/W
		[7:0]	BIOZ_SINE_PHASE_OFFSET_I[7:0]									
0x324	BIOZ_DFTPHASE_I	[15:8]	BIOZ_DFT_PHASE_OFFSET_I[15:8]								0x0000	R/W
		[7:0]	BIOZ_DFT_PHASE_OFFSET_I[7:0]									
0x325	BIOZ_WGOFFSET_I	[15:8]	RESERVED				BIOZ_SINE_OFFSET_I[11:8]				0x0000	R/W
		[7:0]	BIOZ_SINE_OFFSET_I[7:0]									
0x326	BIOZ_WGAMPLITUDE_I	[15:8]	RESERVED					BIOZ_SINEAMPLITUDE_I[10:8]			0x0600	R/W
		[7:0]	BIOZ_SINEAMPLITUDE_I[7:0]									
0x327	BIOZ_DACCON_I	[15:8]	RESERVED		BIOZ_EXBUFEN_I	BIOZ_DACBUFBW_I			BIOZ_BW200KEN_I	BIOZ_BW50KEN_I	0x120D	R/W
		[7:0]	BIOZ_RATE_DIV_I									

REGISTER SUMMARY

Table 23. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x328	BIOZ_ADC_LEVEL_I	[15:8]	BIOZ_ADC_LEVEL_H_I								0xFF00	R/W
		[7:0]	BIOZ_ADC_LEVEL_L_I									
0x329	BIOZ_DC_EXCITATION_I	[15:8]	BIOZ_DCLO_POLARITY_IP_I	BIOZ_DCLO_POLARITY_IN_I	BIOZ_DCLO_L_EN_I	BIOZ_DCLO_L_MAG_I				BIOZ_DCLO_M_EN_I	0x0000	R/W
		[7:0]	BIOZ_DCLO_M_MAG_I			BIOZ_DCLO_H_EN_I	BIOZ_DCLO_H_MAG_I					
0x32A	BIOZ_ANA_CTRL1_I	[15:8]	BIOZ_TIA_RGAIN_I				BIOZ_TIA_CGAIN_I				0x1730	R/W
		[7:0]	BIOZ_EXCBUF_LPMODE_I		BIOZ_CHOP_OFF_IN_I		BIOZ_TIA_LPMODE_I		BIOZ_RX_LPMODE_I	BIOZ_DAC_RCF_LOWBW_EN_I		
0x32B	BIOZ_ANA_CTRL2_I	[15:8]	BIOZ_TIA_VREF_SEL_I	BIOZ_CM_SW_I	BIOZ_NCHAN_I			BIOZ_PCHAN_I			0x0000	R/W
		[7:0]	BIOZ_TSW_I				BIOZ_DSW_I					
0x32C	BIOZ_ANA_CTRL3_I	[15:8]	BIOZ_CHOP_OFF_EXC_I		BIOZ_PGA_GAIN_I		BIOZ_TIA_ECG_I			BIOZ_EXCBUF_ECG_I, Bit 2	0xC000	R/W
		[7:0]	BIOZ_EXCBUF_ECG_I[1:0]		BIOZ_DCLO_IP_EN_I	BIOZ_DCLO_IN_EN_I	BIOZ_CURRENT_LIMIT_I		BIOZ_RINT_SW_I			
0x32D	BIOZ_ADC FILTERCON_I	[15:8]	RESERVED				BIOZ_ADC_PERIOD_I[5:2]				0x0004	R/W
		[7:0]	BIOZ_ADC_PERIOD_I[1:0]		BIOZ_AVRGNUM_I		BIOZ_AVRGEN_I	BIOZ_SINC3BYP_I	BIOZ_SINC3OSR_I			
0x32E	BIOZ_DFTCON_I	[15:8]	RESERVED								0x0009	R/W
		[7:0]	BIOZ_DATA_SIZE_I	BIOZ_DFT_TYPE_I	BIOZ_WG_DFT_DIFF_PHASE_EN_I	BIOZ_HANNINGEN_I	BIOZ_DFTNUM_I					
0x32F	BIOZ_ADC_CONV_DLY_I	[15:8]	BIOZ_PRE_WIDTH_I			BIOZ_PRECON_SEL_I		BIOZ_SUBSAMPLE_RATIO_I[6:4]			0x0011	R/W
		[7:0]	BIOZ_SUBSAMPLE_RATIO_I[3:0]				BIOZ_PRECON_RES_I	BIOZ_ADC_CONV_DLY_I				
0x330	BIOZ_AFECON_J	[15:8]	RESERVED		BIOZ_DACREF_LPMODE_J	BIOZ_REFNORM_J	BIOZ_TIMESLOT_OFFSET_J[9:6]				0x0000	R/W
		[7:0]	BIOZ_TIMESLOT_OFFSET_J[5:0]						BIOZ_TIAEN_J	BIOZ_EXCITATION_TYPE_J		
0x331	BIOZ_WGFCW_LOW_J	[15:8]	BIOZ_SINEFCW_L_J[15:8]								0x0000	R/W
		[7:0]	BIOZ_SINEFCW_L_J[7:0]									
0x332	BIOZ_WGFCW_HI_J	[15:8]	BIOZ_DATA_SELECTION_J	BIOZ_NCHAN_ALT_J			BIOZ_PCHAN_ALT_J			RESERVED	0x0000	R/W
		[7:0]	RESERVED				BIOZ_SINEFCW_H_J					

REGISTER SUMMARY

Table 23. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x333	BIOZ_WG PHASE_J	[15:8]	BIOZ_SINE_PHASE_OFFSET_J[15:8]								0x0000	R/W
		[7:0]	BIOZ_SINE_PHASE_OFFSET_J[7:0]									
0x334	BIOZ_DFT PHASE_J	[15:8]	BIOZ_DFT_PHASE_OFFSET_J[15:8]								0x0000	R/W
		[7:0]	BIOZ_DFT_PHASE_OFFSET_J[7:0]									
0x335	BIOZ_WG OFFSET_J	[15:8]	RESERVED				BIOZ_SINE_OFFSET_J[11:8]				0x0000	R/W
		[7:0]	BIOZ_SINE_OFFSET_J[7:0]									
0x336	BIOZ_WG AMPLITU DE_J	[15:8]	RESERVED					BIOZ_SINEAMPLITUDE_J[10:8]			0x0600	R/W
		[7:0]	BIOZ_SINEAMPLITUDE_J[7:0]									
0x337	BIOZ_DAC CON_J	[15:8]	RESERVED		BIOZ_EXBU FEN_J	BIOZ_DACBUFBW_J			BIOZ_BW20 0KEN_J	BIOZ_BW50 KEN_J	0x120D	R/W
		[7:0]	BIOZ_RATE_DIV_J									
0x338	BIOZ_ADC _LEVEL_J	[15:8]	BIOZ_ADC_LEVEL_H_J								0xFF00	R/W
		[7:0]	BIOZ_ADC_LEVEL_L_J									
0x339	BIOZ_DC_ EXCITATI ON_J	[15:8]	BIOZ_DCLO O_POLARI TY_IP_J	BIOZ_DCLO _POLARITY _IN_J	BIOZ_DCLO _L_EN_J	BIOZ_DCLO_L_MAG_J				BIOZ_DCLO _M_EN_J	0x0000	R/W
		[7:0]	BIOZ_DCLO_M_MAG_J			BIOZ_DCLO _H_EN_J	BIOZ_DCLO_H_MAG_J					
0x33A	BIOZ_ANA _CTRL1_J	[15:8]	BIOZ_TIA_RGAIN_J				BIOZ_TIA_CGAIN_J				0x1730	R/W
		[7:0]	BIOZ_EXCBUF_LPMODE _J		BIOZ_CHOP_OFF_IN_J		BIOZ_TIA_LPMODE_J		BIOZ_RX_L PMODE_J	BIOZ_DAC_ RCF_LOWB W_EN_J		
0x33B	BIOZ_ANA _CTRL2_J	[15:8]	BIOZ_TIA_ VREF_SE L_J	BIOZ_CM_S W_J	BIOZ_NCHAN_J			BIOZ_PCHAN_J			0x0000	R/W
		[7:0]	BIOZ_TSW_J				BIOZ_DSW_J					
0x33C	BIOZ_ANA _CTRL3_J	[15:8]	BIOZ_CHOP_OFF_EXC_ J		BIOZ_PGA_GAIN_J		BIOZ_TIA_ECG_J			BIOZ_EXCB UF_ECG_J, Bit 2	0xC000	R/W
		[7:0]	BIOZ_EXCBUF_ECG_J[1 :0]		BIOZ_DCLO _IP_EN_J	BIOZ_DCLO _IN_EN_J	BIOZ_CURRENT_LIMIT_J		BIOZ_RINT_SW_J			
0x33D	BIOZ_ADC FILTERCO N_J	[15:8]	RESERVED				BIOZ_ADC_PERIOD_J[5:2]				0x0004	R/W
		[7:0]	BIOZ_ADC_PERIOD_J[1: 0]		BIOZ_AVRGNUM_J		BIOZ_AVRG EN_J	BIOZ_SINC 3BYP_J	BIOZ_SINC3OSR_J			
0x33E	BIOZ_DFT CON_J	[15:8]	RESERVED								0x0009	R/W
		[7:0]	BIOZ_DAT A_SIZE_J	BIOZ_DFT_ TYPE_J	BIOZ_WG_ DFT_DIFF_ PHASE_EN _J	BIOZ_HANN INGEN_J	BIOZ_DFTNUM_J					
0x33F	BIOZ_ADC _CONV_D LY_J	[15:8]	BIOZ_PRE_WIDTH_J			BIOZ_PRECON_SEL_J		BIOZ_SUBSAMPLE_RATIO_J[6:4]			0x0011	R/W

REGISTER SUMMARY

Table 23. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
		[7:0]	BIOZ_SUBSAMPLE_RATIO_J[3:0]				BIOZ_PRECON_RES_J	BIOZ_ADC_CONV_DLY_J				
0x340	BIOZ_AFECON_K	[15:8]	RESERVED		BIOZ_DACREF_LPMODE_K	BIOZ_REFNORM_K	BIOZ_TIMESLOT_OFFSET_K[9:6]				0x0000	R/W
		[7:0]	BIOZ_TIMESLOT_OFFSET_K[5:0]						BIOZ_TIAEN_K	BIOZ_EXCITATION_TYPE_K		
0x341	BIOZ_WGFCW_LOW_K	[15:8]	BIOZ_SINEFCW_L_K[15:8]								0x0000	R/W
		[7:0]	BIOZ_SINEFCW_L_K[7:0]									
0x342	BIOZ_WGFCW_HI_K	[15:8]	BIOZ_DATA_SELECTION_K	BIOZ_NCHAN_ALT_K			BIOZ_PCHAN_ALT_K			RESERVED	0x0000	R/W
		[7:0]	RESERVED				BIOZ_SINEFCW_H_K					
0x343	BIOZ_WGPHASE_K	[15:8]	BIOZ_SINE_PHASE_OFFSET_K[15:8]								0x0000	R/W
		[7:0]	BIOZ_SINE_PHASE_OFFSET_K[7:0]									
0x344	BIOZ_DFTPHASE_K	[15:8]	BIOZ_DFT_PHASE_OFFSET_K[15:8]								0x0000	R/W
		[7:0]	BIOZ_DFT_PHASE_OFFSET_K[7:0]									
0x345	BIOZ_WGOFFSET_K	[15:8]	RESERVED				BIOZ_SINE_OFFSET_K[11:8]				0x0000	R/W
		[7:0]	BIOZ_SINE_OFFSET_K[7:0]									
0x346	BIOZ_WGAMPLITUDE_K	[15:8]	RESERVED					BIOZ_SINEAMPLITUDE_K[10:8]			0x0600	R/W
		[7:0]	BIOZ_SINEAMPLITUDE_K[7:0]									
0x347	BIOZ_DACCON_K	[15:8]	RESERVED		BIOZ_EXBUFEN_K	BIOZ_DACBUFBW_K			BIOZ_BW200KEN_K	BIOZ_BW50KEN_K	0x120D	R/W
		[7:0]	BIOZ_RATE_DIV_K									
0x348	BIOZ_ADC_LEVEL_K	[15:8]	BIOZ_ADC_LEVEL_H_K								0xFF00	R/W
		[7:0]	BIOZ_ADC_LEVEL_L_K									
0x349	BIOZ_DC_EXCITATION_K	[15:8]	BIOZ_DCLO_POLARITY_IP_K	BIOZ_DCLO_POLARITY_IN_K	BIOZ_DCLO_L_EN_K	BIOZ_DCLO_L_MAG_K				BIOZ_DCLO_M_EN_K	0x0000	R/W
		[7:0]	BIOZ_DCLO_M_MAG_K			BIOZ_DCLO_H_EN_K	BIOZ_DCLO_H_MAG_K					
0x34A	BIOZ_ANA_CTRL1_K	[15:8]	BIOZ_TIA_RGAIN_K				BIOZ_TIA_CGAIN_K				0x1730	R/W
		[7:0]	BIOZ_EXCBUF_LPMODE_K		BIOZ_CHOP_OFF_IN_K		BIOZ_TIA_LPMODE_K		BIOZ_RX_LPMODE_K	BIOZ_DAC_RCF_LOWBW_EN_K		
0x34B	BIOZ_ANA_CTRL2_K	[15:8]	BIOZ_TIA_VREF_SEL_K	BIOZ_CM_SW_K	BIOZ_NCHAN_K			BIOZ_PCHAN_K			0x0000	R/W
		[7:0]	BIOZ_TSW_K				BIOZ_DSW_K					

REGISTER SUMMARY

Table 23. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x34C	BIOZ_ANA_CTRL3_K	[15:8]	BIOZ_CHOP_OFF_EXC_K		BIOZ_PGA_GAIN_K		BIOZ_TIA_ECG_K			BIOZ_EXCBUF_ECG_K, Bit 2	0xC000	R/W
		[7:0]	BIOZ_EXCBUF_ECG_K[1:0]		BIOZ_DCLOP_EN_K	BIOZ_DCLOIN_EN_K	BIOZ_CURRENT_LIMIT_K		BIOZ_RINT_SW_K			
0x34D	BIOZ_ADCFILTERCON_K	[15:8]	RESERVED				BIOZ_ADC_PERIOD_K[5:2]				0x0004	R/W
		[7:0]	BIOZ_ADC_PERIOD_K[1:0]		BIOZ_AVRGNUM_K		BIOZ_AVRGEN_K	BIOZ_SINC3BYP_K	BIOZ_SINC3OSR_K			
0x34E	BIOZ_DFTCON_K	[15:8]	RESERVED								0x0009	R/W
		[7:0]	BIOZ_DATA_SIZE_K	BIOZ_DFT_TYPE_K	BIOZ_WG_DFT_DIFF_PHASE_EN_K	BIOZ_HANNINGEN_K	BIOZ_DFTNUM_K					
0x34F	BIOZ_ADC_CONV_DLY_K	[15:8]	BIOZ_PRE_WIDTH_K			BIOZ_PRECON_SEL_K	BIOZ_SUBSAMPLE_RATIO_K[6:4]				0x0011	R/W
		[7:0]	BIOZ_SUBSAMPLE_RATIO_K[3:0]				BIOZ_PRECON_RES_K	BIOZ_ADC_CONV_DLY_K				
0x350	BIOZ_AFECON_L	[15:8]	RESERVED		BIOZ_DACREF_LPMODE_L	BIOZ_REFNORM_L	BIOZ_TIMESLOT_OFFSET_L[9:6]				0x0000	R/W
		[7:0]	BIOZ_TIMESLOT_OFFSET_L[5:0]						BIOZ_TIAEN_L	BIOZ_EXCITATION_TYPE_L		
0x351	BIOZ_WGFCW_LOW_L	[15:8]	BIOZ_SINEFCW_L_L[15:8]								0x0000	R/W
		[7:0]	BIOZ_SINEFCW_L_L[7:0]									
0x352	BIOZ_WGFCW_HI_L	[15:8]	BIOZ_DATA_SELECTION_L	BIOZ_NCHAN_ALT_L			BIOZ_PCHAN_ALT_L			RESERVED	0x0000	R/W
		[7:0]	RESERVED				BIOZ_SINEFCW_H_L					
0x353	BIOZ_WGPHASE_L	[15:8]	BIOZ_SINE_PHASE_OFFSET_L[15:8]								0x0000	R/W
		[7:0]	BIOZ_SINE_PHASE_OFFSET_L[7:0]									
0x354	BIOZ_DFTPHASE_L	[15:8]	BIOZ_DFT_PHASE_OFFSET_L[15:8]								0x0000	R/W
		[7:0]	BIOZ_DFT_PHASE_OFFSET_L[7:0]									
0x355	BIOZ_WGOFFSET_L	[15:8]	RESERVED				BIOZ_SINE_OFFSET_L[11:8]				0x0000	R/W
		[7:0]	BIOZ_SINE_OFFSET_L[7:0]									
0x356	BIOZ_WGAMPLITUDE_L	[15:8]	RESERVED					BIOZ_SINEAMPLITUDE_L[10:8]			0x0600	R/W
		[7:0]	BIOZ_SINEAMPLITUDE_L[7:0]									
0x357	BIOZ_DACCON_L	[15:8]	RESERVED		BIOZ_EXBUFEN_L	BIOZ_DACBUFBW_L			BIOZ_BW200KEN_L	BIOZ_BW50KEN_L	0x120D	R/W
		[7:0]	BIOZ_RATE_DIV_L									

REGISTER SUMMARY

Table 23. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x358	BIOZ_ADC_LEVEL_L	[15:8]	BIOZ_ADC_LEVEL_H_L								0xFF00	R/W
		[7:0]	BIOZ_ADC_LEVEL_L_L									
0x359	BIOZ_DC_EXCITATION_L	[15:8]	BIOZ_DCLO_POLARITY_IP_L	BIOZ_DCLO_POLARITY_IN_L	BIOZ_DCLO_L_EN_L	BIOZ_DCLO_L_MAG_L				BIOZ_DCLO_M_EN_L	0x0000	R/W
		[7:0]	BIOZ_DCLO_M_MAG_L			BIOZ_DCLO_H_EN_L	BIOZ_DCLO_H_MAG_L					
0x35A	BIOZ_ANA_CTRL1_L	[15:8]	BIOZ_TIA_RGAIN_L				BIOZ_TIA_CGAIN_L				0x1730	R/W
		[7:0]	BIOZ_EXCBUF_LPMODE_L		BIOZ_CHOP_OFF_IN_L		BIOZ_TIA_LPMODE_L		BIOZ_RX_LPMODE_L	BIOZ_DAC_RCF_LOWBW_EN_L		
0x35B	BIOZ_ANA_CTRL2_L	[15:8]	BIOZ_TIA_VREF_SEL_L	BIOZ_CM_SW_L	BIOZ_NCHAN_L			BIOZ_PCHAN_L			0x0000	R/W
		[7:0]	BIOZ_TSW_L				BIOZ_DSW_L					
0x35C	BIOZ_ANA_CTRL3_L	[15:8]	BIOZ_CHOP_OFF_EXC_L		BIOZ_PGA_GAIN_L		BIOZ_TIA_ECG_L			BIOZ_EXCBUF_ECG_L, Bit 2	0xC000	R/W
		[7:0]	BIOZ_EXCBUF_ECG_L[1:0]		BIOZ_DCLO_IP_EN_L	BIOZ_DCLO_IN_EN_L	BIOZ_CURRENT_LIMIT_L		BIOZ_RINT_SW_L			
0x35D	BIOZ_ADC FILTERCON_L	[15:8]	RESERVED				BIOZ_ADC_PERIOD_L[5:2]				0x0004	R/W
		[7:0]	BIOZ_ADC_PERIOD_L[1:0]		BIOZ_AVRGNUM_L		BIOZ_AVRGEN_L	BIOZ_SINC3BYP_L	BIOZ_SINC3OSR_L			
0x35E	BIOZ_DFTCON_L	[15:8]	RESERVED								0x0009	R/W
		[7:0]	BIOZ_DATA_SIZE_L	BIOZ_DFT_TYPE_L	BIOZ_WG_DFT_DIFF_PHASE_EN_L	BIOZ_HANNINGEN_L	BIOZ_DFTNUM_L					
0x35F	BIOZ_ADC_CONV_DLY_L	[15:8]	BIOZ_PRE_WIDTH_L			BIOZ_PRECON_SEL_L		BIOZ_SUBSAMPLE_RATIO_L[6:4]			0x0011	R/W
		[7:0]	BIOZ_SUBSAMPLE_RATIO_L[3:0]				BIOZ_PRECON_RES_L	BIOZ_ADC_CONV_DLY_L				
0x360	BIOZ_AFECON_M	[15:8]	RESERVED		BIOZ_DACREF_LPMODE_M	BIOZ_REFNORM_M	BIOZ_TIMESLOT_OFFSET_M[9:6]				0x0000	R/W
		[7:0]	BIOZ_TIMESLOT_OFFSET_M[5:0]						BIOZ_TIAEN_M	BIOZ_EXCITATION_TYPE_M		
0x361	BIOZ_WGFCW_LOW_M	[15:8]	BIOZ_SINEFCW_L_M[15:8]								0x0000	R/W
		[7:0]	BIOZ_SINEFCW_L_M[7:0]									
0x362	BIOZ_WGFCW_HI_M	[15:8]	BIOZ_DATA_SELECTION_M	BIOZ_NCHAN_ALT_M			BIOZ_PCHAN_ALT_M			RESERVED	0x0000	R/W
		[7:0]	RESERVED				BIOZ_SINEFCW_H_M					

REGISTER SUMMARY

Table 23. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x363	BIOZ_WG PHASE_M	[15:8]	BIOZ_SINE_PHASE_OFFSET_M[15:8]								0x0000	R/W
		[7:0]	BIOZ_SINE_PHASE_OFFSET_M[7:0]									
0x364	BIOZ_DFT PHASE_M	[15:8]	BIOZ_DFT_PHASE_OFFSET_M[15:8]								0x0000	R/W
		[7:0]	BIOZ_DFT_PHASE_OFFSET_M[7:0]									
0x365	BIOZ_WG OFFSET_ M	[15:8]	RESERVED				BIOZ_SINE_OFFSET_M[11:8]				0x0000	R/W
		[7:0]	BIOZ_SINE_OFFSET_M[7:0]									
0x366	BIOZ_WG AMPLITU DE_M	[15:8]	RESERVED					BIOZ_SINEAMPLITUDE_M[10:8]			0x0600	R/W
		[7:0]	BIOZ_SINEAMPLITUDE_M[7:0]									
0x367	BIOZ_DAC CON_M	[15:8]	RESERVED		BIOZ_EXBU FEN_M	BIOZ_DACBUFBW_M			BIOZ_BW20 0KEN_M	BIOZ_BW50 KEN_M	0x120D	R/W
		[7:0]	BIOZ_RATE_DIV_M									
0x368	BIOZ_ADC _LEVEL_ M	[15:8]	BIOZ_ADC_LEVEL_H_M								0xFF00	R/W
		[7:0]	BIOZ_ADC_LEVEL_L_M									
0x369	BIOZ_DC_ EXCITATI ON_M	[15:8]	BIOZ_DCL O_POLARI TY_IP_M	BIOZ_DCLO _POLARITY _IN_M	BIOZ_DCLO _L_EN_M	BIOZ_DCLO_L_MAG_M				BIOZ_DCLO _M_EN_M	0x0000	R/W
		[7:0]	BIOZ_DCLO_M_MAG_M			BIOZ_DCLO _H_EN_M	BIOZ_DCLO_H_MAG_M					
0x36A	BIOZ_ANA _CTRL1_ M	[15:8]	BIOZ_TIA_RGAIN_M				BIOZ_TIA_CGAIN_M				0x1730	R/W
		[7:0]	BIOZ_EXCBUF_LPMODE _M		BIOZ_CHOP_OFF_IN_M		BIOZ_TIA_LPMODE_M		BIOZ_RX_L PMODE_M	BIOZ_DAC_ RCF_LOWB W_EN_M		
0x36B	BIOZ_ANA _CTRL2_ M	[15:8]	BIOZ_TIA_ VREF_SE L_M	BIOZ_CM_S W_M	BIOZ_NCHAN_M			BIOZ_PCHAN_M			0x0000	R/W
		[7:0]	BIOZ_TSW_M				BIOZ_DSW_M					
0x36C	BIOZ_ANA _CTRL3_ M	[15:8]	BIOZ_CHOP_OFF_EXC_ M		BIOZ_PGA_GAIN_M		BIOZ_TIA_ECG_M			BIOZ_EXCB UF_ECG_M, Bit 2	0xC000	R/W
		[7:0]	BIOZ_EXCBUF_ECG_M[1:0]		BIOZ_DCLO _IP_EN_M	BIOZ_DCLO _IN_EN_M	BIOZ_CURRENT_LIMIT_M		BIOZ_RINT_SW_M			
0x36D	BIOZ_ADC FILTERCO N_M	[15:8]	RESERVED				BIOZ_ADC_PERIOD_M[5:2]				0x0004	R/W
		[7:0]	BIOZ_ADC_PERIOD_M[1 :0]		BIOZ_AVRGNUM_M		BIOZ_AVRG EN_M	BIOZ_SINC 3BYP_M	BIOZ_SINC3OSR_M			
0x36E	BIOZ_DFT CON_M	[15:8]	RESERVED								0x0009	R/W
		[7:0]	BIOZ_DAT A_SIZE_M	BIOZ_DFT_ TYPE_M	BIOZ_WG_ DFT_DIFF_ PHASE_EN _M	BIOZ_HANN INGEN_M	BIOZ_DFTNUM_M					

REGISTER SUMMARY

Table 23. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x36F	BIOZ_ADC_CONV_DLY_M	[15:8]	BIOZ_PRE_WIDTH_M			BIOZ_PRECON_SEL_M		BIOZ_SUBSAMPLE_RATIO_M[6:4]			0x0011	R/W
		[7:0]	BIOZ_SUBSAMPLE_RATIO_M[3:0]				BIOZ_PRECON_RES_M	BIOZ_ADC_CONV_DLY_M				
0x370	BIOZ_AFECON_N	[15:8]	RESERVED		BIOZ_DACREF_LPMODE_N	BIOZ_REFNORM_N	BIOZ_TIMESLOT_OFFSET_N[9:6]				0x0000	R/W
		[7:0]	BIOZ_TIMESLOT_OFFSET_N[5:0]						BIOZ_TIAEN_N	BIOZ_EXCITATION_TYPE_N		
0x371	BIOZ_WGFCW_LOW_N	[15:8]	BIOZ_SINEFCW_L_N[15:8]								0x0000	R/W
		[7:0]	BIOZ_SINEFCW_L_N[7:0]									
0x372	BIOZ_WGFCW_HI_N	[15:8]	BIOZ_DATA_SELECTION_N	BIOZ_NCHAN_ALT_N			BIOZ_PCHAN_ALT_N			RESERVED	0x0000	R/W
		[7:0]	RESERVED				BIOZ_SINEFCW_H_N					
0x373	BIOZ_WGPHASE_N	[15:8]	BIOZ_SINE_PHASE_OFFSET_N[15:8]								0x0000	R/W
		[7:0]	BIOZ_SINE_PHASE_OFFSET_N[7:0]									
0x374	BIOZ_DFTPHASE_N	[15:8]	BIOZ_DFT_PHASE_OFFSET_N[15:8]								0x0000	R/W
		[7:0]	BIOZ_DFT_PHASE_OFFSET_N[7:0]									
0x375	BIOZ_WGOFFSET_N	[15:8]	RESERVED				BIOZ_SINE_OFFSET_N[11:8]				0x0000	R/W
		[7:0]	BIOZ_SINE_OFFSET_N[7:0]									
0x376	BIOZ_WGAMPLITUDE_N	[15:8]	RESERVED					BIOZ_SINEAMPLITUDE_N[10:8]			0x0600	R/W
		[7:0]	BIOZ_SINEAMPLITUDE_N[7:0]									
0x377	BIOZ_DACCON_N	[15:8]	RESERVED		BIOZ_EXBUFEN_N	BIOZ_DACBUFBW_N			BIOZ_BW200KEN_N	BIOZ_BW50KEN_N	0x120D	R/W
		[7:0]	BIOZ_RATE_DIV_N									
0x378	BIOZ_ADC_LEVEL_N	[15:8]	BIOZ_ADC_LEVEL_H_N								0xFF00	R/W
		[7:0]	BIOZ_ADC_LEVEL_L_N									
0x379	BIOZ_DC_EXCITATION_N	[15:8]	BIOZ_DCLO_POLARITY_IP_N	BIOZ_DCLO_POLARITY_IN_N	BIOZ_DCLO_L_EN_N	BIOZ_DCLO_L_MAG_N				BIOZ_DCLO_M_EN_N	0x0000	R/W
		[7:0]	BIOZ_DCLO_M_MAG_N			BIOZ_DCLO_H_EN_N	BIOZ_DCLO_H_MAG_N					
0x37A	BIOZ_ANA_CTRL1_N	[15:8]	BIOZ_TIA_RGAIN_N				BIOZ_TIA_CGAIN_N				0x1730	R/W
		[7:0]	BIOZ_EXCBUF_LPMODE_N		BIOZ_CHOP_OFF_IN_N		BIOZ_TIA_LPMODE_N		BIOZ_RX_LPMODE_N	BIOZ_DAC_RCF_LOWBW_EN_N		
0x37B	BIOZ_ANA_CTRL2_N	[15:8]	BIOZ_TIA_VREF_SEL_N	BIOZ_CM_SW_N	BIOZ_NCHAN_N			BIOZ_PCHAN_N			0x0000	R/W

REGISTER SUMMARY

Table 23. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
		[7:0]	BIOZ_TSW_N				BIOZ_DSW_N					
0x37C	BIOZ_ANA_CTRL3_N	[15:8]	BIOZ_CHOP_OFF_EXC_N		BIOZ_PGA_GAIN_N		BIOZ_TIA_ECG_N			BIOZ_EXCBUF_ECG_N, Bit 2	0xC000	R/W
		[7:0]	BIOZ_EXCBUF_ECG_N[1:0]		BIOZ_DCLO_IP_EN_N	BIOZ_DCLO_IN_EN_N	BIOZ_CURRENT_LIMIT_N		BIOZ_RINT_SW_N			
0x37D	BIOZ_ADCFILTERCON_N	[15:8]	RESERVED				BIOZ_ADC_PERIOD_N[5:2]				0x0004	R/W
		[7:0]	BIOZ_ADC_PERIOD_N[1:0]		BIOZ_AVRGNUM_N		BIOZ_AVRGEN_N	BIOZ_SINC3BYP_N	BIOZ_SINC3OSR_N			
0x37E	BIOZ_DFTCON_N	[15:8]	RESERVED								0x0009	R/W
		[7:0]	BIOZ_DATA_SIZE_N	BIOZ_DFT_TYPE_N	BIOZ_WG_DFT_DIFF_PHASE_EN_N	BIOZ_HANNINGEN_N	BIOZ_DFTNUM_N					
0x37F	BIOZ_ADC_CONV_DLY_N	[15:8]	BIOZ_PRE_WIDTH_N			BIOZ_PRECON_SEL_N	BIOZ_SUBSAMPLE_RATIO_N[6:4]				0x0011	R/W
		[7:0]	BIOZ_SUBSAMPLE_RATIO_N[3:0]				BIOZ_PRECON_RES_N	BIOZ_ADC_CONV_DLY_N				
0x380	BIOZ_AFECON_O	[15:8]	RESERVED		BIOZ_DACREF_LPMODE_O	BIOZ_REFNORM_O	BIOZ_TIMESLOT_OFFSET_O[9:6]				0x0000	R/W
		[7:0]	BIOZ_TIMESLOT_OFFSET_O[5:0]						BIOZ_TIAEN_O	BIOZ_EXCITATION_TYPE_O		
0x381	BIOZ_WGFCW_LOW_O	[15:8]	BIOZ_SINEFCW_L_O[15:8]								0x0000	R/W
		[7:0]	BIOZ_SINEFCW_L_O[7:0]									
0x382	BIOZ_WGFCW_HI_O	[15:8]	BIOZ_DATA_SELECTION_O	BIOZ_NCHAN_ALT_O			BIOZ_PCHAN_ALT_O			RESERVED	0x0000	R/W
		[7:0]	RESERVED				BIOZ_SINEFCW_H_O					
0x383	BIOZ_WGPHASE_O	[15:8]	BIOZ_SINE_PHASE_OFFSET_O[15:8]								0x0000	R/W
		[7:0]	BIOZ_SINE_PHASE_OFFSET_O[7:0]									
0x384	BIOZ_DFTPHASE_O	[15:8]	BIOZ_DFT_PHASE_OFFSET_O[15:8]								0x0000	R/W
		[7:0]	BIOZ_DFT_PHASE_OFFSET_O[7:0]									
0x385	BIOZ_WGOFFSET_O	[15:8]	RESERVED				BIOZ_SINE_OFFSET_O[11:8]				0x0000	R/W
		[7:0]	BIOZ_SINE_OFFSET_O[7:0]									
0x386	BIOZ_WGAMPLITUDE_O	[15:8]	RESERVED				BIOZ_SINEAMPLITUDE_O[10:8]				0x0600	R/W
		[7:0]	BIOZ_SINEAMPLITUDE_O[7:0]									
0x387	BIOZ_DACCON_O	[15:8]	RESERVED		BIOZ_EXBUFEN_O	BIOZ_DACBUFBW_O			BIOZ_BW200KEN_O	BIOZ_BW50KEN_O	0x120D	R/W

REGISTER SUMMARY

Table 23. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
		[7:0]	BIOZ_RATE_DIV_O									
0x388	BIOZ_ADC_LEVEL_O	[15:8]	BIOZ_ADC_LEVEL_H_O								0xFF00	R/W
		[7:0]	BIOZ_ADC_LEVEL_L_O									
0x389	BIOZ_DC_EXCITATION_O	[15:8]	BIOZ_DCLO_POLARITY_IP_O	BIOZ_DCLO_POLARITY_IN_O	BIOZ_DCLO_L_EN_O	BIOZ_DCLO_L_MAG_O				BIOZ_DCLO_M_EN_O	0x0000	R/W
		[7:0]	BIOZ_DCLO_M_MAG_O			BIOZ_DCLO_H_EN_O	BIOZ_DCLO_H_MAG_O					
0x38A	BIOZ_ANA_CTRL1_O	[15:8]	BIOZ_TIA_RGAIN_O				BIOZ_TIA_CGAIN_O				0x1730	R/W
		[7:0]	BIOZ_EXCBUF_LPMODE_O		BIOZ_CHOP_OFF_IN_O		BIOZ_TIA_LPMODE_O		BIOZ_RX_LPMODE_O	BIOZ_DAC_RCF_LOWBW_EN_O		
0x38B	BIOZ_ANA_CTRL2_O	[15:8]	BIOZ_TIA_VREF_SEL_O	BIOZ_CM_SW_O	BIOZ_NCHAN_O			BIOZ_PCHAN_O			0x0000	R/W
		[7:0]	BIOZ_TSW_O				BIOZ_DSW_O					
0x38C	BIOZ_ANA_CTRL3_O	[15:8]	BIOZ_CHOP_OFF_EXC_O		BIOZ_PGA_GAIN_O		BIOZ_TIA_ECG_O			BIOZ_EXCBUF_ECG_O, Bit 2	0xC000	R/W
		[7:0]	BIOZ_EXCBUF_ECG_O[1:0]		BIOZ_DCLO_IP_EN_O	BIOZ_DCLO_IN_EN_O	BIOZ_CURRENT_LIMIT_O		BIOZ_RINT_SW_O			
0x38D	BIOZ_ADCFILTERCON_O	[15:8]	RESERVED				BIOZ_ADC_PERIOD_O[5:2]				0x0004	R/W
		[7:0]	BIOZ_ADC_PERIOD_O[1:0]		BIOZ_AVRGNUM_O		BIOZ_AVRGEN_O	BIOZ_SINC3BYP_O	BIOZ_SINC3OSR_O			
0x38E	BIOZ_DFTCON_O	[15:8]	RESERVED								0x0009	R/W
		[7:0]	BIOZ_DATA_SIZE_O	BIOZ_DFT_TYPE_O	BIOZ_WG_DFT_DIFF_PHASE_EN_O	BIOZ_HANNINGEN_O	BIOZ_DFTNUM_O					
0x38F	BIOZ_ADC_CONV_DLY_O	[15:8]	BIOZ_PRE_WIDTH_O			BIOZ_PRECON_SEL_O		BIOZ_SUBSAMPLE_RATIO_O[6:4]			0x0011	R/W
		[7:0]	BIOZ_SUBSAMPLE_RATIO_O[3:0]				BIOZ_PRECON_RES_O	BIOZ_ADC_CONV_DLY_O				
0x390	BIOZ_AFECON_P	[15:8]	RESERVED		BIOZ_DACREF_LPMODE_P	BIOZ_REFNORM_P	BIOZ_TIMESLOT_OFFSET_P[9:6]				0x0000	R/W
		[7:0]	BIOZ_TIMESLOT_OFFSET_P[5:0]						BIOZ_TIAEN_P	BIOZ_EXCITATION_TYPE_P		
0x391	BIOZ_WGFCW_LOW_P	[15:8]	BIOZ_SINEFCW_L_P[15:8]								0x0000	R/W
		[7:0]	BIOZ_SINEFCW_L_P[7:0]									
0x392	BIOZ_WGFCW_HI_P	[15:8]	BIOZ_DATA_SELECTION_P	BIOZ_NCHAN_ALT_P			BIOZ_PCHAN_ALT_P			RESERVED	0x0000	R/W

REGISTER SUMMARY

Table 23. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
		[7:0]	RESERVED				BIOZ_SINEFCW_H_P					
0x393	BIOZ_WG PHASE_P	[15:8]	BIOZ_SINE_PHASE_OFFSET_P[15:8]								0x0000	R/W
		[7:0]	BIOZ_SINE_PHASE_OFFSET_P[7:0]									
0x394	BIOZ_DFT PHASE_P	[15:8]	BIOZ_DFT_PHASE_OFFSET_P[15:8]								0x0000	R/W
		[7:0]	BIOZ_DFT_PHASE_OFFSET_P[7:0]									
0x395	BIOZ_WG OFFSET_ P	[15:8]	RESERVED				BIOZ_SINE_OFFSET_P[11:8]				0x0000	R/W
		[7:0]	BIOZ_SINE_OFFSET_P[7:0]									
0x396	BIOZ_WG AMPLITU DE_P	[15:8]	RESERVED					BIOZ_SINEAMPLITUDE_P[10:8]			0x0600	R/W
		[7:0]	BIOZ_SINEAMPLITUDE_P[7:0]									
0x397	BIOZ_DAC CON_P	[15:8]	RESERVED		BIOZ_EXBU FEN_P	BIOZ_DACBUFBW_P			BIOZ_BW20 0KEN_P	BIOZ_BW50 KEN_P	0x120D	R/W
		[7:0]	BIOZ_RATE_DIV_P									
0x398	BIOZ_ADC _LEVEL_P	[15:8]	BIOZ_ADC_LEVEL_H_P								0xFF00	R/W
		[7:0]	BIOZ_ADC_LEVEL_L_P									
0x399	BIOZ_DC_ EXCITATI ON_P	[15:8]	BIOZ_DCL O_POLARI TY_IP_P	BIOZ_DCLO _POLARITY _IN_P	BIOZ_DCLO _L_EN_P	BIOZ_DCLO_L_MAG_P				BIOZ_DCLO _M_EN_P	0x0000	R/W
		[7:0]	BIOZ_DCLO_M_MAG_P			BIOZ_DCLO _H_EN_P	BIOZ_DCLO_H_MAG_P					
0x39A	BIOZ_ANA _CTRL1_P	[15:8]	BIOZ_TIA_RGAIN_P				BIOZ_TIA_CGAIN_P				0x1730	R/W
		[7:0]	BIOZ_EXCBUF_LPMODE _P		BIOZ_CHOP_OFF_IN_P		BIOZ_TIA_LPMODE_P		BIOZ_RX_L PMODE_P	BIOZ_DAC_ RCF_LOWB W_EN_P		
0x39B	BIOZ_ANA _CTRL2_P	[15:8]	BIOZ_TIA_ VREF_SE L_P	BIOZ_CM_S W_P	BIOZ_NCHAN_P			BIOZ_PCHAN_P			0x0000	R/W
		[7:0]	BIOZ_TSW_P				BIOZ_DSW_P					
0x39C	BIOZ_ANA _CTRL3_P	[15:8]	BIOZ_CHOP_OFF_EXC_ P		BIOZ_PGA_GAIN_P		BIOZ_TIA_ECG_P			BIOZ_EXCB UF_ECG_P[2]	0xC000	R/W
		[7:0]	BIOZ_EXCBUF_ECG_P[1 :0]		BIOZ_DCLO _IP_EN_P	BIOZ_DCLO _IN_EN_P	BIOZ_CURRENT_LIMIT_P		BIOZ_RINT_SW_P			
0x39D	BIOZ_ADC FILTERCO N_P	[15:8]	RESERVED				BIOZ_ADC_PERIOD_P[5:2]				0x0004	R/W
		[7:0]	BIOZ_ADC_PERIOD_P[1: 0]		BIOZ_AVRGNUM_P		BIOZ_AVRG EN_P	BIOZ_SINC 3BYP_P	BIOZ_SINC3OSR_P			
0x39E	BIOZ_DFT CON_P	[15:8]	RESERVED								0x0009	R/W
		[7:0]	BIOZ_DAT A_SIZE_P	BIOZ_DFT_ TYPE_P	BIOZ_WG_ DFT_DIFF_ PHASE_EN _P	BIOZ_HANN INGEN_P	BIOZ_DFTNUM_P					

REGISTER SUMMARY

Table 23. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x39F	BIOZ_ADC_CONV_DLY_P	[15:8]	BIOZ_PRE_WIDTH_P			BIOZ_PRECON_SEL_P		BIOZ_SUBSAMPLE_RATIO_P[6:4]			0x0011	R/W
		[7:0]	BIOZ_SUBSAMPLE_RATIO_P[3:0]				BIOZ_PRECON_RES_P	BIOZ_ADC_CONV_DLY_P				
0x3A0	BIOZ_AFECON_Q	[15:8]	RESERVED		BIOZ_DACREF_LPMODE_Q	BIOZ_REFNORM_Q	BIOZ_TIMESLOT_OFFSET_Q[9:6]				0x0000	R/W
		[7:0]	BIOZ_TIMESLOT_OFFSET_Q[5:0]						BIOZ_TIAEN_Q	BIOZ_EXCITATION_TYPE_Q		
0x3A1	BIOZ_WGFCW_LOW_Q	[15:8]	BIOZ_SINEFCW_L_Q[15:8]								0x0000	R/W
		[7:0]	BIOZ_SINEFCW_L_Q[7:0]									
0x3A2	BIOZ_WGFCW_HI_Q	[15:8]	BIOZ_DATA_SELECTION_Q	BIOZ_NCHAN_ALT_Q			BIOZ_PCHAN_ALT_Q			RESERVED	0x0000	R/W
		[7:0]	RESERVED				BIOZ_SINEFCW_H_Q					
0x3A3	BIOZ_WGPHASE_Q	[15:8]	BIOZ_SINE_PHASE_OFFSET_Q[15:8]								0x0000	R/W
		[7:0]	BIOZ_SINE_PHASE_OFFSET_Q[7:0]									
0x3A4	BIOZ_DFTPHASE_Q	[15:8]	BIOZ_DFT_PHASE_OFFSET_Q[15:8]								0x0000	R/W
		[7:0]	BIOZ_DFT_PHASE_OFFSET_Q[7:0]									
0x3A5	BIOZ_WGOFFSET_Q	[15:8]	RESERVED				BIOZ_SINE_OFFSET_Q[11:8]				0x0000	R/W
		[7:0]	BIOZ_SINE_OFFSET_Q[7:0]									
0x3A6	BIOZ_WGAMPLITUDE_Q	[15:8]	RESERVED					BIOZ_SINEAMPLITUDE_Q[10:8]			0x0600	R/W
		[7:0]	BIOZ_SINEAMPLITUDE_Q[7:0]									
0x3A7	BIOZ_DACCON_Q	[15:8]	RESERVED		BIOZ_EXBUFEN_Q	BIOZ_DACBUFBW_Q			BIOZ_BW200KEN_Q	BIOZ_BW50KEN_Q	0x120D	R/W
		[7:0]	BIOZ_RATE_DIV_Q									
0x3A8	BIOZ_ADC_LEVEL_Q	[15:8]	BIOZ_ADC_LEVEL_H_Q								0xFF00	R/W
		[7:0]	BIOZ_ADC_LEVEL_L_Q									
0x3A9	BIOZ_DC_EXCITATION_Q	[15:8]	BIOZ_DCLO_POLARITY_IP_Q	BIOZ_DCLO_POLARITY_IN_Q	BIOZ_DCLO_L_EN_Q	BIOZ_DCLO_L_MAG_Q				BIOZ_DCLO_M_EN_Q	0x0000	R/W
		[7:0]	BIOZ_DCLO_M_MAG_Q			BIOZ_DCLO_H_EN_Q	BIOZ_DCLO_H_MAG_Q					
0x3AA	BIOZ_ANA_CTRL1_Q	[15:8]	BIOZ_TIA_RGAIN_Q				BIOZ_TIA_CGAIN_Q				0x1730	R/W
		[7:0]	BIOZ_EXCBUF_LPMODE_Q		BIOZ_CHOP_OFF_IN_Q		BIOZ_TIA_LPMODE_Q		BIOZ_RX_LPMODE_Q	BIOZ_DAC_RCF_LOWBW_EN_Q		

REGISTER SUMMARY

Table 23. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x3AB	BIOZ_ANA_CTRL2_Q	[15:8]	BIOZ_TIA_VREF_SEL_Q	BIOZ_CM_SW_Q	BIOZ_NCHAN_Q			BIOZ_PCHAN_Q			0x0000	R/W
		[7:0]	BIOZ_TSW_Q				BIOZ_DSW_Q					
0x3AC	BIOZ_ANA_CTRL3_Q	[15:8]	BIOZ_CHOP_OFF_EXC_Q		BIOZ_PGA_GAIN_Q		BIOZ_TIA_ECG_Q			BIOZ_EXCBUF_ECG_Q, Bit 2	0xC000	R/W
		[7:0]	BIOZ_EXCBUF_ECG_Q[1:0]		BIOZ_DCLO_IP_EN_Q	BIOZ_DCLO_IN_EN_Q	BIOZ_CURRENT_LIMIT_Q		BIOZ_RINT_SW_Q			
0x3AD	BIOZ_ADC FILTERCON_Q	[15:8]	RESERVED				BIOZ_ADC_PERIOD_Q[5:2]				0x0004	R/W
		[7:0]	BIOZ_ADC_PERIOD_Q[1:0]		BIOZ_AVRGNUM_Q		BIOZ_AVRGEN_Q	BIOZ_SINC3BYP_Q	BIOZ_SINC3OSR_Q			
0x3AE	BIOZ_DFTCON_Q	[15:8]	RESERVED								0x0009	R/W
		[7:0]	BIOZ_DATA_SIZE_Q	BIOZ_DFT_TYPE_Q	BIOZ_WG_DFT_DIFF_PHASE_EN_Q	BIOZ_HANNINGEN_Q	BIOZ_DFTNUM_Q					
0x3AF	BIOZ_ADC_CONV_DLY_Q	[15:8]	BIOZ_PRE_WIDTH_Q			BIOZ_PRECON_SEL_Q	BIOZ_SUBSAMPLE_RATIO_Q[6:4]				0x0011	R/W
		[7:0]	BIOZ_SUBSAMPLE_RATIO_Q[3:0]				BIOZ_PRECON_RES_Q	BIOZ_ADC_CONV_DLY_Q				
0x3B0	BIOZ_AFECON_R	[15:8]	RESERVED		BIOZ_DACREF_LPMODE_R	BIOZ_REFNORM_R	BIOZ_TIMESLOT_OFFSET_R[9:6]				0x0000	R/W
		[7:0]	BIOZ_TIMESLOT_OFFSET_R[5:0]						BIOZ_TIAEN_R	BIOZ_EXCITATION_TYPE_R		
0x3B1	BIOZ_WGFCW_LOW_R	[15:8]	BIOZ_SINEFCW_L_R[15:8]								0x0000	R/W
		[7:0]	BIOZ_SINEFCW_L_R[7:0]									
0x3B2	BIOZ_WGFCW_HI_R	[15:8]	BIOZ_DATA_SELECTION_R	BIOZ_NCHAN_ALT_R			BIOZ_PCHAN_ALT_R			RESERVED	0x0000	R/W
		[7:0]	RESERVED				BIOZ_SINEFCW_H_R					
0x3B3	BIOZ_WGPHASE_R	[15:8]	BIOZ_SINE_PHASE_OFFSET_R[15:8]								0x0000	R/W
		[7:0]	BIOZ_SINE_PHASE_OFFSET_R[7:0]									
0x3B4	BIOZ_DFTPHASE_R	[15:8]	BIOZ_DFT_PHASE_OFFSET_R[15:8]								0x0000	R/W
		[7:0]	BIOZ_DFT_PHASE_OFFSET_R[7:0]									
0x3B5	BIOZ_WGOFFSET_R	[15:8]	RESERVED				BIOZ_SINE_OFFSET_R[11:8]				0x0000	R/W
		[7:0]	BIOZ_SINE_OFFSET_R[7:0]									
0x3B6	BIOZ_WGAMPLITUDE_R	[15:8]	RESERVED					BIOZ_SINEAMPLITUDE_R[10:8]			0x0600	R/W

REGISTER SUMMARY

Table 23. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
		[7:0]	BIOZ_SINEAMPLITUDE_R[7:0]									
0x3B7	BIOZ_DACCON_R	[15:8]	RESERVED		BIOZ_EXBUFEN_R	BIOZ_DACBUFBW_R			BIOZ_BW2000KEN_R	BIOZ_BW500KEN_R	0x120D	R/W
		[7:0]	BIOZ_RATE_DIV_R									
0x3B8	BIOZ_ADC_LEVEL_R	[15:8]	BIOZ_ADC_LEVEL_H_R								0xFF00	R/W
		[7:0]	BIOZ_ADC_LEVEL_L_R									
0x3B9	BIOZ_DC_EXCITATION_R	[15:8]	BIOZ_DCLO_POLARITY_IP_R	BIOZ_DCLO_POLARITY_IN_R	BIOZ_DCLO_L_EN_R	BIOZ_DCLO_L_MAG_R				BIOZ_DCLO_M_EN_R	0x0000	R/W
		[7:0]	BIOZ_DCLO_M_MAG_R			BIOZ_DCLO_H_EN_R	BIOZ_DCLO_H_MAG_R					
0x3BA	BIOZ_ANA_CTRL1_R	[15:8]	BIOZ_TIA_RGAIN_R				BIOZ_TIA_CGAIN_R				0x1730	R/W
		[7:0]	BIOZ_EXCBUF_LPMODE_R		BIOZ_CHOP_OFF_IN_R		BIOZ_TIA_LPMODE_R		BIOZ_RX_LPMODE_R	BIOZ_DAC_RCF_LOWBW_EN_R		
0x3BB	BIOZ_ANA_CTRL2_R	[15:8]	BIOZ_TIA_VREF_SEL_R	BIOZ_CM_SW_R	BIOZ_NCHAN_R			BIOZ_PCHAN_R			0x0000	R/W
		[7:0]	BIOZ_TSW_R				BIOZ_DSW_R					
0x3BC	BIOZ_ANA_CTRL3_R	[15:8]	BIOZ_CHOP_OFF_EXC_R		BIOZ_PGA_GAIN_R		BIOZ_TIA_ECG_R			BIOZ_EXCBUF_ECG_R, Bit 2	0xC000	R/W
		[7:0]	BIOZ_EXCBUF_ECG_R[1:0]		BIOZ_DCLO_IP_EN_R	BIOZ_DCLO_IN_EN_R	BIOZ_CURRENT_LIMIT_R		BIOZ_RINT_SW_R			
0x3BD	BIOZ_ADCFILTERCON_R	[15:8]	RESERVED				BIOZ_ADC_PERIOD_R[5:2]				0x0004	R/W
		[7:0]	BIOZ_ADC_PERIOD_R[1:0]		BIOZ_AVRGNUM_R		BIOZ_AVRGEN_R	BIOZ_SINC3BYP_R	BIOZ_SINC3OSR_R			
0x3BE	BIOZ_DFTCON_R	[15:8]	RESERVED								0x0009	R/W
		[7:0]	BIOZ_DATA_SIZE_R	BIOZ_DFT_TYPE_R	BIOZ_WG_DFT_DIFF_PHASE_EN_R	BIOZ_HANNINGEN_R	BIOZ_DFTNUM_R					
0x3BF	BIOZ_ADC_CONV_DLY_R	[15:8]	BIOZ_PRE_WIDTH_R			BIOZ_PRECON_SEL_R		BIOZ_SUBSAMPLE_RATIO_R[6:4]			0x0011	R/W
		[7:0]	BIOZ_SUBSAMPLE_RATIO_R[3:0]				BIOZ_PRECON_RES_R	BIOZ_ADC_CONV_DLY_R				

REGISTER DETAILS

Table 24. Register Details

Reg	Name	Bits	Bit Name	Description	Reset	Access
0x000	FIFO_STATUS	15	CLEAR_FIFO	Clear FIFO. Write a 1 to empty the FIFO while not operating, which resets the FIFO_BYTE_COUNT and also clears the FIFO overflow, FIFO underflow, and FIFO threshold interrupt status bits.	0x0	R0/W
		14	INT_FIFO_UFLOW	FIFO underflow error. This bit is set when the FIFO is read when it was empty. Write 1 to this bit to clear the interrupt, and it is also cleared when the FIFO is cleared by using the CLEAR_FIFO register.	0x0	R/W1C
		13	INT_FIFO_OFLOW	FIFO overflow error. This bit is set when data is not written to the FIFO due to lack of space. Write 1 to this bit to clear the interrupt, which is also cleared if the FIFO is cleared with the CLEAR_FIFO register bit.	0x0	R/W1C
		12	INT_FIFO_TH	FIFO_TH interrupt status. This bit is set during a FIFO write when the number of bytes in the FIFO exceeds the FIFO_TH register value. Write 1 to this bit to clear this interrupt. This bit can also be automatically cleared when the FIFO data register is read if the INT_ACLEAR_FIFO bit is set.	0x0	R/W1C
		11	FIFO_INIT_DONE_STATUS	FIFO initialization process is finished. Note that this field is a status bit and is not sent to interrupt. This bit is set after the FIFO self-initialization process.	0x0	R
		[10:0]	FIFO_BYTE_COUNT	Number of bytes in the FIFO. This field indicates the number of bytes in the FIFO.	0x0	R
0x001	INT_STATUS_TS1	[15:12]	RESERVED	Reserved.	0x0	R
		11	INT_PPG_LEV0_L	PPG Time Slot L Level 0 interrupt status. This bit is set during a data register update when the configured criteria is met. This bit is set when the Channel 1 TIA saturates during Time Slot L.	0x0	R/W1C
		10	INT_PPG_LEV0_K	PPG Time Slot K Level 0 interrupt status. This bit is set during a data register update when the configured criteria is met. This bit is set when the Channel 1 TIA saturates during Time Slot K.	0x0	R/W1C
		9	INT_PPG_LEV0_J	PPG Time Slot J Level 0 interrupt status. This bit is set during a data register update when the configured criteria is met. This bit is set when the Channel 1 TIA saturates during Time Slot J.	0x0	R/W1C
		8	INT_PPG_LEV0_I	PPG Time Slot I Level 0 interrupt status. This bit is set during a data register update when the configured criteria is met. This bit is set when the Channel 1 TIA saturates during Time Slot I.	0x0	R/W1C
		7	INT_PPG_LEV0_H	PPG Time Slot H Level 0 interrupt status. This bit is set during a data register update when the configured criteria is met. This bit is set when the Channel 1 TIA saturates during Time Slot H.	0x0	R/W1C
		6	INT_PPG_LEV0_G	PPG Time Slot G Level 0 interrupt status. This bit is set during a data register update when the configured criteria is met. This bit is set when the Channel 1 TIA saturates during Time Slot G.	0x0	R/W1C
		5	INT_PPG_LEV0_F	PPG Time Slot F Level 0 interrupt status. This bit is set during a data register update when the	0x0	R/W1C

REGISTER DETAILS

Table 24. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
				configured criteria is met. This bit is set when the Channel 1 TIA saturates during Time Slot F.		
		4	INT_PPG_LEV0_E	PPG Time Slot E Level 0 interrupt status. This bit is set during a data register update when the configured criteria is met. This bit is set when the Channel 1 TIA saturates during Time Slot E.	0x0	R/W1C
		3	INT_PPG_LEV0_D	PPG Time Slot D Level 0 interrupt status. This bit is set during a data register update when the configured criteria is met. This bit is set when the Channel 1 TIA saturates during Time Slot D.	0x0	R/W1C
		2	INT_PPG_LEV0_C	PPG Time Slot C Level 0 interrupt status. This bit is set during a data register update when the configured criteria is met. This bit is set when the Channel 1 TIA saturates during Time Slot C.	0x0	R/W1C
		1	INT_PPG_LEV0_B	PPG Time Slot B Level 0 interrupt status. This bit is set during a data register update when the configured criteria is met. This bit is set when the Channel 1 TIA saturates during Time Slot B.	0x0	R/W1C
		0	INT_PPG_LEV0_A	PPG Time Slot A Level 0 interrupt status. This bit is set during a data register update when the configured criteria is met. This bit is set when the Channel 1 TIA saturates during Time Slot A.	0x0	R/W1C
0x002	INT_STATUS_TS2	[15:12]	RESERVED	Reserved.	0x0	R
		11	INT_PPG_LEV1_L	PPG Time Slot L Level 1 interrupt status. This bit is set during a data register update when the configured criteria is met. This bit is set when the Channel 2 TIA saturates during Time Slot L.	0x0	R/W1C
		10	INT_PPG_LEV1_K	PPG Time Slot K Level 1 interrupt status. This bit is set during a data register update when the configured criteria is met. This bit is set when the Channel 2 TIA saturates during Time Slot K.	0x0	R/W1C
		9	INT_PPG_LEV1_J	PPG Time Slot J Level 1 interrupt status. This bit is set during a data register update when the configured criteria is met. This bit is set when the Channel 2 TIA saturates during Time Slot J.	0x0	R/W1C
		8	INT_PPG_LEV1_I	PPG Time Slot I Level 1 interrupt status. This bit is set during a data register update when the configured criteria is met. This bit is set when the Channel 2 TIA saturates during Time Slot I.	0x0	R/W1C
		7	INT_PPG_LEV1_H	PPG Time Slot H Level 1 interrupt status. This bit is set during a data register update when the configured criteria is met. This bit is set when the Channel 2 TIA saturates during Time Slot H.	0x0	R/W1C
		6	INT_PPG_LEV1_G	PPG Time Slot G Level 1 interrupt status. This bit is set during a data register update when the configured criteria is met. This bit is set when the Channel 2 TIA saturates during Time Slot G.	0x0	R/W1C
		5	INT_PPG_LEV1_F	PPG Time Slot F Level 1 interrupt status. This bit is set during a data register update when the configured criteria is met. This bit is set when the Channel 2 TIA saturates during Time Slot F.	0x0	R/W1C
		4	INT_PPG_LEV1_E	PPG Time Slot E Level 1 interrupt status. This bit is set during a data register update when the	0x0	R/W1C

REGISTER DETAILS

Table 24. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
				configured criteria is met. This bit is set when the Channel 2 TIA saturates during Time Slot E.		
		3	INT_PPG_LEV1_D	PPG Time Slot D Level 1 interrupt status. This bit is set during a data register update when the configured criteria is met. This bit is set when the Channel 2 TIA saturates during Time Slot D.	0x0	R/W1C
		2	INT_PPG_LEV1_C	PPG Time Slot C Level 1 interrupt status. This bit is set during a data register update when the configured criteria is met. This bit is set when the Channel 2 TIA saturates during Time Slot C.	0x0	R/W1C
		1	INT_PPG_LEV1_B	PPG Time Slot B Level 1 interrupt status. This bit is set during a data register update when the configured criteria is met. This bit is set when the Channel 2 TIA saturates during Time Slot B.	0x0	R/W1C
		0	INT_PPG_LEV1_A	PPG Time Slot A Level 1 interrupt status. This bit is set during a data register update when the configured criteria is met. This bit is set when the Channel 2 TIA saturates during Time Slot A.	0x0	R/W1C
0x003	INT_STATUS_BIOZ	15	INT_BIOZ_SAT_P	BIOZ ADC saturation interrupt for Time Slot A.	0x0	R/W1C
		14	INT_BIOZ_SAT_O	BIOZ ADC saturation interrupt for Time Slot A.	0x0	R/W1C
		13	INT_BIOZ_SAT_N	BIOZ ADC saturation interrupt for Time Slot A.	0x0	R/W1C
		12	INT_BIOZ_SAT_M	BIOZ ADC saturation interrupt for Time Slot A.	0x0	R/W1C
		11	INT_BIOZ_SAT_L	BIOZ ADC saturation interrupt for Time Slot L.	0x0	R/W1C
		10	INT_BIOZ_SAT_K	BIOZ ADC saturation interrupt for Time Slot K.	0x0	R/W1C
		9	INT_BIOZ_SAT_J	BIOZ ADC saturation interrupt for Time Slot J.	0x0	R/W1C
		8	INT_BIOZ_SAT_I	BIOZ ADC saturation interrupt for Time Slot I.	0x0	R/W1C
		7	INT_BIOZ_SAT_H	BIOZ ADC saturation interrupt for Time Slot H.	0x0	R/W1C
		6	INT_BIOZ_SAT_G	BIOZ ADC saturation interrupt for Time Slot G.	0x0	R/W1C
		5	INT_BIOZ_SAT_F	BIOZ ADC saturation interrupt for Time Slot F.	0x0	R/W1C
		4	INT_BIOZ_SAT_E	BIOZ ADC saturation interrupt for Time Slot E.	0x0	R/W1C
		3	INT_BIOZ_SAT_D	BIOZ ADC saturation interrupt for Time Slot D.	0x0	R/W1C
		2	INT_BIOZ_SAT_C	BIOZ ADC saturation interrupt for Time Slot C.	0x0	R/W1C
		1	INT_BIOZ_SAT_B	BIOZ ADC saturation interrupt for Time Slot B.	0x0	R/W1C
		0	INT_BIOZ_SAT_A	BIOZ ADC saturation interrupt for Time Slot A.	0x0	R/W1C
0x004	ECG_STATUS	15	INT_BIOZ_SAT_R	BIOZ ADC saturation interrupt for Time Slot A.	0x0	R/W1C
		14	INT_BIOZ_SAT_Q	BIOZ ADC saturation interrupt for Time Slot A.	0x0	R/W1C
		[13:8]	RESERVED	Reserved.	0x0	R
		7	ECG_ACLO_STATUS	ECG ACLO status bit. Write 1 to this bit to clear this status.	0x1	R/W1C
		6	ECGIN_DCLO_HI_STATUS	ECGIN DCLO high status bit. Write 1 to this bit to clear this status.	0x1	R/W1C
		5	ECGIP_DCLO_HI_STATUS	ECGIP DCLO high status bit. Write 1 to this bit to clear this status.	0x1	R/W1C
		4	ECG_RLD_DCLO_HI_STATUS	ECG RLD DCLO high status bit. Write 1 to this bit to clear this status.	0x1	R/W1C
		3	ECG_RLD_DCLO_LO_STATUS	ECG RLD DCLO low status bit. Write 1 to this bit to clear this status.	0x1	R/W1C
		2	ECG_DCLO_STATUS	ECG DCLO status bit. Write 1 to this bit to clear this status.	0x1	R/W1C

REGISTER DETAILS

Table 24. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
		1	ECG_PGA_SAT_STATUS	ECG PGA saturation status bit. Write 1 to this bit to clear this status.	0x0	R/W1C
		0	ECG_ADC_SAT_STATUS	ECG ADC saturation status bit. Write 1 to this bit to clear this status.	0x0	R/W1C
0x005	GLOBAL_STATUS	[15:12]	RESERVED	Reserved.	0x0	R
		11	ECG_RLD_LEADON_HI_STATUS	ECG RLD lead-on high status bit. Write 1 to this bit to clear this status.	0x0	R/W1C
		10	ECG_RLD_LEADON_LO_STATUS	ECG RLD lead-on low status bit. Write 1 to this bit to clear this status.	0x0	R/W1C
		9	ECGIN_LEADON_HI_STATUS	ECGIN lead-on high status bit. Write 1 to this bit to clear this status.	0x0	R/W1C
		8	ECGIP_LEADON_HI_STATUS	ECGIP lead-on high status bit. Write 1 to this bit to clear this status.	0x0	R/W1C
		[7:1]	RESERVED	Reserved.	0x0	R
		0	INVALID_CFG_STATUS	Status bit indicating that TIMESLOT_PERIOD_x is not correctly configured. Write 1 to this bit to clear this status.	0x0	R/W1C
0x006	FIFO_TH	[15:10]	RESERVED	Reserved.	0x0	R
		[9:0]	FIFO_TH	FIFO interrupt generation threshold. Generate the FIFO interrupt during a FIFO write when the number of bytes in the FIFO exceeds this value.	0xC	R/W
0x007	INT_ACLEAR	15	INT_ACLEAR_FIFO	FIFO threshold Interrupt auto clear enabled. Set this bit to enable automatic clearing of the FIFO_TH interrupt each time the FIFO is read.	0x1	R/W
		[14:0]	RESERVED	Reserved.	0x0	R
0x008	CHIP_ID	[15:8]	VERSION	Mask version. R0 = 0x0.	0x0	R
		[7:0]	CHIP_ID	Chip ID.	0xC6	R
0x009	OSC32M	[15:9]	RESERVED	Reserved.	0x0	R
		8	OSC_32M_EFUSE_CTRL	Enables the high frequency oscillator frequency control from the eFuse bits. Write 0 to this bit to enable the frequency control from the OSC_32M_FREQ_ADJ bits.	0x0	R/W
		[7:0]	OSC_32M_FREQ_ADJ	High frequency oscillator frequency control. 0x000 is the lowest frequency, 0x0FF is the maximum frequency.	0x80	R/W
0x00A	OSC32M_CAL	15	OSC_32M_CAL_START	Start high frequency oscillator calibration cycle. Writing a 1 to this bit causes the high frequency oscillator calibration cycle to occur. It enables the oscillator, waits for it to start, and then counts the number 32 MHz cycles during either 128 (1 MHz) or 4 (32 kHz) low frequency cycles based on which one is selected. It updates the OSC_32M_CAL_COUNT bits with this count. The calibration circuit clears the OSC_32M_CAL_START bit when the calibration cycle completes. Silicon Version 0 counts 32 low frequency cycles if using the 32 kHz low frequency oscillator.	0x0	R/W

REGISTER DETAILS

Table 24. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
		[14:0]	OSC_32M_CAL_COUNT	High frequency oscillator calibration count. This register contains the total number of 32 MHz cycles that occurred during the last high frequency oscillator calibration cycle.	0x0	R
0x00B	OSC960K	15	CAPTURE_TIMESTAMP	Enables time stamp capture. This bit is used to arm the time stamp capture function. When set, the next rising edge on the time stamp input (defaults to GPIO0) causes a time stamp capture. This bit is cleared when the time stamp occurs.	0x0	R/W
		[14:12]	RESERVED	Reserved.	0x0	R
		11	OSC_960K_EFUSE_CTRL	Enables the frequency oscillator frequency control from the eFuse bits. Write 0 to this bit to enable the frequency control from the OSC_960K_FREQ_ADJ bits.	0x1	R/W
		10	OSC_CAL_ENABLE	Enables clock calibration clocking. Writing a 1 to this bit enables the clocking of the low frequency and high frequency calibration circuits.	0x0	R/W
		[9:0]	OSC_960K_FREQ_ADJ	Low frequency oscillator frequency control. 0x000 is the lowest frequency, and 0x3FF is the maximum frequency.	0x2B2	R/W
0x00D	TS_FREQ	[15:0]	TIMESLOT_PERIOD_L	Lower 16 bits of time slot period in low frequency oscillator cycles. The time slot rate is (timer clock frequency)/(TIMESLOT_PERIOD_x). The default value operates at 100 Hz when using the 960 kHz clock. If the timer clock is set as an external source from the GPIO, either 960 kHz or 32 kHz, TM_CLK_GPIO_SEL must be configured to match the real clock frequency.	0x2580	R/W
0x00E	TS_FREQH	[15:7]	RESERVED	Reserved.	0x0	R
		[6:0]	TIMESLOT_PERIOD_H	Upper seven bits of time slot period in low frequency oscillator cycles. The time slot rate is (timer clock frequency)/(TIMESLOT_PERIOD_x). The default value operates at 100 Hz when using the 960 kHz clock. If the timer clock is set to be an external source from the GPIO, either 960 kHz or 32 kHz, TM_CLK_GPIO_SEL must be configured to match the real clock frequency.	0x0	R/W
0x00F	SYS_CTL	15	SW_RESET	Software Reset. Write 1 to this bit to assert a software reset. This resets the chip to its default values and stopping all analog front end operations. It does not reset the SPI (or optional I^2C) port. The write to this register completes normally.	0x0	R0/W
		[14:12]	RESERVED	Reserved.	0x0	R
		11	LEAD_ON_MODE	Enables the lead-on detection mode. This mode is an ultra-low power operating mode that can be enabled when OP_MODE is set to standby or PPG only mode. When the OP_MODE is set to go with any ECG or BIOZ time slot enabled, some of the lead-on detection circuits are controlled by the ECG and BIOZ time slot operation, so the lead-on detection mode is ignored.	0x0	R/W

REGISTER DETAILS

Table 24. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
		[10:8]	ALT_CLOCKS	External clock select. 000: uses internal clocks. 001: uses GPIO for low frequency oscillator (960 kHz). Timer clock also uses this as source. 010: uses GPIO for high frequency oscillator (32 MHz). 011: uses GPIO for high frequency oscillator (32 MHz), generate the low frequency oscillator (1 MHz) from the high frequency oscillator. This feature must be disabled when the ECG is enabled. 100: uses GPIO for timer clock, 32 kHz or 960 kHz.	0x0	R/W
		[7:6]	ALT_CLK_GPIO	Alternate clock GPIO select. 00: uses GPIO0 for an alternate clock. 01: uses GPIO1 for an alternate clock. 10: reserved. 11: reserved.	0x0	R/W
		5	LP_MODE_SLEEP	Enable the low power mode during the sleep state. It is useful to reduce the power when the output data rate is slow.	0x0	R/W
		4	GO_SLEEP	Sleep before first time slot group on go. Set this bit to force a sleep period before the first sample when setting the device to run, which is especially useful for external sample triggers. 0: starts first time slot sequence on go. 1: sleep before first time slot sequence on go.	0x0	R/W
		3	RANDOM_SLEEP	Enables random sleep linear feedback shift register (LFSR). When enabled, the time slot wake up is varied ±7 cycles with the average being 0.	0x0	R/W
		2	TM_CLK_GPIO_SEL	Selects low frequency clock between 960 kHz and 32 kHz. Use this bit when ALT_CLOCKS is 3'b100. 0: uses the 32 kHz external source from the GPIO as the timer clock. 1: uses the 960 kHz external source from the GPIO as the timer clock.	0x0	R/W
		1	OSC_960K_EN	Enables low frequency oscillator. This bit turns on the 960 kHz low frequency oscillator, which must be left running during all operations using this oscillator.	0x0	R/W
		0	LOWPOWER_BIAS_EN	Enables the low power bias circuits for the lead-on detection mode and the lead-off circuits enabled in low frequency BIOZ mode. Use this bit as a test bit to force enable the low power bias circuits. This bit turns on the 960 kHz low frequency oscillator, which must be left running during all operations using this oscillator.	0x0	R/W
0x010	OPMODE	15	ECG_TIMESLOTT_EN	ECG time slot enable control. 0: disables ECG time slot. 1: enables ECG time slot.	0x0	R/W
		14	RESERVED	Reserved.	0x0	R

REGISTER DETAILS

Table 24. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
		13	BIOZ_TIMESLOT_MODE	Selects the operating mode of the BIOZ time slot. 0: high frequency BIOZ mode using 32 MHz clock. 1: low frequency BIOZ mode using 960 kHz clock.	0x0	R/W
		[12:8]	BIOZ_TIMESLOT_EN	BIOZ time slot enable control. 0: no BIOZ time slot. 1: BIOZ Time Slot Sequence A only. 10: BIOZ Time Slot Sequence AB. 11: BIOZ Time Slot Sequence ABC. 100: BIOZ Time Slot Sequence ABCD. 101: BIOZ Time Slot Sequence ABCDE. 110: BIOZ Time Slot Sequence ABCDEF. 111: BIOZ Time Slot Sequence ABCDEFG. 1000: BIOZ Time Slot Sequence ABCDEFGH. 1001: BIOZ Time Slot Sequence ABCDEFGHI. 1010: BIOZ Time Slot Sequence ABCDEFGHIJ. 1011: BIOZ Time Slot Sequence ABCDEFGHIJK. 1100: BIOZ Time Slot Sequence ABCDEFGHIJKL. 1101: BIOZ Time Slot Sequence ABCDEFGHIJKLM. 1110: BIOZ Time Slot Sequence ABCDEFGHIJKLMN. 1111: BIOZ Time Slot Sequence ABCDEFGHIJKLMNO. 10000: BIOZ Time Slot Sequence ABCDEFGHIJKLMNOP. 10001: BIOZ Time Slot Sequence ABCDEFGHIJKLMNOPQ. 10010: BIOZ Time Slot Sequence ABCDEFGHIJKLMNOPQR.	0x0	R/W
		[7:4]	PPG_TIMESLOT_EN	PPG time slot enable control. 0000: no PPG time slot. 0001: PPG Time Slot Sequence A. 0010: PPG Time Slot Sequence AB. 0011: PPG Time Slot Sequence ABC. 0100: PPG Time Slot Sequence ABCD. 0101: PPG Time Slot Sequence ABCDE. 0110: PPG Time Slot Sequence ABCDEF. 0111: PPG Time Slot Sequence ABCDEFG. 1000: PPG Time Slot Sequence ABCDEFGH. 1001: PPG Time Slot Sequence ABCDEFGHI. 1010: PPG Time Slot Sequence ABCDEFGHIJ. 1011: PPG Time Slot Sequence ABCDEFGHIJK. 1100: PPG Time Slot Sequence ABCDEFGHIJKL.	0x0	R/W
		3	RESERVED	Reserved.	0x0	R
		[2:0]	OP_MODE	Operating mode. Operating mode selection. 000: standby. 001: operate selected time slots. 011: ADC test mode. This mode goes through the normal wake-up sequence and then does	0x0	R/W

REGISTER DETAILS

Table 24. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
				continuous ADC cycles based on the PPG Time Slot A setting. 101: Repeat selected time slots without sleep. This mode does one normal wake-up sequence and then cycles through the enabled time slot sequences without going to sleep between. 111: DAC test mode. This mode goes through the normal wake-up sequence and then runs continuous DAC cycles based on the BIOZ Time Slot A settings. BIOZ Time Slot A must be enabled before starting the DAC test mode.		
0x011	STAMP_L	[15:0]	TIMESTAMP_COUNT_L	Count at last time stamp.	0x0	R
0x012	STAMP_H	[15:0]	TIMESTAMP_COUNT_H	Count at last time stamp.	0x0	R
0x013	STAMPDELTA	[15:0]	TIMESTAMP_SLOT_DELTA	Count remaining until next wake-up start.	0x0	R
0x014	INT_ENABLE_XD	15	INTX_EN_FIFO_TH	FIFO threshold interrupt enable. Write a 1 to this bit to enable drive of the FIFO threshold status to the Interrupt Channel X function.	0x0	R/W
		14	INTX_EN_FIFO_UFLOW	FIFO underflow Interrupt enable for Interrupt Channel X. Write a 1 to this bit to enable drive of the FIFO underflow status to the Interrupt Channel X function.	0x0	R/W
		13	INTX_EN_FIFO_OFLOW	FIFO overflow interrupt enable for Interrupt Channel X. Write a 1 to this bit to enable drive of the FIFO overflow status to the Interrupt Channel X function.	0x0	R/W
		[12:0]	RESERVED	Reserved.	0x0	R
0x015	INT_ENABLE_YD	15	INTY_EN_FIFO_TH	FIFO threshold interrupt enable. Write a 1 to this bit to enable drive of the FIFO threshold status to the Interrupt Channel Y function.	0x0	R/W
		14	INTY_EN_FIFO_UFLOW	FIFO underflow interrupt enable for Interrupt Channel Y. Write a 1 to this bit to enable drive of the FIFO underflow status to the Interrupt Channel Y function.	0x0	R/W
		13	INTY_EN_FIFO_OFLOW	FIFO overflow Interrupt enable for Interrupt Channel Y. Write a 1 to this bit to enable drive of the FIFO overflow status to the Interrupt Channel Y function.	0x0	R/W
		[12:0]	RESERVED	Reserved.	0x0	R
0x01E	FIFO_STATUS_BYTES	[15:10]	RESERVED	Reserved.	0x0	R
		9	ENA_STAT_ECG	Enables ECG saturation status byte.	0x1	R/W
		8	ENA_STAT_LEVX	Enables Level 0 and Level 1 interrupt status byte upper. This byte contains the interrupt status for Level Interrupt 0 and Level Interrupt 1 for PPG Time Slot I to Time Slot L.	0x0	R/W
		7	ENA_STAT_LEV1	Enables Level 1 interrupt status byte lower. This byte contains the interrupt status for Level Interrupt 1 for PPG Time Slot A to Time Slot H.	0x0	R/W

REGISTER DETAILS

Table 24. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
		6	ENA_STAT_LEV0	Enables Level 0 interrupt status byte lower. This byte contains the interrupt status for Level Interrupt 0 for PPG Time Slot A to Time Slot H.	0x0	R/W
		5	ENA_SEQ_NUM	Enables the 4-bit sequence number for the time slot sequence, which cycles from 0 to 15 and is incremented with wraparound every time the time slot sequence completes.	0x0	R/W
		[4:0]	RESERVED	Reserved.	0x0	R
0x020	INPUT_SLEEP	[15:8]	RESERVED	Reserved.	0x0	R
		[7:4]	INP_SLEEP_34	Input pair sleep state for Input 3 and Input 4. 0x0: both inputs float. 0x1: even and odd shorted together (floating short of differential). Only shorts if PAIR34 is 1. 0x2: both connected to Cathode 1 (also shorted together if configured as differential pair). 0x4: odd connected to Cathode 1. Even floating. 0x8: odd floating. Even connected to Cathode 1.	0x0	R/W
		[3:0]	INP_SLEEP_12	Input pair sleep state for Input 1 and Input 2. 0x0: both inputs float. 0x1: even and odd shorted together (floating short of differential). Only shorts if PAIR12 is 1. 0x2: both connected to Cathode 1 (also shorted together if configured as differential pair). 0x4: odd connected to Cathode 1. Even floating. 0x8: odd floating. Even connected to Cathode 1.	0x0	R/W
0x021	INPUT_CFG	[15:6]	RESERVED	Reserved.	0x0	R
		[5:4]	VC1_SLEEP	Cathode 1 sleep state. 0: cathode set to AVDD during sleep. 1: cathode set to GND during sleep. 10: cathode floating during sleep.	0x0	R/W
		[3:2]	RESERVED	Reserved.	0x0	R
		1	PAIR34	Input pair configuration. 0: uses as two single-ended inputs. 1: uses as a differential pair.	0x0	R/W
		0	PAIR12	Input pair configuration. 0: uses as two single-ended inputs. 1: used as a differential pair.	0x0	R/W
0x022	GPIO_CFG	[15:14]	GPIO_SLEW	Slew control for GPIO pins. 0: slowest. 1: slow. 10: fastest. 11: fast.	0x0	R/W
		[13:12]	GPIO_DRV	Drive control for GPIO pins. 0: medium. 1: weak. 10: strong.	0x0	R/W

REGISTER DETAILS

Table 24. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
				11: strong.		
		[11:9]	RESERVED	Reserved.	0x0	R
		[8:6]	RESERVED	Reserved.	0x0	R
		[5:3]	GPIO_PIN_CFG1	GPIO1 pin configuration. 000: disabled (tristate, input buffer off). 001: enabled Input. 010: output—normal. 011: output—inverted. 100: pull-down only—normal. 101: pull-down only—inverted. 110: pull-up only—normal. 111: pull-up only—inverted.	0x0	R/W
		[2:0]	GPIO_PIN_CFG0	GPIO0 pin configuration. 000: disabled (tristate, input buffer off). 001: enabled input. 010: output—normal. 011: output—inverted. 100: pull-down only—normal. 101: pull-down only—inverted. 110: pull-up only—normal. 111: pull-up only—inverted.	0x0	R/W
0x023	GPIO01	[15:8]	GPIOOUT1	GPIO Pin 1 Output Select. 0x00: Output 0. 0x01: Output 1. 0x02: Interrupt X. 0x03: Interrupt Y. 0x08: LED1x amplifier enable. 0x09: LED2x amplifier enable. 0x0C: any LED amplifier enable. 0x0F: 32 MHz oscillator output divided by 64 (500 kHz). 0x10: time slot specific output pattern defined by GOUT_x and GOUT_SLEEP bits. 0x16: low frequency oscillator output. 0x17: 32 MHz oscillator output. 0x18: 32 MHz oscillator output divided by 32 (1 MHz). 0x20: Time Slot A active. 0x21: Time Slot B active. 0x22: Time Slot C active. 0x23: Time Slot D active. 0x24: Time Slot E active. 0x25: Time Slot F active. 0x26: Time Slot G active. 0x27: Time Slot H active. 0x28: Time Slot I active. 0x29: Time Slot J active.	0x0	R/W

REGISTER DETAILS

Table 24. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
				0x2A: Time Slot K active. 0x2B: Time Slot L active. 0x31: Time Slot A LED pulse. 0x32: Time Slot B LED pulse. 0x33: Time Slot C LED pulse. 0x34: Time Slot D LED pulse. 0x35: Time Slot E LED pulse. 0x36: Time Slot F LED pulse. 0x37: Time Slot G LED pulse. 0x38: Time Slot H LED pulse. 0x39: Time Slot I LED pulse. 0x3A: Time Slot J LED pulse. 0x3B: Time Slot K LED pulse. 0x3C: Time Slot L LED pulse. 0x3F: Time Slot x LED pulse. 0x40: Time Slot A modulation pulse. 0x41: Time Slot B modulation pulse. 0x42: Time Slot C modulation pulse. 0x43: Time Slot D modulation pulse. 0x44: Time Slot E modulation pulse. 0x45: Time Slot F modulation pulse. 0x46: Time Slot G modulation pulse. 0x47: Time Slot H modulation pulse. 0x48: Time Slot I modulation pulse. 0x49: Time Slot J modulation pulse. 0x4A: Time Slot K modulation pulse. 0x4B: Time Slot L modulation pulse. 0x4F: Time Slot x modulation pulse. 0x50: output data cycle occurred in Time Slot A. 0x51: output data cycle occurred in Time Slot B. 0x52: output data cycle occurred in Time Slot C. 0x53: output data cycle occurred in Time Slot D. 0x54: output data cycle occurred in Time Slot E. 0x55: output data cycle occurred in Time Slot F. 0x56: output data cycle occurred in Time Slot G. 0x57: output data cycle occurred in Time Slot H. 0x58: output data cycle occurred in Time Slot I. 0x59: output data cycle occurred in Time Slot J. 0x5A: output data cycle occurred in Time Slot K. 0x5B: output data cycle occurred in Time Slot L. 0x5F: output data cycle occurred in any time slot.		
		[7:0]	GPIOOUT0	GPIO Pin 0 Output Select. Output options are identical to those described in the GPIOOUT1 bits.	0x0	R/W
0x025	GPIO_IN	[15:4]	RESERVED	Reserved.	0x0	R
		[3:0]	GPIO_INPUT	GPIO input value (if enabled).	0x0	R
0x026	GPIO_EXT	[15:9]	RESERVED	Reserved.	0x0	R
		8	GOUT_SLEEP	Time slot specific GPIO signal sleep value.	0x0	R/W

REGISTER DETAILS

Table 24. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
		7	TIMESTAMP_INV	Time stamp trigger invert. 0: time stamp trigger is rising edge. 1: time stamp trigger is falling edge.	0x0	R/W
		6	TIMESTAMP_ALWAYS_EN	Enables time stamp always on. When set, it does not automatically clear the CAPTURE_TIMESTAMP. This bit provides an always armed time stamp.	0x0	R/W
		[5:4]	TIMESTAMP_GPIO	Time stamp GPIO selection. 00: uses GPIO0 for time stamp (default). 01: uses GPIO1 for time stamp. 10: reserved. 11: reserved.	0x0	R/W
		3	RESERVED	Reserved.	0x0	R
		2	EXT_SYNC_EN	External synchronization enabled. When enabled, use the GPIO selected by EXT_SYNC_GPIO to trigger samples rather than the period counter.	0x0	R/W
		[1:0]	EXT_SYNC_GPIO	External sync GPIO selection. 00: uses GPIO0 for external synchronization (default). 01: uses GPIO1 for external synchronization. 10: reserved. 11: reserved.	0x0	R/W
0x02F	FIFO_DATA	[15:0]	FIFO_DATA	FIFO data port.	0x0	R
0x044	EFUSE	15	EFUSE_REFRESH	Write 1 to this bit to assert a shadow register reset. It enables the eFuse auto refresh operation and cause shadow registers to update from fuses. The write to this register completes normally.	0x0	R0/W
		[14:3]	RESERVED	Reserved.	0x0	R
		[2:1]	EFUSE_EN	eFuse enable. 00: off (eFuse held in reset, and shadow register is also reset). 01: reserved. 10: standby (eFuse in low power state, and shadow register available). 11: on. Must have 32 MHz high frequency oscillator running. Transitions from 00 to 11 cause shadow registers to update from fuses. Must be in on state to refresh, run built-in self test (BIST), or program. Off and standby states have lowest power. Must have 32 MHz high frequency oscillator operating for eFuse block to operate.	0x2	R/W
		0	EFUSE_REG_EN	eFuse register access enable.	0x1	R/W
0x057	IO_ADJUST	[15:7]	RESERVED	Reserved.	0x0	R
		6	LOW_IOVDD_EN	Set to 0x0 if a IOVDD of 3 V or higher is used. Default value of 1 is used for a IOVDD lower than 3 V because the typical value of IOVDD is 1.8 V.	0x1	R/W
		[5:4]	RESERVED	Reserved.	0x1	R/W
		[3:2]	SPI_SLEW	Slew control for SPI pins.	0x0	R/W

REGISTER DETAILS

Table 24. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
				0: slowest. 1: slow. 10: fastest. 11: fast.		
		[1:0]	SPI_DRV	Drive control for SPI pins. 0: medium. 1: weak. 10: strong. 11: strong.	0x0	R/W
0x100	ECG_ANA_CTRL	[15:13]	RESERVED	Reserved.	0x0	R
		12	ECG_SHORT_IN_RLD	ECG input short switch. When set to 1, it internally shorts the ECG negative side input to the RLD output. This feature can be used for ECG noise measurements.	0x0	R/W
		11	ECG_SHORT_IP_RLD	ECG input short switch. When set to 1, it internally shorts the ECG positive side input to the RLD output. This feature can be used for ECG noise measurements.	0x0	R/W
		10	RESERVED	Reserved.	0x0	R
		9	ECG_CGA_PREBUF_ALWAYSON	Keep CGA prebuffers always on.	0x0	R/W
		8	ECG_CGA_GAIN	Select CGA gain value. 0: gain = 32. 1: gain = 16.	0x0	R/W
		7	ECG_RLD_VCM_EN	Enable the V_{CM} (= AVDD3/2) generator in the RLD circuit.	0x0	R/W
		6	ECG_RLD_OUT_DISCONNECT	Disconnect the RLD output.	0x1	R/W
		[5:4]	ECG_RLD_OUT_SEL	Select the RLD output. 0: AGND. 1: AVDD3. 10: AVDD3/2 (without buffer output depending on the RLD amplifier is enabled or not). 11: regulated common-mode input.	0x3	R/W
		3	ECG_RLD_SAT_EN	Enables the DCLO for the RLD pin. 0: DCLO for RLD is disabled. 1: DCLO for RLD is enabled.	0x0	R/W
		[2:1]	ECG_RLD_SAT_THRESHOLD	DCLO threshold selection for the RLD. 0: high threshold = AVDD3 − 0.2 V and low threshold = +0.2 V. 1: high threshold = AVDD3 − 0.4 V and low threshold = +0.4 V. 10: high threshold = AVDD3 − 0.6 V and low threshold = +0.6V. 11: high threshold = AVDD3 − 0.8 V and low threshold = +0.8V.	0x0	R/W
		0	ECG_RLD_EN	Enable the RLD amplifier.	0x0	R/W
0x101	ECG_LEADOFF_CTRL	15	ECG_ACLO_EN	Enable the ACLO detector for the ECG inputs.	0x0	R/W
		[14:12]	ECG_ACLO_MAG	ACLO excite current magnitude. 0: 0 nA.	0x0	R/W

REGISTER DETAILS

Table 24. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
				1: 10 nA. 10: 20 nA. 11: 30 nA. 100: 40 nA. 101: 50 nA. 110: 60 nA. 111: 70 nA.		
		[11:9]	ECG_ACLO_THRESHOLD	ACLO threshold selection for the ECG inputs.	0x0	R/W
		8	ECG_DCLO_L_EN	Enables the low range DCLO detector circuit for ECG inputs.	0x0	R/W
		[7:4]	ECG_DCLO_MAG	DCLO excite current magnitude. 0: 0 nA. 1: reserved. 10: reserved. 11: reserved. 100: reserved. 101: reserved. 110: reserved. 111: reserved. 1000: 2 nA. 1001: 4 nA. 1010: 6 nA. 1011: 8 nA. 1100: 10 nA. 1101: 12 nA. 1110: 14 nA. 1111: 16 nA.	0x0	R/W
		3	ECG_DCLO_POLARITY_IN	DCLO output current polarity at ECGIN. 0: sink current. 1: source current.	0x0	R/W
		2	ECG_DCLO_POLARITY_IP	DCLO output current polarity at ECGIP. 0: sink current. 1: source current.	0x1	R/W
		[1:0]	ECG_DCLO_THRESHOLD	DCLO threshold selection for the ECG inputs. 0: high threshold = AVDD3 − 0.2 V. 1: high threshold = AVDD3 − 0.4 V. 10: high threshold = AVDD3 − 0.6 V. 11: high threshold = AVDD3 − 0.8 V.	0x0	R/W
0x102	ECG_DIG_CTRL1	[15:11]	RESERVED	Reserved.	0x0	R
		10	ECG_DEBOUNCER_INIT	Selects the settling time of the DCLO and ACLO debouncer after enabled. 0: same as the delay time for the DCLO and ACLO debouncer. 1: half of the delay time for the DCLO and ACLO debouncer.	0x0	R/W
		9	ECG_DEBOUNCER_SEL	Selects the delay time of the DCLO and ACLO debouncer.	0x0	R/W

REGISTER DETAILS

Table 24. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
				0: 128 ms. 1: 64 ms.		
		[8:3]	ECG_OVERSAMPLING_RATIO	This field must be configured as ratio = ECG_ODR_SEL/(960 kHz/ TIMESLOT_PERIOD_x) if using internal low frequency oscillator, or ratio = ECG_ODR_SEL/ (external sync rate) if using external triggers. The result is rounded up to the nearest integer.	0x3	R/W
		[2:0]	ECG_ODR_SEL	ECG ODR. 0: 250 Ω. 1: 500 Ω. 10: 1 kΩ. 11: 2 kΩ. 100: 4 kΩ.	0x0	R/W
0x103	ECG_DIG_CTRL2	15	ECG_DCLO_H_EN	Enables the high-range DCLO current circuit for the ECG inputs. The current polarity follows the register set by the ECG_DCLO_POLARITY_IN and ECG_DCLO_POLARITY_IP bits. The current output pin selection follows the register set by the ECG_DCLO_IP_EN and ECG_DCLO_IN_EN bits.	0x0	R/W
		[14:11]	ECG_DCLO_H_MAG	High-range DCLO excite current magnitude. 0: 0 nA. 1: 100 nA. 10: 200 nA. 11: 300 nA. 100: 400 nA. 101: 500 nA. 110: 600 nA. 111: 700 nA. 1000: reserved. 1001: reserved. 1010: reserved. 1011: reserved. 1100: 800 nA. 1101: 900 nA. 1110: 1 µA. 1111: 1.1 µA.	0x0	R/W
		10	ECG_DCLO_IP_EN	Enables the DCLO current output at ECGIP.	0x0	R/W
		9	ECG_DCLO_IN_EN	Enables the DCLO current output at ECGIN.	0x0	R/W
		8	ECG_DCLO_DET_IN_EN	Enables the DCLO detection comparator at ECGIN.	0x0	R/W
		7	ECG_DCLO_DET_IP_EN	Enables the DCLO detection comparator at ECGIP.	0x0	R/W
		6	ECG_DCLO_M_EN	Enables the DC mode of the ACLO current circuit. When set to 1, it stops the ACLO current transition and generates constant DC current outputs. The current polarity follows the register set by the ECG_DCLO_POLARITY_IN and ECG_DCLO_POLARITY_IP bits. The current output pin selection follows the register set by the	0x0	R/W

REGISTER DETAILS

Table 24. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
				ECG_DCLO_IP_EN and ECG_DCLO_IN_EN bits. The current magnitude follows the register set by the ECG_ACLO_MAG bits.		
		5	ECG_ACLO_INV	The polarity of the ACLO signal can be inverted, and this can be used to have the signal inverted on every other channel. When set to 1, ACLO is inverted, and when cleared (set to 0), ACLO is not inverted.	0x0	R/W
		4	ECG_BYPASS_EQLZR	Bypass equalizer filter in ECG post processing path.	0x0	R/W
		[3:0]	ECG_CAL_GAIN	Calibrated gain ECG. 0: 1.0000. 1: 1.0039. 10: 1.0078. 11: 1.0117. 100: 1.0156. 101: 1.0195. 110: 1.0234. 111: 1.0273. 1000: 0.9688. 1001: 0.9727. 1010: 0.9766. 1011: 0.9805. 1100: 0.9844. 1101: 0.9883. 1110: 0.9922. 1111: 0.9961.	0x0	R/W
0x104	ECG_MATRIX	[15:10]	RESERVED	Reserved.	0x0	R
		9	ECG_SWAP_POLARITY	Set to 1 to swap the ECG signal path polarity.	0x0	R/W
		8	ECG_PINS_CON_BIOZ	Set to 1 to connect the selected ECGx pins to the BIOZ path.	0x0	R/W
		7	ECG_E1_CON_ECGIP	Set to 1 to connect ECG1 pin to ECGIP.	0x0	R/W
		6	ECG_E1_CON_RLD	Set to 1 to connect ECG1 pin to RLD.	0x0	R/W
		5	ECG_E2_CON_ECGIP	Set to 1 to connect ECG2 pin to ECGIP.	0x0	R/W
		4	ECG_E2_CON_RLD	Set to 1 to connect ECG2 pin to RLD.	0x0	R/W
		3	ECG_E3_CON_ECGIN	Set to 1 to connect ECG3 pin to ECGIN.	0x0	R/W
		2	ECG_E3_CON_RLD	Set to 1 to connect ECG3 pin to RLD.	0x0	R/W
		1	ECG_E4_CON_ECGIN	Set to 1 to connect ECG4 pin to ECGIN.	0x0	R/W
		0	ECG_E4_CON_RLD	Set to 1 to connect ECG4 pin to RLD.	0x0	R/W
0x120	TS_CTRL_A	[15:14]	RESERVED	Reserved.	0x0	R
0x140 0x160 0x180 0x1A0 0x1C0 0x1E0 0x200	TS_CTRL_B TS_CTRL_C TS_CTRL_D TS_CTRL_E TS_CTRL_F TS_CTRL_G TS_CTRL_H	[13:11]	SAMPLE_TYPE_x	Time slot sampling type. 000: multiplexed one region digital integrate mode. 001: multiplexed two region digital integrate mode. 010: one region digital integrate mode. 011: two region digital integrate mode. 100: direct sample mode. 101: reserved.	0x2	R/W

REGISTER DETAILS

Table 24. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
0x220	TS_CTRL_I			110: reserved.		
0x240	TS_CTRL_J			111: reserved.		
0x260	TS_CTRL_K	10	RESERVED	Reserved.	0x0	R
0x280	TS_CTRL_L	[9:0]	TIMESLOT_OFFSET_x	Time Slot x offset in 64 × 960 kHz or 64 × (external 960 kHz) cycles.	0x0	R/W
0x121	TS_PATH_A	[15:12]	PRE_WIDTH_x	Precondition duration for this time slot. This value is in 2 µs increments. A value of 0 skips the precondition state.	0x4	R/W
0x141	TS_PATH_B	[11:10]	AMBIENT_CANCELLATION_x	Select the control type for the ambient cancellation DAC.	0x0	R/W
0x161	TS_PATH_C			0: disables the ambient cancellation loop.		
0x181	TS_PATH_D			1: enables coarse and fine loop.		
0x1A1	TS_PATH_E			10: enables coarse loop only.		
0x1C1	TS_PATH_F			11: enables MCU control.		
0x1E1	TS_PATH_G	9	GOUT_x	Time slot specific GPIO value for this time slot.	0x0	R/W
0x201	TS_PATH_H	[8:7]	RESERVED	Reserved.	0x0	R
0x221	TS_PATH_I	[6:0]	AFE_PATH_CFG_x	Bypass and input mux select. Integrator is either an integrator or buffer based on mode and AFE_INT_C_BUF for the active time slot.	0x20	R/W
0x241	TS_PATH_J			0x20: TIA, buffer, and ADC (2× TIA gain).		
0x261	TS_PATH_K			0x28: TIA buffer, and ADC (1× TIA gain).		
0x281	TS_PATH_L			0x35: buffer and ADC.		
				0x41: ADC.		
0x122	INPUTS_A	[15:14]	INP4_SEL_x	Input 4 to Channel 3 and Channel 4 enable. Set Bit 0 to 1 to enable the connection between Input 4 and Channel 3, and set Bit 1 to 1 to enable the connection between Input 4 and Channel 4.	0x0	R/W
0x142	INPUTS_B	[13:12]	INP3_SEL_x	IN3 to Channel 3 and Channel 4 enable. Set Bit 0 to 1 to enable the connection between IN3 and Channel 3, and set Bit 1 to 1 to enable the connection between IN3 and Channel 4.	0x0	R/W
0x162	INPUTS_C	[11:10]	INP2_SEL_x	IN2 to Channel 3 and Channel 4 enable. Set Bit 0 to 1 to enable the connection between IN2 and Channel 3, and set Bit 1 to 1 to enable the connection between IN2 and Channel 4.	0x0	R/W
0x182	INPUTS_D	[9:8]	INP1_SEL_x	IN1 to Channel 3 and Channel 4 enable. Set Bit 0 to 1 to enable the connection between IN1 and Channel 3, and set Bit 1 to 1 to enable the connection between IN1 and Channel 4.	0x0	R/W
0x1A2	INPUTS_E	[7:4]	INP34_x	IN3 and IN4 input pair enabled.	0x0	R/W
0x1C2	INPUTS_F			0000: input pair disabled. IN3 and IN4 disconnected.		
0x1E2	INPUTS_G			0001: IN3 connected to Channel 1 and IN4 disconnected.		
0x202	INPUTS_H			0010: IN3 connected to Channel 2 and IN4 disconnected.		
0x222	INPUTS_I			0011: IN4 connected to Channel 1 and IN3 disconnected.		
0x242	INPUTS_J			0100: IN4 connected to Channel 2 and IN3 disconnected.		
0x262	INPUTS_K			0101: IN3 connected to Channel 1 and IN4 connected to Channel 2.		

REGISTER DETAILS

Table 24. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
0x282	INPUTS_L			0110: IN4 connected to Channel 1 and IN3 connected to Channel 2. 0111: IN3 and IN4 to Channel 1, single-ended or differentially based on PAIR34, and none to Channel 2. 1000: IN3 and IN4 connected to Channel 2, and single-ended or differentially based on PAIR34.		
		[3:0]	INP12_x	IN1 and IN2 input pair enabled. 0000: input pair disabled. IN1 and IN2 disconnected. 0001: IN1 connected to Channel 1, and IN2 disconnected. 0010: IN1 connected to Channel 2, and IN2 disconnected. 0011: IN2 connected to Channel 1, and IN1 disconnected. 0100: IN2 connected to Channel 2, and IN1 disconnected. 0101: IN1 connected to Channel 1, and IN2 connected to Channel 2. 0110: IN2 connected to Channel 1, and IN1 connected to Channel 2. 0111: IN1 and IN2 connected to Channel 1, and single-ended or differentially based on PAIR12. 1000: IN1 and IN2 connected to Channel 2, and single-ended or differentially based on PAIR12.	0x0	R/W
0x123	CATHODE_A	15	RESERVED	Reserved.	0x0	R
0x143 0x163 0x183 0x1A3 0x1C3 0x1E3 0x203 0x223	CATHODE_B CATHODE_C CATHODE_D CATHODE_E CATHODE_F CATHODE_G CATHODE_H CATHODE_I	[14:12]	PRECON_x	Precondition value for enabled inputs during this time slot. 000: float inputs. 001: precondition to VC1. 010: reserved. 011: reserved. 100: precondition with TIA input. 101: precondition with TIA_VREF. 110: precondition by shorting differential pair.	0x0	R/W
0x243	CATHODE_J	[11:10]	RESERVED	Reserved.	0x0	R
0x263 0x283	CATHODE_K CATHODE_L	[9:8]	AFE_VREF_AMB_SEL_x	Voltage trim for reference buffer during the coarse ambient phase. 0: TIA_VREF = 0.8855 V, photodiode reverse bias = 600mV. 1: TIA_VREF = 0.8855 V, photodiode reverse bias = 400mV. 10: TIA_VREF = 0.8855 V, photodiode reverse bias = 200 mV. 11: TIA_VREF = 1.265 V.	0x2	R/W
		[7:6]	VC1_AMB_SEL_x	VC1 state during the coarse ambient phase. 0: AVDD. 1: TIA_VREF.	0x0	R/W

REGISTER DETAILS

Table 24. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
				10: V_DELTA (TIA_VREF + photodiode reverse bias). 11: GND.		
		[5:4]	VC1_PULSE_x	VC1 pulse control. 0: no pulsing. 1: alternate odd/even time slots. 10: pulse to alternate value using modulate pulse. 11: leave VC1 floating.	0x0	R/W
		[3:2]	VC1_ALT_x	VC1 alternate pulsed state for this time slot. 0: AVDD. 1: TIA_VREF. 10: V_DELTA. 11: GND.	0x0	R/W
		[1:0]	VC1_SEL_x	VC1 active state for this time slot. 0: AVDD. 1: TIA_VREF. 10: V_DELTA. 11: GND.	0x0	R/W
0x124	AFE_TRIM1_A	15	AFE_TIA_SAT_DETECT_EN_x	Enable TIA saturation detection. Set to 1 to enable TIA saturation detection circuitry. Enables Channel 1 and also Channel 2 if Channel 2 is enabled.	0x0	R/W
0x144	AFE_TRIM1_B	[14:13]	RESERVED	Reserved.	0x0	R
0x164 0x184 0x1A4 0x1C4 0x1E4	AFE_TRIM1_C AFE_TRIM1_D AFE_TRIM1_E AFE_TRIM1_F AFE_TRIM1_G	[12:11]	AFE_BUFFER_GAIN_x	Buffer gain selection. 0: buffer gain = 1 (R_{FB}/R_{IN} = 200 kΩ/200 kΩ). 1: buffer gain = 2 (R_{FB}/R_{IN} = 200 kΩ/100 kΩ). 10: buffer gain = 1 (R_{FB}/R_{IN} = 100 kΩ/100 kΩ). 11: buffer gain = 2 (R_{FB}/R_{IN} = 100 kΩ/50 kΩ).	0x0	R/W
0x204 0x224 0x244	AFE_TRIM1_H AFE_TRIM1_I AFE_TRIM1_J	10	VREF_PULSE_x	Reference voltage (V_{REF}) pulse control. 0: no pulsing. 1: pulse V_{REF} based on modulate pulse.	0x0	R/W
0x264 0x284	AFE_TRIM1_K AFE_TRIM1_L	[9:8]	AFE_TRIM_VREF_x	Voltage trim for reference buffer. 00: TIA_VREF = 0.8855 V, photodiode reverse bias = 600 mV. 01: TIA_VREF = 0.8855 V, photodiode reverse bias = 400 mV. 10: TIA_VREF = 0.8855 V, photodiode reverse bias = 200 mV. 11: TIA_VREF = 1.265 V.	0x2	R/W
		[7:6]	VREF_PULSE_VAL_x	V_{REF} pulse alternate value. 00: modulate TIA_VREF = 0.8855 V, photodiode reverse bias = 600 mV. 01: modulate TIA_VREF = 0.8855 V, photodiode reverse bias = 400 mV. 10: modulate TIA_VREF = 0.8855 V, photodiode reverse bias = 200 mV. 11: modulate TIA_VREF = 1.265 V.	0x3	R/W
		[5:3]	TIA_GAIN_CH2_x	TIA resistor gain setting for Channel 2. 0: 400 kΩ.	0x1	R/W

REGISTER DETAILS

Table 24. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
				1: 200 kΩ. 10: 100 kΩ. 11: 50 kΩ. 100: 25 kΩ. 101: 12.5 kΩ.		
		[2:0]	TIA_GAIN_CH1_x	TIA resistor gain setting for Channel 1. 0: 400 kΩ. 1: 200 kΩ. 10: 100 kΩ. 11: 50 kΩ. 100: 25 kΩ. 101: 12.5 kΩ.	0x1	R/W
0x125	AFE_TRIM2_A	[15:13]	RESERVED	Reserved.	0x0	R
0x145	AFE_TRIM2_B	12	AFE_BUFFER_CAP_x	Buffer feedback capacitor selection. 0: 6.3 pF. 1: 12.6 pF.	0x0	R/W
0x165	AFE_TRIM2_C					
0x185	AFE_TRIM2_D					
0x1A5	AFE_TRIM2_E	[11:6]	RESERVED	Reserved.	0x0	R
0x1C5	AFE_TRIM2_F	[5:3]	TIA_GAIN_CH4_x	TIA resistor gain setting for Channel 4. 000: 400 kΩ. 001: 200 kΩ. 010: 100 kΩ. 011: 50 kΩ. 100: 25 kΩ. 101: 12.5 kΩ.	0x0	R/W
0x1E5	AFE_TRIM2_G					
0x205	AFE_TRIM2_H					
0x225	AFE_TRIM2_I					
0x245	AFE_TRIM2_J					
0x265	AFE_TRIM2_K					
0x285	AFE_TRIM2_L					
		[2:0]	TIA_GAIN_CH3_x	TIA resistor gain setting for Channel 3. 000: 400 kΩ. 001: 200 kΩ. 010: 100 kΩ. 011: 50 kΩ. 100: 25 kΩ. 101: 12.5 kΩ.	0x0	R/W
0x126	AFE_DAC1_A	[15:7]	DAC_AMBIENT_CH1_x	Channel 1 ambient cancellation DAC code, from 0 µA to 300 µA with 0.6 µA/LSB.	0x0	R/W
0x146	AFE_DAC1_B	[6:0]	DAC_LED_DC_CH1_x	Channel 1 LED DC offset cancellation DAC code, from 0 µA to 190 µA with 1.5 µA/LSB. Set to 0 to disable.	0x0	R/W
0x166	AFE_DAC1_C					
0x186	AFE_DAC1_D					
0x1A6	AFE_DAC1_E					
0x1C6	AFE_DAC1_F					
0x1E6	AFE_DAC1_G					
0x206	AFE_DAC1_H					
0x226	AFE_DAC1_I					
0x246	AFE_DAC1_J					
0x266	AFE_DAC1_K					
0x286	AFE_DAC1_L					

REGISTER DETAILS

Table 24. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
0x127	AFE_DAC2_A	[15:7]	DAC_AMBIENT_CH2_x	Channel 2 ambient cancellation DAC code, from 0 µA to 300 µA with 0.6 µA/LSB.	0x0	R/W
0x147	AFE_DAC2_B	[6:0]	DAC_LED_DC_CH2_x	Channel 2 LED DC offset cancellation DAC code, from 0 µA to 190 µA with 1.5 µA/LSB. Set to 0 to disable.	0x0	R/W
0x167	AFE_DAC2_C					
0x187	AFE_DAC2_D					
0x1A7	AFE_DAC2_E					
0x1C7	AFE_DAC2_F					
0x1E7	AFE_DAC2_G					
0x207	AFE_DAC2_H					
0x227	AFE_DAC2_I					
0x247	AFE_DAC2_J					
0x267	AFE_DAC2_K					
0x287	AFE_DAC2_L					
0x128	LED_POW12_A	15	RESERVED	Reserved.	0x0	R
0x148	LED_POW12_B	[14:8]	LED_CURRENT2_x	LED current setting for the LED2A, LED2B, LED2C, or LED2D output. Set to 0 to disable. Output current varies monotonically from 1.57 mA to 200 mA for values between 0x01 and 0x7F.	0x0	R/W
0x168	LED_POW12_C	7	RESERVED	Reserved.	0x0	R
0x188	LED_POW12_D	[6:0]	LED_CURRENT1_x	Led current setting for the LED1A, LED1B, LED1C, or LED1D output. Set to 0 to disable. Output current varies monotonically from 1.57 mA to 200 mA for values between 0x01 and 0x7F.	0x0	R/W
0x1A8	LED_POW12_E					
0x1C8	LED_POW12_F					
0x1E8	LED_POW12_G					
0x208	LED_POW12_H					
0x228	LED_POW12_I					
0x248	LED_POW12_J					
0x268	LED_POW12_K					
0x288	LED_POW12_L					
0x129	LED_MODE_A	[15:8]	RESERVED	Reserved.	0x0	R
0x149	LED_MODE_B	[7:6]	LED_DRIVESIDE2_x	Led output select for LED2x. 00: drives LED on Output LED2A. 01: drives LED on Output LED2B. 10: drives LED on Output LED2C. 11: drives LED on Output LED2D.	0x0	R/W
0x169	LED_MODE_C					
0x189	LED_MODE_D					
0x1A9	LED_MODE_E					
0x1C9	LED_MODE_F					
0x1E9	LED_MODE_G	[5:4]	LED_DRIVESIDE1_x	Led output select for LED1x. 00: drives LED on Output LED1A. 01: drives LED on Output LED1B. 10: drives LED on Output LED1C. 11: drives LED on Output LED1D.	0x0	R/W
0x209	LED_MODE_H					
0x229	LED_MODE_I					
0x249	LED_MODE_J					
0x269	LED_MODE_K					
0x289	LED_MODE_L	[3:2]	RESERVED	Reserved.	0x0	R
		1	LED_MODE2_x	Choose the operation mode of the LED2x. 0: high SNR mode. 1: low compliance mode.	0x0	R/W
		0	LED_MODE1_x	Choose the operation mode of the LED1x.	0x0	R/W

REGISTER DETAILS

Table 24. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
				0: high SNR mode. 1: low compliance mode.		
0x12A	COUNTS_A	[15:8]	NUM_INT_x	Number of ADC cycles or acquisition width. Number of analog integration cycles per ADC conversion or the acquisition width for digital integration. A setting of 0 is not allowed.	0x1	R/W
0x14A 0x16A 0x18A 0x1AA 0x1CA 0x1EA 0x20A 0x22A 0x24A 0x26A 0x28A	COUNTS_B COUNTS_C COUNTS_D COUNTS_E COUNTS_F COUNTS_G COUNTS_H COUNTS_I COUNTS_J COUNTS_K COUNTS_L	[7:0]	NUM_REPEAT_x	Number of sequence repeats. Total number of pulses = NUM_INT_x × NUM_REPEAT_x. A setting of 0 is not allowed.	0x1	R/W
0x12B	PERIOD_A	15	RESERVED	Reserved.	0x0	R
0x14B 0x16B 0x18B 0x1AB 0x1CB	PERIOD_B PERIOD_C PERIOD_D PERIOD_E PERIOD_F	14	COARSE_LOOP_WIDTH_x	The time duration for the coarse ambient cancellation loop. 0: 10 µs. 1: 20 µs.	0x0	R/W
0x1EB 0x20B 0x22B 0x24B	PERIOD_G PERIOD_H PERIOD_I PERIOD_J	[13:12]	MOD_TYPE_x	Modulation connection type. 00: TIA is continuously connected to the input after the precondition. No connection modulation. 01: float type operation. Pulse connection from the input to the TIA with modulate pulse, floating between pulses. 10: nonfloat type connection modulation. Pulse connection from the input to the TIA. Connect to the precondition value between pulses.	0x0	R/W
0x26B	PERIOD_K	[11:10]	RESERVED	Reserved.	0x0	R
0x28B	PERIOD_L	[9:0]	MIN_PERIOD_x	Minimum period for pulse repetition. Override for the automatically calculated period. Used in float type operations to set the float time of second and subsequent floats using the formula float = MIN_PERIOD_x − MOD_WIDTH_x.	0x0	R/W
0x12C	LED_PULSE1_A	[15:8]	LED_WIDTH_A	LED pulse width.	0x2	R/W
0x14C 0x16C 0x18C 0x1AC 0x1CC 0x1EC	LED_PULSE1_B LED_PULSE1_C LED_PULSE1_D LED_PULSE1_E LED_PULSE1_F LED_PULSE1_G	[7:0]	LED_OFFSET_A	LED pulse offset.	0x10	R/W

REGISTER DETAILS

Table 24. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
0x20C	LED_PULSE1_H					
0x22C	LED_PULSE1_I					
0x24C	LED_PULSE1_J					
0x26C	LED_PULSE1_K					
0x28C	LED_PULSE1_L					
0x12D	AFE_DAC3_A	[15:7]	DAC_AMBIENT_CH3_x	Channel 3 ambient cancellation DAC code, from 0 µA to 300 µA with 0.6 µA/LSB.	0x0	R/W
0x14D	AFE_DAC3_B	[6:0]	DAC_LED_DC_CH3_x	Channel 3 LED DC offset cancellation DAC code, from 0 µA to 190 µA with 1.5 µA/LSB. Set to 0 to disable.	0x0	R/W
0x16D	AFE_DAC3_C					
0x18D	AFE_DAC3_D					
0x1AD	AFE_DAC3_E					
0x1CD	AFE_DAC3_F					
0x1ED	AFE_DAC3_G					
0x20D	AFE_DAC3_H					
0x22D	AFE_DAC3_I					
0x24D	AFE_DAC3_J					
0x26D	AFE_DAC3_K					
0x28D	AFE_DAC3_L					
0x12E	AFE_DAC4_A	[15:7]	DAC_AMBIENT_CH4_x	Channel 4 ambient cancellation DAC code, from 0 µA to 300 µA with 0.6 µA/LSB.	0x0	R/W
0x14E	AFE_DAC4_B	[6:0]	DAC_LED_DC_CH4_x	Channel 4 LED DC offset cancellation DAC code, from 0 µA to 190 µA with 1.5 µA/LSB. Set to 0 to disable.	0x0	R/W
0x16E	AFE_DAC4_C					
0x18E	AFE_DAC4_D					
0x1AE	AFE_DAC4_E					
0x1CE	AFE_DAC4_F					
0x1EE	AFE_DAC4_G					
0x20E	AFE_DAC4_H					
0x22E	AFE_DAC4_I					
0x24E	AFE_DAC4_J					
0x26E	AFE_DAC4_K					
0x28E	AFE_DAC4_L					
0x12F	THRESH0_A	[15:13]	RESERVED	Reserved.	0x0	R
0x14F	THRESH0_B	[12:8]	THRESH0_SHIFT_x	Shift for threshold compare Level Interrupt 0. Shift THRESH0_VALUE_x by this amount before comparing.	0x0	R/W
0x16F	THRESH0_C	[7:0]	THRESH0_VALUE_x	Value for threshold compare Level Interrupt 0.	0x0	R/W
0x18F	THRESH0_D					
0x1AF	THRESH0_E					
0x1CF	THRESH0_F					
0x1EF	THRESH0_G					
0x20F	THRESH0_H					
0x22F	THRESH0_I					
0x24F	THRESH0_J					
0x26F	THRESH0_K					
0x28F	THRESH0_L					

REGISTER DETAILS

Table 24. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
0x130	MOD_PULSE_A	[15:8]	MOD_WIDTH_x	Modulation pulse width. 0 = disable.	0x0	R/W
0x150	MOD_PULSE_B	[7:0]	MOD_OFFSET_x	Modulation pulse offset.	0x1	R/W
0x170	MOD_PULSE_C					
0x190	MOD_PULSE_D					
0x1B0	MOD_PULSE_E					
0x1D0	MOD_PULSE_F					
0x1F0	MOD_PULSE_G					
0x210	MOD_PULSE_H					
0x230	MOD_PULSE_I					
0x250	MOD_PULSE_J					
0x270	MOD_PULSE_K					
0x290	MOD_PULSE_L					
0x131	PATTERN1_A	[15:12]	LED_DISABLE_x	Four pulse LED disable pattern. Set to 1 to disable the LED pulse in the matching position in a group of four pulses. The LSB maps to the first pulse.	0x0	R/W
0x151	PATTERN1_B	[11:8]	MOD_DISABLE_x	Four pulse modulation disable pattern. Set to 1 to disable the modulation pulse in the matching position in a group of four pulses. The LSB maps to the first pulse.	0x0	R/W
0x171	PATTERN1_C	[7:4]	SUBTRACT_x	Four pulse subtract pattern. Set to 1 to negate the math operation in the matching position in a group of four pulses. The LSB maps to the first pulse.	0x0	R/W
0x191	PATTERN1_D	[3:0]	AFE_SWAP_x	Four pulse integration reverse pattern. Set to 1 to reverse the integrator positive or negative pulse order in the matching position in a group of four pulses. The LSB maps to the first pulse.	0x0	R/W
0x1B1	PATTERN1_E					
0x1D1	PATTERN1_F					
0x1F1	PATTERN1_G					
0x211	PATTERN1_H					
0x231	PATTERN1_I					
0x251	PATTERN1_J					
0x271	PATTERN1_K					
0x291	PATTERN1_L					
0x132	THRESH_CFG_A	[15:11]	RESERVED	Reserved.	0x0	R
0x152	THRESH_CFG_B	10	THRESH1_DIR_x	Type of comparison for Level Interrupt 1. 0: set when less than the threshold. 1: set when more than the threshold.	0x0	R/W
0x172	THRESH_CFG_C					
0x192	THRESH_CFG_D					
0x1B2	THRESH_CFG_E	[9:8]	THRESH1_TYPE_x	Type of comparison for Level Interrupt 1. 0: off (no comparison). 1: compare to signal. 10: compare to lit. 11: compare to dark.	0x0	R/W
0x1D2	THRESH_CFG_F					
0x1F2	THRESH_CFG_G					
0x212	THRESH_CFG_H					
0x232	THRESH_CFG_I					
0x252	THRESH_CFG_J	[7:3]	RESERVED	Reserved.	0x0	R
0x272	THRESH_CFG_K	2	THRESH0_DIR_x	Type of comparison for Level Interrupt 0. 0: set when less than the threshold. 1: set when more than the threshold.	0x0	R/W
0x292	THRESH_CFG_L					
		[1:0]	THRESH0_TYPE_x	Type of comparison for Level Interrupt 0.	0x0	R/W

REGISTER DETAILS

Table 24. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
				0: off (no comparison). 1: compare to signal. 10: compare to lit. 11: compare to dark.		
0x133	ADC_OFF1_A	[15:14]	RESERVED	Reserved.	0x0	R
0x153	ADC_OFF1_B	[13:0]	CH1_ADC_ADJUST_x	Adjustment to the ADC value, which is subtracted from the ADC value for Channel 1.	0x0	R/W
0x173	ADC_OFF1_C					
0x193	ADC_OFF1_D					
0x1B3	ADC_OFF1_E					
0x1D3	ADC_OFF1_F					
0x1F3	ADC_OFF1_G					
0x213	ADC_OFF1_H					
0x233	ADC_OFF1_I					
0x253	ADC_OFF1_J					
0x273	ADC_OFF1_K					
0x293	ADC_OFF1_L					
0x134	ADC_OFF2_A	[15:14]	RESERVED	Reserved.	0x0	R/W
0x154	ADC_OFF2_B	[13:0]	CH2_ADC_ADJUST_x	Adjustment to the ADC value, which is subtracted from the ADC value for Channel 2.	0x0	R/W
0x174	ADC_OFF2_C					
0x194	ADC_OFF2_D					
0x1B4	ADC_OFF2_E					
0x1D4	ADC_OFF2_F					
0x1F4	ADC_OFF2_G					
0x214	ADC_OFF2_H					
0x234	ADC_OFF2_I					
0x254	ADC_OFF2_J					
0x274	ADC_OFF2_K					
0x294	ADC_OFF2_L					
0x135	DATA1_A	[15:11]	DARK_SHIFT_x	Dark data shift.	0x0	R/W
0x155	DATA1_B	[10:8]	DARK_SIZE_x	Dark data size.	0x0	R/W
0x175	DATA1_C	[7:3]	SIGNAL_SHIFT_x	Signal data shift.	0x0	R/W
0x195	DATA1_D	[2:0]	SIGNAL_SIZE_x	Signal data size.	0x3	R/W
0x1B5	DATA1_E					
0x1D5	DATA1_F					
0x1F5	DATA1_G					
0x215	DATA1_H					
0x235	DATA1_I					
0x255	DATA1_J					
0x275	DATA1_K					
0x295	DATA1_L					
0x136	DATA2_A	[15:8]	RESERVED	Reserved.	0x0	R
0x156	DATA2_B	[7:3]	LIT_SHIFT_x	Lit data shift.	0x0	R/W

REGISTER DETAILS

Table 24. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
0x176	DATA2_C	[2:0]	LIT_SIZE_x	Lit data size.	0x0	R/W
0x196	DATA2_D					
0x1B6	DATA2_E					
0x1D6	DATA2_F					
0x1F6	DATA2_G					
0x216	DATA2_H					
0x236	DATA2_I					
0x256	DATA2_J					
0x276	DATA2_K					
0x296	DATA2_L					
0x137	DECIMATE_A	[15:14]	CHANNEL_EN_x	Channel enable. 00: only Channel 1 enabled. 01: Channel 1 and Channel 2 enabled. 10: Channel 1, Channel 2, and Channel 3 enabled. 11: Channel 1, Channel 2, Channel 3, and Channel 4 enabled.	0x0	R/W
0x157	DECIMATE_B					
0x177	DECIMATE_C					
0x197	DECIMATE_D					
0x1B7	DECIMATE_E					
0x1D7	DECIMATE_F	[13:11]	RESERVED	Reserved.	0x0	R
0x1F7	DECIMATE_G	[10:4]	SUBSAMPLE_RATIO_x	Reduce the output data rate that is equal to (the timer clock frequency)/(TIMESLOT_PERIOD_x)/(SUBSAMPLE_RATIO_x).When this bit is set larger than 1, operate the time slot only once per (SUBSAMPLE_RATIO_x) time slot sequence. This subsampling aligns to other time slots using the same SUBSAMPLE_RATIO_x. It skips (SUBSAMPLE_RATIO_x − 1) times and then executes the time slot. Output data rate is the sample rate/(SUBSAMPLE_RATIO_x).	0x1	R/W
0x217	DECIMATE_H	[3:0]	RESERVED	Reserved.	0x0	R
0x237	DECIMATE_I					
0x257	DECIMATE_J					
0x277	DECIMATE_K					
0x297	DECIMATE_L					
0x138	DIGINT_LIT_A	[15:9]	RESERVED	Reserved.	0x0	R
0x158	DIGINT_LIT_B	[8:0]	LIT_OFFSET_x	Acquisition Window Lit Offset for Time Slot x.	0x26	R/W
0x178	DIGINT_LIT_C					
0x198	DIGINT_LIT_D					
0x1B8	DIGINT_LIT_E					
0x1D8	DIGINT_LIT_F					
0x1F8	DIGINT_LIT_G					
0x218	DIGINT_LIT_H					
0x238	DIGINT_LIT_I					
0x258	DIGINT_LIT_J					
0x278	DIGINT_LIT_K					
0x298	DIGINT_LIT_L					
0x139	DIGINT_DARK_A	[15:7]	DARK2_OFFSET_x	Acquisition window Dark Offset 2 for Time Slot x.	0x1	R/W
0x159	DIGINT_DARK_B	[6:0]	DARK1_OFFSET_x	Acquisition window Dark Offset 1 for Time Slot x.	0x6	R/W

REGISTER DETAILS

Table 24. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
0x179	DIGINT_DARK_C					
0x199	DIGINT_DARK_D					
0x1B9	DIGINT_DARK_E					
0x1D9	DIGINT_DARK_F					
0x1F9	DIGINT_DARK_G					
0x219	DIGINT_DARK_H					
0x239	DIGINT_DARK_I					
0x259	DIGINT_DARK_J					
0x279	DIGINT_DARK_K					
0x299	DIGINT_DARK_L					
0x13A	ADC_OFF3_A	[15:14]	RESERVED	Reserved.	0x0	R
0x15A	ADC_OFF3_B	[13:0]	CH3_ADC_ADJUST_x	Adjustment to ADC value, which is subtracted from the ADC value for Channel 3.	0x0	R/W
0x17A	ADC_OFF3_C					
0x19A	ADC_OFF3_D					
0x1BA	ADC_OFF3_E					
0x1DA	ADC_OFF3_F					
0x1FA	ADC_OFF3_G					
0x21A	ADC_OFF3_H					
0x23A	ADC_OFF3_I					
0x25A	ADC_OFF3_J					
0x27A	ADC_OFF3_K					
0x29A	ADC_OFF3_L					
0x13B	ADC_OFF4_A	[15:14]	RESERVED	Reserved.	0x0	R
0x15B	ADC_OFF4_B	[13:0]	CH4_ADC_ADJUST_x	Adjustment to ADC value, which is subtracted from the ADC value for Channel 4.	0x0	R/W
0x17B	ADC_OFF4_C					
0x19B	ADC_OFF4_D					
0x1BB	ADC_OFF4_E					
0x1DB	ADC_OFF4_F					
0x1FB	ADC_OFF4_G					
0x21B	ADC_OFF4_H					
0x23B	ADC_OFF4_I					
0x25B	ADC_OFF4_J					
0x27B	ADC_OFF4_K					
0x29B	ADC_OFF4_L					
0x13C	THRESH1_A	[15:13]	RESERVED	Reserved.	0x0	R
0x15C	THRESH1_B	[12:8]	THRESH1_SHIFT_x	Shift for threshold compare Level Interrupt 1. Shift THRESH0_VALUE_x by this amount before comparing.	0x0	R/W
0x17C	THRESH1_C	[7:0]	THRESH1_VALUE_x	Value for threshold compare Level Interrupt 1.	0x0	R/W
0x19C	THRESH1_D					
0x1BC	THRESH1_E					
0x1DC	THRESH1_F					
0x1FC	THRESH1_G					
0x21C	THRESH1_H					

REGISTER DETAILS

Table 24. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
0x23C	THRESH1_I					
0x25C	THRESH1_J					
0x27C	THRESH1_K					
0x29C	THRESH1_L					
0x2A0	BIOZ_AFECON_A	[15:14]	RESERVED	Reserved.	0x0	R
0x2B0	BIOZ_AFECON_B	13	BIOZ_DACREF_LPMODE_x	Low power mode enable for the DAC reference block. 0: high power mode. 1: low power mode.	0x0	R/W
0x2C0	BIOZ_AFECON_C					
0x2D0	BIOZ_AFECON_D					
0x2E0	BIOZ_AFECON_E	12	BIOZ_REFNORM_x	Set different power mode for DAC. 0: high power mode. 1: low power mode.	0x0	R/W
0x2F0	BIOZ_AFECON_F					
0x300	BIOZ_AFECON_G					
0x310	BIOZ_AFECON_H	[11:2]	BIOZ_TIMESLOT_OFFSET_x	BIOZ Time Slot x Offset in 64 × 960 kHz or 64 × (external 960 kHz) cycles.	0x0	R/W
0x320	BIOZ_AFECON_I	1	BIOZ_TIAEN_x	High power TIA enable. Enable high power TIA.	0x0	R/W
0x330	BIOZ_AFECON_J	0	BIOZ_EXCITATION_TYPE_x	Excitation source type selection. 0: voltage from BIOZ DAC. 1: current from DCLO circuits.	0x0	R/W
0x340	BIOZ_AFECON_K					
0x350	BIOZ_AFECON_L					
0x360	BIOZ_AFECON_M					
0x370	BIOZ_AFECON_N					
0x380	BIOZ_AFECON_O					
0x390	BIOZ_AFECON_P					
0x3A0	BIOZ_AFECON_Q					
0x3B0	BIOZ_AFECON_R					
0x2A1	BIOZ_WGFCW_LOW_A	[15:0]	BIOZ_SINEFCW_L_x	Sinusoid generator frequency control word. BIOZ_SINEFCW_H_x and BIOZ_SINEFCW_L_x constitute BIOZ_SINEFCW_x_x, Bits[19:0]. BIOZ_SINEFCW_x_x, Bits[19:0] = 2^{26} × f/32^6 or 2^{26} × f/960 kHz, f is the frequency value of the sinusoid. To get an accurate DFT result and avoid spectral leakage, recommend f/(DFT_FS/N) to be integer. N means the number of DFT input data, and DFT_FS means the DFT input data rate. DFT_FS can be different due to different input data sources.	0x0	R/W
0x2B1	BIOZ_WGFCW_LOW_B					
0x2C1	BIOZ_WGFCW_LOW_C					
0x2D1	BIOZ_WGFCW_LOW_D					
0x2E1	BIOZ_WGFCW_LOW_E					
0x2F1	BIOZ_WGFCW_LOW_F					
0x301	BIOZ_WGFCW_LOW_G					
0x311	BIOZ_WGFCW_LOW_H					
0x321	BIOZ_WGFCW_LOW_I					
0x331	BIOZ_WGFCW_LOW_J					
0x341	BIOZ_WGFCW_LOW_K					
0x351	BIOZ_WGFCW_LOW_L					
0x361	BIOZ_WGFCW_LOW_M					
0x371	BIOZ_WGFCW_LOW_N					
0x381	BIOZ_WGFCW_LOW_O					
0x391	BIOZ_WGFCW_LOW_P					
0x3A1	BIOZ_WGFCW_LOW_Q					
0x3B1	BIOZ_WGFCW_LOW_R					
0x2A2	BIOZ_WGFCW_HI_A	15	BIOZ_DATA_SELECTION_x	BIOZ output 32-bit data selection.	0x0	R/W

REGISTER DETAILS

Table 24. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
0x2B2	BIOZ_WGFCW_HI_B			0: one byte of the BIOZ ADC saturation status + three bytes of BIOZ data.		
0x2C2	BIOZ_WGFCW_HI_C			1: 4 bytes of the BIOZ 32-bit raw data.		
0x2D2	BIOZ_WGFCW_HI_D	[14:12]	BIOZ_NCHAN_ALT_x	N-channel alternate input selection.	0x0	R/W
0x2E2	BIOZ_WGFCW_HI_E			0: connects HPTIA_n to BUFFER_N (the negative input of the buffer).		
0x2F2	BIOZ_WGFCW_HI_F			1: connects IMPIN to BUFFER_N.		
0x302	BIOZ_WGFCW_HI_G			10: connects EXCP to BUFFER_N.		
0x312	BIOZ_WGFCW_HI_H			11: connects R_{INT_SN} to BUFFER_N.		
0x322	BIOZ_WGFCW_HI_I			100: connects IMPIP to BUFFER_N.		
0x332	BIOZ_WGFCW_HI_J			101: connects EXCN to BUFFER_N.		
0x342	BIOZ_WGFCW_HI_K			110: connects ECG RLD to BUFFER_N.		
0x352	BIOZ_WGFCW_HI_L			111: connects ECGIP to BUFFER_N.		
0x362	BIOZ_WGFCW_HI_M	[11:9]	BIOZ_PCHAN_ALT_x	P-channel alternate input selection.	0x0	R/W
0x372	BIOZ_WGFCW_HI_N			0: connects HPTIA_p to BUFFER_P (the positive input of the buffer).		
0x382	BIOZ_WGFCW_HI_O			1: connects IMPIP to BUFFER_P.		
0x392	BIOZ_WGFCW_HI_P			10: connects EXCN to BUFFER_P.		
0x3A2	BIOZ_WGFCW_HI_Q			11: connects R_{INT_SP} to BUFFER_P		
0x3B2	BIOZ_WGFCW_HI_R			100: connects IMPIN to BUFFER_P.		
				101: connects EXCP to BUFFER_P.		
				110: connects ECGIN to BUFFER_P.		
				111: connects ECGIP to BUFFER_P.		
		[8:4]	RESERVED	Reserved.	0x0	R
		[3:0]	BIOZ_SINEFCW_H_x	Sinusoid generator frequency control word. BIOZ_SINEFCW_H_x and BIOZ_SINEFCW_L_x constitute BIOZ_SINEFCW_x_x, Bits[19:0]. BIOZ_SINEFCW_x_x, Bits[19:0] = 2^{26} × f/32^6 or 2^{26} × f/960 kHz, f is the frequency value of the sinusoid. To get an accurate DFT result and avoid spectral leakage, recommend f/(DFT_FS/N) to be integer. N means the number of DFT input data, and DFT_FS means the DFT input data rate. DFT_FS can be different due to different input data sources.	0x0	R/W
0x2A3	BIOZ_WGPHASE_A	[15:0]	BIOZ_SINE_PHASE_OFFSET_x	Sinusoid phase offset. BIOZ_SINE_PHASE_OFFSET_x, Bits[15:0] = Phase (Degree)/360 × 2^{16}. For example, to get 45° phase offset, set BIOZ_SINE_PHASE_OFFSET_x, Bits[15:0] = 45°/360 × 2^{16}.	0x0	R/W
0x2B3	BIOZ_WGPHASE_B					
0x2C3	BIOZ_WGPHASE_C					
0x2D3	BIOZ_WGPHASE_D					
0x2E3	BIOZ_WGPHASE_E					
0x2F3	BIOZ_WGPHASE_F					
0x303	BIOZ_WGPHASE_G					
0x313	BIOZ_WGPHASE_H					
0x323	BIOZ_WGPHASE_I					
0x333	BIOZ_WGPHASE_J					
0x343	BIOZ_WGPHASE_K					

REGISTER DETAILS

Table 24. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
0x353	BIOZ_WGPHASE_L					
0x363	BIOZ_WGPHASE_M					
0x373	BIOZ_WGPHASE_N					
0x383	BIOZ_WGPHASE_O					
0x393	BIOZ_WGPHASE_P					
0x3A3	BIOZ_WGPHASE_Q					
0x3B3	BIOZ_WGPHASE_R					
0x2A4	BIOZ_DFTPHASE_A	[15:0]	BIOZ_DFT_PHASE_OFFSET_x	BIOZ_DFT_PHASE_OFFSET_x, Bits[15:0] = Phase (Degree)/360 × 2^{16}. For example, to get 45° phase offset, set BIOZ_DFT_PHASE_OFFSET_x, Bits[15:0] = 45°/360 × 2^{16}.	0x0	R/W
0x2B4	BIOZ_DFTPHASE_B					
0x2C4	BIOZ_DFTPHASE_C					
0x2D4	BIOZ_DFTPHASE_D					
0x2E4	BIOZ_DFTPHASE_E					
0x2F4	BIOZ_DFTPHASE_F					
0x304	BIOZ_DFTPHASE_G					
0x314	BIOZ_DFTPHASE_H					
0x324	BIOZ_DFTPHASE_I					
0x334	BIOZ_DFTPHASE_J					
0x344	BIOZ_DFTPHASE_K					
0x354	BIOZ_DFTPHASE_L					
0x364	BIOZ_DFTPHASE_M					
0x374	BIOZ_DFTPHASE_N					
0x384	BIOZ_DFTPHASE_O					
0x394	BIOZ_DFTPHASE_P					
0x3A4	BIOZ_DFTPHASE_Q					
0x3B4	BIOZ_DFTPHASE_R					
0x2A5	BIOZ_WGOFFSET_A	[15:12]	RESERVED	Reserved.	0x0	R
0x2B5	BIOZ_WGOFFSET_B	[11:0]	BIOZ_SINE_OFFSET_x	Sinusoid offset. Added to the waveform generator output in sinusoid mode. Signed number represented in twos complement format.	0x0	R/W
0x2C5	BIOZ_WGOFFSET_C					
0x2D5	BIOZ_WGOFFSET_D					
0x2E5	BIOZ_WGOFFSET_E					
0x2F5	BIOZ_WGOFFSET_F					
0x305	BIOZ_WGOFFSET_G					
0x315	BIOZ_WGOFFSET_H					
0x325	BIOZ_WGOFFSET_I					
0x335	BIOZ_WGOFFSET_J					
0x345	BIOZ_WGOFFSET_K					
0x355	BIOZ_WGOFFSET_L					
0x365	BIOZ_WGOFFSET_M					
0x375	BIOZ_WGOFFSET_N					
0x385	BIOZ_WGOFFSET_O					
0x395	BIOZ_WGOFFSET_P					
0x3A5	BIOZ_WGOFFSET_Q					
0x3B5	BIOZ_WGOFFSET_R					
0x2A6	BIOZ_WGAMPLITUDE_A	[15:11]	RESERVED	Reserved.	0x0	R

REGISTER DETAILS

Table 24. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
0x2B6	BIOZ_WGAMPLITUDE_B	[10:0]	BIOZ_SINEAMPLITUDE_x	Sinusoid amplitude. Unsigned number. Scales the waveform generator in sinusoid mode. Gain coefficient = BIOZ_SINEAMPLITUDE_x, Bits[10:0]/(2^{11}). Maximum output is 800 mV.	0x600	R/W
0x2C6	BIOZ_WGAMPLITUDE_C					
0x2D6	BIOZ_WGAMPLITUDE_D					
0x2E6	BIOZ_WGAMPLITUDE_E					
0x2F6	BIOZ_WGAMPLITUDE_F					
0x306	BIOZ_WGAMPLITUDE_G					
0x316	BIOZ_WGAMPLITUDE_H					
0x326	BIOZ_WGAMPLITUDE_I					
0x336	BIOZ_WGAMPLITUDE_J					
0x346	BIOZ_WGAMPLITUDE_K					
0x356	BIOZ_WGAMPLITUDE_L					
0x366	BIOZ_WGAMPLITUDE_M					
0x376	BIOZ_WGAMPLITUDE_N					
0x386	BIOZ_WGAMPLITUDE_O					
0x396	BIOZ_WGAMPLITUDE_P					
0x3A6	BIOZ_WGAMPLITUDE_Q					
0x3B6	BIOZ_WGAMPLITUDE_R					
0x2A7	BIOZ_DACCON_A	[15:14]	RESERVED	Reserved.	0x0	R
0x2B7	BIOZ_DACCON_B	13	BIOZ_EXBUFEN_x	Enable excitation buffer. Enable excitation buffer to drive the resistance under measurement. 0: disabled. 1: enabled.	0x0	R/W
0x2C7	BIOZ_DACCON_C					
0x2D7	BIOZ_DACCON_D					
0x2E7	BIOZ_DACCON_E	[12:10]	BIOZ_DACBUFBW_x	DAC reconstruction filter power consumption tuning. 0: bypass the reconstruction filter. 1: 30 µA. 10: 40 µA. 100: 111 µA.	0x4	R/W
0x2F7	BIOZ_DACCON_F					
0x307	BIOZ_DACCON_G					
0x317	BIOZ_DACCON_H					
0x327	BIOZ_DACCON_I					
0x337	BIOZ_DACCON_J	9	BIOZ_BW200KEN_x	Reconstruction filter cutoff frequency of 200 kHz. 0: disables 200 kHz cutoff frequency. 1: enables 200 kHz cutoff frequency.	0x1	R/W
0x347	BIOZ_DACCON_K					
0x357	BIOZ_DACCON_L					
0x367	BIOZ_DACCON_M	8	BIOZ_BW50KEN_x	Reconstruction filter cutoff frequency of 50 kHz. 0: disables 50 kHz cutoff frequency. 1: enables 50 kHz cutoff frequency.	0x0	R/W
0x377	BIOZ_DACCON_N					
0x387	BIOZ_DACCON_O					
0x397	BIOZ_DACCON_P	[7:0]	BIOZ_RATE_DIV_x	DAC update rate. DAC update rate = 32 MHz/BIOZ_RATE_DIV_x or 960 kHz/BIOZ_RATE_DIV_x.	0xD	R/W
0x3A7	BIOZ_DACCON_Q					
0x3B7	BIOZ_DACCON_R					
0x2A8	BIOZ_ADC_LEVEL_A	[15:8]	BIOZ_ADC_LEVEL_H_x	High threshold level for ADC saturation detection. The LSB corresponds to ADC LSB × 64.	0xFF	R/W
0x2B8	BIOZ_ADC_LEVEL_B	[7:0]	BIOZ_ADC_LEVEL_L_x	Low threshold level for ADC saturation detection. The LSB corresponds to ADC LSB × 64.	0x0	R/W
0x2C8	BIOZ_ADC_LEVEL_C					
0x2D8	BIOZ_ADC_LEVEL_D					
0x2E8	BIOZ_ADC_LEVEL_E					
0x2F8	BIOZ_ADC_LEVEL_F					
0x308	BIOZ_ADC_LEVEL_G					
0x318	BIOZ_ADC_LEVEL_H					

REGISTER DETAILS

Table 24. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
0x328 0x338 0x348 0x358 0x368 0x378 0x388 0x398 0x3A8 0x3B8	BIOZ_ADC_LEVEL_I BIOZ_ADC_LEVEL_J BIOZ_ADC_LEVEL_K BIOZ_ADC_LEVEL_L BIOZ_ADC_LEVEL_M BIOZ_ADC_LEVEL_N BIOZ_ADC_LEVEL_O BIOZ_ADC_LEVEL_P BIOZ_ADC_LEVEL_Q BIOZ_ADC_LEVEL_R					
0x2A9 0x2B9 0x2C9	BIOZ_DC_EXCITATION_A BIOZ_DC_EXCITATION_B BIOZ_DC_EXCITATION_C	15	BIOZ_DCLO_POLARITY_IP_x	DCLO output current polarity at ECGIP. 0: sink current 1: source current	0x0	R/W
0x2D9 0x2E9 0x2F9	BIOZ_DC_EXCITATION_D BIOZ_DC_EXCITATION_E BIOZ_DC_EXCITATION_F	14	BIOZ_DCLO_POLARITY_IN_x	DCLO output current polarity at ECGIN. 0: sink current 1: source current	0x0	R/W
0x309	BIOZ_DC_EXCITATION_G	13	BIOZ_DCLO_L_EN_x	Enable the low-range DCLO current for the ECGx inputs with a current range from 0 nA to 16 nA by 2 nA per step.	0x0	R/W
0x319 0x329 0x339 0x349 0x359 0x369 0x379 0x389 0x399 0x3A9 0x3B9	BIOZ_DC_EXCITATION_H BIOZ_DC_EXCITATION_I BIOZ_DC_EXCITATION_J BIOZ_DC_EXCITATION_K BIOZ_DC_EXCITATION_L BIOZ_DC_EXCITATION_M BIOZ_DC_EXCITATION_N BIOZ_DC_EXCITATION_O BIOZ_DC_EXCITATION_P BIOZ_DC_EXCITATION_Q BIOZ_DC_EXCITATION_R	[12:9]	BIOZ_DCLO_L_MAG_x	Low-range DCLO excite current magnitude. 0: 0 nA. 0001: reserved. 0010: reserved. 0011: reserved. 0100: reserved. 0101: reserved. 0110: reserved. 0111: reserved. 1000: 2 nA. 1001: 4 nA. 1010: 6 nA. 1011: 8 nA. 1100: 10 nA. 1101: 12 nA. 1110: 14 nA. 1111: 16 nA.	0x0	R/W
		8	BIOZ_DCLO_M_EN_x	Enables the midrange DCLO current for the ECGx inputs with the current range from 0 nA to 70 nA by 10 nA per step.	0x0	R/W
		[7:5]	BIOZ_DCLO_M_MAG_x	Midrange DCLO excite current magnitude. 0: 0 nA. 001: 10 nA. 010: 20 nA. 011: 30 nA. 100: 40 nA. 101: 50 nA. 110: 60 nA. 111: 70 nA.	0x0	R/W

REGISTER DETAILS

Table 24. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
		4	BIOZ_DCLO_H_EN_x	Enable the high-range DCLO current for the ECGx inputs with the current range from 0 µA to 1 µA by 100 nA per step.	0x0	R/W
		[3:0]	BIOZ_DCLO_H_MAG_x	High-range DCLO excite current magnitude. 0: 0 nA. 1: 100 nA. 10: 200 nA. 11: 300 nA. 100: 400 nA. 101: 500 nA. 110: 600 nA. 111: 700 nA. 1000: reserved. 1001: reserved. 1010: reserved. 1011: reserved. 1100: 800 nA. 1101: 900 nA. 1110: 1 µA. 1111: 1.1 µA.	0x0	R/W
0x2AA 0x2BA 0x2CA 0x2DA 0x2EA 0x2FA 0x30A 0x31A 0x32A 0x33A 0x34A 0x35A 0x36A 0x37A 0x38A	BIOZ_ANA_CTRL1_A BIOZ_ANA_CTRL1_B BIOZ_ANA_CTRL1_C BIOZ_ANA_CTRL1_D BIOZ_ANA_CTRL1_E BIOZ_ANA_CTRL1_F BIOZ_ANA_CTRL1_G BIOZ_ANA_CTRL1_H BIOZ_ANA_CTRL1_I BIOZ_ANA_CTRL1_J BIOZ_ANA_CTRL1_K BIOZ_ANA_CTRL1_L BIOZ_ANA_CTRL1_M BIOZ_ANA_CTRL1_N BIOZ_ANA_CTRL1_O	[15:12]	BIOZ_TIA_RGAIN_x	Control signal for the high power TIA feedback resistor. 0: 1 kΩ. 1: 2 kΩ. 10: 3 kΩ. 11: 4 kΩ. 100: 6 kΩ. 101: 8 kΩ. 110: 10 kΩ. 111: 15 kΩ. 1000: 30 kΩ. 1001: 60 kΩ. 1010: 125 kΩ. 1011: 250 kΩ. 1100: 500 kΩ. 1101: 1 MΩ.	0x1	R/W
0x39A 0x3AA 0x3BA	BIOZ_ANA_CTRL1_P BIOZ_ANA_CTRL1_Q BIOZ_ANA_CTRL1_R	[11:8]	BIOZ_TIA_CGAIN_x	Control signal for the high power TIA feedback capacitor. 0: off. 1: 1 pF. 10: 2 pF. 11: 3 pF. 100: 4 pF (default value for low power). 101: 5 pF. 110: 6 pF. 111: 7 pF (default value for high power). 1000: 8 pF. 1001: 9 pF. 1010: 10 pF.	0x7	R/W

REGISTER DETAILS

Table 24. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
				1011: 11 pF. 1100: 12 pF. 1101: 13 pF. 1110: 14 pF. 1111: 15 pF.		
		[7:6]	BIOZ_EXCBUF_LPMODE_x	Low power mode enable for excitation buffer. 0: high power mode. 1: low power mode. 11: ultra-low power mode.	0x0	R/W
		[5:4]	BIOZ_CHOP_OFF_IN_x	Disables chop off front buffer and PGA. 0: enables front buffer and PGA chopping. 1: only enables PGA chopping. 10: only enables front buffer chopping. 11: disables front buffer and PGA chopping.	0x3	R/W
		[3:2]	BIOZ_TIA_LPMODE_x	Low power mode enable for TIA. 0: high power mode. 1: low power mode. 11: ultra-low power mode.	0x0	R/W
		1	BIOZ_RX_LPMODE_x	Low power mode enable for ADC receiver channel. 0: high power mode. 1: low power mode.	0x0	R/W
		0	BIOZ_DAC_RCF_LOWBW_EN_x	DAC RC filters bandwidth tuning. High to set a bandwidth reduced to 80% of its original value. 0: disables. 1: enables.	0x0	R/W
0x2AB 0x2BB 0x2CB	BIOZ_ANA_CTRL2_A BIOZ_ANA_CTRL2_B BIOZ_ANA_CTRL2_C	15	BIOZ_TIA_VREF_SEL_x	Select the TIA_VREF voltage. 0: 0.9 V. 1: 1.2 V.	0x0	R/W
0x2DB 0x2EB 0x2FB	BIOZ_ANA_CTRL2_D BIOZ_ANA_CTRL2_E BIOZ_ANA_CTRL2_F	14	BIOZ_CM_SW_x	Weak V_{CM} driven for IMPIP and IMPIN. 0: disables weak V_{CM} driven. 1: weak V_{CM} driven.	0x0	R/W
0x30B 0x31B 0x32B 0x33B 0x34B 0x35B 0x36B 0x37B 0x38B	BIOZ_ANA_CTRL2_G BIOZ_ANA_CTRL2_H BIOZ_ANA_CTRL2_I BIOZ_ANA_CTRL2_J BIOZ_ANA_CTRL2_K BIOZ_ANA_CTRL2_L BIOZ_ANA_CTRL2_M BIOZ_ANA_CTRL2_N BIOZ_ANA_CTRL2_O	[13:11]	BIOZ_NCHAN_x	N-channel selection. 0: connects HPTIA_n to BUFFER_N (negative input of the buffer). 1: connects IMPIN to BUFFER_N. 010: connects EXCP to BUFFER_N. 011: connects R_{INT_SN} to BUFFER_N. 100: connects IMPIP to BUFFER_N. 101: connects EXCN to BUFFER_N. 110: connects ECG RLD to BUFFER_N. 111: connects ECGIP to BUFFER_N.	0x0	R/W
0x39B 0x3AB 0x3BB	BIOZ_ANA_CTRL2_P BIOZ_ANA_CTRL2_Q BIOZ_ANA_CTRL2_R	[10:8]	BIOZ_PCHAN_x	P-channel selection. 0: connects HPTIA_p to BUFFER_P. 1: connects IMPIP to BUFFER_P. 010: connects EXCN to BUFFER_P. 011: connects R_{INT_SP} to BUFFER_P.	0x0	R/W

REGISTER DETAILS

Table 24. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
				100: connects IMPIN to BUFFER_P. 101: connects EXCP to BUFFER_P. 110: connects ECGIN to BUFFER_P. 111: connects ECGIP to BUFFER_P.		
		[7:4]	BIOZ_TSW_x	T switch in the mux for IMPIP, IMPIN, EXCP, and EXCN. 1: connects high power TIA to IMPIP. 10: connects high power TIA to IMPIN. 100: connects high power TIA to EXCP. 1000: connects high power TIA to EXCN.	0x0	R/W
		[3:0]	BIOZ_DSW_x	D switch in the mux for IMPIP, IMPIN, EXCP, and EXCN. 1: connects EXCBUF to IMPIP. 10: connects EXCBUF to IMPIN. 100: connects EXCBUF to EXCP. 1000: connects EXCBUF to EXCN.	0x0	R/W
0x2AC	BIOZ_ANA_CTRL3_A	[15:14]	BIOZ_CHOP_OFF_EXC_x	Disables chop of EXCBUF and TIA. 0: enables EXCBUF and TIA chopping. 1: only enables TIA chopping. 10: only enables EXCBUF chopping. 11: disables EXCBUF and TIA chopping.	0x3	R/W
0x2BC	BIOZ_ANA_CTRL3_B					
0x2CC	BIOZ_ANA_CTRL3_C					
0x2DC	BIOZ_ANA_CTRL3_D					
0x2EC	BIOZ_ANA_CTRL3_E					
0x2FC	BIOZ_ANA_CTRL3_F	[13:12]	BIOZ_PGA_GAIN_x	PGA gain selection. 0: 1.5 V/V. 1: 2 V/V. 10: 3 V/V. 11: 6 V/V.	0x0	R/W
0x30C	BIOZ_ANA_CTRL3_G					
0x31C	BIOZ_ANA_CTRL3_H					
0x32C	BIOZ_ANA_CTRL3_I					
0x33C	BIOZ_ANA_CTRL3_J					
0x34C	BIOZ_ANA_CTRL3_K	[11:9]	BIOZ_TIA_ECG_x	Receiver switch mux for ECGIN, ECGIP, and RLD. 1: connects high power TIA to ECGIN. 010: connects high power TIA to ECGIP. 100: connects high power TIA to ECG RLD.	0x0	R/W
0x35C	BIOZ_ANA_CTRL3_L					
0x36C	BIOZ_ANA_CTRL3_M					
0x37C	BIOZ_ANA_CTRL3_N					
0x38C	BIOZ_ANA_CTRL3_O	[8:6]	BIOZ_EXCBUF_ECG_x	Excitation switch mux for ECGIN, ECGIP, and RLD. 1: connects EXCBUF to ECGIN. 10: connects EXCBUF to ECGIP. 100: connects EXCBUF to ECG RLD.	0x0	R/W
0x39C	BIOZ_ANA_CTRL3_P					
0x3AC	BIOZ_ANA_CTRL3_Q					
0x3BC	BIOZ_ANA_CTRL3_R					
		5	BIOZ_DCLO_IP_EN_x	Enables the DC excitation current output at ECGIP, which reuses the DCLO circuit with low, mid, and high current ranges.	0x0	R/W
		4	BIOZ_DCLO_IN_EN_x	Enables the DC excitation current output at ECGIN, which reuses the DCLO circuit with low, mid, and high current ranges.	0x0	R/W
		[3:2]	BIOZ_CURRENT_LIMIT_x	Internal current-limit resistance selection. 00: no current limit. 01: use 650 Ω. 10: use 1.3 kΩ. 11: reserved.	0x0	R/W

REGISTER DETAILS

Table 24. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
		[1:0]	BIOZ_RINT_SW_x	Supports internal calibration resistor. Set 0x11 to enable the internal calibration resistance. 0: floating internal calibration resistance. 11: connects internal calibration resistance to EXCBUF and high power TIA.	0x0	R/W
0x2AD	BIOZ_ADCFILTERCON_A	[15:12]	RESERVED	Reserved.	0x0	R
0x2BD	BIOZ_ADCFILTERCON_B	[11:6]	BIOZ_ADC_PERIOD_x	Select the ADC sampling clock period. For 32 MHz controller clock mode, the ADC sampling clock period = 1 µs × (BIOZ_ADC_PERIOD_x, Bits[5:0] + 1). For 960 kHz controller clock mode, the ADC sampling clock period = 8.333 µs × (BIOZ_ADC_PERIOD_x, Bits[5:0] + 1).	0x0	R/W
0x2CD	BIOZ_ADCFILTERCON_C	[5:4]	BIOZ_AVRGNUM_x	Sets the number of samples used by the averaging function. 0: two ADC samples. 1: four ADC samples. The number of input data for one average is 4. 10: eight ADC samples. The number of input data for one average is 8. 11: 16 ADC samples. The number of input data for one average is 16.	0x0	R/W
0x2DD	BIOZ_ADCFILTERCON_D					
0x2ED	BIOZ_ADCFILTERCON_E					
0x2FD	BIOZ_ADCFILTERCON_F					
0x30D	BIOZ_ADCFILTERCON_G					
0x31D	BIOZ_ADCFILTERCON_H	3	BIOZ_AVRGEN_x	Average function enable. Enable average operation of sinc3 filter output result. 0: disables. Sinc3 result feeds to next stage. 1: enables. Average result feeds to next stage.	0x0	R/W
0x32D	BIOZ_ADCFILTERCON_I					
0x33D	BIOZ_ADCFILTERCON_J					
0x34D	BIOZ_ADCFILTERCON_K	2	BIOZ_SINC3BYP_x	Bypass sinc3 filter. 0: enables sinc3 filter. 1: bypasses sinc3 filter.	0x1	R/W
0x35D	BIOZ_ADCFILTERCON_L					
0x36D	BIOZ_ADCFILTERCON_M					
0x37D	BIOZ_ADCFILTERCON_N	[1:0]	BIOZ_SINC3OSR_x	Sinc3 filter oversampling rate. 0: oversampling rate of five. 1: oversampling rate of four. 10: oversampling rate of two. 11: oversampling rate of five.	0x0	R/W
0x38D	BIOZ_ADCFILTERCON_O					
0x39D	BIOZ_ADCFILTERCON_P					
0x3AD	BIOZ_ADCFILTERCON_Q					
0x3BD	BIOZ_ADCFILTERCON_R					
0x2AE	BIOZ_DFTCON_A	[15:8]	RESERVED	Reserved.	0x0	R
0x2BE	BIOZ_DFTCON_B	7	BIOZ_DATA_SIZE_x	BIOZ output data size. 0: 3 bytes. 1: 4 bytes.	0x0	R/W
0x2CE	BIOZ_DFTCON_C					
0x2DE	BIOZ_DFTCON_D					
0x2EE	BIOZ_DFTCON_E	6	BIOZ_DFT_TYPE_x	BIOZ DFT output data type selection. 0: real and imaginary. 1: real and real with alternating ADC samples.	0x0	R/W
0x2FE	BIOZ_DFTCON_F					
0x30E	BIOZ_DFTCON_G					
0x31E	BIOZ_DFTCON_H	5	BIOZ_WG_DFT_DIFF_PHASE_EN_x	Wave generator block sine wave and DFT block sine wave use a different offset. 0: uses the same offset. 1: uses the different offset.	0x0	R/W
0x32E	BIOZ_DFTCON_I					
0x33E	BIOZ_DFTCON_J					
0x34E	BIOZ_DFTCON_K	4	BIOZ_HANNINGEN_x	Enable Hanning window. 0: disables. 1: enables.	0x0	R/W
0x35E	BIOZ_DFTCON_L					
0x36E	BIOZ_DFTCON_M					
0x37E	BIOZ_DFTCON_N	[3:0]	BIOZ_DFTNUM_x	ADC samples used. DFT number can be 4 up to 8192.	0x9	R/W

REGISTER DETAILS

Table 24. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
0x38E 0x39E 0x3AE 0x3BE	BIOZ_DFTCON_O BIOZ_DFTCON_P BIOZ_DFTCON_Q BIOZ_DFTCON_R			0: DFT point number is 4. 1: DFT point number is 8. 10: DFT point number is 16. 11: DFT point number is 32. 100: DFT point number is 64. 101: DFT point number is 128. 110: DFT point number is 256. 111: DFT point number is 512. 1000: DFT point number is 1024. 1001: DFT point number is 2048. 1010: DFT point number is 4096. 1011: DFT point number is 8192.		
0x2AF 0x2BF 0x2CF 0x2DF 0x2EF 0x2FF 0x30F 0x31F 0x32F	BIOZ_ADC_CONV_DLY_A BIOZ_ADC_CONV_DLY_B BIOZ_ADC_CONV_DLY_C BIOZ_ADC_CONV_DLY_D BIOZ_ADC_CONV_DLY_E BIOZ_ADC_CONV_DLY_F BIOZ_ADC_CONV_DLY_G BIOZ_ADC_CONV_DLY_H BIOZ_ADC_CONV_DLY_I	[15:13]	BIOZ_PRE_WIDTH_x	Precondition duration for this time slot, which is equal to the number of ADC clock cycles as defined in this register. Default value is 0. 0: 0. 1: 25 ADC clock cycles. 10: 50 ADC clock cycles. 11: 100 ADC clock cycles. 100: 200 ADC clock cycles. 101: 400 ADC clock cycles. 110: 800 ADC clock cycles. 111: 1600 ADC clock cycles.	0x0	R/W
0x33F 0x34F 0x35F 0x36F 0x37F	BIOZ_ADC_CONV_DLY_J BIOZ_ADC_CONV_DLY_K BIOZ_ADC_CONV_DLY_L BIOZ_ADC_CONV_DLY_M BIOZ_ADC_CONV_DLY_N	[12:11]	BIOZ_PRECON_SEL_x	Selects the buffer inputs for precondition. 0: none. 1: Buffer n input. 10: Buffer p input. 11: Buffer n and Buffer p inputs.	0x0	R/W
0x38F	BIOZ_ADC_CONV_DLY_O	[10:4]	BIOZ_SUBSAMPLE_RATIO_x	Reduces the output data rate, which is equal to (the timer clock frequency)/(TIMSLOT_PERIOD_x)/(BIOZ_SUBSAMPLE_RATIO_x). When this bit is set larger than 1, operate the time slot only once per (BIOZ_SUBSAMPLE_RATIO_x) time slot sequence. This subsampling aligns to other time slots using the same BIOZ_SUBSAMPLE_RATIO_x. It skips (BIOZ_SUBSAMPLE_RATIO_x − 1) times and then executes the time slot.	0x1	R/W
0x39F 0x3AF 0x3BF	BIOZ_ADC_CONV_DLY_P BIOZ_ADC_CONV_DLY_Q BIOZ_ADC_CONV_DLY_R	3	BIOZ_PRECON_RES_x	Selects the resistor value used for the precondition. 0: 1 kΩ. 1: 1 MΩ.	0x0	R/W
		[2:0]	BIOZ_ADC_CONV_DLY_x	Delays between ADC enable and sinc3 enable. This register defines the number of ADC samples discarded in this delay time. Default number of ADC samples to discard is 25. 0: 10 ADC samples. 1: 25 ADC samples. 10: 50 ADC samples.	0x1	R/W

REGISTER DETAILS

Table 24. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
				11: 100 ADC samples. 100: 200 ADC samples. 101: 400 ADC samples. 110: 800 ADC samples. 111: 1600 ADC samples.		

OUTLINE DIMENSIONS

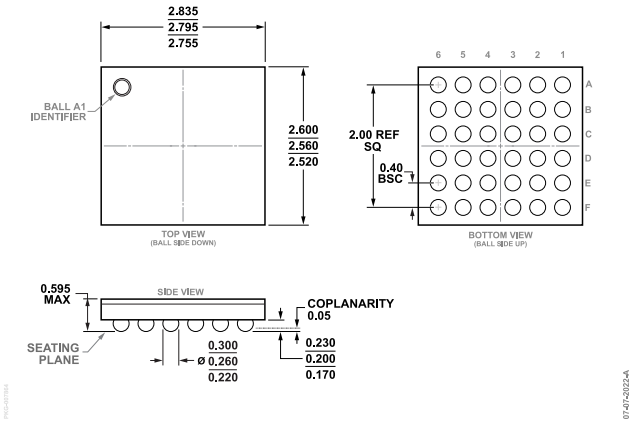

Figure 54. 36-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-36-11)
Dimensions shown in millimeters

Updated: April 13, 2023

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADPD7000BCBZR7	−40°C to +85°C	CHIPS W/SOLDER BUMPS/WLCSP	Reel, 1500	CB-36-11

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Table 25. Evaluation Boards

Model[1]	Description
EVAL-ADPD7000Z	Evaluation Board

[1] Z = RoHS-Compliant Part.