

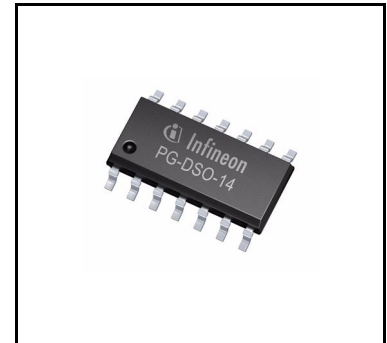
# OPTIREG™ Linear TLE4262

## 5 V low drop voltage regulator



### Features

- Output voltage tolerance  $\leq \pm 2\%$
- 200 mA output current capability
- Low-drop voltage
- Very low standby current consumption
- Overtemperature protection
- Reverse polarity protection
- Short-circuit proof
- Adjustable reset threshold
- Wide temperature range
- Suitable for use in automotive electronics
- Green Product (RoHS compliant)



### Potential applications

General automotive applications.

### Product validation

Qualified for automotive applications. Product validation according to AEC-Q100/101.

### Description

The OPTIREG™ Linear TLE4262 is a 5 V low drop voltage regulator in a PG-DSO-14 SMD package. The maximum input voltage is 45 V. The maximum output current is more than 200 mA. The IC is short-circuit proof and includes a temperature protection which turns off the IC at overtemperature.

The IC regulates an input voltage  $V_I$  in the range of  $6\text{ V} < V_I < 45\text{ V}$  to  $V_{Q,nom} = 5.0\text{ V}$ . A reset signal is generated for an output voltage of  $V_{Q,rt} < 4.5\text{ V}$ . This voltage threshold can be decreased to 3.5 V by external connection of a voltage divider. The reset delay can be set externally with a capacitor. The IC can be switched off via the inhibit input, which reduces the current consumption from 900  $\mu\text{A}$  to typical 0  $\mu\text{A}$ .

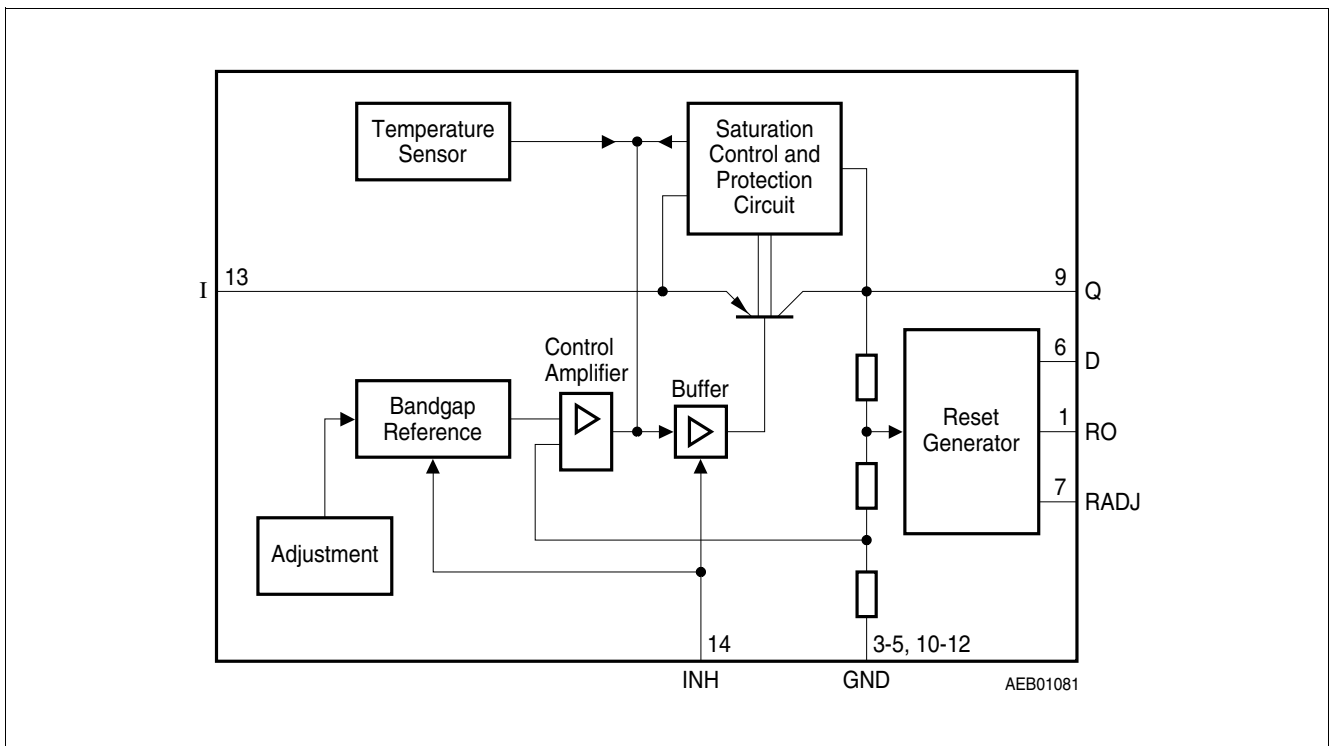
Type	Package	Marking
TLE4262GM	PG-DSO-14	TLE4262GM

## Table of contents

	<b>Features</b> .....	<b>1</b>
	<b>Potential applications</b> .....	<b>1</b>
	<b>Product validation</b> .....	<b>1</b>
	<b>Description</b> .....	<b>1</b>
	<b>Table of contents</b> .....	<b>2</b>
<b>1</b>	<b>Block diagram</b> .....	<b>3</b>
<b>2</b>	<b>Pin configuration</b> .....	<b>4</b>
<b>3</b>	<b>General product characteristics</b> .....	<b>5</b>
3.1	Absolute maximum ratings .....	5
3.2	Functional range .....	5
3.3	Thermal resistance .....	6
<b>4</b>	<b>Functional description</b> .....	<b>7</b>
4.1	Choosing external components .....	7
4.2	Electrical characteristics .....	7
4.3	Typical performance characteristics .....	9
<b>5</b>	<b>Application information</b> .....	<b>12</b>
5.1	Reset timing .....	13
<b>6</b>	<b>Package information</b> .....	<b>14</b>
<b>7</b>	<b>Revision history</b> .....	<b>15</b>

**Block diagram**

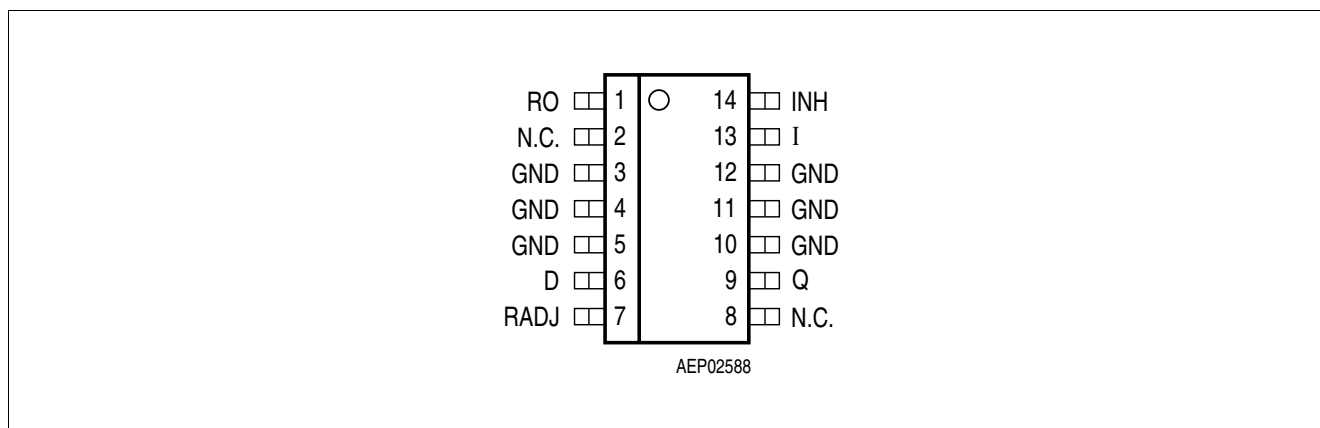
**1 Block diagram**



**Figure 1 Block diagram**

**Pin configuration**

**2 Pin configuration**



**Figure 2 Pin configuration** (top view)

**Table 1 Pin definitions and functions**

Pin PG-DSO-14	Symbol	Function
1	RO	<b>Reset output;</b> open-collector output internally connected to the output via a resistor of 30 kΩ.
2, 8	N.C.	Not connected
3 - 5, 10 - 12	GND	<b>Ground</b>
6	D	<b>Reset delay;</b> connect capacitor to GND for setting delay time
7	RADJ	<b>Reset threshold;</b> for setting the switching threshold connect by a voltage divider from output to ground. If this input is connected to GND, reset is triggered at an output voltage of 4.5 V.
9	Q	<b>5 V output voltage;</b> block to ground by capacitor with $C \geq 22 \mu\text{F}$ , $\text{ESR} \leq 3 \Omega$ at 10 kHz.
13	I	<b>Input voltage;</b> block to ground directly at the IC by a ceramic capacitor.
14	INH	<b>Inhibit;</b> TTL-compatible, low-active input

**General product characteristics**

### 3 General product characteristics

#### 3.1 Absolute maximum ratings

**Table 2 Absolute maximum ratings<sup>1)</sup>**

$T_j = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
<b>Input I</b>							
Input voltage	$V_I$	-42	-	45	V	-	P_3.1.1
Input current	$I_I$	-	-	-	-	Internally limited	
<b>Reset output RO</b>							
Input voltage	$V_{RO}$	-0.3	-	42	V	-	P_3.1.2
Input current	$I_{RO}$	-	-	-	-	Internally limited	
<b>Reset threshold RADJ</b>							
Voltage	$V_{RADJ}$	-0.3	-	6	V	-	P_3.1.3
<b>Reset delay D</b>							
Voltage	$V_D$	-0.3	-	42	V	-	P_3.1.4
Current	$I_D$	-	-	-	-	Internally limited	
<b>Output Q</b>							
Voltage	$V_Q$	5.25	-	$V_I$	V	-	P_3.1.5
Current	$I_Q$	-	-	-	-	Internally limited	
<b>Inhibit INH</b>							
Input voltage	$V_{INH}$	-42	-	45	V	-	P_3.1.6
Input current	$I_{INH}$	-	-	-	-	Internally limited	
<b>Ground GND</b>							
Current	$I_{GND}$	-0.5	-	-	A	-	P_3.1.8
<b>Temperature</b>							
Junction temperature	$T_j$	-	-	150	$^\circ\text{C}$	-	P_3.1.9
Storage temperature	$T_{stg}$	-50	-	150	$^\circ\text{C}$	-	

1) Not subject to production test, specified by design.

Note: The reset output is low within the range  $1\text{V} \leq V_Q \leq V_{Q,rt}$ .

#### 3.2 Functional range

**Table 3 Functional range**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input voltage	$V_I$	5.2	-	45	V	<sup>1)</sup>	P_3.2.1
Junction temperature	$T_j$	-40	-	150	$^\circ\text{C}$	-	P_3.2.2

**General product characteristics**

1) Corresponds with characteristics of drop voltage, output current and power description (see diagrams).

### 3.3 Thermal resistance

**Table 4 Thermal resistance**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Junction to ambient	$R_{thJA}$	–	–	112	K/W	1)
Junction to case	$R_{thJP}$	–	–	32	K/W	2)

1) Package mounted on PCB  $80 \times 80 \times 1.5 \text{ mm}^3$ ;  $35 \text{ }\mu\text{m Cu}$ ;  $5 \text{ }\mu\text{m Sn}$ ; footprint only; zero airflow

2) Measured to pin 4.

**Functional description**

## 4 Functional description

The control amplifier compares a reference voltage, which is kept highly accurate by resistance adjustment, to a voltage that is proportional to the output voltage and drives the base of the series transistor via a buffer. Saturation control as a function of the load current prevents any over-saturation of the power element. If the externally scaled down output voltage at the reset threshold input drops below 1.35 V, the external reset delay capacitor is discharged by the reset generator. If the voltage on the capacitor reaches the lower threshold  $V_{DRL}$ , a reset signal is issued on the reset output and not cancelled again until the upper threshold  $V_{DU}$  is exceeded. If the reset threshold input is connected to GND, reset is triggered at an output voltage of 4.5 V. The IC can be switched at the TTL-compatible, low-active inhibit input. It also includes a number of internal circuits for protection against:

- Overload
- Overtemperature
- Reverse polarity

### 4.1 Choosing external components

The input capacitor  $C_1$  is necessary for compensation of line influences. Using a resistor of approx. 1  $\Omega$  in series with  $C_1$ , the oscillating circuit consisting of input inductivity and input capacitance can be damped. The output capacitor is necessary for the stability of the regulating circuit. Stability is ensured at values  $C_Q \geq 22 \mu\text{F}$  and an ESR of  $\leq 3 \Omega$  within the operating temperature range. For small tolerances of the reset delay the spread of the capacitance of the delay capacitor and its temperature coefficient should be noted.

### 4.2 Electrical characteristics

**Table 5 Electrical characteristics**

$V_I = 13.5 \text{ V}$ ;  $V_{INH} > 3.5 \text{ V}$   $T_j = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ; (unless specified otherwise)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
<b>Normal Operation</b>							
Output voltage	$V_Q$	4.90	5.00	5.10	V	$5 \text{ mA} \leq I_Q \leq 150 \text{ mA}$ ; $6 \text{ V} \leq V_I \leq 28 \text{ V}$	P_4.2.1
Output voltage	$V_Q$	4.90	5.00	5.10	V	$6 \text{ V} \leq V_I \leq 32 \text{ V}$ ; $I_Q = 100 \text{ mA}$ ; $T_j = 100^\circ\text{C}$	P_4.2.2
Output current limitation	$I_{Q,max}$	200	250	–	mA	–	P_4.2.3
Current consumption; $I_q = I_I - I_Q$	$I_q$	–	0	50	$\mu\text{A}$	$V_{INH} = 0$	P_4.2.4
Current consumption; $I_q = I_I - I_Q$	$I_q$	–	0.90	1.30	mA	$I_Q = 0 \text{ mA}$	P_4.2.5
Current consumption; $I_q = I_I - I_Q$	$I_q$	–	10	18	mA	$I_Q = 150 \text{ mA}$	P_4.2.6
Current consumption; $I_q = I_I - I_Q$	$I_q$	–	15	23	mA	$I_Q = 150 \text{ mA}$ ; $V_I = 4.5 \text{ V}$	P_4.2.7
Dropout voltage	$V_{dr}$	–	0.35	0.50	V	$I_Q = 150 \text{ mA}$ <sup>1)</sup>	P_4.2.8
Load regulation	$\Delta V_{Q,lo}$	–	–	25	mV	$I_Q = 5 \text{ mA}$ to $150 \text{ mA}$	P_4.2.9

**Functional description**

**Table 5 Electrical characteristics (cont'd)**

$V_i = 13.5\text{ V}$ ;  $V_{INH} > 3.5\text{ V}$   $T_j = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ; (unless specified otherwise)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Line regulation	$\Delta V_{Q,li}$	–	3	25	mV	$V_i = 6\text{ V}$ to $28\text{ V}$ ; $I_Q = 150\text{ mA}$	P_4.2.10
Power supply ripple rejection	$PSRR$	–	54	–	dB	$f_r = 100\text{ Hz}$ ; $V_r = 0.5\text{ Vpp}$	P_4.2.11

**Reset Generator**

Switching threshold	$V_{Q,rt}$	4.5	4.65	4.8	V	$V_{RADJ} = 0\text{ V}$	P_4.2.12
Reset adjust threshold	$V_{RADJ,th}$	1.26	1.35	1.44	V	$V_Q > 3.5\text{ V}$	P_4.2.13
Reset low voltage	$V_{RO,l}$	–	0.10	0.40	V	$I_{RO} = 1\text{ mA}$	P_4.2.14
Saturation voltage	$V_{D,sat}$	–	50	100	mV	$V_Q < V_{R,th}$	P_4.2.15
Upper timing threshold	$V_{DU}$	1.4	1.8	2.20	V	–	P_4.2.16
Lower reset timing threshold	$V_{DRL}$	0.20	0.35	0.55	V	–	P_4.2.17
Charge current	$I_{D,ch}$	6	10	15	$\mu\text{A}$	–	P_4.2.18
Reset delay time	$t_{rd}$	–	17	–	ms	$C_D = 100\text{ nF}$	P_4.2.19
Reset reaction time	$t_{rr}$	–	1.2	–	$\mu\text{s}$	$C_D = 100\text{ nF}$	P_4.2.20

**Inhibit**

Switching voltage	$V_{INH,ON}$	3.6	–	–	V	IC turned on	P_4.2.29
Turn-OFF voltage	$V_{INH,OFF}$	–	–	0.8	V	IC turned off	P_4.2.30
Input current	$I_{INH}$	5	10	25	$\mu\text{A}$	$V_{INH} = 5\text{ V}$	P_4.2.31

1) Drop voltage =  $V_i \geq 4.5\text{ V}$  drop voltage =  $V_i - V_Q$  (below regulating voltage range).

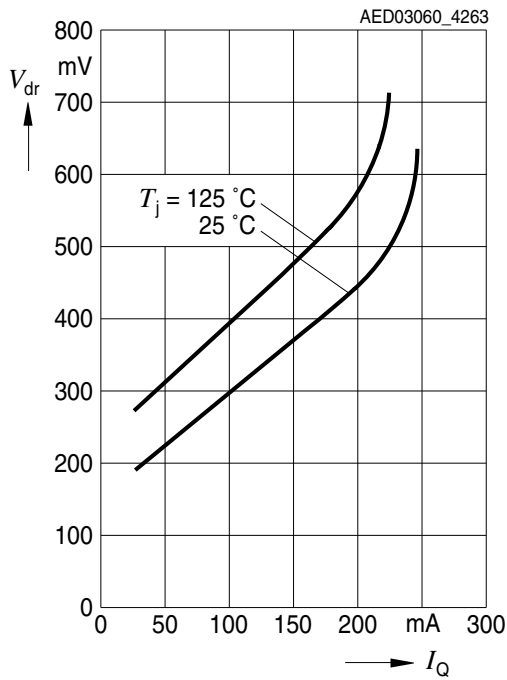
*Note:* The reset output is “low” within the range  $V_Q = 1\text{ V}$  to  $V_{Q,rt}$ .



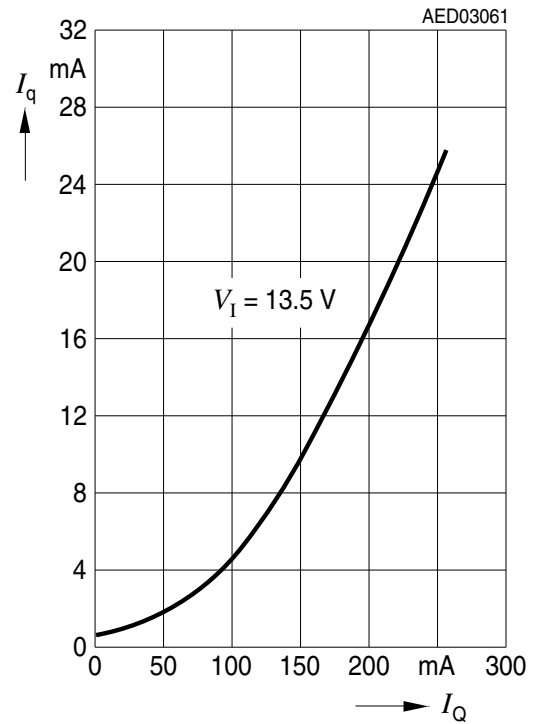
**Functional description**

**4.3 Typical performance characteristics**

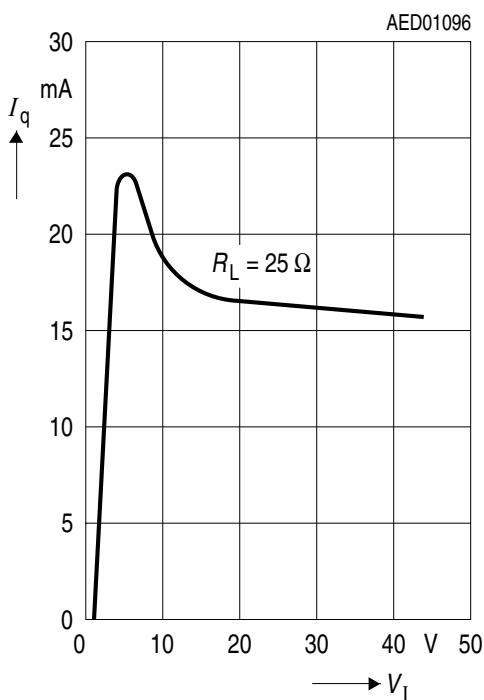
**Drop voltage  $V_{DR}$  versus output current  $I_Q$**



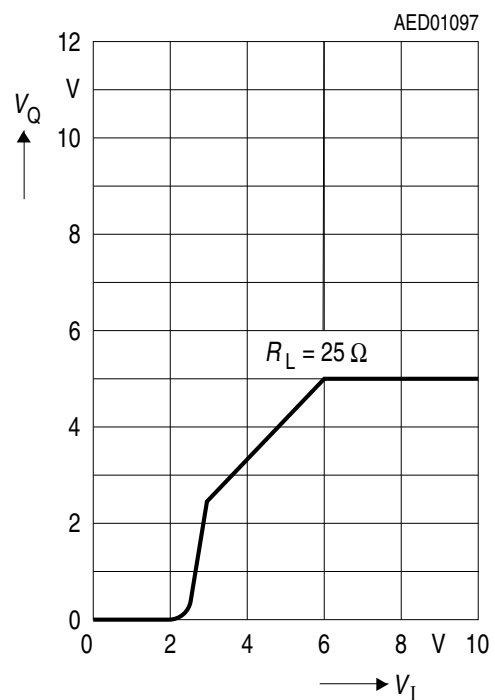
**Current consumption  $I_q$  versus output current  $I_Q$**



**Current consumption  $I_q$  versus input voltage  $V_I$**

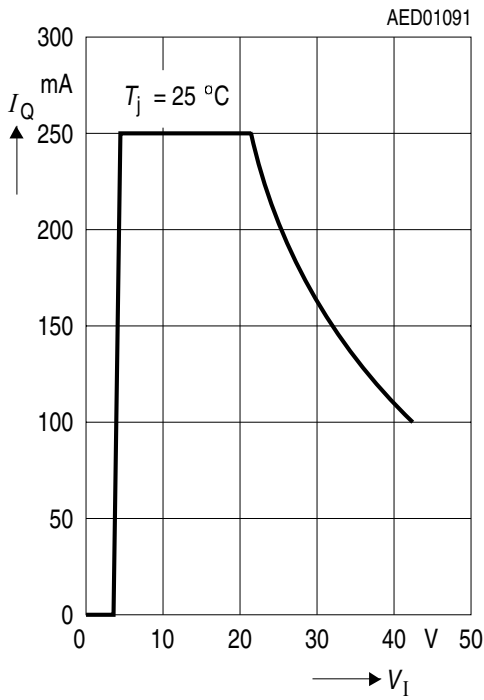


**Output voltage  $V_Q$  versus input voltage  $V_I$**

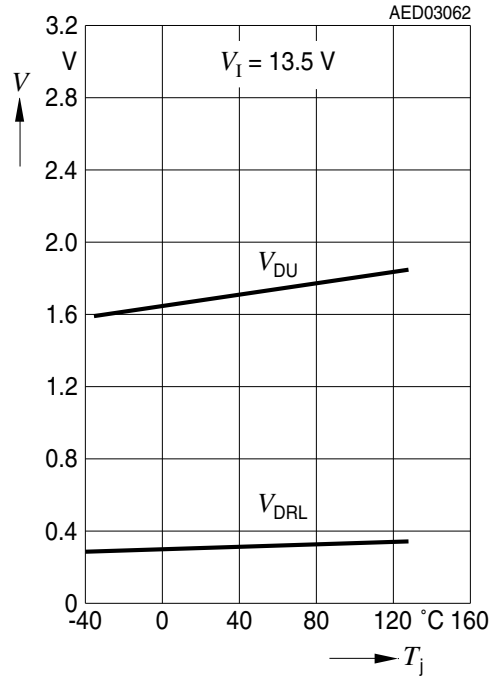


**Functional description**

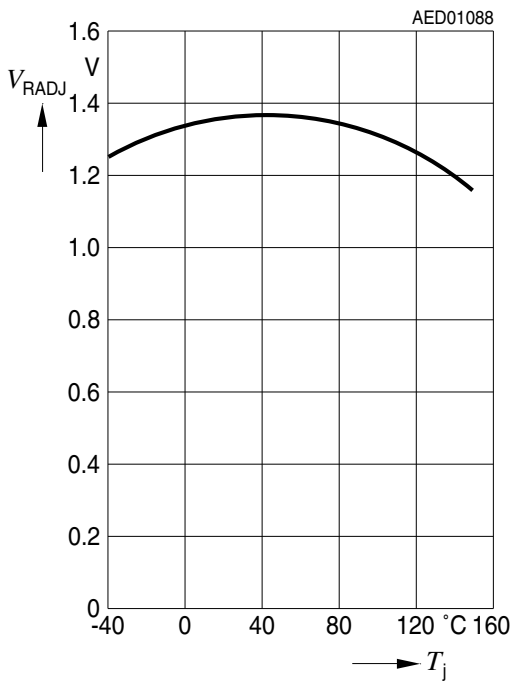
**Output current  $I_Q$  versus input voltage  $V_I$**



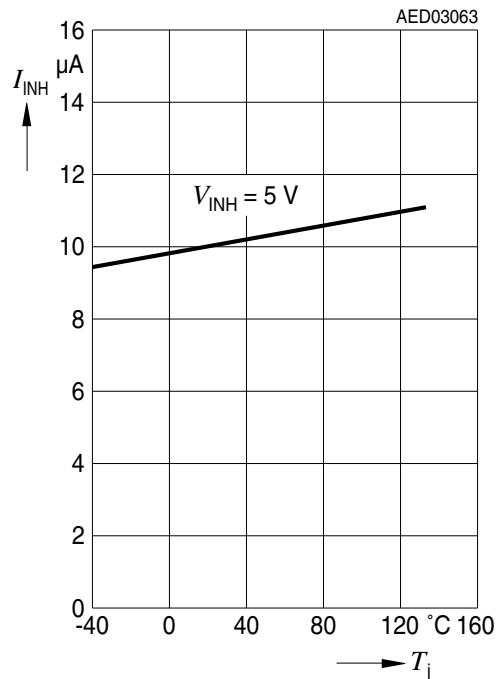
**Timing threshold voltage  $V_{DU}$  and  $V_{DRL}$  versus junction temperature**



**Reset switching threshold  $V_{RADJ}$  versus junction temperature  $T_J$**

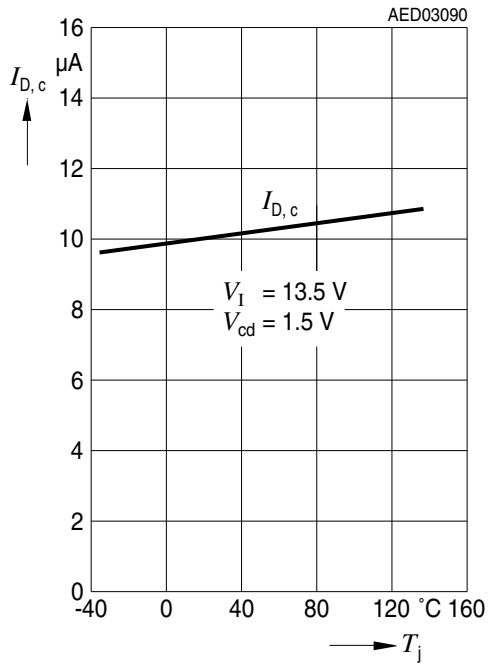


**Current consumption of inhibit  $I_{INH}$  versus junction temperature  $T_J$**

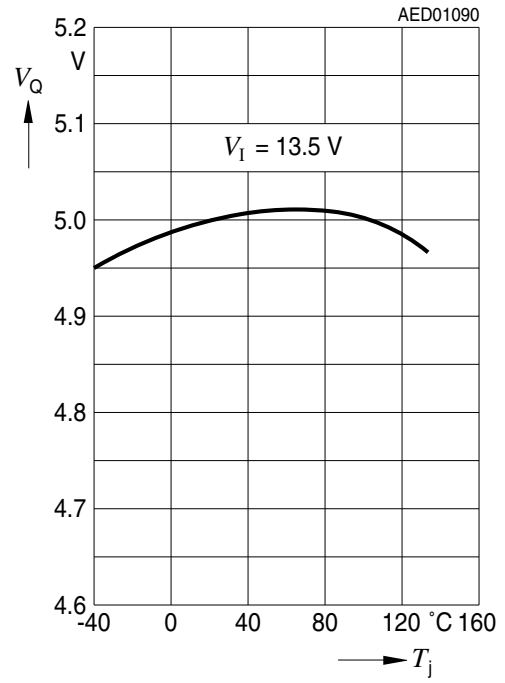


**Functional description**

**Charge current and discharge current  $I_{D,ch}$  ;  $I_{D,dis}$  versus junction temperature  $T_j$**

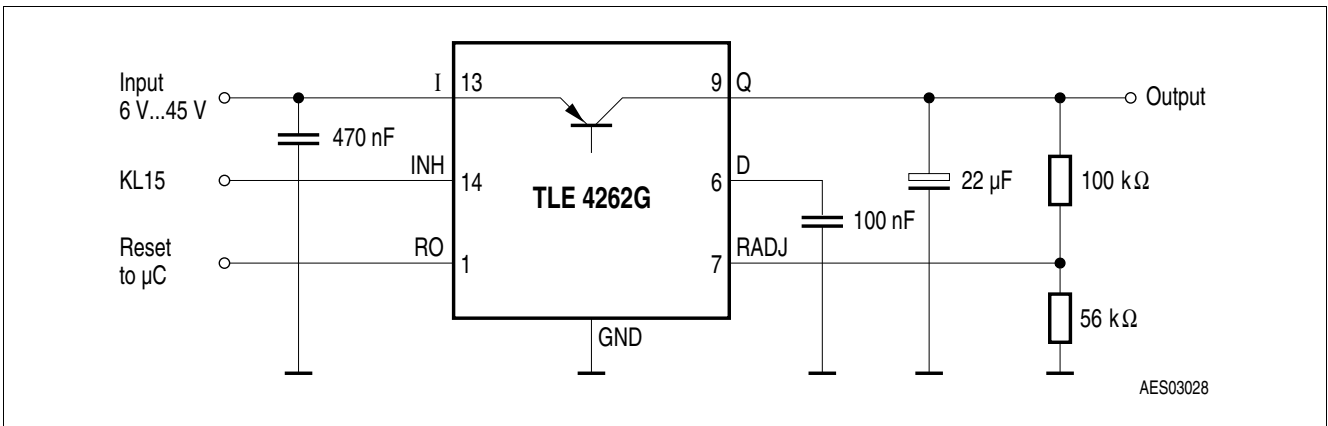


**Output voltage  $V_Q$  versus junction temperature  $T_j$**

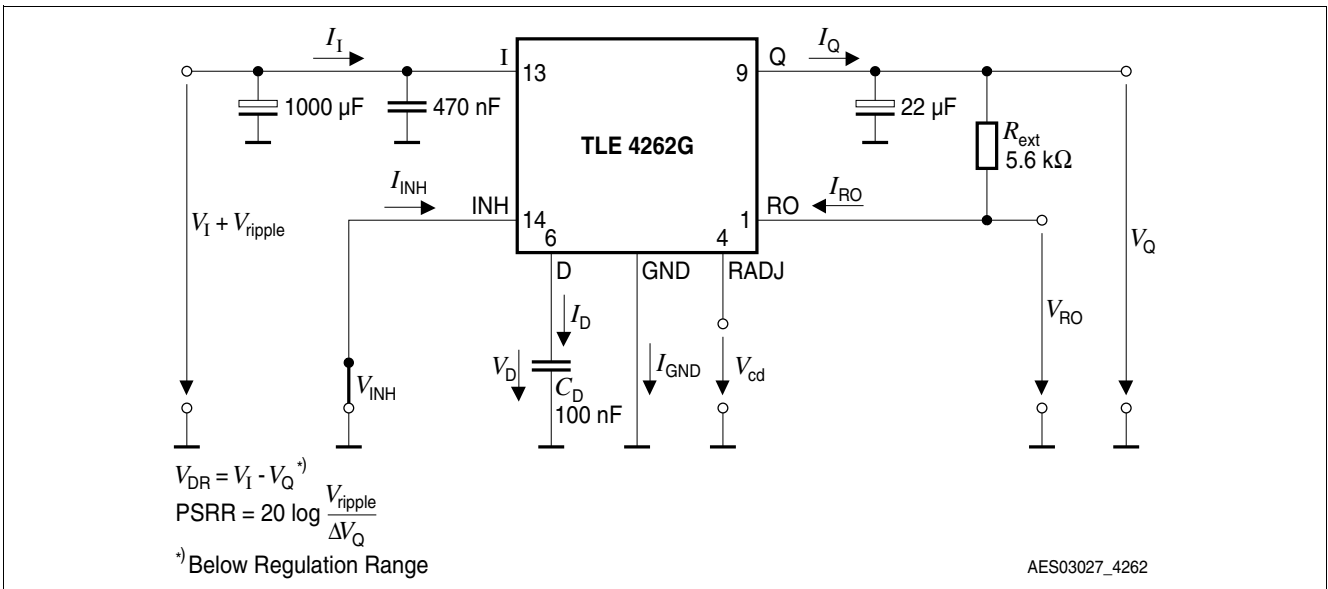


**Application information**

**5 Application information**

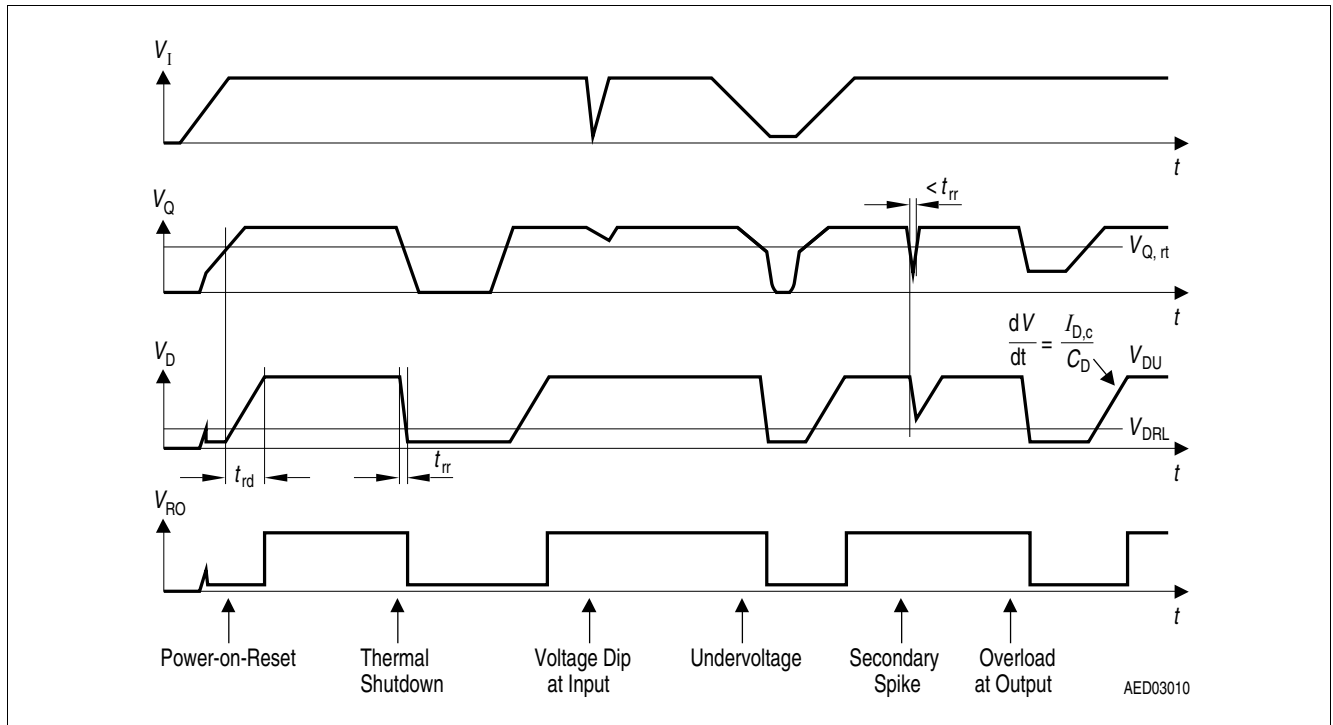


**Figure 3 Application circuit**



**Figure 4 Test circuit**

**Application information**



**Figure 5 Time response**

**5.1 Reset timing**

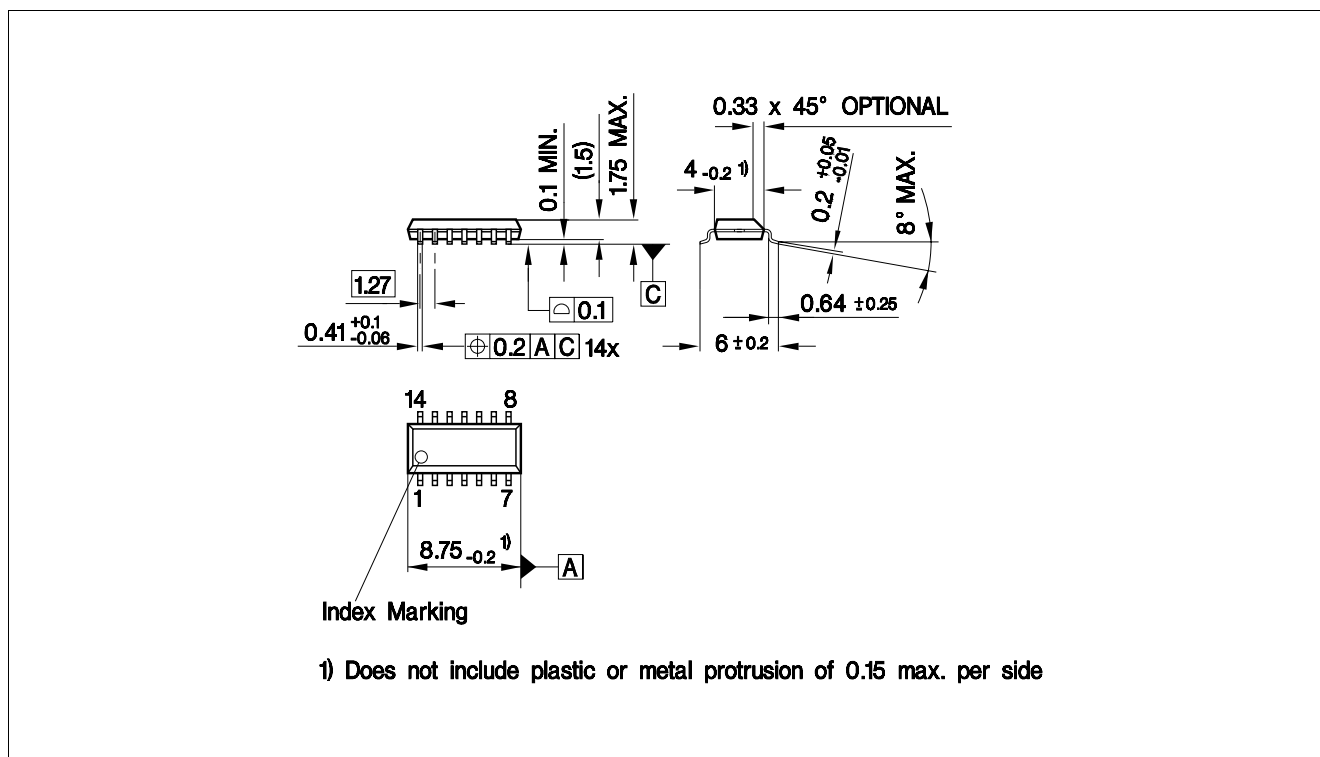
The power-on reset delay time is defined by the charging time of an external capacitor  $C_D$  which can be calculated as follows:

$$C_D = (\Delta t_{rd} \times I_{D,c}) / \Delta V \tag{5.1}$$

Definitions:

- $C_D$  = delay capacitor
- $\Delta t_{rd}$  = delay time
- $I_{D,c}$  = charge current, typical 10  $\mu$ A
- $\Delta V = V_{DU}$ , typical 1.8 V
- $V_{DU}$  = upper delay switching threshold at  $C_D$  for reset delay time

## 6 Package information



**Figure 6 PG-DSO-14 (Plastic Dual Small Outline)<sup>1)</sup>**

### Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

### Further information on packages

<https://www.infineon.com/packages>

1) Dimension in mm

**Revision history**

## **7 Revision history**

<b>Revision</b>	<b>Date</b>	<b>Changes</b>
3.1	2019-03-27	Updated layout and structure Package PG-DSO-20 deleted Updated package drawing "PG-DSO-14" Editorial changes

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**Document reference**

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