OPTIREG™ Linear TLE4262

5 V low drop voltage regulator

AEC Qualified RoHS

Features

- Output voltage tolerance ≤ ±2%
- 200 mA output current capability
- Low-drop voltage
- Very low standby current consumption
- Overtemperature protection
- Reverse polarity protection
- Short-circuit proof
- Adjustable reset threshold
- Wide temperature range
- Suitable for use in automotive electronics
- Green Product (RoHS compliant)

Potential applications

General automotive applications.

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100/101.

Description

The OPTIREG™ Linear TLE4262 is a 5 V low drop voltage regulator in a PG-DSO-14 SMD package. The maximum input voltage is 45 V. The maximum output current is more than 200 mA. The IC is short-circuit proof and includes a temperature protection which turns off the IC at overtemperature.

The IC regulates an input voltage V_I in the range of 6 V < V_I < 45 V to $V_{Q,nom}$ = 5.0 V. A reset signal is generated for an output voltage of $V_{Q,rt}$ < 4.5 V. This voltage threshold can be decreased to 3.5 V by external connection of a voltage divider. The reset delay can be set externally with a capacitor. The IC can be switched off via the inhibit input, which reduces the current consumption from 900 µA to typical 0 µA.

Type	Package	Marking
TLE4262GM	PG-DSO-14	TLE4262GM

Table of contents

1 Block diagram

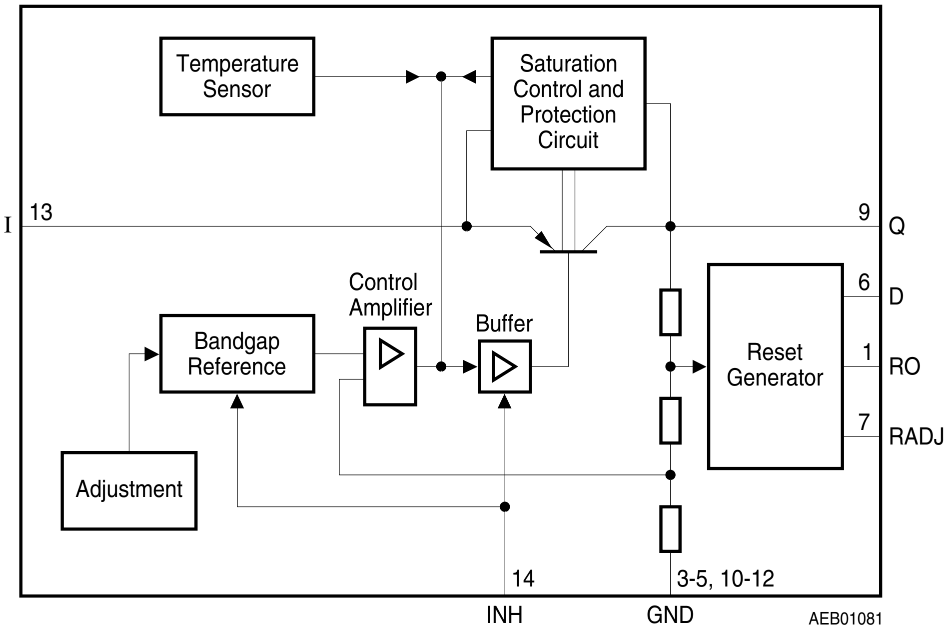


Figure 1 Block diagram

2 Pin configuration

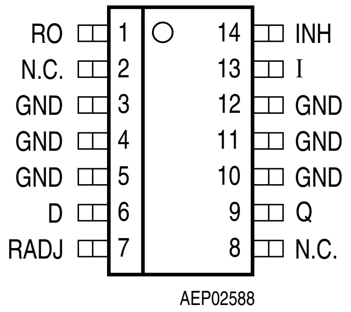


Figure 2 Pin configuration (top view)

Table 1 Pin definitions and functions

Pin PG-DSO-14	Symbol	Function
1	RO	**Reset output;** open-collector output internally connected to the output via a resistor of 30 kΩ.
2, 8	N.C.	Not connected
3 - 5, 10 - 12	GND	**Ground**
6	D	**Reset delay;** connect capacitor to GND for setting delay time
7	RADJ	**Reset threshold;** for setting the switching threshold connect by a voltage divider from output to ground. If this input is connected to GND, reset is triggered at an output voltage of 4.5 V.
9	Q	**5 V output voltage;** block to ground by capacitor with $C \geq 22$ µF, ESR ≤ 3 Ω at 10 kHz.
13	I	**Input voltage;** block to ground directly at the IC by a ceramic capacitor.
14	INH	**Inhibit;** TTL-compatible, low-active input

3 General product characteristics

3.1 Absolute maximum ratings

Table 2 Absolute maximum ratings[1]

T_j = -40°C to +125°C; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input I							
Input voltage Input current	V_I I_I	- 42 –	– –	45 –	V –	– Internally limited	P_3.1.1
Reset output RO							
Input voltage Input current	V_{RO} I_{RO}	- 0.3 –	– –	42 –	V –	– Internally limited	P_3.1.2
Reset threshold RADJ							
Voltage	V_{RADJ}	- 0.3	–	6	V	–	P_3.1.3
Reset delay D							
Voltage Current	V_D I_D	- 0.3 –	– –	42 –	V –	– Internally limited	P_3.1.4
Output Q							
Voltage Current	V_Q I_Q	5.25 –	– –	V_I –	V –	– Internally limited	P_3.1.5
Inhibit INH							
Input voltage Input current	V_{INH} I_{INH}	-42 –	– –	45 –	V –	– Internally limited	P_3.1.6
Ground GND							
Current	I_{GND}	-0.5	–	–	A	–	P_3.1.8
Temperature							
Junction temperature Storage temperature	T_j T_{stg}	– -50	– –	150 150	°C °C	– –	P_3.1.9

1) Not subject to production test, specified by design.

Note: The reset output is low within the range $1V \leq V_Q \leq V_{Q,rt}$.

3.2 Functional range

Table 3 Functional range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input voltage	V_I	5.2	–	45	V	[1]	P_3.2.1
Junction temperature	T_j	-40	–	150	°C	–	P_3.2.2

1) Corresponds with characteristics of drop voltage, output current and power description (see diagrams).

3.3 Thermal resistance

Table 4 Thermal resistance

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Junction to ambient	R_{thJA}	–	–	112	K/W	[1)]
Junction to case	R_{thJP}	–	–	32	K/W	[2)]

1) Package mounted on PCB 80 × 80 × 1.5 mm^3; 35 µm Cu; 5 µm Sn; footprint only; zero airflow

2) Measured to pin 4.

4 Functional description

The control amplifier compares a reference voltage, which is kept highly accurate by resistance adjustment, to a voltage that is proportional to the output voltage and drives the base of the series transistor via a buffer. Saturation control as a function of the load current prevents any over-saturation of the power element. If the externally scaled down output voltage at the reset threshold input drops below 1.35 V, the external reset delay capacitor is discharged by the reset generator. If the voltage on the capacitor reaches the lower threshold V_{DRL}, a reset signal is issued on the reset output and not cancelled again until the upper threshold V_{DU} is exceeded. If the reset threshold input is connected to GND, reset is triggered at an output voltage of 4.5 V. The IC can be switched at the TTL-compatible, low-active inhibit input. It also includes a number of internal circuits for protection against:

- Overload
- Overtemperature
- Reverse polarity

4.1 Choosing external components

The input capacitor C_I is necessary for compensation of line influences. Using a resistor of approx. 1 Ω in series with C_I, the oscillating circuit consisting of input inductivity and input capacitance can be damped. The output capacitor is necessary for the stability of the regulating circuit. Stability is ensured at values $C_Q \geq 22$ µF and an ESR of ≤ 3 Ω within the operating temperature range. For small tolerances of the reset delay the spread of the capacitance of the delay capacitor and its temperature coefficient should be noted.

4.2 Electrical characteristics

Table 5 Electrical characteristics

V_I = 13.5 V; V_{INH} > 3.5 V T_j = -40°C to +125°C ; (unless specified otherwise)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Normal Operation							
Output voltage	V_Q	4.90	5.00	5.10	V	5 mA ≤ I_Q ≤ 150 mA; 6 V ≤ V_I ≤ 28 V	P_4.2.1
Output voltage	V_Q	4.90	5.00	5.10	V	6 V ≤ V_I ≤ 32 V; I_Q = 100 mA; T_j = 100°C	P_4.2.2
Output current limitation	$I_{Q,max}$	200	250	–	mA	–	P_4.2.3
Current consumption; $I_q = I_I - I_Q$	I_q	–	0	50	µA	V_{INH} = 0	P_4.2.4
Current consumption; $I_q = I_I - I_Q$	I_q	–	0.90	1.30	mA	I_Q = 0 mA	P_4.2.5
Current consumption; $I_q = I_I - I_Q$	I_q	–	10	18	mA	I_Q = 150 mA	P_4.2.6
Current consumption; $I_q = I_I - I_Q$	I_q	–	15	23	mA	I_Q = 150 mA; V_I = 4.5 V	P_4.2.7
Dropout voltage	V_{dr}	–	0.35	0.50	V	I_Q = 150 mA [1)]	P_4.2.8
Load regulation	$\Delta V_{Q,lo}$	–	–	25	mV	I_Q = 5 mA to 150 mA	P_4.2.9

Table 5 Electrical characteristics (cont'd)

V_I = 13.5 V; V_{INH} > 3.5 V T_j = -40°C to +125°C ; (unless specified otherwise)

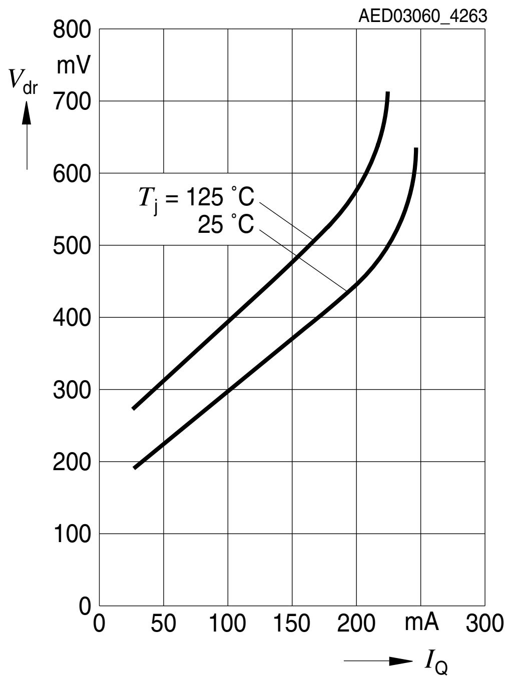
Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Line regulation	$\Delta V_{Q.li}$	–	3	25	mV	V_I = 6 V to 28 V; I_Q = 150 mA	P_4.2.10
Power supply ripple rejection	*PSRR*	–	54	–	dB	f_r = 100 Hz; V_r = 0.5 Vpp	P_4.2.11
Reset Generator							
Switching threshold	$V_{Q,rt}$	4.5	4.65	4.8	V	V_{RADJ} = 0 V	P_4.2.12
Reset adjust threshold	$V_{RADJ,th}$	1.26	1.35	1.44	V	V_Q > 3.5 V	P_4.2.13
Reset low voltage	$V_{RO,l}$	–	0.10	0.40	V	I_{RO} = 1 mA	P_4.2.14
Saturation voltage	$V_{D,sat}$	–	50	100	mV	$V_Q < V_{R,th}$	P_4.2.15
Upper timing threshold	V_{DU}	1.4	1.8	2.20	V	–	P_4.2.16
Lower reset timing threshold	V_{DRL}	0.20	0.35	0.55	V	–	P_4.2.17
Charge current	$I_{D,ch}$	6	10	15	µA	–	P_4.2.18
Reset delay time	t_{rd}	–	17	–	ms	C_D = 100 nF	P_4.2.19
Reset reaction time	t_{rr}	–	1.2	–	µs	C_D = 100 nF	P_4.2.20
Inhibit							
Switching voltage	$V_{INH,ON}$	3.6	–	–	V	IC turned on	P_4.2.29
Turn-OFF voltage	$V_{INH,OFF}$	–	–	0.8	V	IC turned off	P_4.2.30
Input current	I_{INH}	5	10	25	µA	V_{INH} = 5 V	P_4.2.31

1) Drop voltage = $V_i \geq$ 4.5V drop voltage = V_i - V_Q (below regulating voltage range).

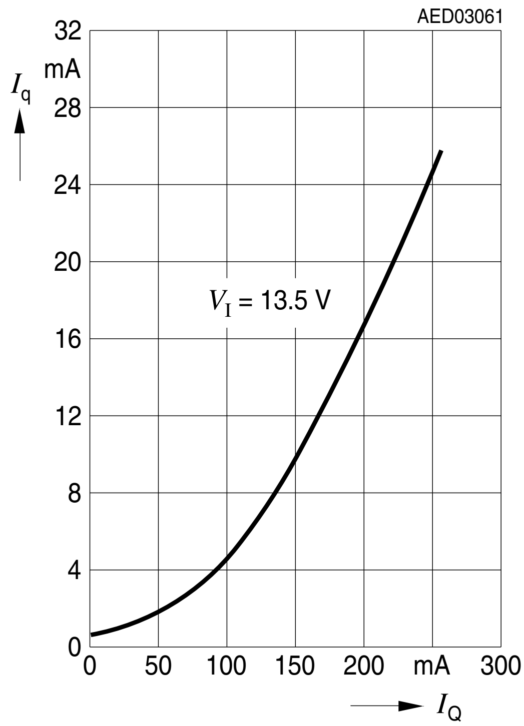
Note: The reset output is "low" within the range V_Q = 1 V to $V_{Q,rt}$.

4.3 Typical performance characteristics

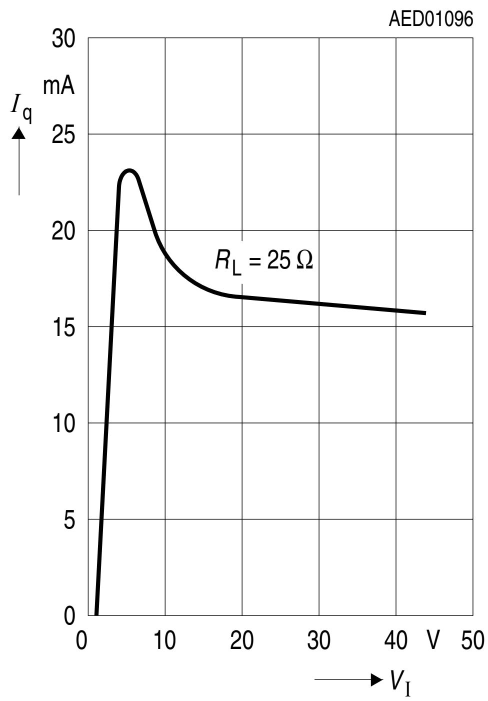
Drop voltage V_{DR} versus output current I_Q



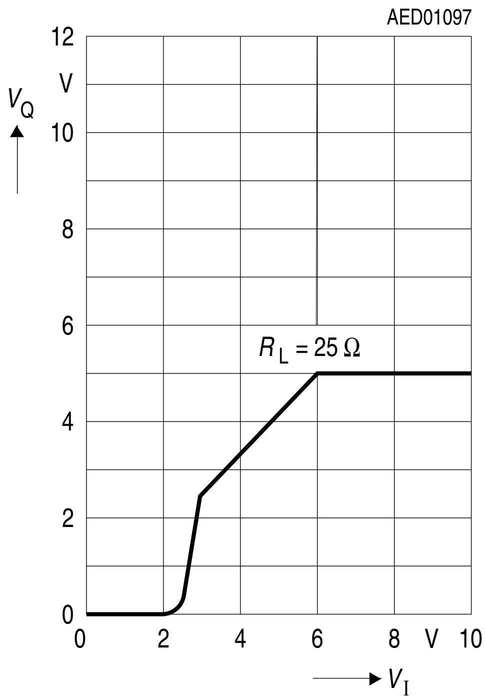
Current consumption I_q versus output current I_Q



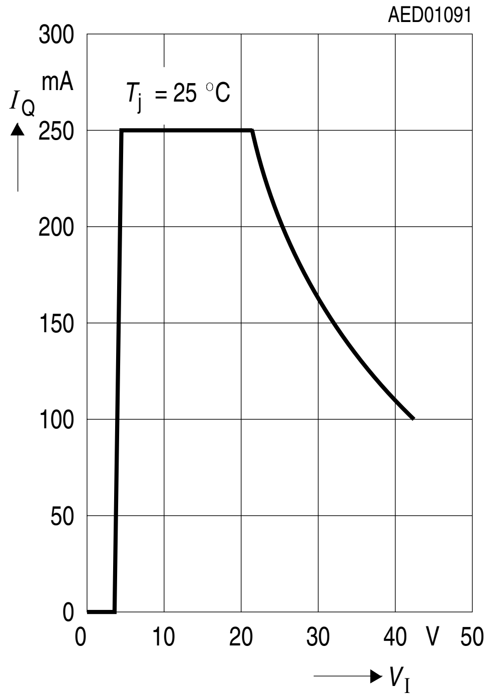
Current consumption I_q versus input voltage V_I



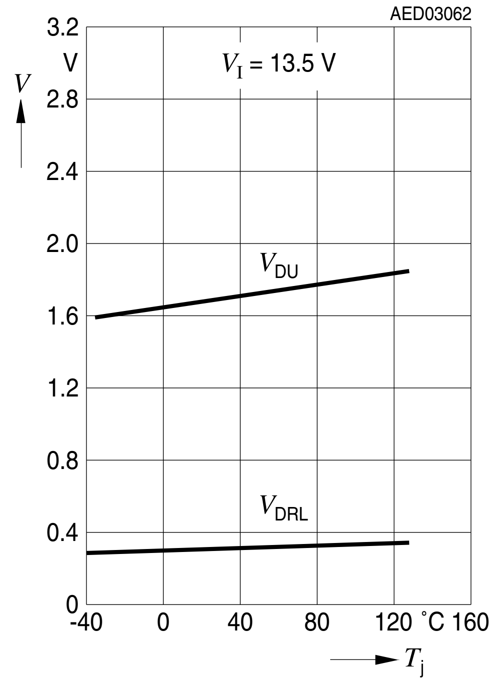
Output voltage V_Q versus input voltage V_I



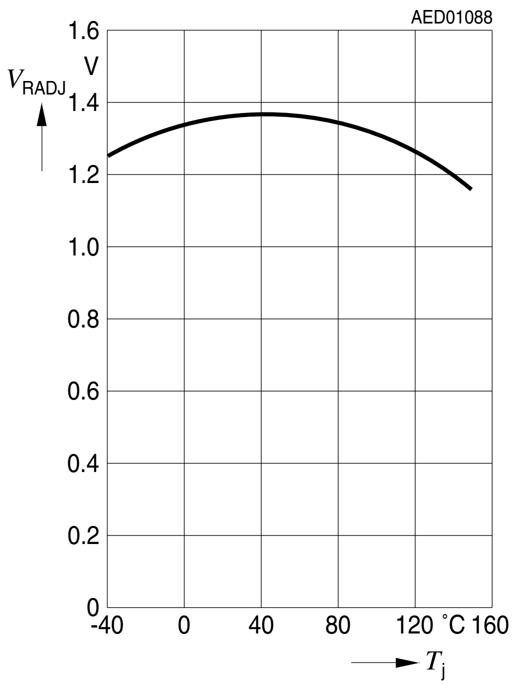
Output current I_Q versus input voltage V_I



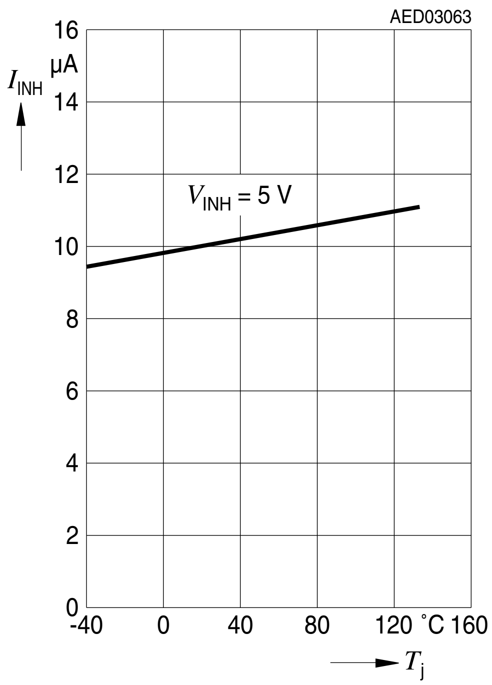
Timing threshold voltage V_{DU} and V_{DRL} versus junction temperature



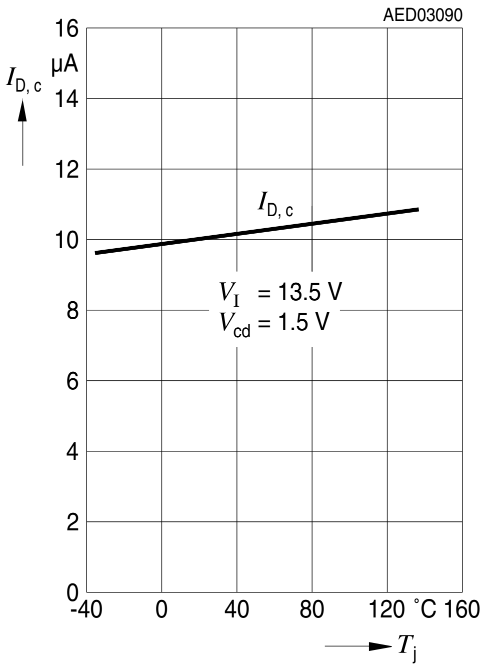
Reset switching threshold V_{RADJ} versus junction temperature T_J



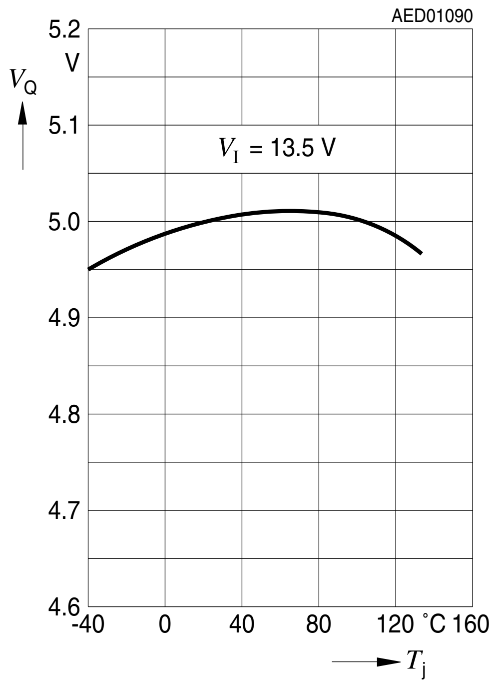
Current consumption of inhibit I_{INH} versus junction temperature T_J



Charge current and discharge current $I_{D,ch}$; $I_{D,dis}$ versus junction temperature T_J



Output voltage V_Q versus junction temperature T_J



5 Application information

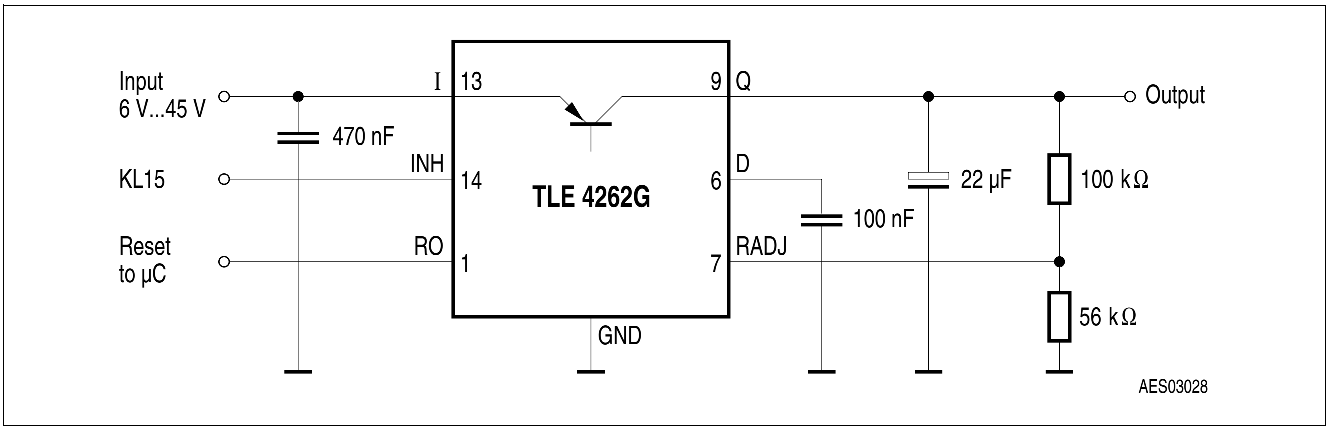


Figure 3 Application circuit

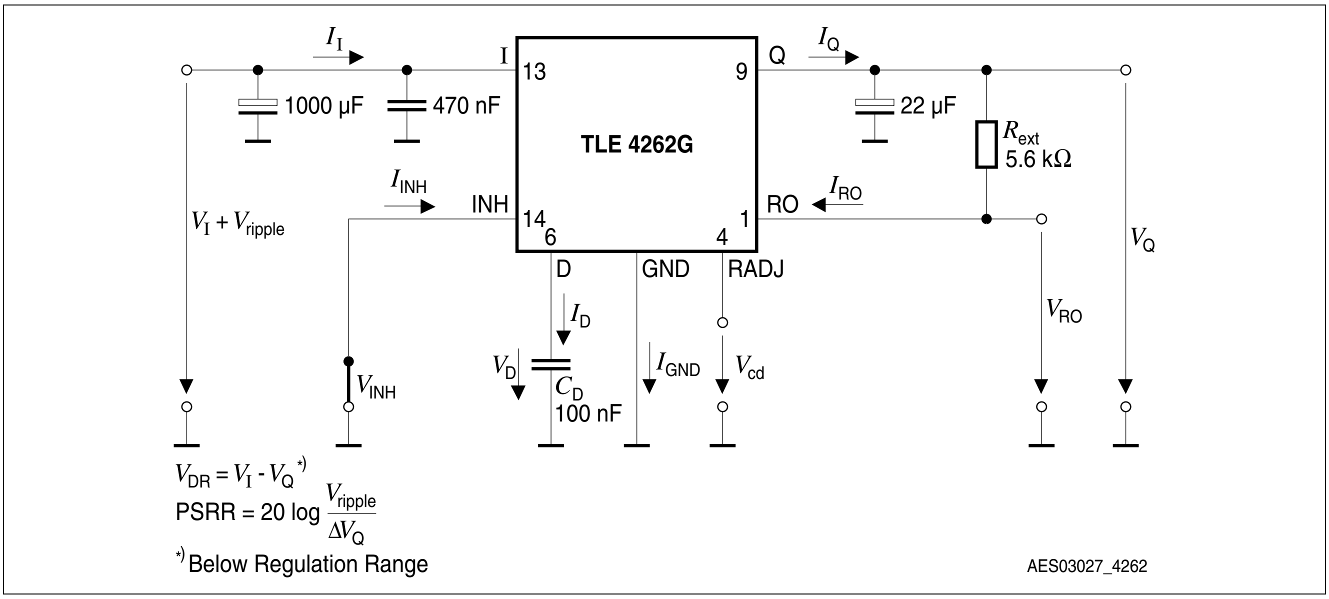


Figure 4 Test circuit

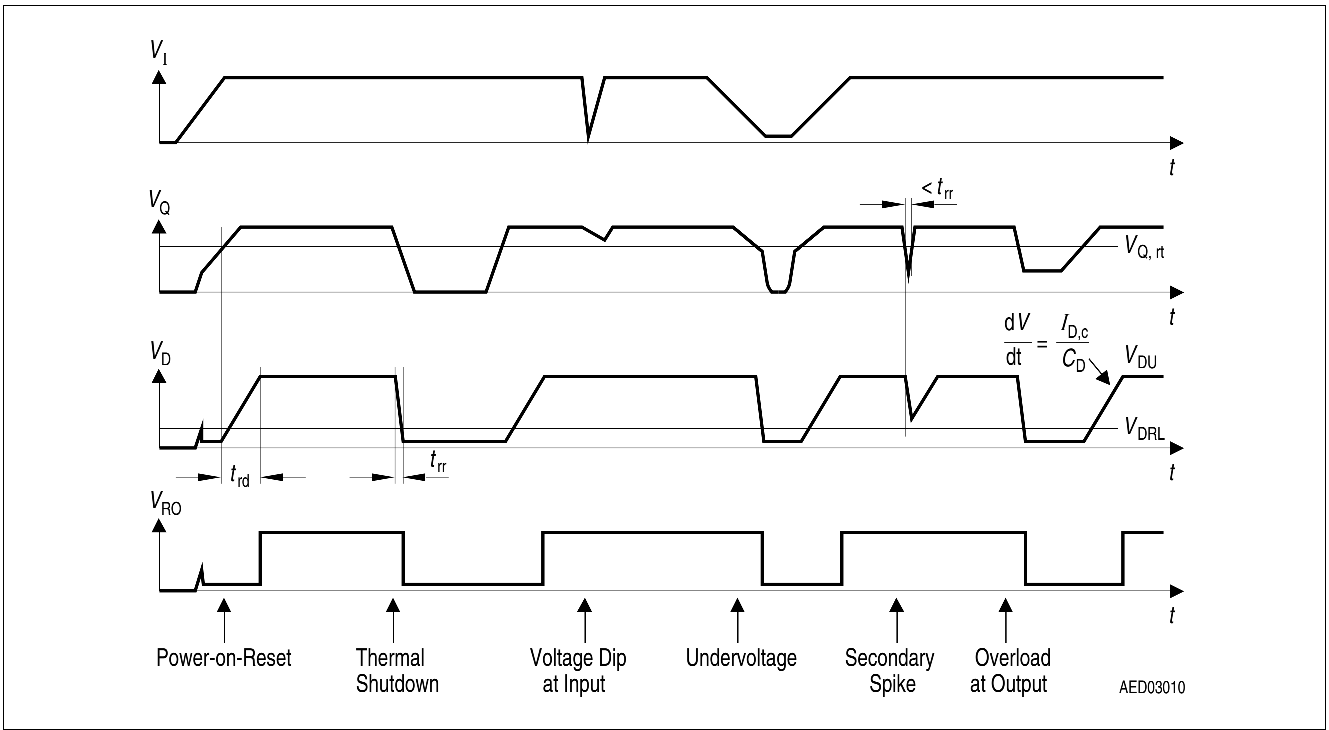


Figure 5 Time response

5.1 Reset timing

The power-on reset delay time is defined by the charging time of an external capacitor C_D which can be calculated as follows:

$$C_D = (\Delta t_{rd} \times I_{D,c}) / \Delta V \tag{5.1}$$

Definitions:

- C_D = delay capacitor
- Δt_{rd} = delay time
- $I_{D,c}$ = charge current, typical 10 µA
- $\Delta V = V_{DU}$, typical 1.8 V
- V_{DU} = upper delay switching threshold at C_D for reset delay time

6 Package information

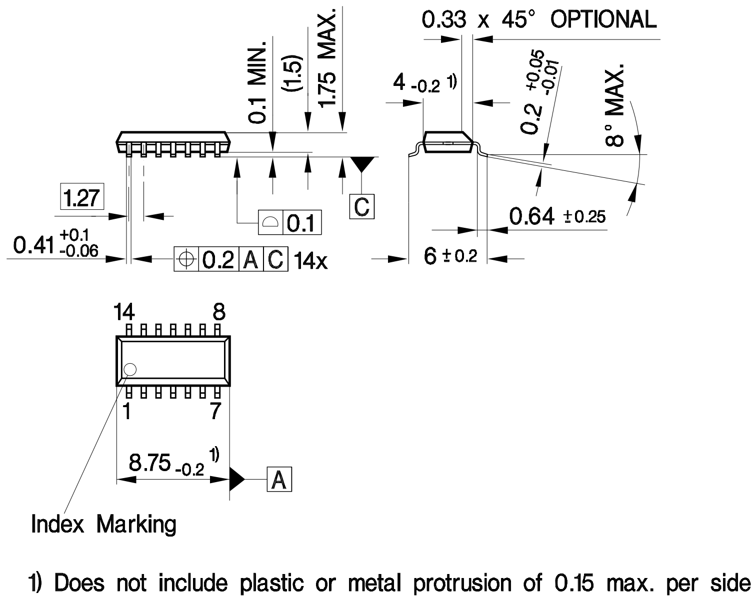


Figure 6 PG-DSO-14 (Plastic Dual Small Outline)[1)]

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

https://www.infineon.com/packages

1) Dimension in mm

7 Revision history

Revision	Date	Changes
3.1	2019-03-27	Updated layout and structure Package PG-DSO-20 deleted Updated package drawing "PG-DSO-14" Editorial changes

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