

300 mA LDO Regulator, Low Dropout Voltage, Ultra Low Noise, High PSRR with Power Good



ON Semiconductor®

www.onsemi.com

NCV8164C

The NCV8164C is a 300 mA LDO, next generation of high PSRR, ultra-low noise and low dropout regulators with Power Good open collector output. Designed to meet the requirements of RF and sensitive analog circuits, the NCV8164C device provides ultra-low noise, high PSRR and low quiescent current. The device also offer excellent load/line transients. The NCV8164C is designed to work with a 1 μ F input and a 1 μ F output ceramic capacitor. It is available in industry standard TSOP-5, WDFNW6 0.65P, 2 mm x 2 mm and DFNW8 0.65P, 3 mm x 3 mm.

Features

- Operating Input Voltage Range: 1.6 V to 5.0 V
- Available in Fixed Voltage Option: 1.2 V to 4.5 V
- Adjustable Version Reference Voltage: 1.2 V
- $\pm 2\%$ Accuracy Over Load and Temperature
- Ultra Low Quiescent Current Typ. 30 μ A
- Standby Current: Typ. 0.1 μ A
- Very Low Dropout: 110 mV at 300 mA for 3.3 V Variant
- Ultra High PSRR: Typ. 85 dB at 10 mA, f = 1 kHz
- Ultra Low Noise: 9 μ V_{RMS} (Fixed Version)
- Stable with a 1 μ F Small Case Size Ceramic Capacitors
- Available in – TSOP-5 3 mm x 1.5 mm x 1 mm CASE 483
 - ♦ WDFNW6 2 mm x 2 mm x 0.75 mm CASE 511DW
 - ♦ DFNW8 3 mm x 3 mm x 0.9 mm CASE 507AD
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements
- AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Communication Systems
- In-Vehicle Networking
- Telematics, Infotainment and Clusters
- General Purpose Automotive

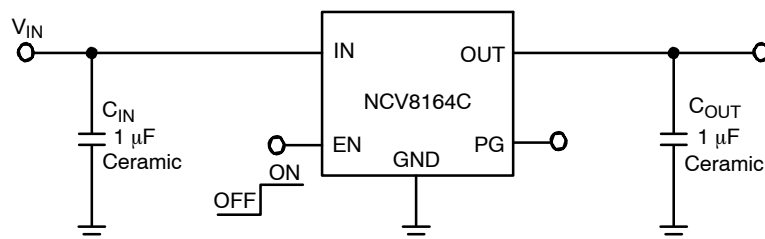
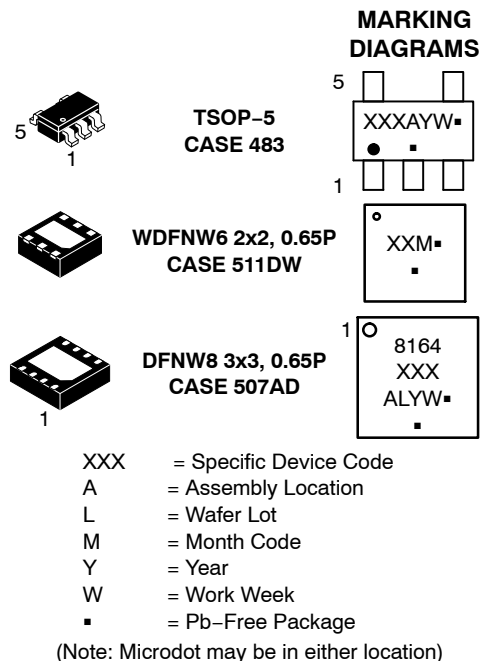
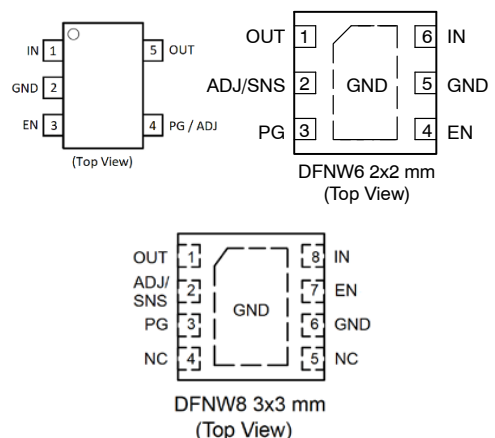


Figure 1. Typical Application Schematic



PIN CONNECTONS



ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 8 of this data sheet.

NCV8164C

Table 1. PIN FUNCTION DESCRIPTION

Pin No. TSOP-5	Pin No. WDFNW6	Pin No. DFNW8	Pin Name	Description
1	6	8	IN	Input voltage supply pin
5	1	1	OUT	Regulated output voltage. The output should be bypassed with small 1 μ F ceramic capacitor
3	4	7	EN	Chip enable: Applying $V_{EN} < 0.2$ V disables the regulator, Pulling $V_{EN} > 0.7$ V enables the LDO
4 / -	3	3	PG	Power Good, open collector. Use 10 k Ω to 100 k Ω pull-up resistor connected to output or input voltage
2	5	6	GND	Common ground connection
- / 4	2	2	ADJ	Adjustable output feedback pin (for adjustable version only)
-	2	2	SNS	Sense feedback pin. Must be connected to OUT pin on PCB (for fixed versions only)
-	-	4, 5	N/C	Not connected, pin can be tied to ground plane for better power dissipation
-	EPAD	EPAD	EPAD	Expose pad should be tied to ground plane for better power dissipation

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	-0.3 to 5.3	V
Output Voltage	V_{OUT}	-0.3 to $V_{IN}+0.3$, max. 5.3	V
Chip Enable Input	V_{CE}	-0.3 to 5.3	V
Power Good Voltage	V_{PG}	-0.3 to 5.3	V
Power Good Current	I_{PG}	30	mA
Output Short Circuit Duration	t_{SC}	unlimited	s
Maximum Junction Temperature	T_J	150	$^{\circ}$ C
Storage Temperature	T_{STG}	-55 to 150	$^{\circ}$ C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Charged Device Model (Note 2)	ESD_{CDM}	1000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
 ESD Human Body Model tested per AEC-Q100-002 (EIA/JESD22-A114)
 ESD Charged Device Model tested per EIA/JESD22-C101, Field Induced Charge Model

NCV8164C

Table 3. THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
THERMAL CHARACTERISTICS, TSOP-5 PACKAGE			
Thermal Resistance, Junction-to-Ambient (Note 3)	$R_{\theta JA}$	158	$^{\circ}C/W$
Thermal Resistance, Junction-to-Case (top)	$R_{\theta JC(top)}$	155	$^{\circ}C/W$
Thermal Resistance, Junction-to-Case (bottom) (Note 4)	$R_{\theta JC(bot)}$	102	$^{\circ}C/W$
Thermal Resistance, Junction-to-Board	$R_{\theta JB}$	197	$^{\circ}C/W$
Characterization Parameter, Junction-to-Top	Ψ_{JT}	40	$^{\circ}C/W$
Characterization Parameter, Junction-to-Board	Ψ_{JB}	82	$^{\circ}C/W$
THERMAL CHARACTERISTICS, WDFNW6-2X2, 0.65 PITCH PACKAGE			
Thermal Resistance, Junction-to-Ambient (Note 3)	$R_{\theta JA}$	51	$^{\circ}C/W$
Thermal Resistance, Junction-to-Case (top)	$R_{\theta JC(top)}$	142	$^{\circ}C/W$
Thermal Resistance, Junction-to-Case (bottom) (Note 4)	$R_{\theta JC(bot)}$	2.0	$^{\circ}C/W$
Thermal Resistance, Junction-to-Board	$R_{\theta JB}$	117	$^{\circ}C/W$
Characterization Parameter, Junction-to-Top	Ψ_{JT}	1.9	$^{\circ}C/W$
Characterization Parameter, Junction-to-Board	Ψ_{JB}	7.7	$^{\circ}C/W$
THERMAL CHARACTERISTICS, DFNW8-3X3, 0.65 PITCH PACKAGE			
Thermal Resistance, Junction-to-Ambient (Note 3)	$R_{\theta JA}$	50	$^{\circ}C/W$
Thermal Resistance, Junction-to-Case (top)	$R_{\theta JC(top)}$	142	$^{\circ}C/W$
Thermal Resistance, Junction-to-Case (bottom) (Note 4)	$R_{\theta JC(bot)}$	7.9	$^{\circ}C/W$
Thermal Resistance, Junction-to-Board	$R_{\theta JB}$	125	$^{\circ}C/W$
Characterization Parameter, Junction-to-Top	Ψ_{JT}	2.0	$^{\circ}C/W$
Characterization Parameter, Junction-to-Board	Ψ_{JB}	7.5	$^{\circ}C/W$

3. The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a high-K board, following the JEDEC51.7 guidelines with assumptions as above, in an environment described in JESD51-2a.
4. The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the IC exposed pad. Test description can be found in the ANSI SEMI standard G30-88.

NCV8164C

Table 4. ELECTRICAL CHARACTERISTICS ($-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$; $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$; $I_{OUT} = 1\text{ mA}$, $C_{IN} = C_{OUT} = 1\text{ }\mu\text{F}$, $V_{EN} = V_{IN}$, unless otherwise noted. Typical values are at $T_J = +25^{\circ}\text{C}$ (Note 5))

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Operating Input Voltage			V_{IN}	1.6		5.0	V
Output Voltage Accuracy	$V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$ to 5.0 V , $0.1\text{ mA} \leq I_{OUT} \leq 300\text{ mA}$		V_{OUT}	-2		+2	%
Reference Voltage (Adjustable Ver. ADJ pin connected to OUT)	$V_{IN} = 1.6\text{ V}$ to 5.0 V , $0.1\text{ mA} \leq I_{OUT} \leq 300\text{ mA}$		V_{ADJ}	1.176	1.2	1.224	V
Line Regulation	$V_{OUT(NOM)} + 0.5\text{ V} \leq V_{IN} \leq 5.0\text{ V}$		$Line_{Reg}$		0.5		mV/V
Load Regulation	$I_{OUT} = 1\text{ mA}$ to 300 mA		$Load_{Reg}$		2		mV
Dropout Voltage (Note 6) TSOP-5, WDFNW6	$I_{OUT} = 300\text{ mA}$	$V_{OUT(NOM)} = 1.5\text{ V}$	V_{DO}		170	295	mV
		$V_{OUT(NOM)} = 1.8\text{ V}$			155	255	
		$V_{OUT(NOM)} = 2.5\text{ V}$			125	200	
		$V_{OUT(NOM)} = 2.8\text{ V}$			115	185	
		$V_{OUT(NOM)} = 3.0\text{ V}$			113	177	
		$V_{OUT(NOM)} = 3.3\text{ V}$			110	170	
		$V_{OUT(NOM)} = 4.5\text{ V}$			95	135	
Dropout Voltage (Note 6) DFNW8	$I_{OUT} = 300\text{ mA}$	$V_{OUT(NOM)} = 1.5\text{ V}$	V_{DO}		180	315	mV
		$V_{OUT(NOM)} = 1.8\text{ V}$			165	275	
		$V_{OUT(NOM)} = 2.5\text{ V}$			140	220	
		$V_{OUT(NOM)} = 2.8\text{ V}$			130	205	
		$V_{OUT(NOM)} = 3.0\text{ V}$			127	197	
		$V_{OUT(NOM)} = 3.3\text{ V}$			125	190	
		$V_{OUT(NOM)} = 4.5\text{ V}$			112	170	
Output Current Limit	$V_{OUT} = 90\% V_{OUT(NOM)}$		I_{CL}	350	560		mA
Short Circuit Current	$V_{OUT} = 0\text{ V}$		I_{SC}		580		
Quiescent Current	$I_{OUT} = 0\text{ mA}$		I_Q		30	40	μA
Shutdown Current	$V_{EN} \leq 0.4\text{ V}$		I_{DIS}		0.01	1.5	μA
EN Pin Threshold Voltage	EN Input Voltage "H"		V_{ENH}	0.7			V
	EN Input Voltage "L"		V_{ENL}			0.2	
EN Pull Down Current	$V_{EN} = 5.0\text{ V}$		I_{EN}		0.2	0.6	μA
Power Good Threshold Voltage	Output Voltage Raising		V_{PGUP}		95		%
	Output Voltage Falling		V_{PGDW}		90		
Power Good Output Voltage Low	$I_{PG} = 5\text{ mA}$, Open drain		V_{PGLO}			0.3	V
Turn-On Time (Note 7)	$C_{OUT} = 1\text{ }\mu\text{F}$, From assertion of V_{EN} to $V_{OUT} = 95\% V_{OUT(NOM)}$				120		μs
Power Supply Rejection Ratio (Note 7)	$V_{OUT(NOM)} = 3.3\text{ V}$, $I_{OUT} = 10\text{ mA}$	$f = 100\text{ Hz}$	$PSRR$		83		dB
		$f = 1\text{ kHz}$			85		
		$f = 10\text{ kHz}$			80		
		$f = 100\text{ kHz}$			61		
Output Voltage Noise (Fixed Ver.)	$f = 10\text{ Hz}$ to 100 kHz	$I_{OUT} = 10\text{ mA}$	V_N		9		μV_{RMS}
Thermal Shutdown Threshold (Note 7)	Temperature rising		T_{SDH}		165		$^{\circ}\text{C}$
	Temperature hysteresis		T_{HYST}		15		$^{\circ}\text{C}$
Active output discharge resistance	$V_{EN} < 0.2\text{ V}$, Version A only		R_{DIS}		260		Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Performance guaranteed over the indicated operating temperature range by design and/or characterization.

Production tested at $T_J = T_A = 25^{\circ}\text{C}$.

6. Low duty cycle pulse techniques are used during the testing to maintain the junction temperature as close to ambient as possible. Dropout voltage is characterized when V_{OUT} falls 3% below $V_{OUT(NOM)}$.

7. Guaranteed by design and characterization.

TYPICAL CHARACTERISTICS

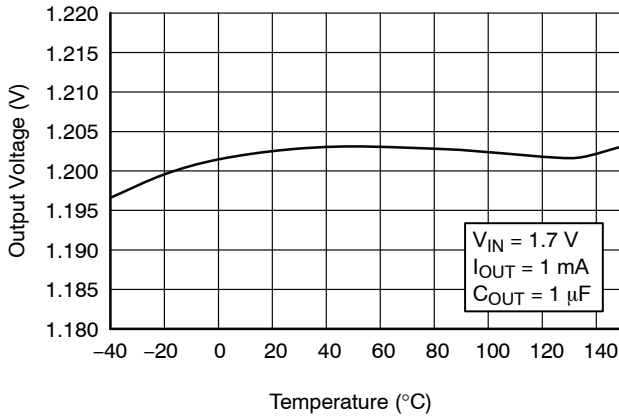


Figure 2. Output Voltage vs. Temperature – $V_{OUT} = 1.2\text{ V}$

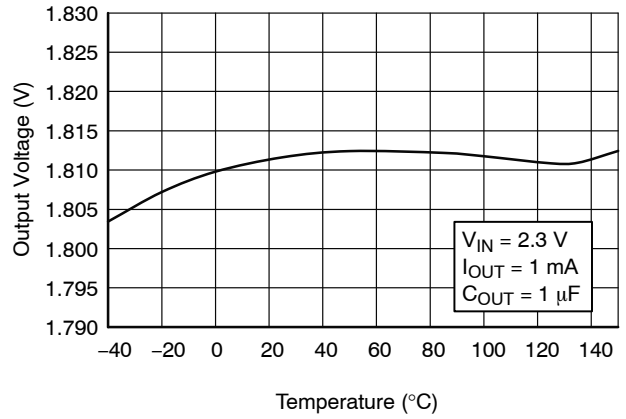


Figure 3. Output Voltage vs. Temperature – $V_{OUT} = 1.8\text{ V}$

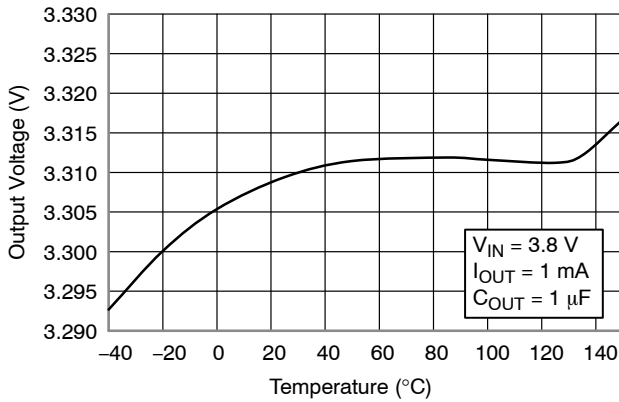


Figure 4. Output Voltage vs. Temperature – $V_{OUT} = 3.3\text{ V}$

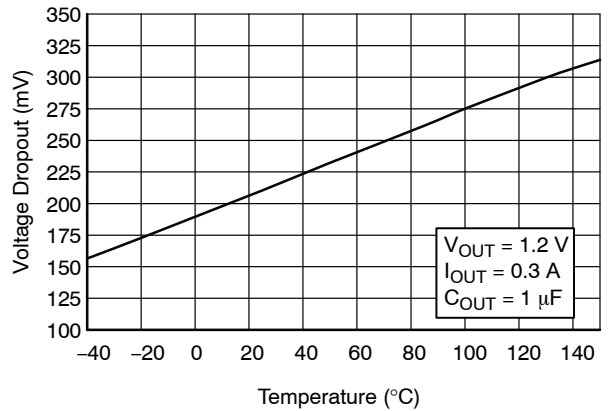


Figure 5. Dropout Voltage vs. Temperature – $V_{OUT} = 1.2\text{ V}$

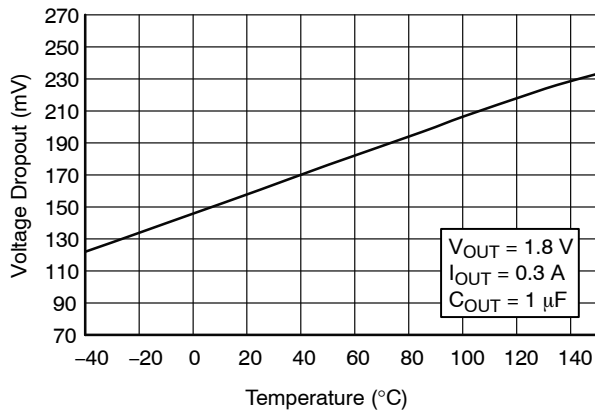


Figure 6. Dropout Voltage vs. Temperature – $V_{OUT} = 1.8\text{ V}$

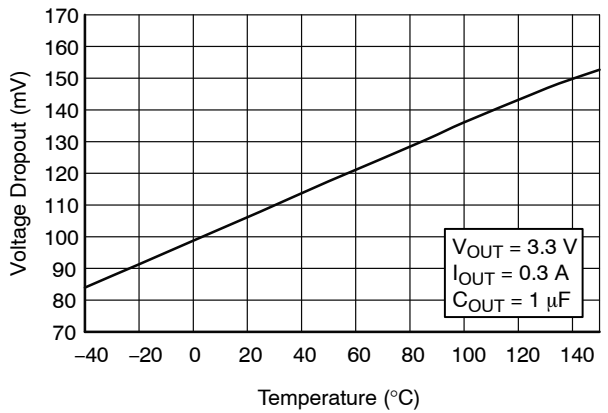


Figure 7. Dropout Voltage vs. Temperature – $V_{OUT} = 3.3\text{ V}$

NCV8164C

TYPICAL CHARACTERISTICS (continued)

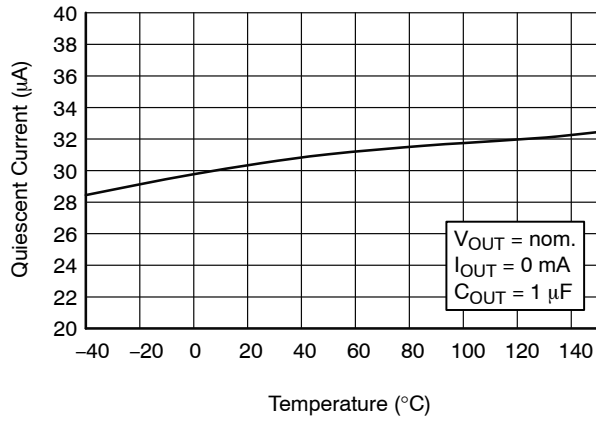


Figure 8. Quiescent Current vs. Temperature

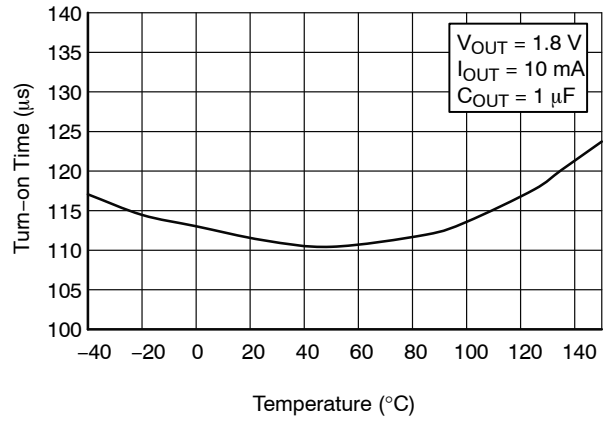


Figure 9. Turn-on Time vs. Temperature

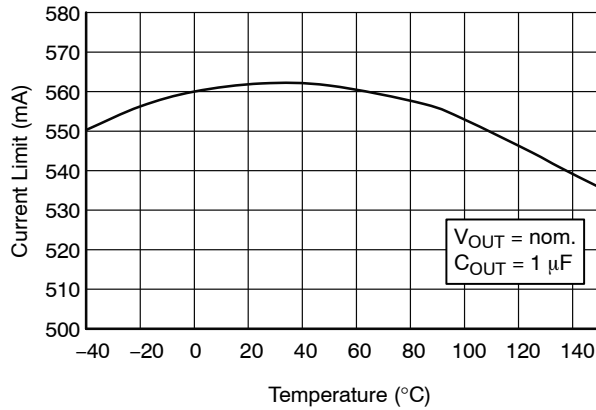


Figure 10. Current Limit vs. Temperature

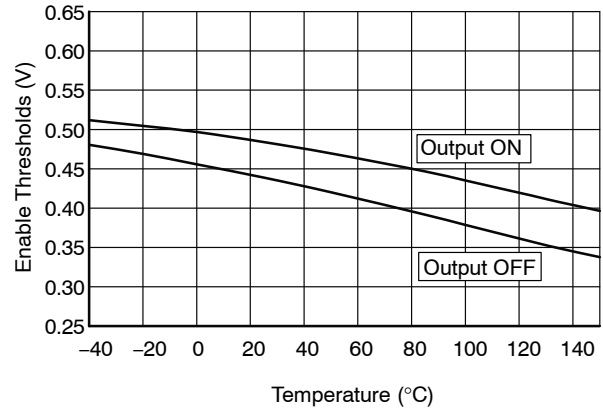


Figure 11. Enable Thresholds vs. Temperature

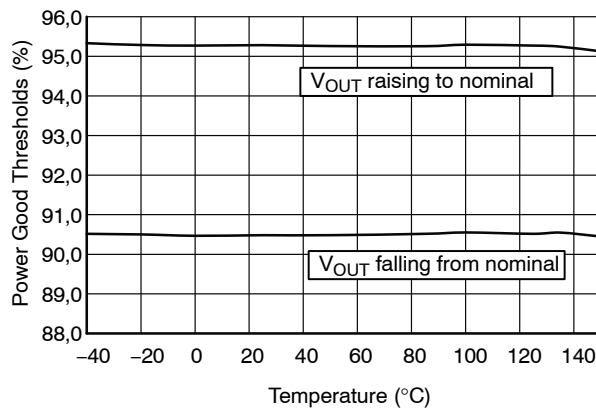


Figure 12. Power Good Threshold vs. Temperature

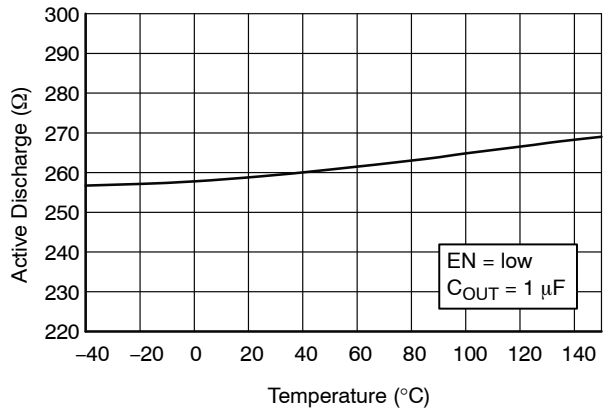


Figure 13. Active Discharge Resistance vs. Temperature

NCV8164C

TYPICAL CHARACTERISTICS (continued)

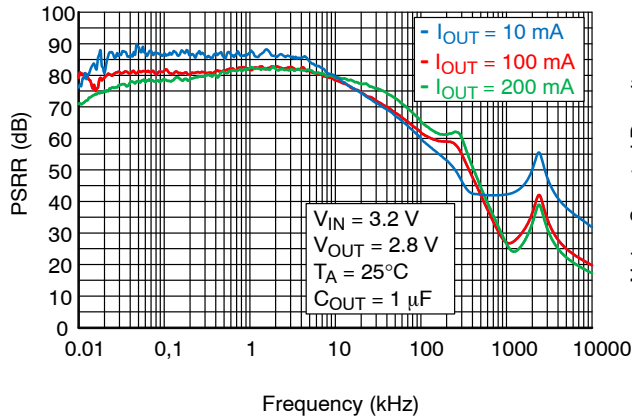


Figure 14. Power Supply Rejection Ratio for $V_{OUT} = 2.8\text{ V}$, $C_{OUT} = 1\ \mu\text{F}$

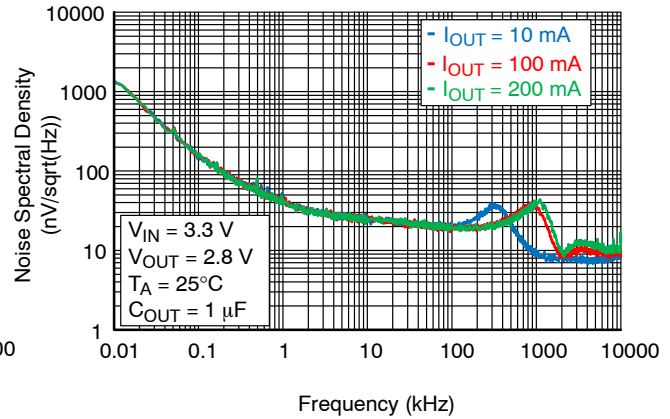


Figure 15. Output Voltage Noise Spectral Density for $V_{OUT} = 2.8\text{ V}$, $C_{OUT} = 1\ \mu\text{F}$

APPLICATIONS INFORMATION

The NCV8164C is the member of new family of high output current and low dropout regulators which delivers low quiescent and ground current consumption, good noise and power supply ripple rejection ratio performance. The NCV8164C incorporates EN pin and power good output for simple controlling by MCU or logic. Standard features include current limiting, soft-start feature and thermal protection.

Input Decoupling (C_{IN})

It is recommended to connect at least $1\ \mu\text{F}$ ceramic X5R or X7R capacitor between IN and GND pin of the device. This capacitor will provide a low impedance path for any unwanted AC signals or noise superimposed onto constant input voltage. The good input capacitor will limit the influence of input trace inductances and source resistance during sudden load current changes. Higher capacitance and lower ESR capacitors will improve the overall line transient response.

Output Decoupling (C_{OUT})

The NCV8164C does not require a minimum Equivalent Series Resistance (ESR) for the output capacitor. The device is designed to be stable with standard ceramics capacitors with values of $1\ \mu\text{F}$ or greater. The X5R and X7R types have the lowest capacitance variations over temperature thus they are recommended.

Power Good Output Connection

The NCV8164C include Power Good functionality for better interfacing to MCU system. Power Good output is open collector type, capable to sink up to 10 mA. Recommended operating current is between 10 μA and

1 mA to obtain low saturation voltage. External pull-up resistor can be connected to any voltage up to 5.0 V (please see Absolute Maximum Ratings table).

Power Dissipation and Heat Sinking

The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. For reliable operation junction temperature should be limited to $+125^\circ\text{C}$, however device is capable to work up to junction temperature $+150^\circ\text{C}$. The maximum power dissipation the NCV8164C can handle is given by:

$$P_{D(\text{MAX})} = \frac{[T_{J(\text{MAX})} - T_A]}{R_{\theta\text{JA}}} \quad (\text{eq. 1})$$

The power dissipated by the NCV8164C for given application conditions can be calculated from the following equations:

$$P_D \approx V_{IN}(I_{\text{GND}} + I_{\text{OUT}}) + I_{\text{OUT}}(V_{IN} - V_{OUT}) \quad (\text{eq. 2})$$

or

$$V_{IN(\text{MAX})} \approx \frac{P_{D(\text{MAX})} + (V_{OUT} \times I_{\text{OUT}})}{I_{\text{OUT}} + I_{\text{GND}}} \quad (\text{eq. 3})$$

Hints

V_{IN} and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high, there is a chance to pick up noise or cause the regulator to malfunction. Place external components, especially the output capacitor, as close as possible to the NCV8164C, and make traces as short as possible.

NCV8164C

Adjustable Version

Not only adjustable version, but also any fixed version can be used to create adjustable voltage, where original fixed voltage becomes reference voltage for resistor divider and feedback loop. Output voltage can be equal or higher than original fixed option, while possible range is from 1.2 V up to 4.5 V. Figure 16 shows how to add external resistors to increase output voltage above fixed value.

Output voltage is then given by equation

$$V_{OUT} = V_{FIX} \times (1 + R1/R2) \quad (\text{eq. 4})$$

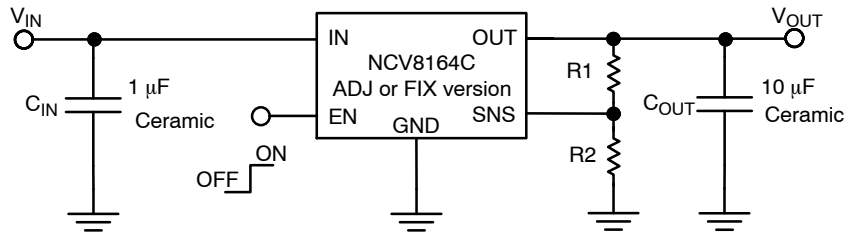


Figure 16. Adjustable Variant Application

Please note that output noise is amplified by V_{OUT} / V_{FIX} ratio. For example, if original 1.2 V fixed variant is used to create 3.6 V output voltage, output noise is increased $3.6 / 1.2 = 3$ times and real value will be $3 \times 9 \mu\text{Vrms} = 27 \mu\text{Vrms}$. For noise sensitive applications it is recommended to use as

where V_{FIX} is voltage of original fixed version (from 1.2 V up to 4.5 V) or adjustable version (1.2 V). Do not operate the device at output voltage about 4.7 V, as device can be damaged.

In order to avoid influence of current flowing into SNS pin to output voltage accuracy (SNS current varies with voltage option and temperature, typical value is 300 nA) it is recommended to use values of R1 and R2 below 500 kΩ.

high fixed variant as possible – for example in case above it is better to use 3.3 V fixed variant to create 3.6 V output voltage, as output noise will be amplified only $3.6 / 3.3 = 1.09 \times (9.8 \mu\text{Vrms})$.

ORDERING INFORMATION

Device Part No.	Wafer Part	Marking	Package Option	Package	Shipping †
NCV8164CSN180T1G	A0C00HJ-FNT8	EJ	N/A	TSOP5 (Pb-Free)	3000 / Tape & Reel
NCV8164CSN280T1G	A0C00HH-FNT8	EK	N/A	TSOP5 (Pb-Free)	3000 / Tape & Reel
NCV8164CSNADJT1G	A0C00HP-FNT8	E4	N/A	TSOP5 (Pb-Free)	3000 / Tape & Reel
NCV8164CMTW180TAG	A0C00HJ-FNT8	HJ	Wettable	WDFNW6 2 x 2 (WF, Pb-Free)	3000 / Tape & Reel
NCV8164CMTW280TAG	A0C00HH-FNT8	HK	Wettable	WDFNW6 2 x 2 (WF, Pb-Free)	3000 / Tape & Reel
NCV8164CMTW290TAG	A0C00HK-FNT8	HH	Wettable	WDFNW6 2 x 2 (WF, Pb-Free)	3000 / Tape & Reel
NCV8164CMTWADJTAG	A0C00HP-FNT8	H2	Wettable	WDFNW6 2 x 2 (WF, Pb-Free)	3000 / Tape & Reel
NCV8164CAMLADJTCG	A0C00HP-FNT8	G2	Wettable	DFNW8 3 x 3 (WF, Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT

North American Technical Support:

Voice Mail: 1 800-282-9855 Toll Free USA/Canada

Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative