RENESAS

LED DRIVER

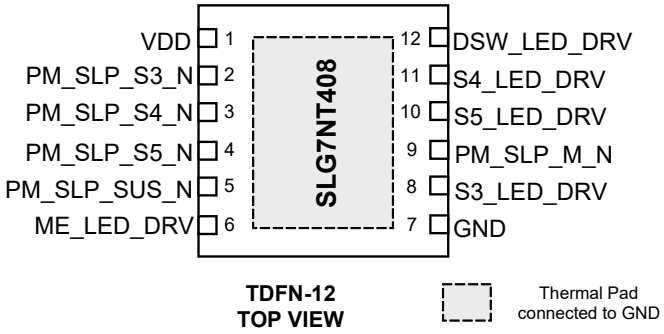
General Description

Renesas GreenPAK 2 SLG7NT4082 is a low power and small form device. The SoC is housed in a 2.5mm x 2.5mm TDFN package which is optimal for using with small devices.

Features

- Low Power Consumption
- Dynamic Voltage Supply Range
- RoHS Compliant / Halogen-Free
- Pb-Free TDFN-12 Package

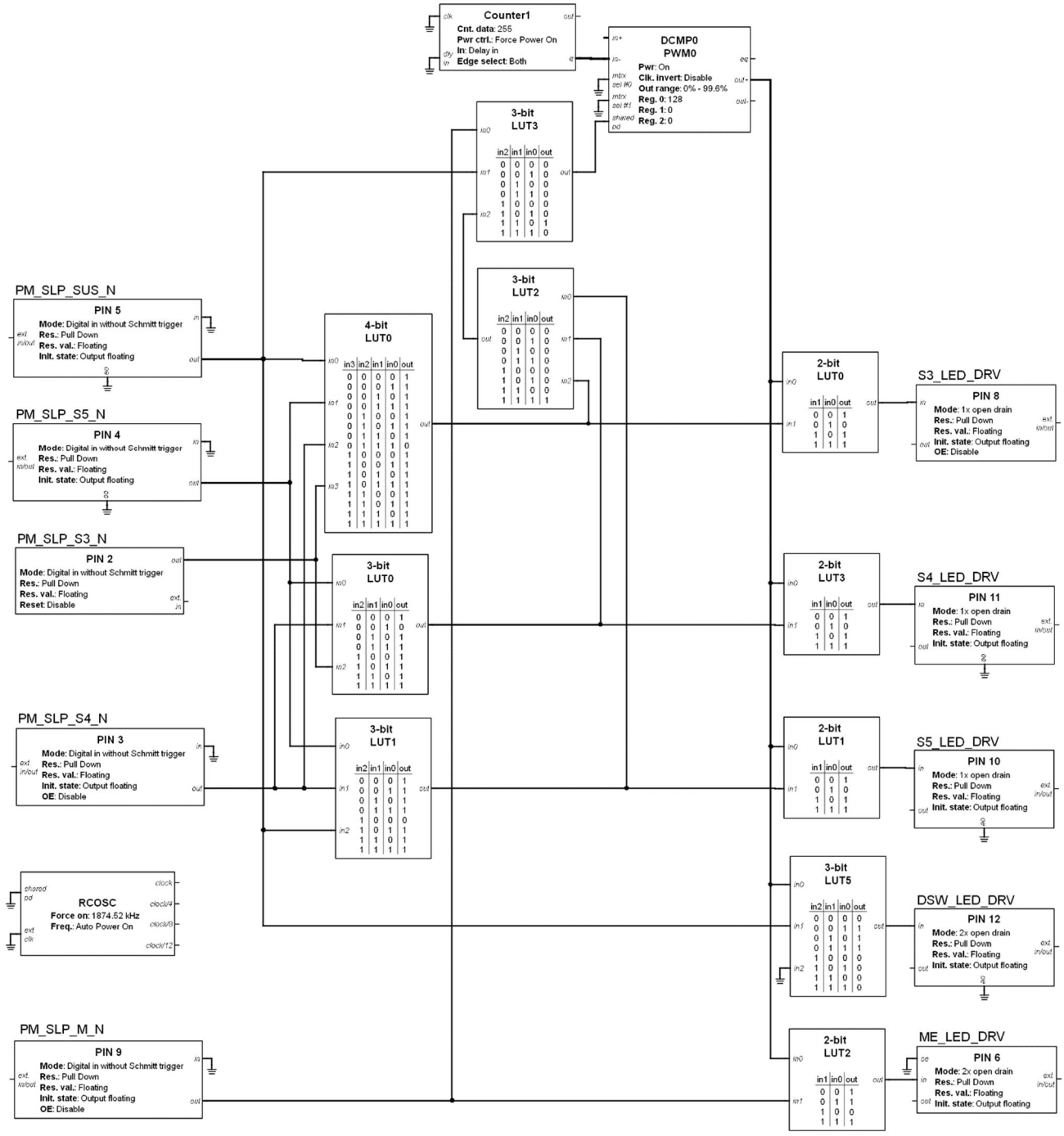
Pin Configuration



Output Summary

- 3 Outputs — Open Drain NMOS 1X
- 2 Outputs — Open Drain NMOS 2X

Block Diagram



Pin Configuration

Pin #	Pin Name	Type	Pin Description
1	VDD	PWR	Supply Voltage
2	PM_SLP_S3_N	Digital Input	Digital Input without Schmitt trigger
3	PM_SLP_S4_N	Digital Input	Digital Input without Schmitt trigger
4	PM_SLP_S5_N	Digital Input	Digital Input without Schmitt trigger
5	PM_SLP_SUS_N	Digital Input	Digital Input without Schmitt trigger
6	ME_LED_DRV	Digital Output	Open Drain NMOS 2X
7	GND	GND	Ground
8	S3_LED_DRV	Digital Output	Open Drain NMOS 1X
9	PM_SLP_M_N	Digital Input	Digital Input without Schmitt trigger
10	S5_LED_DRV	Digital Output	Open Drain NMOS 1X
11	S4_LED_DRV	Digital Output	Open Drain NMOS 1X
12	DSW_LED_DRV	Digital Output	Open Drain NMOS 2X
Exposed Bottom Pad	Exposed Bottom Pad	GND	Ground

Ordering Information

Part Number	Package Type
SLG7NT4082V	V = TDFN-12
SLG7NT4082VTR	VTR = TDFN-12 - Tape and Reel (3k units)

Absolute Maximum Conditions

Parameter	Min.	Max.	Unit
V_{HIGH} to GND	-0.3	7	V
Voltage at input pins	-0.3	7	V
Current at input pin	-1.0	1.0	mA
Storage temperature range	-65	125	°C
Junction temperature	--	150	°C
ESD Protection (Human Body Model)	2000	--	V
ESD Protection (Charged Device Model)	1000	--	V
Moisture Sensitivity Level	1		

Electrical Characteristics

(@ 25°C, unless otherwise stated)

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		1.71	3.3	5.5	V
T_A	Operating Temperature		-40	+25	+85	°C
I_Q	Quiescent Current	Static inputs and outputs	--	1	--	µA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD	V
I_O	Maximal Average or DC Current (note 1)	Per Each Chip Side	--	--	24	mA
V_{IH}	HIGH-Level Input Voltage	Logic Input, at VDD=1.8V	1.1	--	--	V
		Logic Input, at VDD=3.3V	1.8	--	--	
		Logic Input, at VDD=5.0V	2.6	--	--	
V_{IL}	LOW-Level Input Voltage	Logic Input, at VDD=1.8V	--	--	0.65	V
		Logic Input, at VDD=3.3V	--	--	1.1	
		Logic Input, at VDD=5.0V	--	--	1.7	
I_{IH}	HIGH-Level Input Current	Logic Input Pins;V_{IN} = VDD	-1.0	--	1.0	µA
I_{IL}	LOW-Level Input Current	Logic Input Pins; V_{IN} = 0V	-1.0	--	1.0	µA
V_{OL}	LOW-Level Output Voltage (note 1)	Open Drain, I_{OL} = 5mA, 1X Driver, at VDD=1.8 V	--	--	0.340	V
		Open Drain, I_{OL} = 5mA, 2X Driver, at VDD=1.8 V	--	--	0.138	
		Open Drain, I_{OL} = 20mA, 1X Driver, at VDD=3.3 V	--	--	0.605	
		Open Drain, I_{OL} = 20mA, 2X Driver, at VDD=3.3 V	--	--	0.252	

		Open Drain, I_{OL} = 20mA, 1X Driver, at VDD=5.0 V	--	--	0.36	
		Open Drain, I_{OL} = 20mA, 2X Driver, at VDD=5.0 V	--	--	0.17	
I_{OL}	LOW-Level Output Current (note 1)	Open Drain, V_{OL} =0.15V, 1X Driver, at VDD=1.8 V	2.72	--	--	mA
		Open Drain, V_{OL} =0.15V, 2X Driver, at VDD=1.8 V	5.44	--	--	
		Open Drain, V_{OL} =0.4V, 1X Driver, at VDD=3.3 V	14.688	--	--	
		Open Drain, V_{OL} =0.4V, 2X Driver, at VDD=3.3 V	29.376	--	--	
		Open Drain, V_{OL} =0.4V, 1X Driver, at VDD=5.0 V	21.96	--	--	
		Open Drain, V_{OL} =0.4V, 2X Driver, at VDD=5.0 V	43.92	--	--	
T_{SU}	Start up Time	After VDD reaches 1.6V level		7		ms

1. Guaranteed by Design.

Description

The device is specially designed to replace a big amount of discrete elements. Its main function is to drive 5 LEDs.

Truth tables:

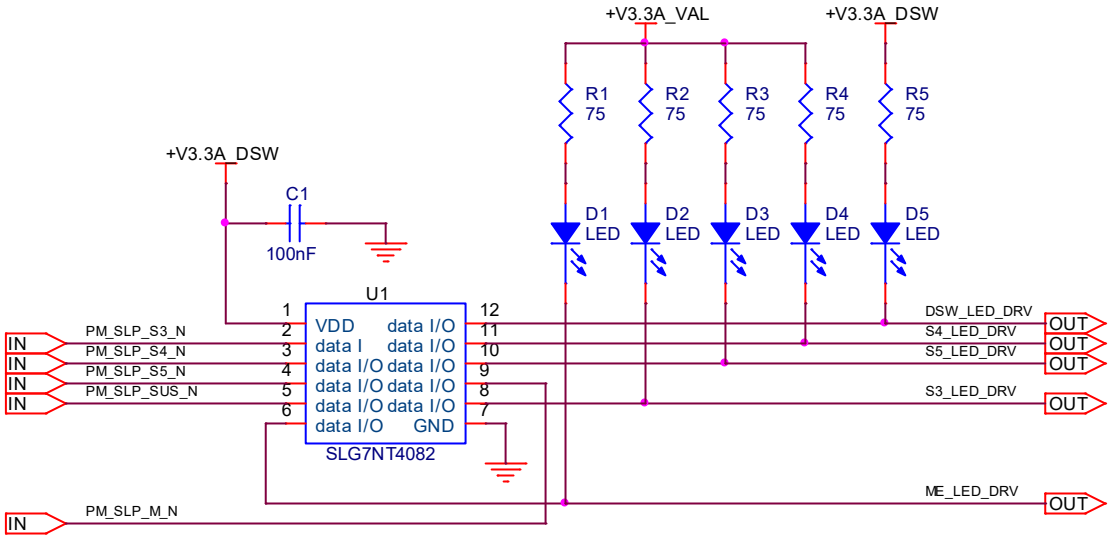
Inputs				Outputs			
PIN5	PIN4	PIN3	PIN2	PIN12	PIN10	PIN11	PIN8
PM_SLP_SUS_N	PM_SLP_S5_N	PM_SLP_S4_N	PM_SLP_S3_N	DSW_LED_DRV	S5_LED_DRV	S4_LED_DRV	S3_LED_DRV
1	1	1	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z
1	1	1	0	Hi-Z	Hi-Z	Hi-Z	PWM
1	1	0	0	Hi-Z	Hi-Z	PWM	Hi-Z
1	0	0	0	Hi-Z	PWM	Hi-Z	Hi-Z
0	0	0	0	PWM	Hi-Z	Hi-Z	Hi-Z
0	0	1	0	PWM	Hi-Z	Hi-Z	Hi-Z

Inputs					Outputs
PIN5	PIN4	PIN3	PIN2	PIN9	PIN6
PM_SLP_SUS_N	PM_SLP_S5_N	PM_SLP_S4_N	PM_SLP_S3_N	PM_SLP_M_N	ME_LED_DRV
X	X	X	X	1	PWM
X	X	X	X	0	Hi-Z

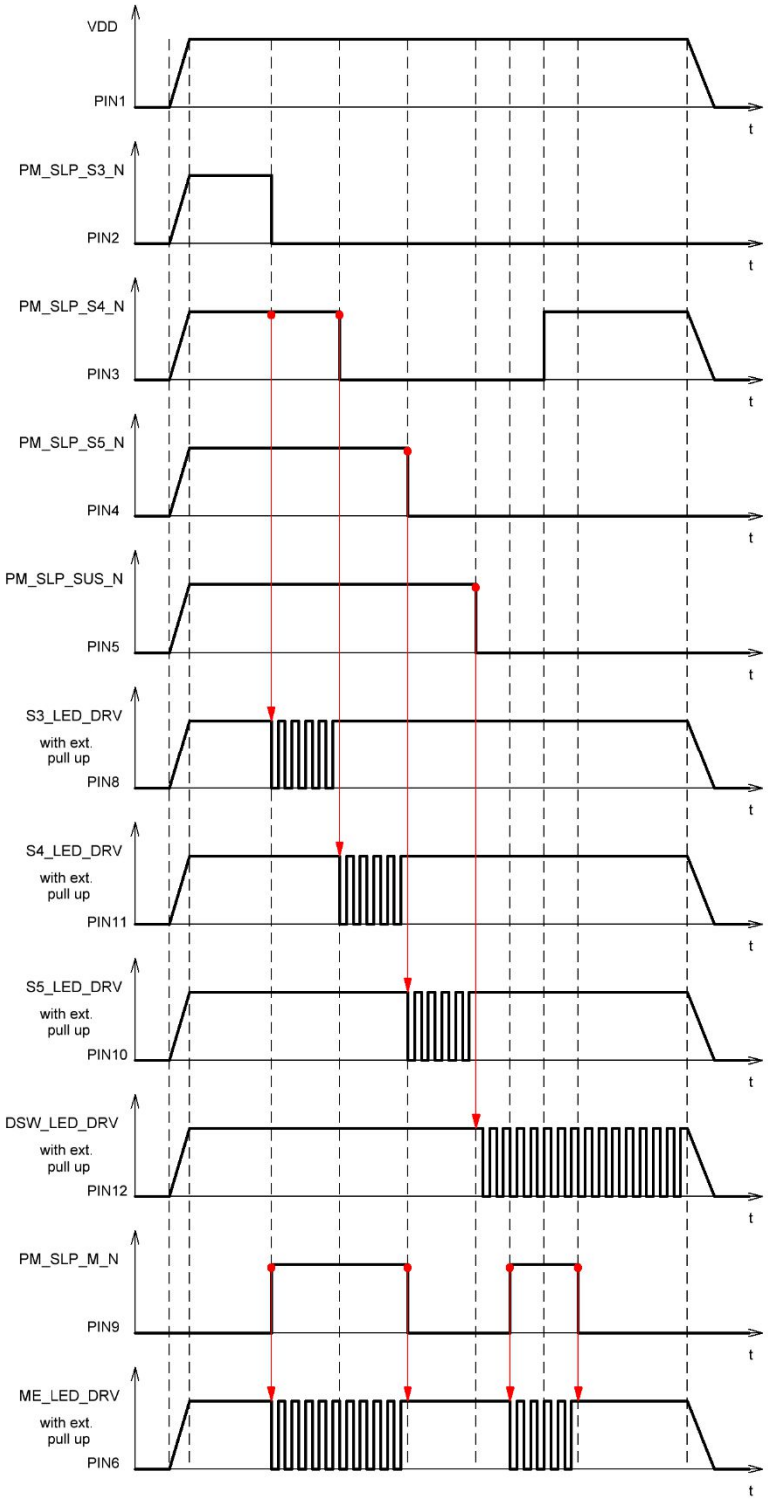
0 – Logic state LOW;
1 – Logic state HIGH;
X – Don't care;
Hi-Z – high impedance state;
PWM – 50% duty cycle PWM signal with ~ 7.3 kHz frequency

All pins are in a high impedance state until the chip has powered up.

Typical Application Circuit



Timing Diagrams



SLG7NT4082 Functionality Waveforms

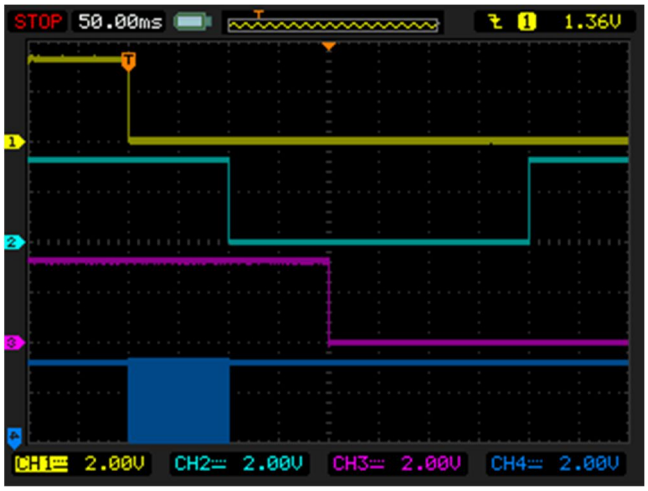
Channel 1 (yellow/top) – Pin #2 (PM_SLP_S3_N)

Channel 2 (light blue/2nd line) – Pin #3 (PM_SLP_S4_N)

Channel 3 (magenta/3rd line) – Pin #4 (PM_SLP_S5_N)

Channel 4 (blue/bottom) – Pin #8 (S3_LED_DRV) with external 5kΩ pull up resistor

1. S3 LED functionality, PM_SLP_SUS_N is HIGH, goes LOW 100ms after S3_LED_DRV goes LOW



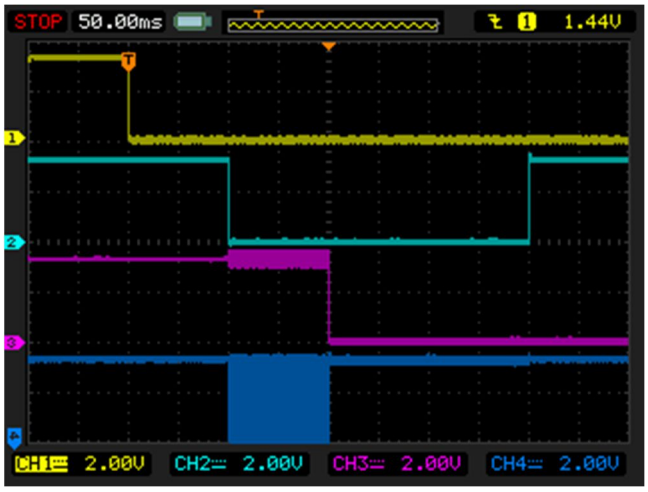
Channel 1 (yellow/top) – Pin #2 (PM_SLP_S3_N)

Channel 2 (light blue/2nd line) – Pin #3 (PM_SLP_S4_N)

Channel 3 (magenta/3rd line) – Pin #4 (PM_SLP_S5_N)

Channel 4 (blue/bottom) – Pin #11 (S4_LED_DRV) with external 5kΩ pull up resistor

2. S4 LED functionality, PM_SLP_SUS_N is HIGH, goes LOW 100ms after S3_LED_DRV goes LOW



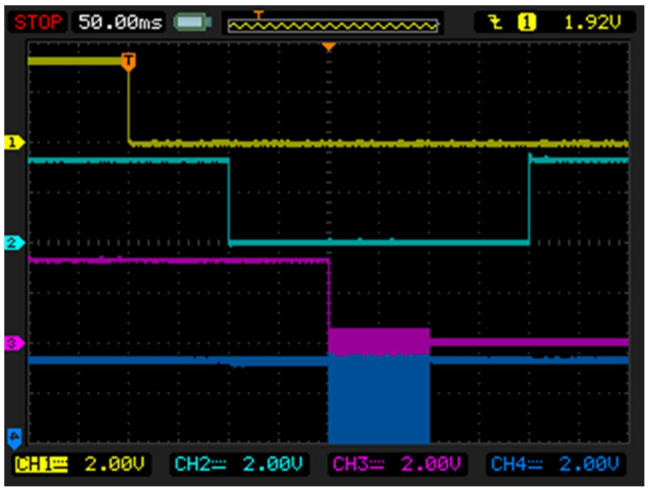
Channel 1 (yellow/top) – Pin #2 (PM_SLP_S3_N)

Channel 2 (light blue/2nd line) – Pin #3 (PM_SLP_S4_N)

Channel 3 (magenta/3rd line) – Pin #4 (PM_SLP_S5_N)

Channel 4 (blue/bottom) – Pin #10 (S5_LED_DRV) with external 5kΩ pull up resistor

3. S5 LED functionality, PM_SLP_SUS_N is HIGH, goes LOW 100ms after S3_LED_DRV goes LOW



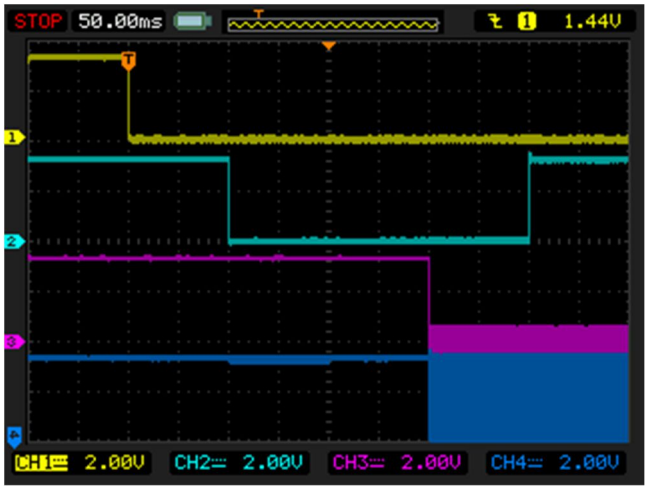
Channel 1 (yellow/top) – Pin #2 (PM_SLP_S3_N)

Channel 2 (light blue/2nd line) – Pin #3 (PM_SLP_S4_N)

Channel 3 (magenta/3rd line) – Pin #5 (PM_SLP_SUS_N)

Channel 4 (blue/bottom) – Pin #12 (DSW_LED_DRV) with external 5kΩ pull up resistor

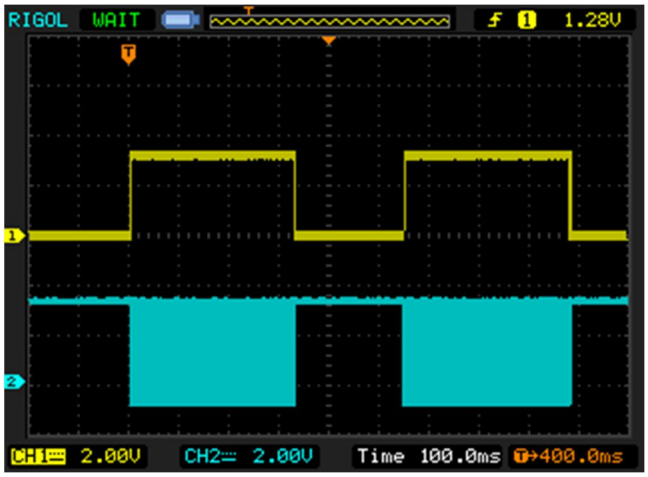
4. DSW LED functionality



Channel 1 (yellow/top) – Pin #9 (PM_SLP_M_N)

Channel 2 (light blue/2nd line) – Pin #6 (ME_LED_DRV) with external 5kΩ pull up resistor

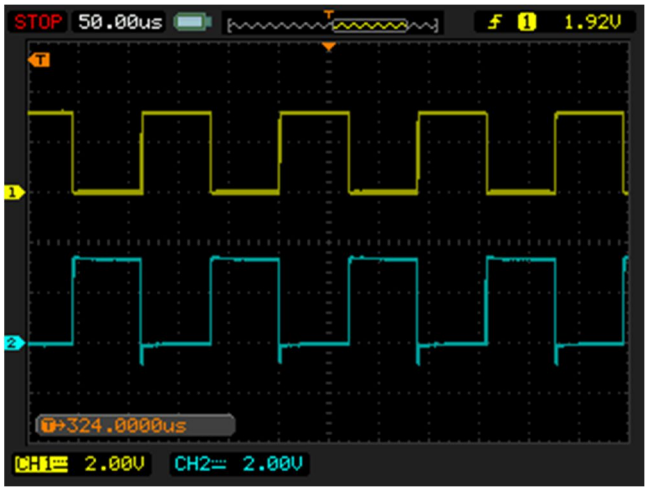
5. DSW LED functionality



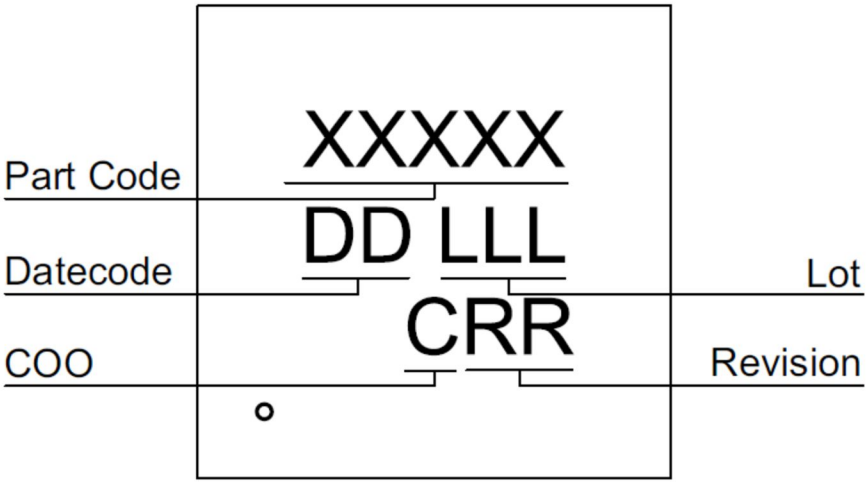
Channel 1 (yellow/top) – Pin #12 (DSW_LED_DRV) with external 5kΩ pull up resistor

Channel 2 (light blue/2nd line) – Pin #11 (S4_LED_DRV) with external 5kΩ pull up resistor

6. PWM difference in one chip side to prevent overcurrent



Package Top Marking



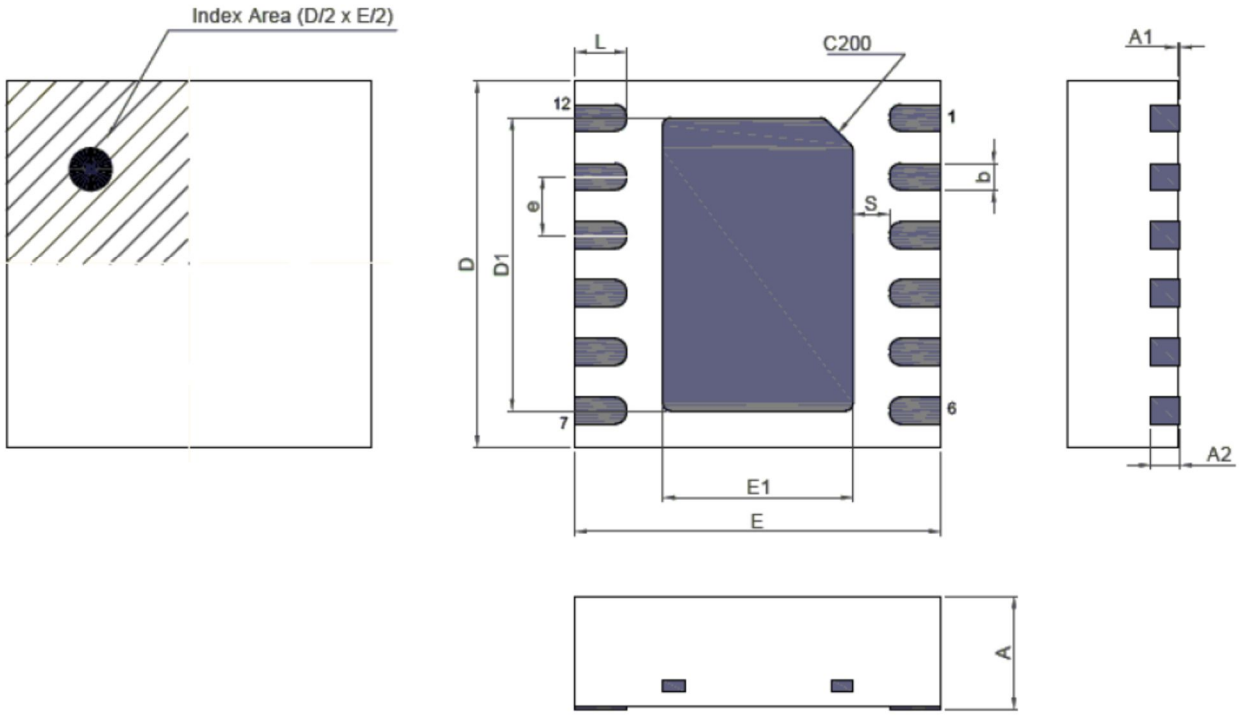
XXXXX – Part ID Field: identifies the specific device configuration
DD – Date Code Field: Coded date of manufacture
LLL – Lot Code: Designates Lot #
C – COO: Specifies Country of Origin
RR – Revision Code: Device Revision

Datasheet Revision	Programming Code Number	Locked Status	Part Code	Revision	Date
1.04	007	U	4082V	AG	02/25/2022

The IC security bit is locked/set for code security for production unless otherwise specified. Revision number is not changed for bit locking.

Package Drawing and Dimensions

12 Lead TDFN Package
JEDEC MO-252, Variation 2525E



Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.70	0.75	0.80	D1	1.95	2.00	2.05
A1	0.005	-	0.060	E1	1.25	1.30	1.35
A2	0.15	0.20	0.25	e	0.40 BSC		
b	0.13	0.18	0.23	L	0.30	0.35	0.40
D	2.45	2.50	2.55	S	0.18	-	-
E	2.45	2.50	2.55				

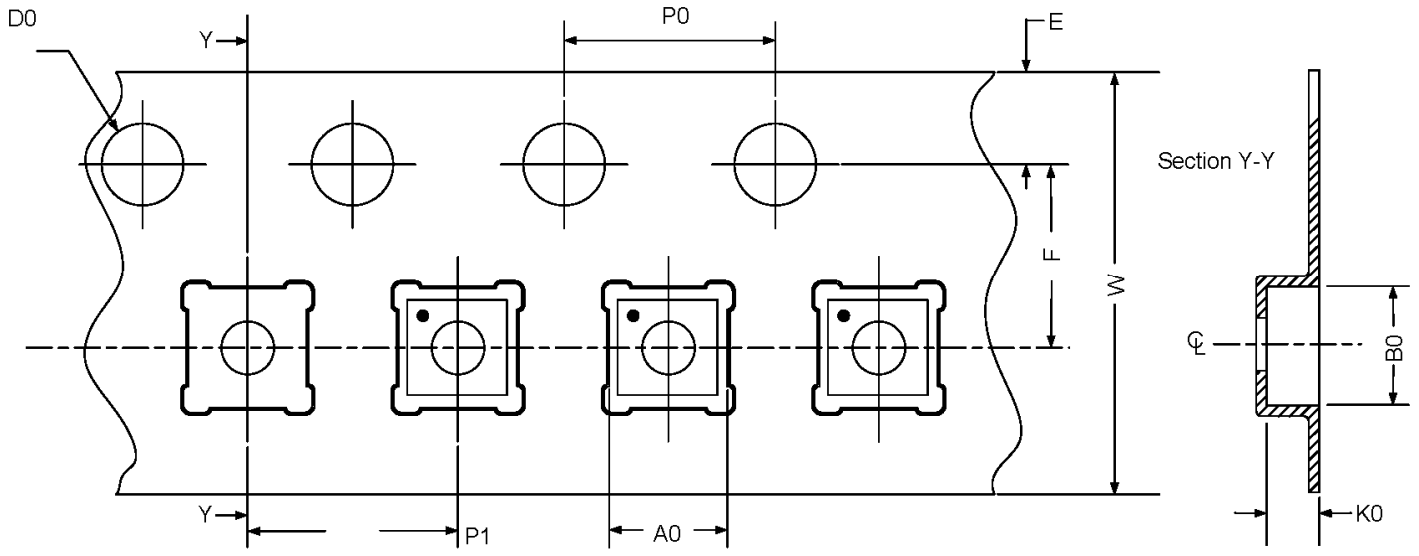
Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size (mm)	Max Units		Reel & Hub Size (mm)	Trailer A		Leader B		Pocket (mm)	
			per reel	per box		Pockets	Length (mm)	Pockets	Length (mm)	Width	Pitch
TDFN 12L 2.5x2.5mm 0.4P Green	12	2.5x2.5x0.75	3000	3000	178/60	42	168	42	168	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length (mm)	Pocket BTM Width (mm)	Pocket Depth (mm)	Index Hole Pitch (mm)	Pocket Pitch (mm)	Index Hole Diameter (mm)	Index Hole to Tape Edge (mm)	Index Hole to Pocket Center (mm)	Tape Width (mm)
	A0	B0	K0	P0	P1	D0	E	F	W
TDFN 12L 2.5x2.5mm 0.4P Green	2.75	2.75	1.05	4	4	1.55	1.75	3.5	8

Refer to EIA-481 Specifications



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 4.6875 mm^3 (nominal). More information can be found at www.jedec.org.

Datasheet Revision History

Date	Version	Change
06/04/2012	0.10	New design
06/12/2012	0.20	Added PWM output
06/12/2012	0.21	Corrected Truth Table
06/26/2012	0.22	Changed ME_LED truth table
07/10/2012	0.23	Changed PIN names
07/30/2012	0.24	Corrected LUT4.0 truth table
08/17/2012	0.25	Updated Device Revision Table
08/30/2012	0.26	Added Timing Diagrams, Typical Application Circuit
09/21/2012	1.00	Production Release
12/11/2012	1.01	Updated Device Revision Table
12/22/2021	1.02	Changed to full VDD range for Rev B chip
01/20/2022	1.03	Added Vih parameter
02/25/2022	1.04	Updated Company name and logo

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