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MDT1010D1IH-MIPI	1024 x 600	MIPI Interface	TFT Module

Specification

Version: 1	Date: 27/08/2021

Revision

1	26/08/2021	First issue

Display Features	
Display Size	10.10”
Resolution	1024 x 600
Orientation	Landscape
Appearance	RGB
Logic Voltage	1.8V
Interface	MIPI
Brightness	1100 cd/m^2
Touchscreen	---
Module Size	235.00 x 143.00 x 5.05mm
Operating Temperature	-20°C ~ +70°C
Pinout	30 way FFC
Pitch	0.5mm

RoHS compliant

Box Quantity	Weight / Display
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* - For full design functionality, please use this specification in conjunction with the EK79007AD3 + EK73217BCGA specification. (Provided Separately)

Display Accessories

Part Number	Description
MPBV7	30-way FFC 0.5mm, crimp-wire conect. SHDR-30V-S-B

Optional Variants

Appearances	Voltage

Summary

TFT 10.1" is a color active matrix thin film transistor (TFT) liquid crystal display without polarizer. This model is composed of amorphous silicon TFT as a switching device.
This TFT LCD has a 10.1" wide (16:9) diagonally measured active display area with WVGA (1024 horizontal by 600 vertical pixel) resolution. Each pixel is divided into Red, Green, Blue dots which are arranged in vertical stripes.

General Specifications

- Size: 10.1 inch
- Dot Matrix: 1024 RGB X 600 dots
- Module dimension: 235(W) x143(H) x 5.05(D) mm
- Active area: 222.72 (H) x 125.28(V) mm
- Pixel pitch: 0.2175(W) x 0.2088(H) mm
- LCD type: TFT, Normally Black, Transmissive
- TFT Interface: 4-Lanes MIPI
- Driver IC: EK79007AD3 + EK73217BCGA or equivalent
- Viewing Angle: 85/85/85/85
- Aspect Ratio: 16:9
- Backlight Type: LED,Normally White
- With /Without TP: Without TP
- Surface: Anti-Glare

*Color tone slight changed by temperature and driving voltage.

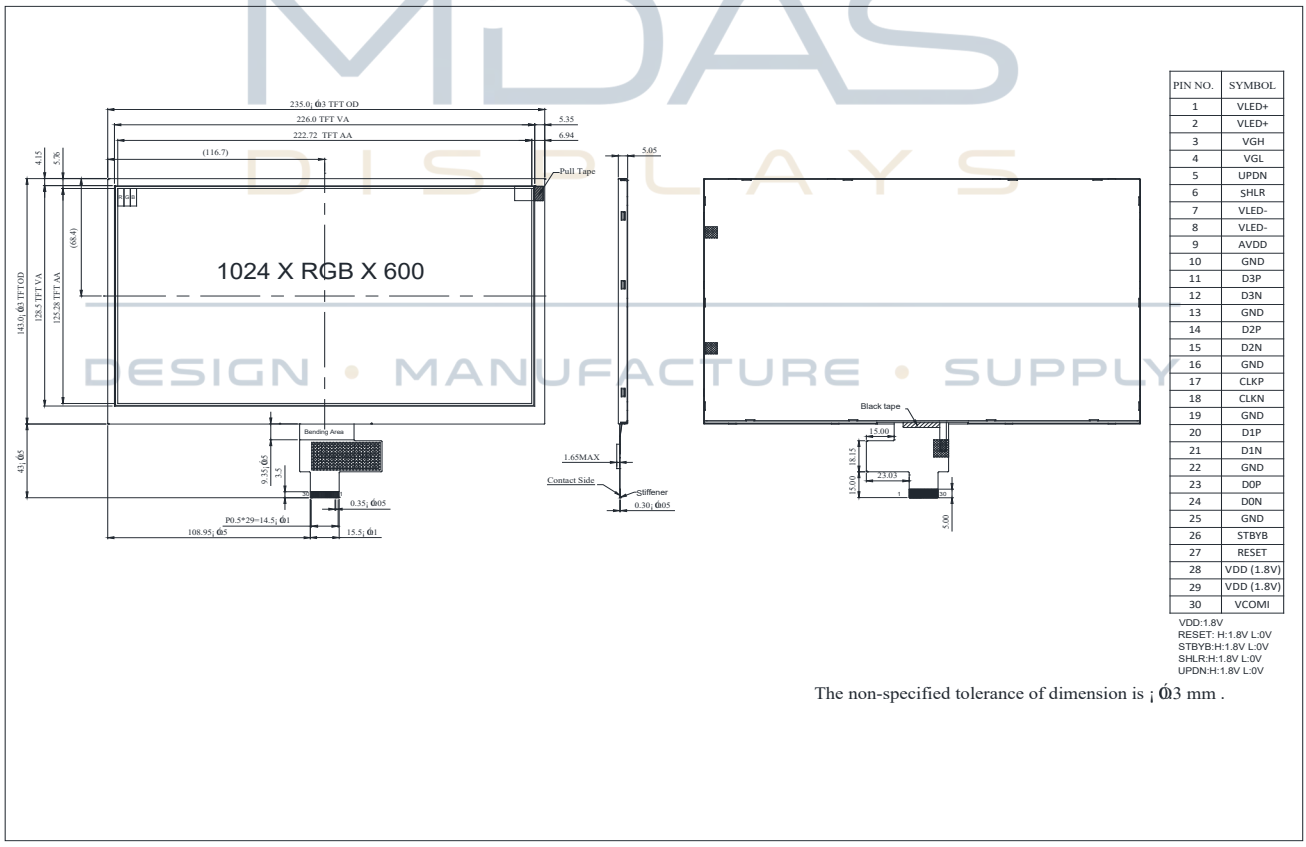
Interface

1. TFT LCD MODULE

Pin No.	Symbol	Description
1	VLED+	LED Anode
2	VLED+	LED Anode
3	VGH	Positive power for TFT
4	VGL	Negative power for TFT
5	UPDN	Gate up or down scan control. UPDN = ”L”, STV2 output vertical start pulse and UD pin output logical “L” to Gate driver. (default) UPDN = ”H”, STV1 output vertical start pulse and UD pin output logical “H” to Gate driver
6	SHLR	Source right or left sequence control. SHLR = ”L“, shift left: last data = S1←S2←S3…….←S1536 = first data. SHLR = ”H“, shift right: first data = S1→S2→S3…….→S1536 = last data.(default)
7	VLED-	LED Cathode
8	VLED-	LED Cathode
9	AVDD	Analog power
10	GND	Digital ground
11	D3P	MIPI data input.
12	D3N	MIPI data input.
13	GND	Digital ground
14	D2P	MIPI data input.
15	D2N	MIPI data input.
16	GND	Digital ground
17	CLKP	MIPI clock input
18	CLKN	MIPI clock input
19	GND	Digital ground
20	D1P	MIPI data input.
21	D1N	MIPI data input.
22	GND	Digital ground
23	D0P	MIPI data input.
24	D0N	MIPI data input.
25	GND	Digital ground
26	STBYB	Standby mode.

		STBYB = ”H“,normal operation(default) STBYB = ”L”, timing controller, source driver will turn off, all output are GND.
27	RESET	Global reset pin. Active Low to enter Reset State. Normally pull high. Connecting with an RC reset circuit for stability.
28	VDD (1.8V)	Digital power
29	VDD (1.8V)	Digital power
30	VCOMI	Common voltage

Contour Drawing



Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	TOP	-20	—	+70	℃
Storage Temperature	TST	-30	—	+80	℃

Note: Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above

1. Temp. ≦60℃, 90% RH MAX. Temp.＞60℃, Absolute humidity shall be less than 90% RH at 60℃

Electrical Characteristics

1. Typical Operation Conditions (At Ta = 25 °C,)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Power Supply Voltage For LCD	VDD	1.71	1.8	1.89	V	Note1
Analog Power Supply Voltage	AVDD	9.89	10.2	10.5	V	-
Gate On Power Supply Voltage	VGH	19.4	20.0	20.6	V	-
Gate Off Power Supply Voltage	VGL	-10.3	-10.0	-9.7	V	-
Common Power Supply Voltage	VCOMI	4.0	4.3	4.6	V	Note2

Note1:VDD setting should match the signals output voltage (refer to Note 3) of customer's system board.

Note 2.Please adjust VCOMI to make the flicker level be minimum.

Note 3:RESET,STBYB,U/D,L/R,SELB

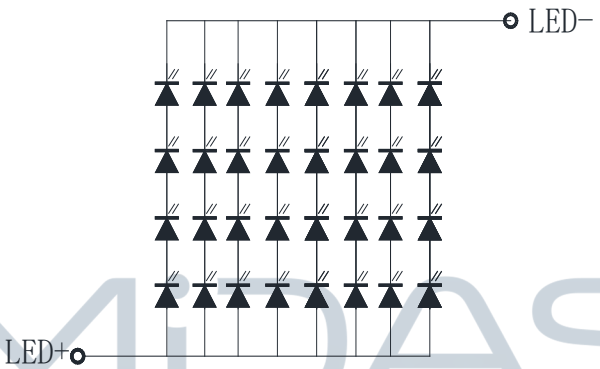
2. Current Consumption

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Current for Driver	I_{VGH}	-	0.5	1.0	mA	VGH =20.0V
	I_{VGL}	-	1.4	2.1	mA	VGL = -10.0V
	I_{VDD}	-	16	24	mA	VDD =1.8V
	I_{AVDD}	-	19	28.5	mA	AVDD =10.2V
	I_{VCOMIN}	-	0	-	mA	VCOMIN=4.3V

3. Backlight Driving Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage of white LED backlight	VL	10.8	12.4	14.0	V	Note 1
Current for LED backlight	IL	-	480	-	mA	
LED life time	-	50,000	-	-	Hr	Note2

Note 1 : There are 1 Groups LED



CIRCUIT DIAGRAM

Note 2 : Ta = 25 ℃
Note 3 : Brightness to be decreased to 50% of the initial value
Note 4 : The single LED lamp case

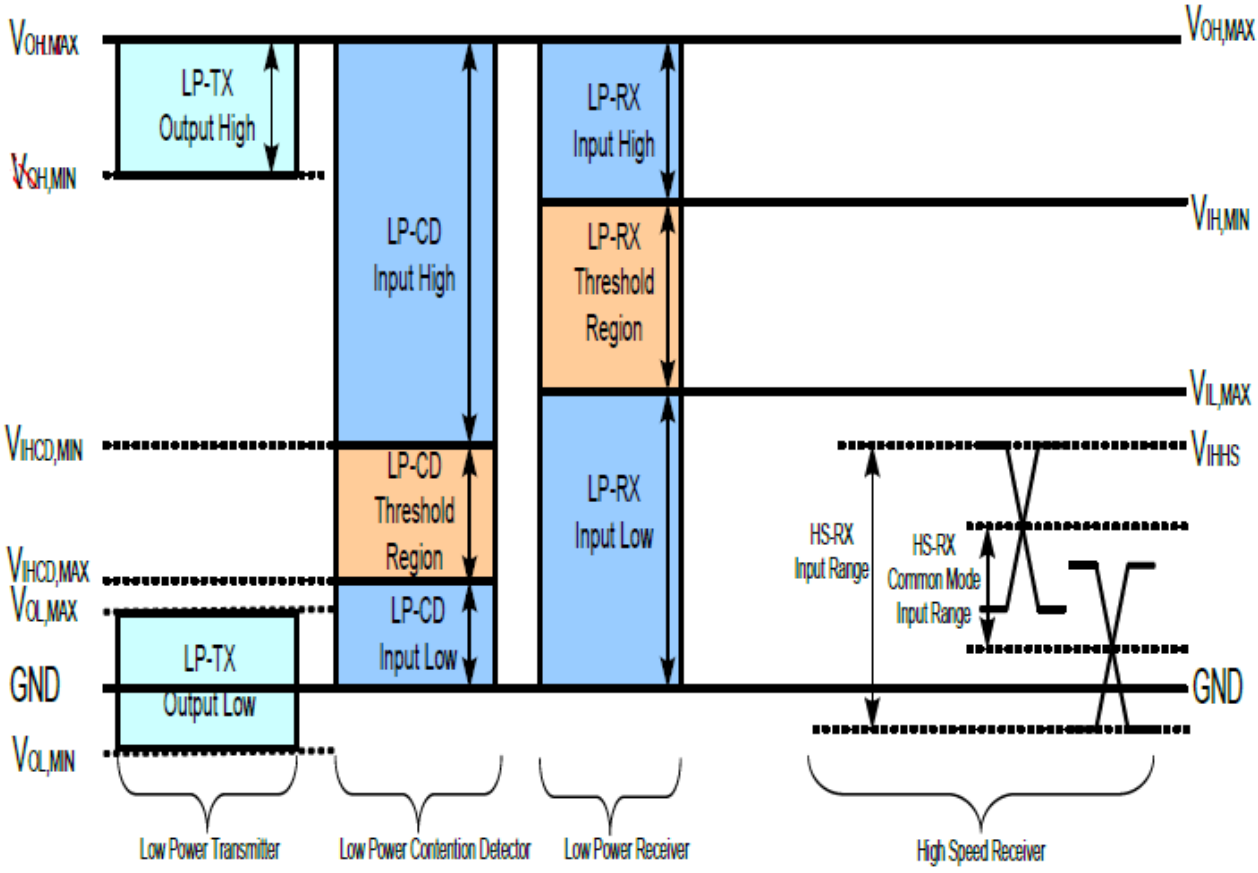
DC Electrical Characteristics

8.1. Parameter	Symbol	Rating			Unit	Condition
		Min	Typ	Max		
Low level input voltage	VIL	0	-	0.3VDD	V	Note 1
High level input voltage	VIH	0.7VDD	-	VDD	V	

Note 1:RESET,STBYB, UPDN, SHLR

2. MIPI Interface DC Characteristic

Parameter	Symbol	Min.	Typ.	Max.	Unit
MIPI Characteristics for High Speed Receiver					
Single-ended input low voltage	V_{ILHS}	-40	-	-	mV
Single-ended input high voltage	V_{IHHS}	-	-	460	mV
Common-mode voltage	V_{CDRXDC}	70	-	330	mV
Differential input impedance	Z_{ID}		100		ohm
HS transmit differential voltage(VOD=VDP-VDN)	$\|V_{OD}\|$	140	200	250	mV
MIPI Characteristics for Low Power Mode					
Pad signal voltage range	V_I	-50	-	1350	mV
Ground shift	V_{GNDSH}	-50	-	50	mV
Logic 0 input threshold	V_{IL}	0	-	550	mV
Logic 1 input threshold	V_{IH}	880	-	1350	mV
Input hysteresis	V_{HYST}	25	-	-	mV
Output low level	V_{OL}	-50	-	50	mV
Output high level	V_{OH}	1.1	1.2	1.3	V
Output impedance of Low Power Transmitter	Z_{OLP}	80	100	125	ohm
Logic 0 contention threshold	$V_{ILCD,MAX}$	-	-	200	mV
Logic 0 contention threshold	$V_{IHCD,MIN}$	450	-	-	mV

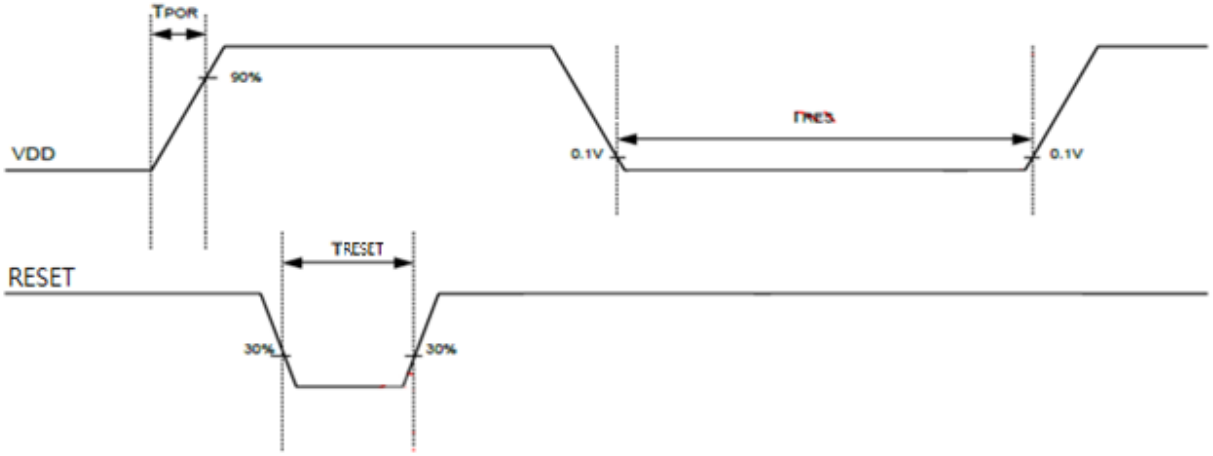


AC Electrical Characteristics

1. Basic AC Characteristic

VDD/RESET AC characteristic

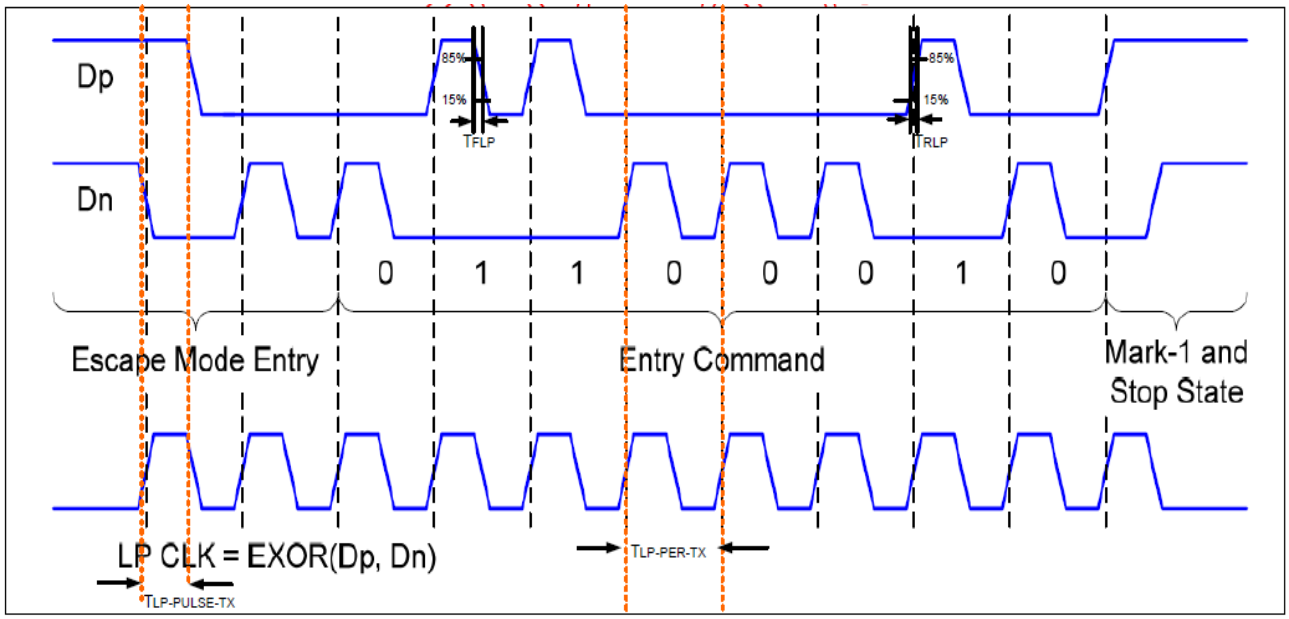
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
VDD power slew rate	T_{POR}	-	-	20	ms	From 0 to 90% VDD
RESETactive pulse width	T_{RESET}	1	-	-	ms	VDD=1.8V
VDD resettle time	T_{RES}	1	-	-	s	



2. MIPI AC Characteristic

1.Transmitter AC Specification

Parameter		Symbol	Min	Typ	Max	Units	Notes
15%~85% rising time and falling time		T_{RLP} /T_{FLP}	-	-	25	ns	-
30%~85% rising time and falling time		T_{REOT}	-	-	35	ns	-
Pulse width of LP exclusive-OR clock	First LP EXOR clock pulse after STOP state or Last pulse before stop state	$T_{LP-PULSE-TX}$	40	-	-	ns	-
	All other pulses		20	-	-	ns	-
Period of the LP EXOR clock		$T_{LP-PER-TX}$	90	-	-	mV/ns	-
Slew Rate @C_{LOAD} =0pF		δ V/δ t_{SR}	30	-	500	mV/ns	-
Slew Rate @C_{LOAD} =5pF			30	-	200	mV/ns	-
Slew Rate @C_{LOAD} =20pF			30	-	150	mV/ns	-
Slew Rate @C_{LOAD} =70pF			30	-	100	mV/ns	-
Load Capacitance		T_{RLP}	-	-	70	pF	-

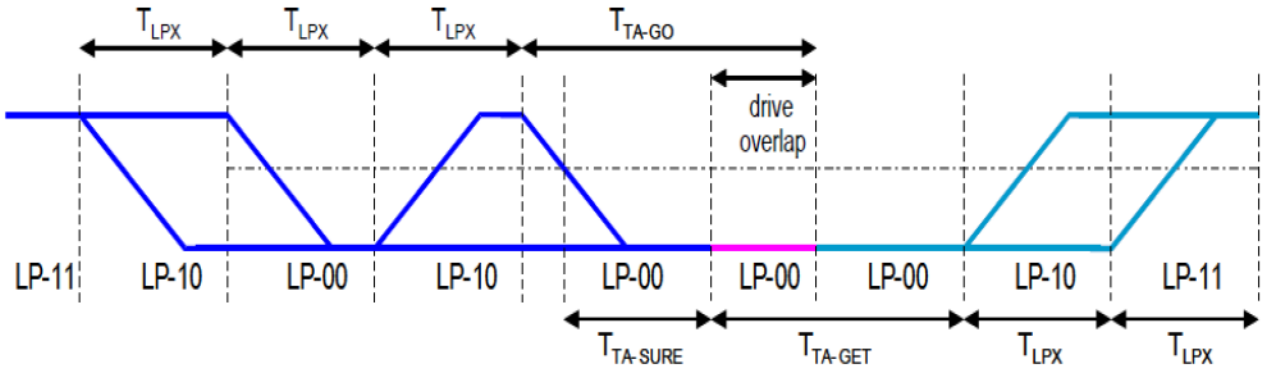


DP:MIPI_D1P / MIPI_D0P
DN: MIPI_D1N / MIPI_D0N

Turnaround Procedure

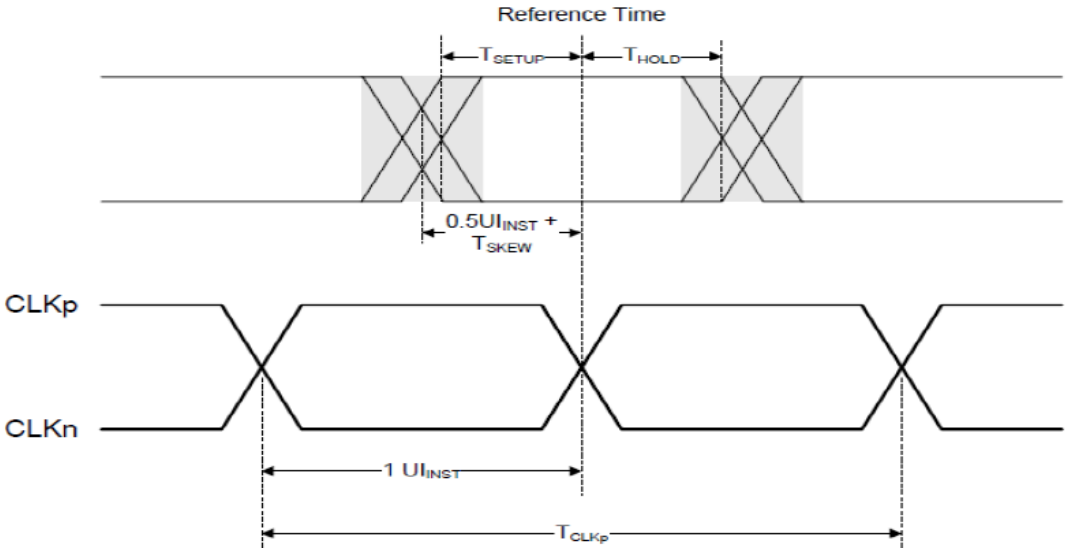
Turnaround Procedure Operation Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
Length of any Low-Power state period: Master side	T_{LPX}	50	-	75	ns
Length of any Low-Power state period: Slave side	T_{LPX}	50	55.56	58.34	ns
Ratio of T_{LPX}(Master)/ T_{LPX} (Slave) between Master and Slave side	Ratio T_{LPX}	2/3	-	3/2	
Time-out before new TX side start driving	$T_{TA-Sure}$	T_{LPX}	-	$2T_{LPX}$	ns
Time to drive LP-00 by new TX	T_{TA-GET}	-	$5T_{LPX}$	-	ns
Time to drive LP-00 after Turnaround Request	T_{TA-GO}	-	$4T_{LPX}$	-	ns



3.High speed transmission

Parameter	Symbol	Min	Typ	Max	Units
UI instantaneous	UI_{INST}	2	-	12.5	ns
Data to Clock Skew(measured at transmitter)	$T_{SKEW(TX)}$	-0.15	-	0.15	UI_{INST}
Data to Clock Setup time(measured at receiver)	$T_{SETUP(RX)}$	0.15	-	-	UI_{INST}
Data to Clock Hold time(measured at receiver)	$T_{HOLD(RX)}$	0.15	-	-	UI_{INST}
20%~80% rise time and fall time	T_R, T_F	150	-	-	ps
		-	-	0.3	UI_{INST}

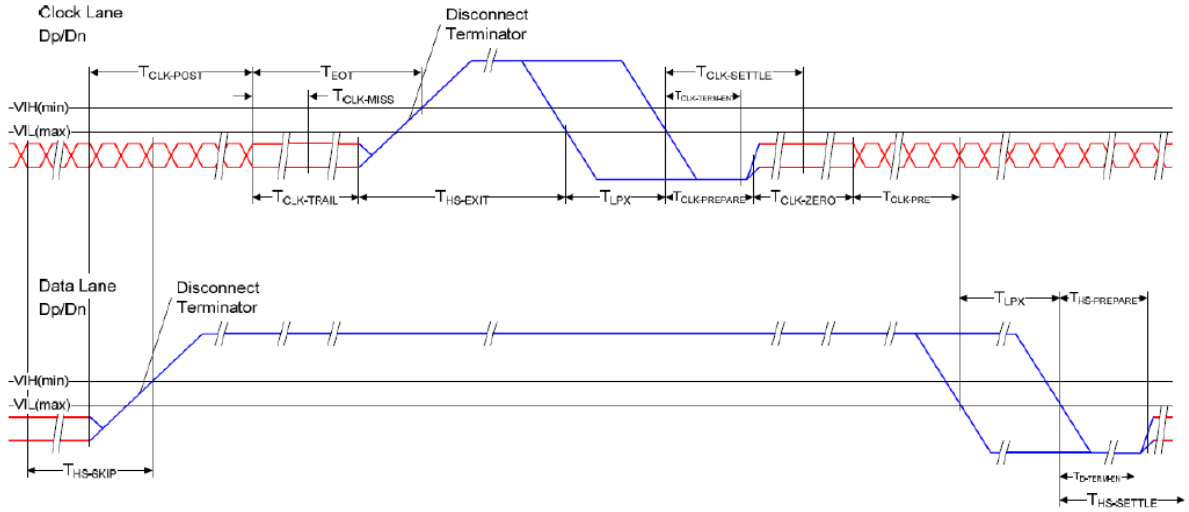


CLKP: MIPI_CLKP
CLKN: MIPI_CLKN

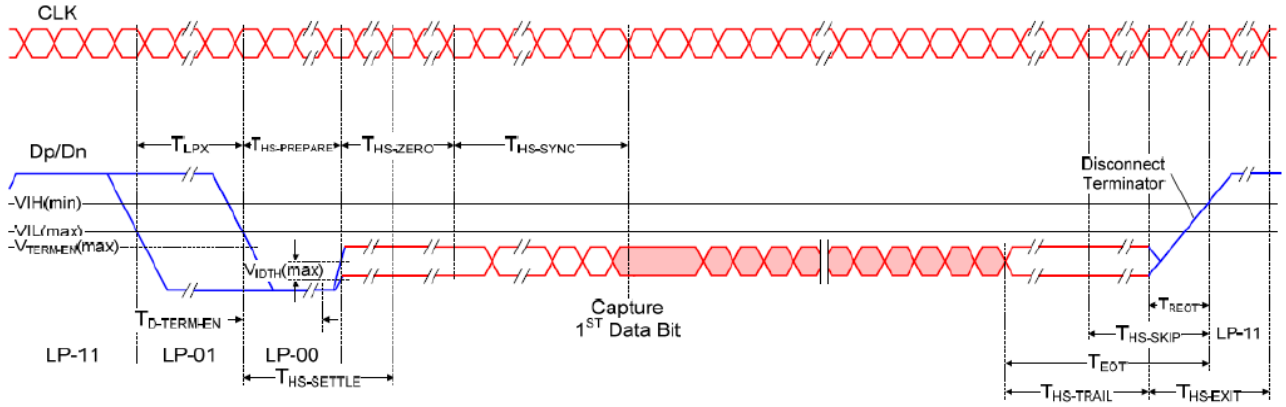
4.High Speed Clock Transmission

DP:MIPI_D1P / MIPI_D0P
DN: MIPI_D1N / MIPI_D0N
CLKP: MIPI_CLKP
CLKN: MIPI_CLKN

Parameter	Symbol	Min	Typ	Max	Units
Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	TCLK-POST	60+52UI	-	-	ns
Detection time that the clock has stopped toggling	TCLK-MISS	-	-	60	ns
Time to drive LP-00 to prepare for HS clock transmission	TCLK-PREPARE	38	-	95	ns
Minimum lead HS-0 drive period before starting clock	TCLK-PREPARE + TCLK-ZERO	300	-	-	ns
Time to enable Clock Lane receiver line termination measured from when Dn cross VIL,MAX	THS-TERM-EN	-	-	38	ns
Minimum time that the HS clock must be prior to any associated data lane beginning the transmission from LP to HS mode	TCLK-PRE	8	-	-	UI
Time to drive HS differential state after last payload clock bit of a HS transmission burst	TCLK-TRAIL	60	-	-	ns



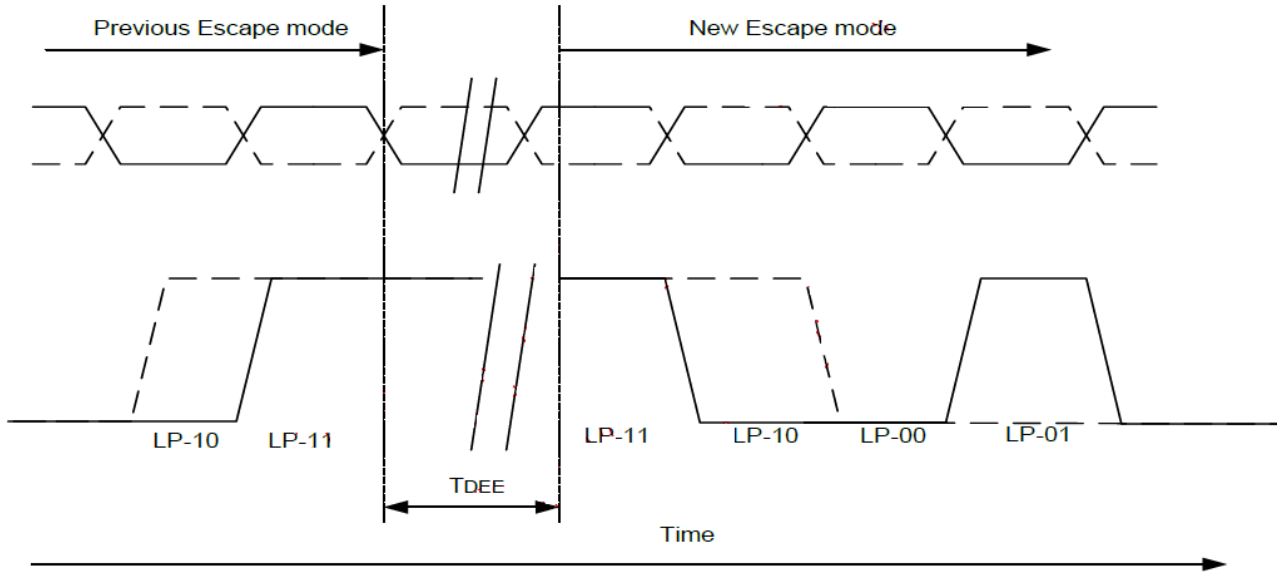
5.High Speed Data Transmission in Bursts



6.LP11 timing request between data transformation

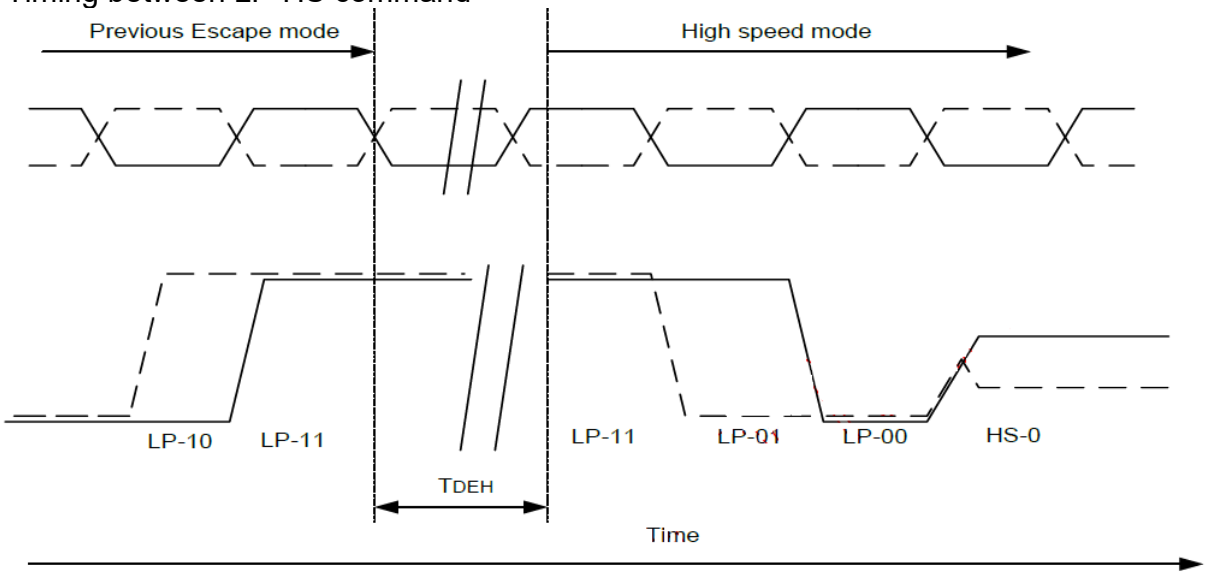
When Clock lane of DSI TX chip always keeps High speed mode, then Clock lane never go back to Low power mode. If Date lane of TX chip needs to transmit the next new data transmission or sequence, after the end of Low power mode or High speed mode or BTA. Then TX chip needs to keep LP-11 stop state before the next new data transmission, no matter in Low power mode or High speed mode or BTA. The LP-11 minimum timing is required for RX chip in the following 9 conditions, include of LP—LP, LP—HS, HS— LP, HS—HS, BTA— BTA, LP— BTA, BTA— LP, HS— BTA, and BTA— HS.This rule is suitable for short or long packet between TX and RX data transmission.

(1) Timing between LP-LP command



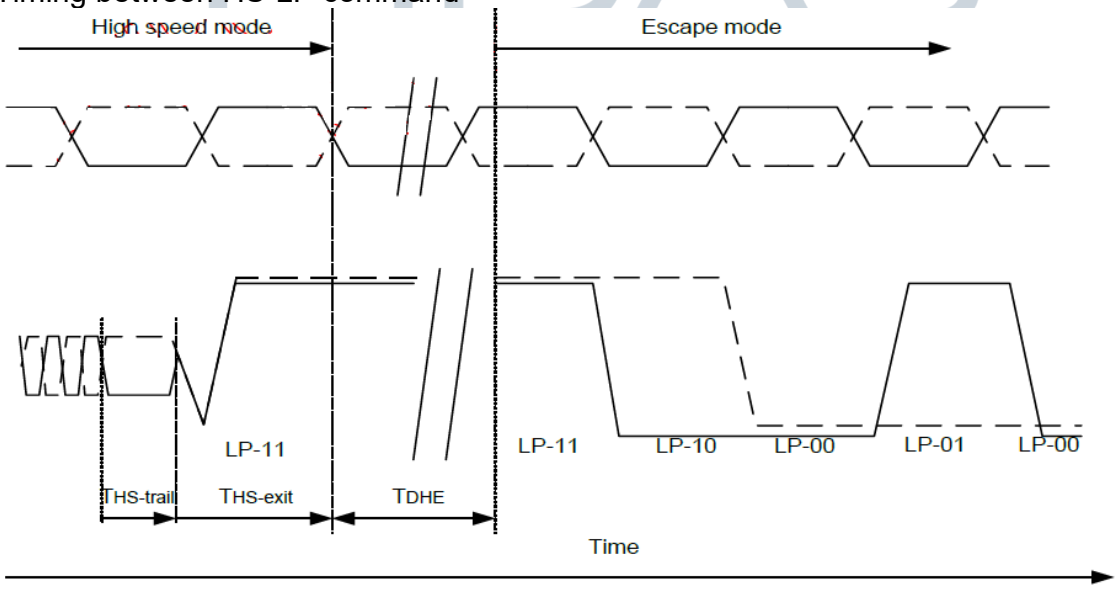
Parameter	Symbol	Min	Typ	Max	Unit
LP-11 delay to start of the new Escape Mode Entry	TDEE	150	-	-	ns

(2) Timing between LP-HS command



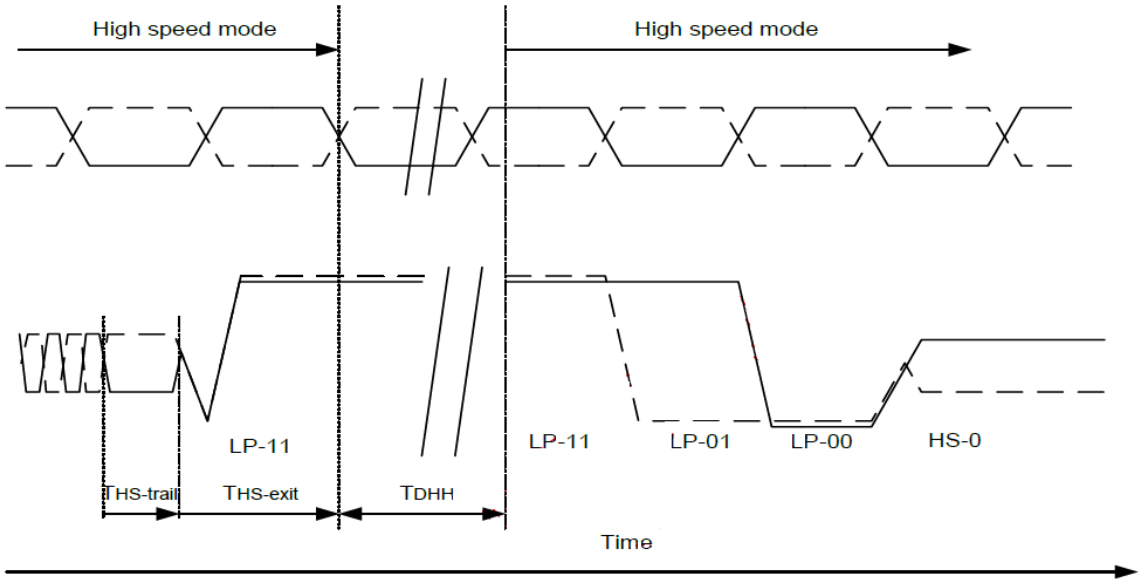
Parameter	Symbol	Min	Typ	Max	Unit
LP-11 delay to start of the Entering High Speed Mode	TDEH	Max(150,32UI)	-	-	ns

(3) Timing between HS-LP command



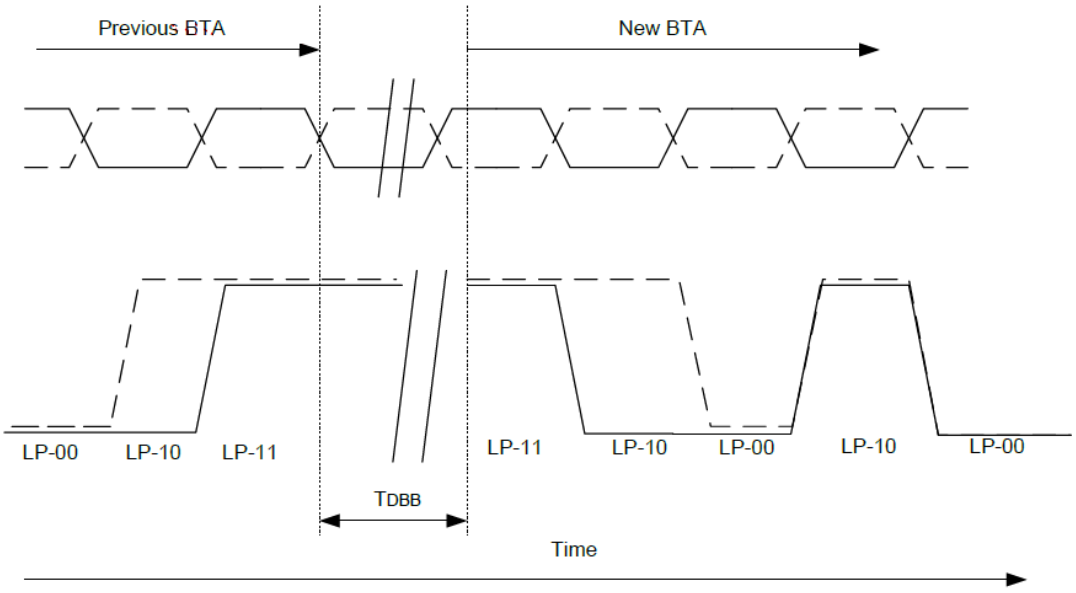
Parameter	Symbol	Min	Typ	Max	Unit
LP-11 delay to start of the Escape Mode Entry	TDHE	Max(150,32UI)	-	-	ns

(4) Timing between HS-HS command



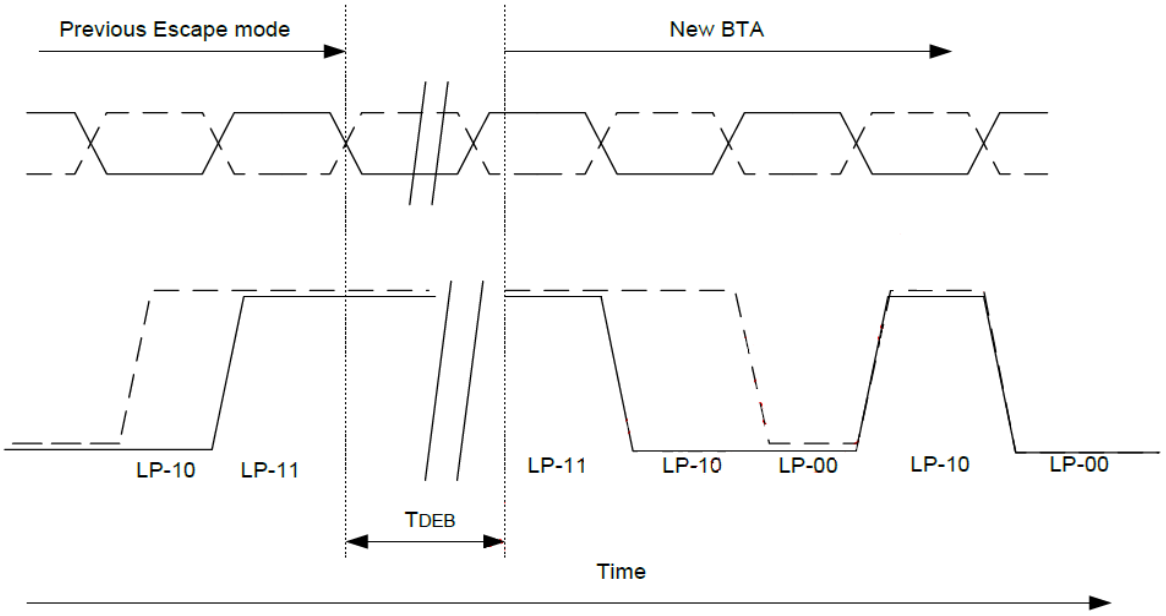
Parameter	Symbol	Min	Typ	Max	Unit
LP-11 delay to start of the Entering High Speed Mode	TDHH	Max(150,32UI)	-	-	ns

(5) Timing between BTA-BTA command



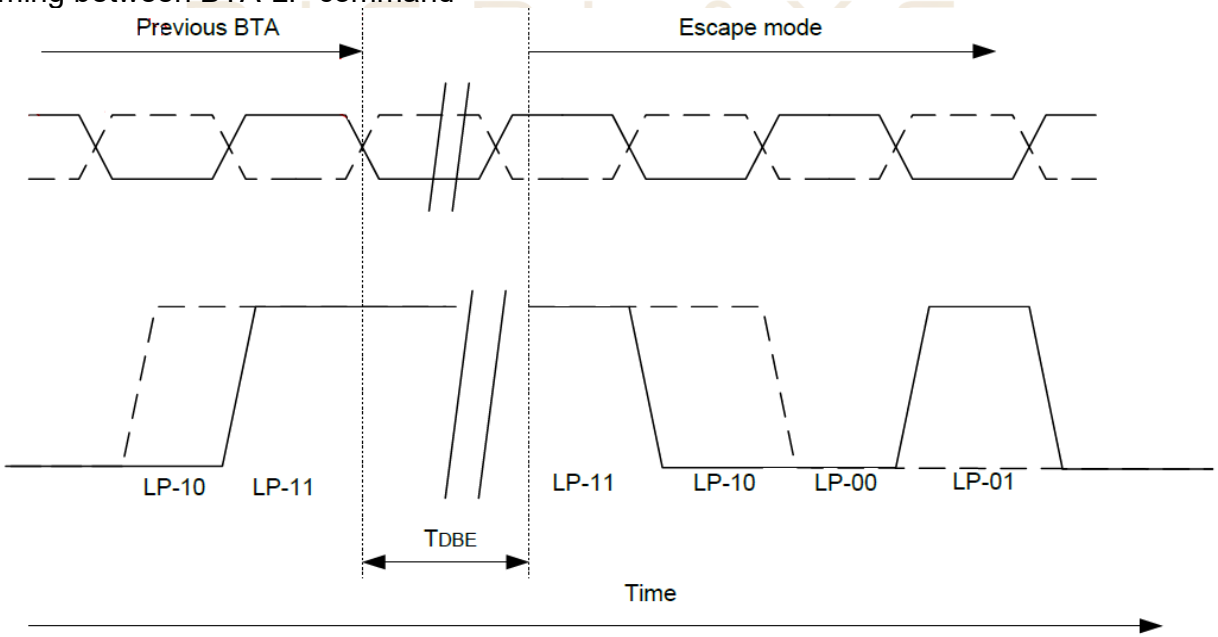
Parameter	Symbol	Min	Typ	Max	Unit
LP-11 delay to start of the new BTA	TDBB	150	-	-	ns

(6) Timing between LP-BTA command



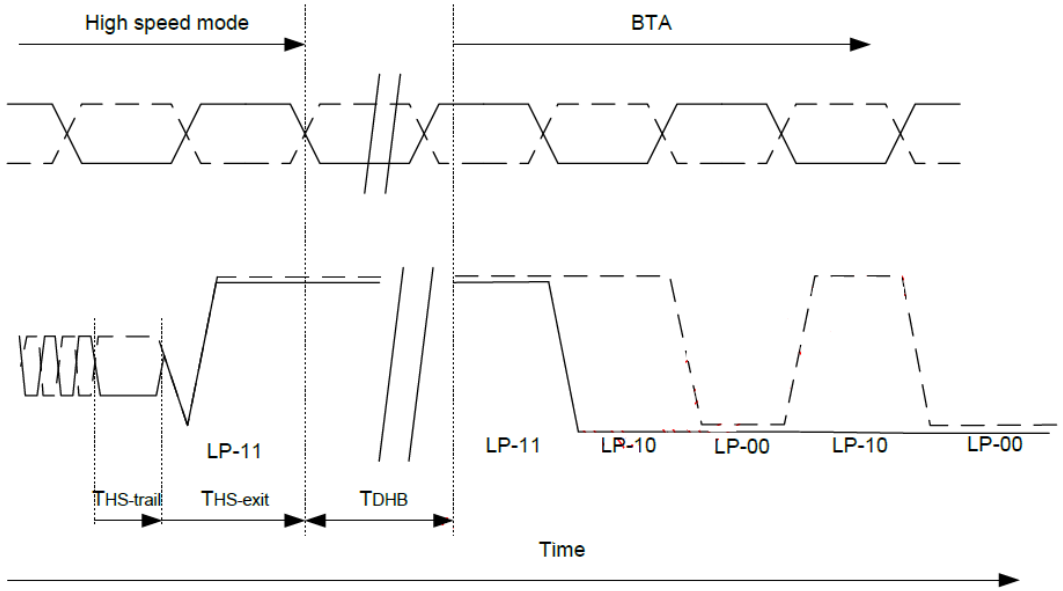
Parameter	Symbol	Min	Typ	Max	Unit
LP-11 delay to start of the new BTA	TDEB	150	-	-	ns

(7) Timing between BTA-LP command



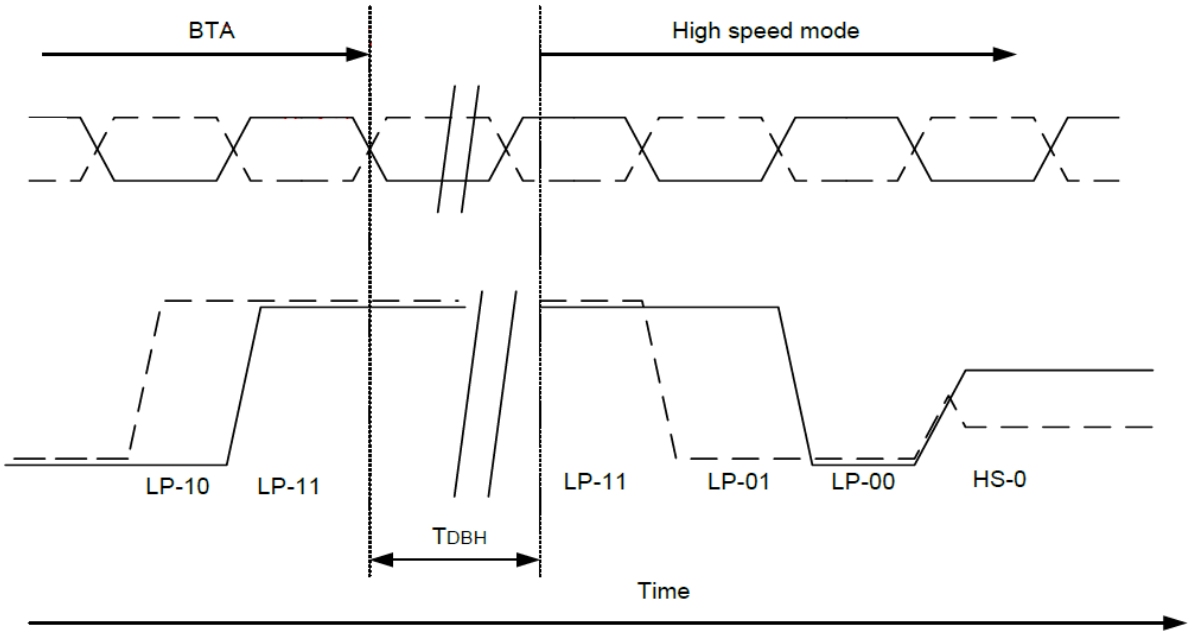
Parameter	Symbol	Min	Typ	Max	Unit
LP-11 delay to start of the Escape Mode Entry	TDBE	150	-	-	ns

(8) Timing between HS-BTA command



Parameter	Symbol	Min	Typ	Max	Unit
LP-11 delay to start of the BTA	T_{DHB}	Max(150,32UI)	-	-	ns

(9) Timing between BTA-HP command



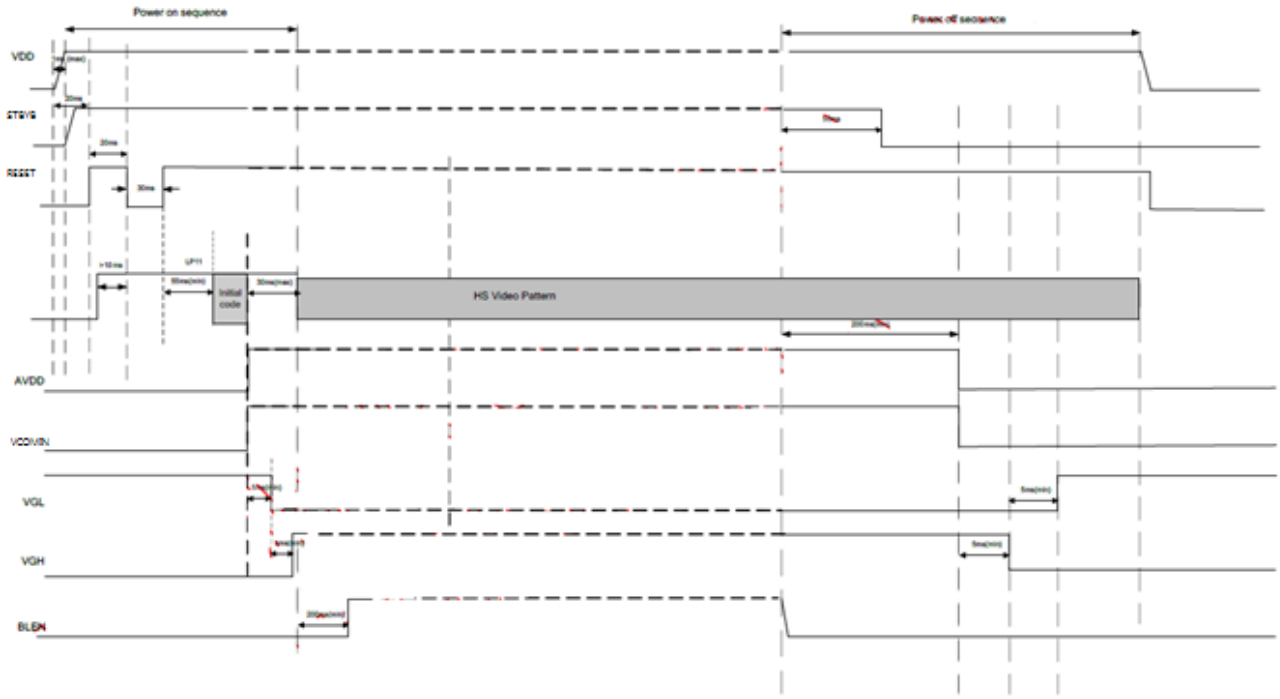
Parameter	Symbol	Min	Typ	Max	Unit
LP-11 delay to start of the Entering High Speed Mode	T_{DBH}	Max(150,32UI)	-	-	ns

Function Description

1. Power On/Off Sequence

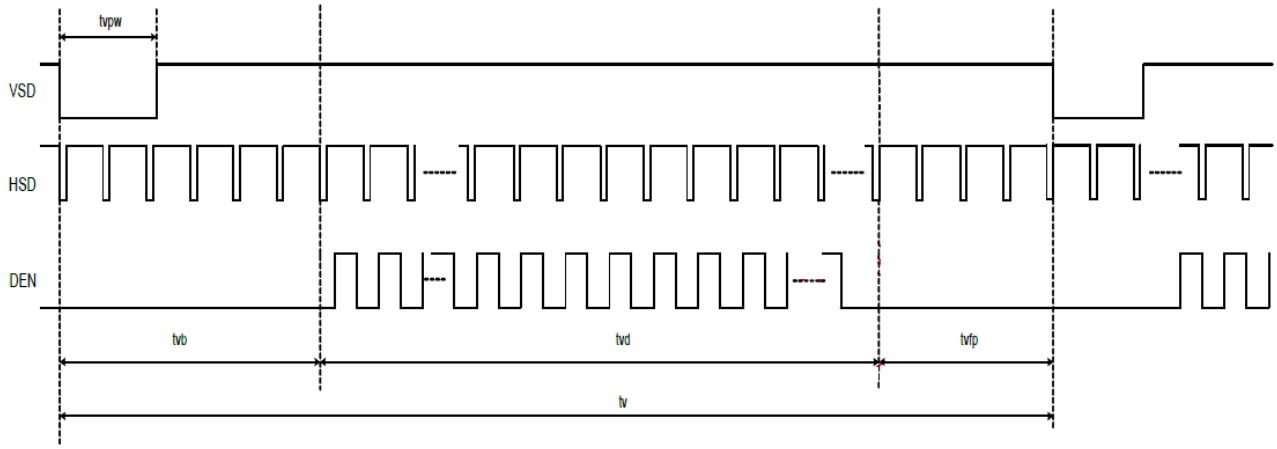
In order to prevent IC from power on reset fail, the rising time (TPOR) of the digital power supply VDD should be maintained within the given specifications. Refer to “AC Characteristics” for more detail on timing.

Power On/Off Sequence



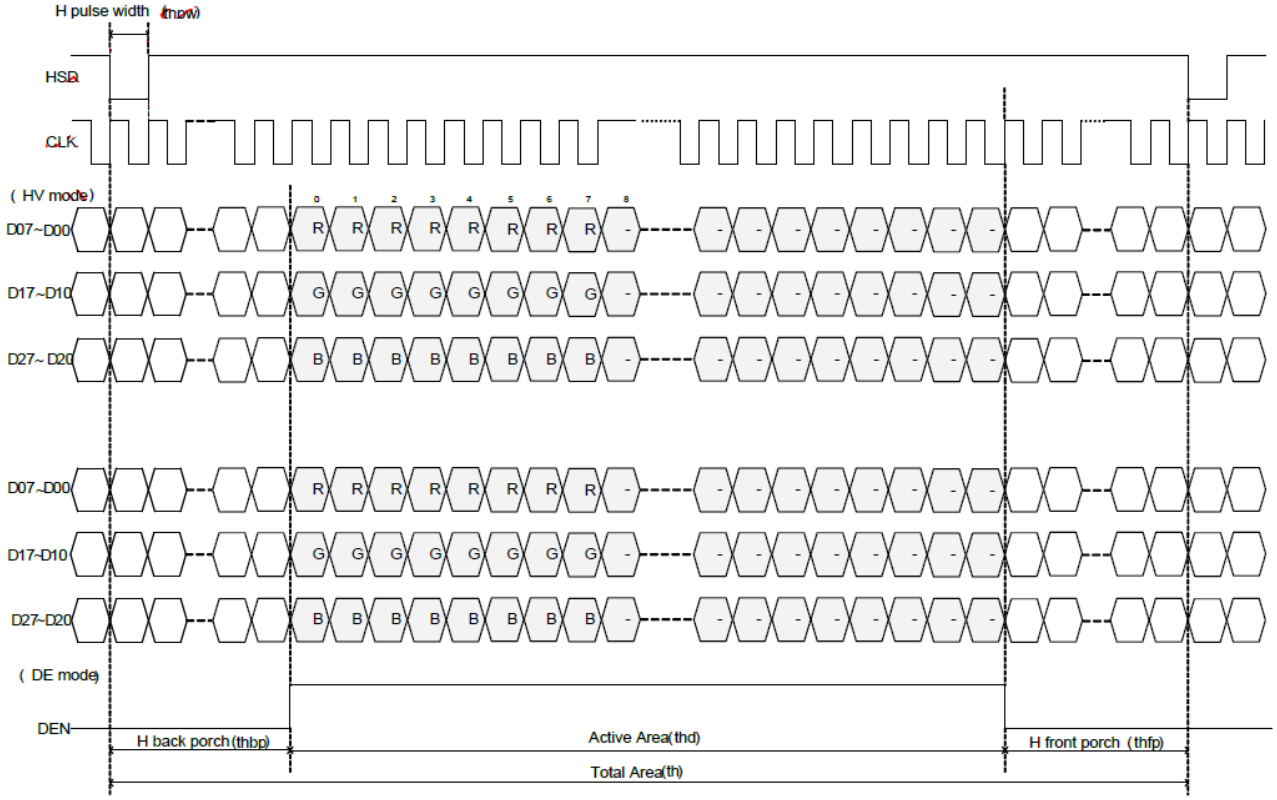
Note: CLK and Data Lanes should keep in LP11(stop state) before RESET.

2. Vertical input timing



Vertical input timing

3. Horizontal input timing



Horizontal input timing

4. Input Timing Table (2Lane)
For 1024RGB x 600 panel

DE mode

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
DCLK frequency @Frame rate=60hz	fclk	40.8	51.2		Mhz
Horizontal display area	thd		1024		DCLK
HSYNC period time	th	1114	1344		DCLK
HSYNC blanking	thb+thfp	90	320		DCLK
Vertical display area	Tvd		600		H
VSYNC period time	Tv	610	635		H
VSYNC blanking	Tvb+Tvfp	10	35		H

HV mode
Horizontal input timing

Parameter		Symbol	Value			Unit
Horizontal display area		thd	1024			DCLK
DCLK frequency@ Frame rate=60hz		fclk	Min.	Typ.	Max.	
			44.9	51.2		Mhz
1 Horizontal Line		th	1200	1344		DCLK
HSYNC pulse width	Min.	thpw	1			
	Typ.		70			
	Max.		140			
HSYNC blanking		thb	160	160		
HSYNC front porch		thfp	16	160		

HV mode
Vertical input timing

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Vertical display area	tvd	600			H
VSYNC period time	tv	624	635		H
VSYNC pulse width	tvpw	1	20		H
VSYNC back porch	tvb	23	23		H
VSYNC front porch	tvfp	1	12		H

MIPI Interface

1. MIPI INTERFACE (MOBILE INDUSTRY PROCESSING INTERFACE)

The Display Serial Interface standard defines protocols between a host processor and peripheral devices that adhere to MIPI Alliance standards for mobile device interfaces. The DSI standard builds on existing standards by adopting pixel formats and command set defined in MIPI Alliance standards.

DSI-compliant peripherals support either of two basic modes of operation: Command Mode and Video Mode. Which mode is used depends on the architecture and capabilities of the peripheral. The mode definitions reflect the primary intended use of DSI for display interconnect, but are not intended to restrict DSI from operating in other applications.

Command Mode refers to operation in which transactions primarily take the form of sending commands and data to a peripheral, such as a display module, that incorporates a display controller. The display controller may include local registers. Systems using Command Mode write to, and read from, the registers. The host processor indirectly controls activity at the peripheral by sending commands, parameters and data to the display controller. The host processor can also read display module status information. Command Mode operation requires a bidirectional interface.

Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High Speed Mode. To reduce complexity and cost, systems that only operate in Video Mode may use a unidirectional data path.

MIPI Lane Configuration:

	MCU (Master) Display Module (Slave)
Clock Lane	Unidirectional Lane • Clock Only • Escape Mode(ULPS Only)
Data Lane0	Bi-directional Lane ● Forward High-Speed ● Bi-directional Escape Mode ● Bi-directional LPDT
Data Lane1	Unidirectional ● Forward High speed

2. Display Serial Interface (DSI)

Video Mode Communication

Video Mode peripherals require pixel data delivered in real time. This section specifies the format and timing of DSI traffic for this type of display module.

Transmission Packet Sequences

DSI supports several formats, or packet sequences, for Video Mode data transmission. The peripheral's timing requirements dictate which format is appropriate. These terms are used throughout the following sections:

 Non-Burst Mode with Sync Pulses — enables the peripheral to accurately reconstruct original video timing, including sync pulse widths.

 Non-Burst Mode with Sync Events — similar to above, but accurate reconstruction of sync pulse widths is not required, so a single Sync Event is substituted.

 Burst mode — RGB pixel packets are time-compressed, leaving more time during a scan line for LP mode(saving power) or for multiplexing other transmissions onto the DSI link.

In the following figures the Blanking or Low-Power Interval (BLLP) is defined as a period during which video packets such as pixel-stream and sync event packets are not actively transmitted to the peripheral. To enable PHY synchronization the host processor should periodically end HS transmission and drive the Data Lanes to the LP state. This transition should take place at least once per frame; shown as LPM in the figures in this section. It is recommended to return to LP state once per scanline during the horizontal blanking time. Regardless of the frequency of BLLP periods, the host processor is responsible for meeting all documented peripheral timing requirements. Note, at lower frequencies BLLP periods will approach, or become, zero.

During the BLLP the DSI Link may do any of the following:

 Remain in Idle Mode with the host processor in LP-11 state and the peripheral in LP-RX.

 Transmit one or more non-video packets from the host processor to the peripheral using Escape Mode.

 Transmit one or more non-video packets from the host processor to the peripheral using HS Mode.

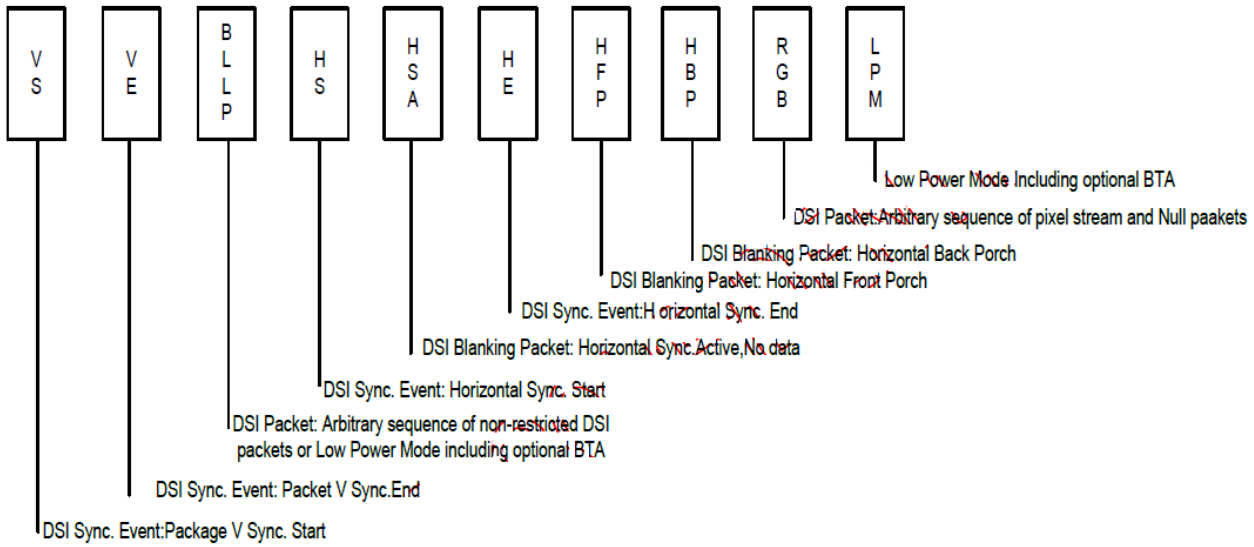
 If the previous processor-to-peripheral transmission ended with BTA, transmit one or more packets from the peripheral to the host processor using Escape Mode.

 Transmit one or more packets from the host processor to a different peripheral using a different Virtual Channel ID.

The sequence of packets within the BLLP or RGB portion of a HS transmission is arbitrary. The host processor may compose any sequence of packets, including iterations, within the limits of the packet format definitions. For all timing cases, the first line of a frame shall start with VS; all other lines shall start with HS. This is also true in the special case when VSA+VBP=0. Note that the position of synchronization packets, such as VS and HS, in time is of utmost importance since this has a direct impact on the visual performance of the display panel.

Normally, RGB pixel data is sent with one full scan line of pixels in a single packet. Individual pixels shall not be split across packets.

Transmission packet components used in the figures in this section are defined in Figure below unless otherwise specified.



DSI Video Mode Interface Timing Legend

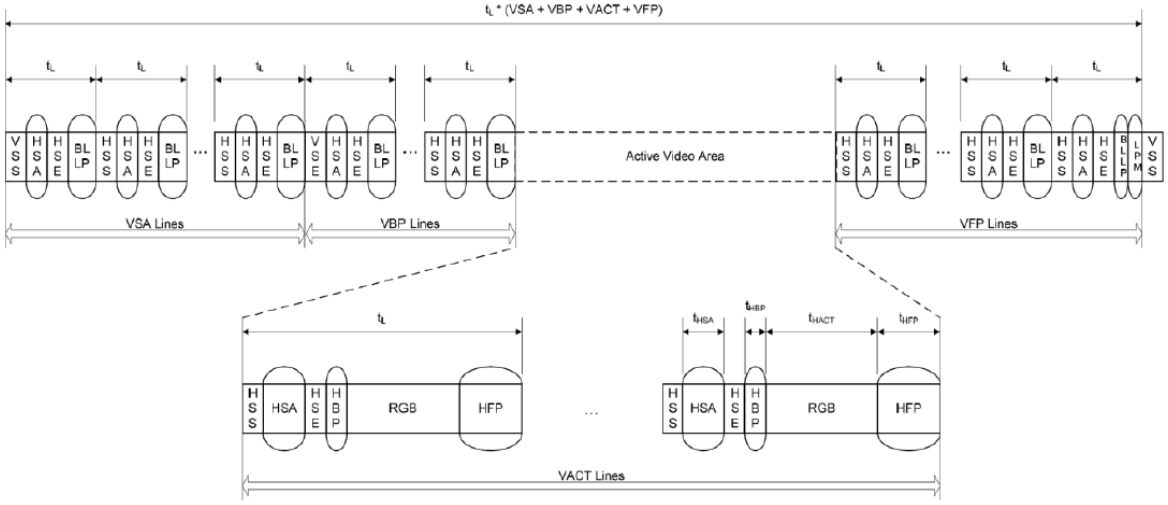
If a peripheral timing specification for HBP or HFP minimum period is zero, the corresponding Blanking Packet may be omitted. If the HBP or HFP maximum period is zero, the corresponding blanking packet shall be omitted.

Clock Requirements

A DSI host processor shall support continuous clock on the Clock Lane for display module that require it, so the host processor needs to keep the HS serial clock running.

Non-Burst Mode with Sync Pulses

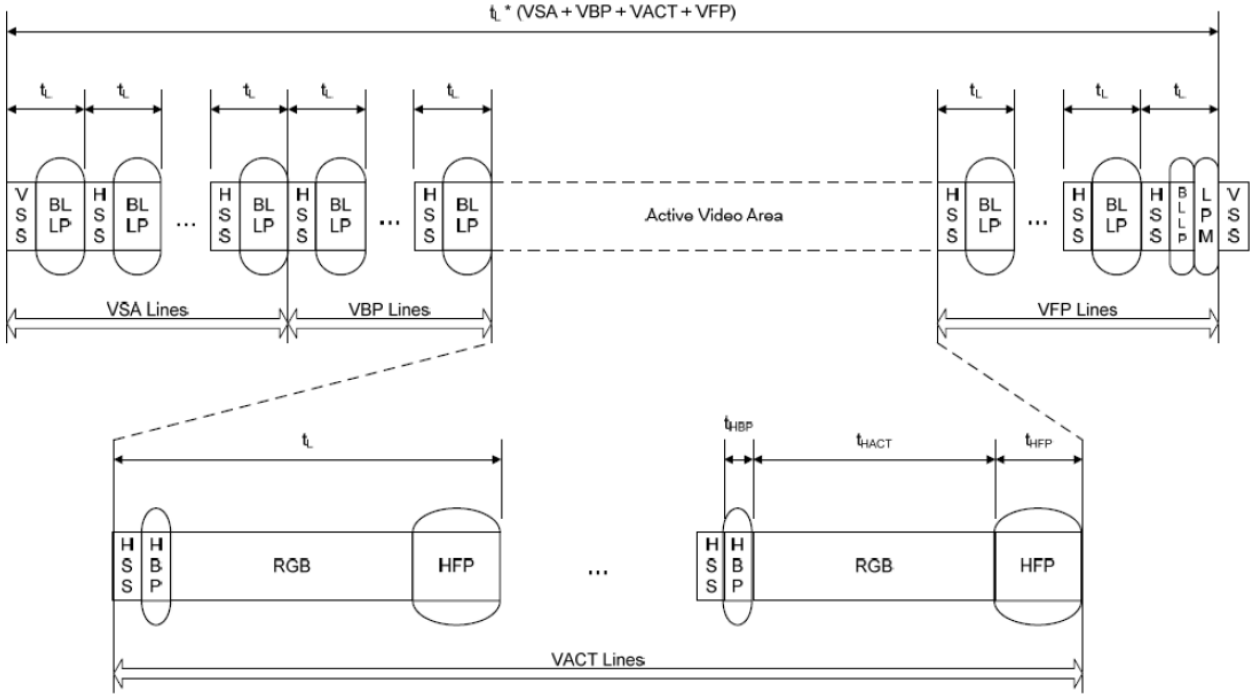
With this format, the goal is to accurately convey DPI-type timing over the DSI serial Link. This includes matching DPI pixel-transmission rates, and widths of timing events like sync pulses. Accordingly, synchronization periods are defined using packets transmitting both start and end of sync pulses. An example of this mode is shown in Figure below.



Normally, periods shown as I (Horizontal Sync Active), HBP (Horizontal Back Porch) and HFP (Horizontal Front Porch) are filled by Blanking Packets, with lengths (including packet overhead) calculated to match the period specified by the peripheral's data sheet. Alternatively, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power

Non-Burst Mode with Sync Events

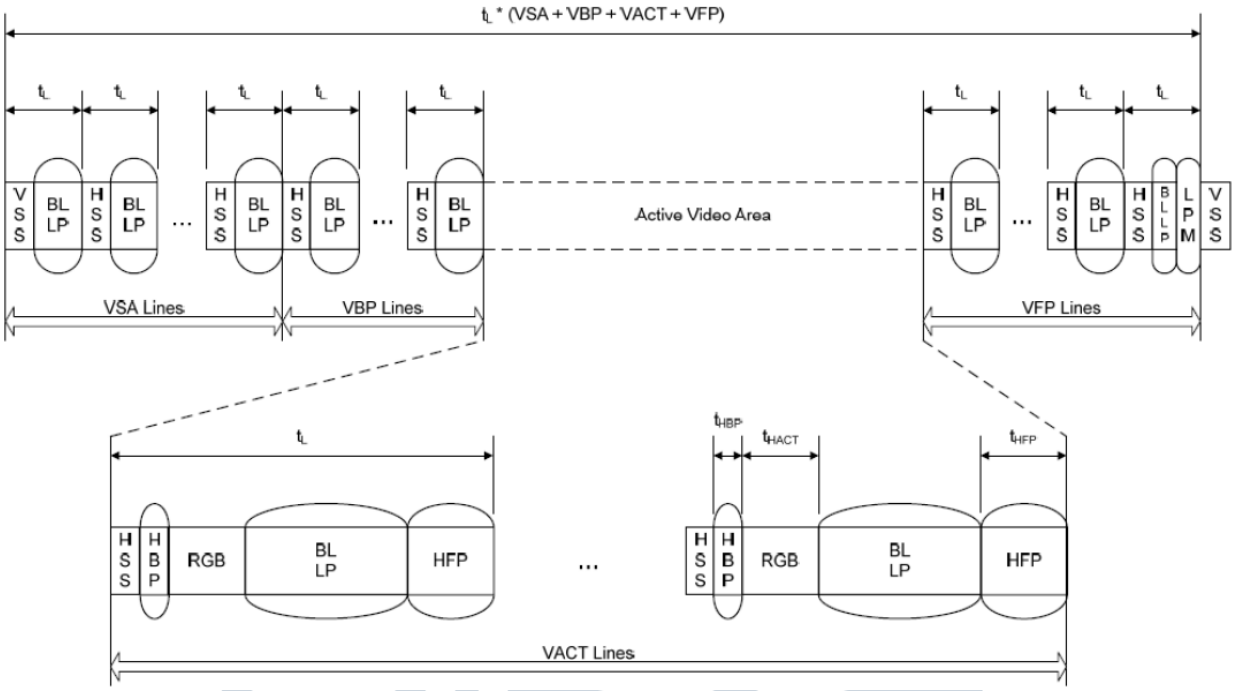
This mode is a simplification of the format described in section “Non-Burst Mode with Sync Pulse” .Only the start of each synchronization pulse is transmitted. The peripheral may regenerate sync pulses as needed from each Sync Event packet received. Pixels are transmitted at the same rate as they would in a corresponding parallel display interface such as DPI-2. An example of this mode is shown in Figure below.



As with the previous Non-Burst Mode, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

Burst Mode

In this mode, blocks of pixel data can be transferred in a shorter time using a time-compressed burst format. This is a good strategy to reduce overall DSI power consumption, as well as enabling larger blocks of time for other data transmissions over the Link in either direction. There may be a line buffer or similar memory on the peripheral to accommodate incoming data at high speed. Following HS pixel data transmission, the bus goes to Low Power Mode, during which it may remain idle, i.e. the host processor remains in LP-11 state, or LP transmission may take place in either direction. If the peripheral takes control of the bus for sending data to the host processor, its transmission time shall be limited to ensure data underflow does not occur from its internal buffer memory to the display device. An example of this mode is shown in Figure below



Similar to the Non-Burst Mode scenario, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

Optical Characteristics

Item		Symbol	Condition.	Min	Typ.	Max.	Unit	Remark
Response time		Tr	θ=0°、Φ=0°	-	10	20	.ms	Note 3
		Tf		-	20	25	.ms	
Contrast ratio		CR	At optimized viewing angle	600	800	-	-	Note 4
Color Chromaticity	White	Wx	θ=0°、Φ=0	0.252	0.302	0.352	-	Note 2,6,7
		Wy		0.274	0.324	0.374	-	
Viewing angle	Hor.	ΘR	CR≧10	80	85	-	Deg.	Note 1
		ΘL		80	85	-		
	Ver.	ΦT		80	85	-		
		ΦB		80	85	-		
Brightness		-	-	1000	1100	-	cd/m2	Center of display
Uniformity		(U)	-	70	-	-	%	Note 5

Ta=25±2℃

Note 1: Definition of viewing angle range

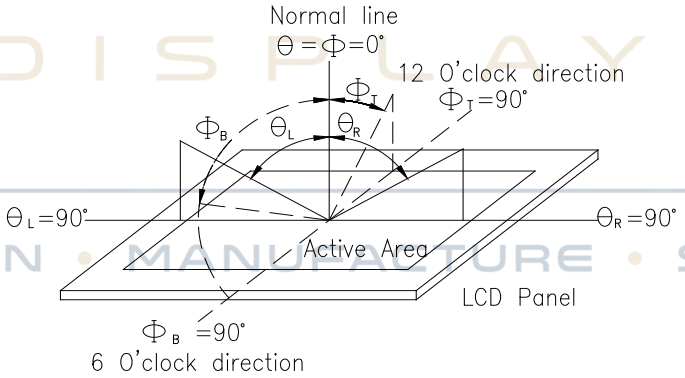


Fig. 12.1. Definition of viewing angle

Note 2: Test equipment setup:

After stabilizing and leaving the panel alone at a driven temperature for 10 minutes, the measurement should be executed. Measurement should be executed in a stable, windless, and dark room. Optical specifications are measured by Topcon BM-7 or BM-5 luminance meter 1.0° field of view at a distance of 50cm and normal direction.

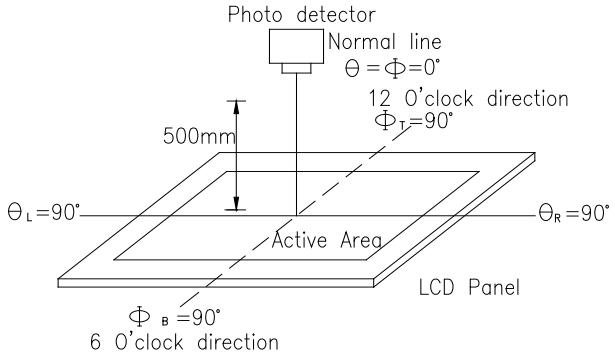
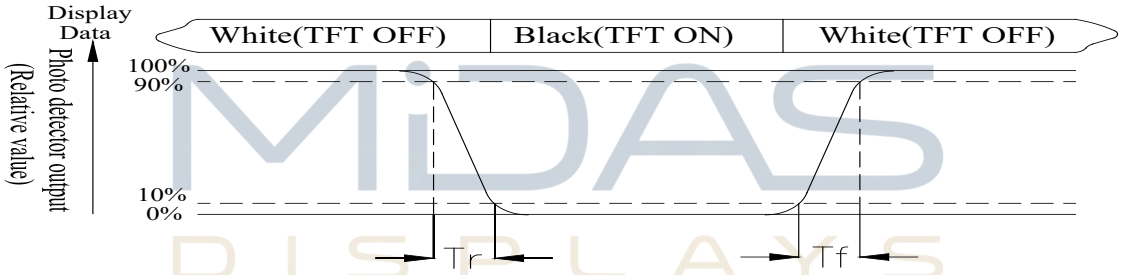


Fig. 12.2. Optical measurement system setup

Note 3: Definition of Response time:
The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time, Tr, is the time between photo detector output intensity changed from 90%to 10%. And fall time, Tf, is the time between photo detector output intensity changed from 10%to 90%



Note 4: Definition of contrast ratio:
The contrast ratio is defined as the following expression.

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note 5: Definition of Luminance Uniformity
Active area is divided into 9 measuring areas (reference the picture in below). Every measuring point is placed at the center of each measuring area.
Luminance Uniformity (U) = Lmin/Lmax x100%
L = Active area length
W = Active area width

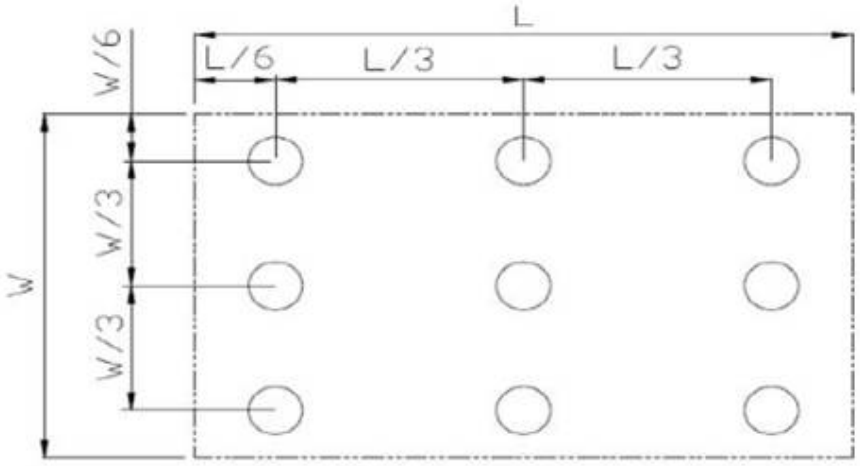


Fig 12.3. Definition of uniformity

Note 6: Definition of color chromaticity (CIE 1931)
Color coordinates measured at the center point of LCD

Note 7: Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

Reliability

Content of Reliability Test (Wide temperature, -20℃~70℃)

Environmental Test			
Test Item	**Content of Test**	**Test Condition**	**Note**
High Temperature storage	Endurance test applying the high storage temperature for a long time.	80℃ 200hrs	2
Low Temperature storage	Endurance test applying the low storage temperature for a long time.	-30℃ 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70℃ 200hrs	——
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20℃ 200hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60℃,90%RH max	60℃,90%RH 96hrs	1,2
Thermal shock resistance	The sample should be allowed stand the following 10 cycles of operation -20℃ 25℃ 70℃ 30min 5min 30min 1 cycle	-20℃/70℃ 10 cycles	——
Vibration test	Endurance test applying the vibration during transportation and using.	Total fixed amplitude : 1.5mm Vibration Frequency : 10~55Hz One cycle 60 seconds to 3 directions of X,Y,Z for Each 15 minutes	3
Static electricity test	Endurance test applying the electric stress to the terminal.	VS=±600V(contact) ,±800v(air), RS=330Ω CS=150pF 10 times	——

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal Temperature and humidity after remove from the test chamber.

Note3: The packing have to including into the vibration testing.

Initial Code For Reference

command:

regw(0xB2,0x10); //Panel Control Register NW/2 Lanes

// 0x30=4LANE

// 0x20=3LANE

// 0x10=2LANE

regw(0x80,0x5B); //Gamma Control Register G2R/G1R

regw(0x81,0x47); //Gamma Control Register G4R/G3R

regw(0x82,0x84); //Gamma Control Register G6R/G5R

regw(0x83,0x88); //Gamma Control Register G8R/G7R

regw(0x84,0x88); //Gamma Control Register G10R/G9R

regw(0x85,0x23); //Gamma Control Register G12R/G11R

regw(0x86,0xB6); //Gamma Control Register G14R/G13R

* Use MIPI Short Packet (0x15) To Write Command and Parameter