

## Description

The SiT92114 is a high-performance LVCMOS clock buffer family of devices. It has an additive phase jitter of 50 fs RMS.

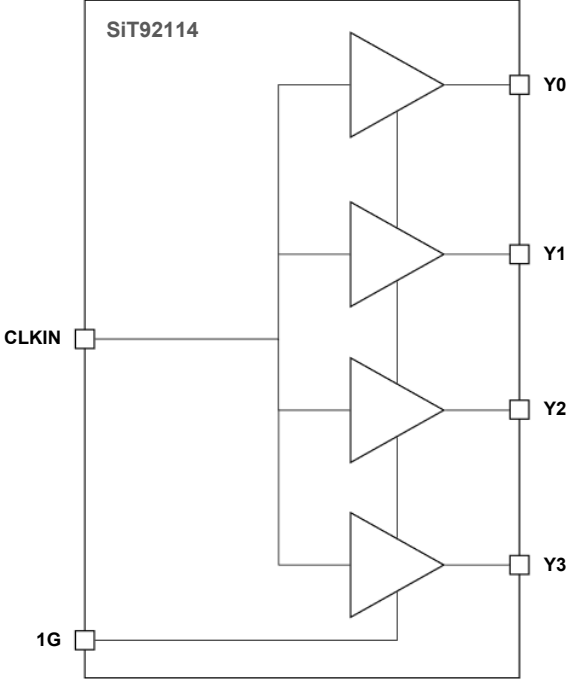
The SiT92114 supports a synchronous glitch-free output enable (OE) function to eliminate any potential intermediate incorrect output clock cycles when enabling or disabling outputs. It can operate from a 1.8 V to 3.3 V supply.

## Applications

- 5G, 4G Base stations
- Telecom Equipment
- Servers

## Features

- High-performance 1:4 Buffer
- LVCMOS clock buffer
- Very low pin-to-pin skew: <50 ps
- Very low additive jitter: <50 fs
- Supply voltage: 1.8 V to 3.3 V
- 3.3 V tolerant input clock
- $F_{MAX} = 200$  MHz
- Integrated serial termination for 50  $\Omega$  channel
- Packaged in 8 pin, 2 x 2 mm DFN packages.

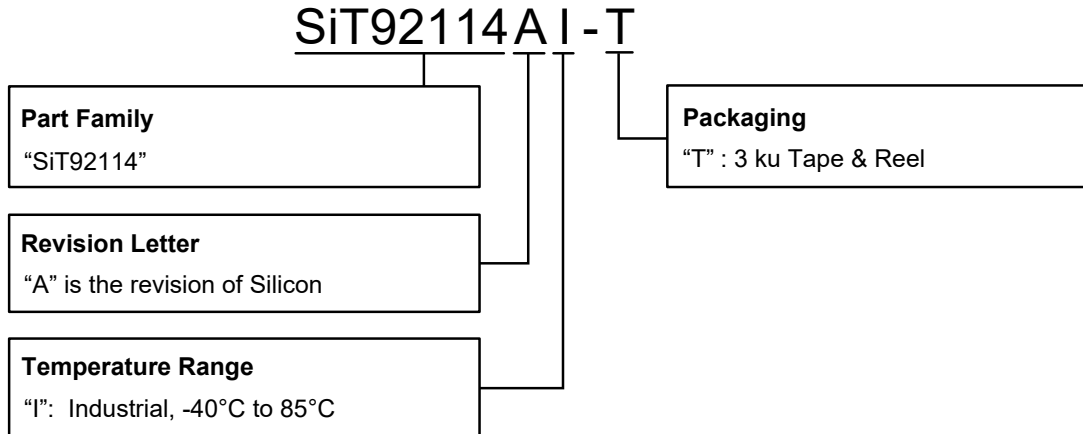


**Figure 1. SiT92114 Functional Overview**

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## Ordering Information



## Electrical Characteristics

**Table 1. Absolute Maximum Ratings**

Parameters	Conditions	Symbol	Min	Typ	Max	Units
Supply Voltage, VDD			3.6		3.6	V
Output Enable and All Outputs			-0.4		VDD+0.3	V
Input voltage, CLKIN			-0.4		3.465	V
Ambient Operating Temperature,			-40		+105	°C
Storage Temperature			-65		+150	°C
Junction Temperature					+150	°C
Soldering Temperature					+260	°C
Moisture Sensitivity Level	8-DFN	MSL			3	

**Notes:**

- Exceeding maximum ratings may shorten the useful life of the device.
- Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or at any other conditions beyond those indicated under the DC Electrical Characteristics is not implied. Exposure to Absolute-Maximum-Rated conditions for extended periods may affect device reliability or cause permanent device damage.

**Table 2. Recommended Operating Supply and Temperature**

Parameter	Symbol	Min	Typ	Max	Units
Ambient Operating Temperature		-40		+105	°C
Power Supply Voltage (Measured in respect to GND)		+1.71		+3.465	V

**Table 3. DC Electrical Characteristics V<sub>DD</sub> = 1.8 V ±5%**

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Operating Voltage		V <sub>DD</sub>	1.71	1.8	1.89	V
Input High Voltage, CLKIN <sup>[1]</sup>		V <sub>IH</sub>	0.7×V <sub>DD</sub>			V
Input Low Voltage, CLKIN <sup>[1]</sup>		V <sub>IL</sub>			0.3×V <sub>DD</sub>	V
Input High Voltage, 1G		V <sub>IH</sub>	1.6		V <sub>DD</sub>	V
Input Low Voltage, 1G		V <sub>IL</sub>			0.6	V
Output High Voltage	I <sub>OH</sub> = -5 mA.	V <sub>OH</sub>	1.4			V
Output Low Voltage	I <sub>OL</sub> = 5 mA.	V <sub>OL</sub>			0.2	V
Nominal Output Impedance		Z <sub>O</sub>		50		Ω
Input Capacitance	CLKIN, 1G pin.	C <sub>IN</sub>		5		pF
Operating Supply Current <sup>[2]</sup>	0.001 MHz, C <sub>L</sub> = 5 pF.	I <sub>DD</sub>		0.7	1.7	mA
	0.008 MHz, C <sub>L</sub> = 5 pF.			0.7	1.7	
	40 MHz, C <sub>L</sub> = 5 pF.			11	13	
	100 MHz, C <sub>L</sub> = 5 pF.			25	30	
	156.25 MHz, C <sub>L</sub> = 5 pF.			37	47	
	200 MHz, C <sub>L</sub> = 5 pF.			39	57	

**Notes:**

- Nominal switching threshold is V<sub>DD</sub>/2.
- TA = -40 °C to +105 °C unless stated otherwise.

**Table 4. DC Electrical Characteristics  $V_{DD} = 2.5\text{ V} \pm 5\%$** 

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Operating Voltage		$V_{DD}$	2.375	2.5	2.625	V
Input High Voltage, CLKIN <sup>[1]</sup>		$V_{IH}$	$0.7 \times V_{DD}$			V
Input Low Voltage, CLKIN <sup>[1]</sup>		$V_{IL}$			$0.3 \times V_{DD}$	V
Input High Voltage, 1G		$V_{IH}$	1.8		$V_{DD}$	V
Input Low Voltage, 1G		$V_{IL}$			0.7	V
Output High Voltage	$I_{OH} = -8\text{ mA}$ .	$V_{OH}$	1.9			V
Output Low Voltage	$I_{OL} = 8\text{ mA}$ .	$V_{OL}$			0.5	V
Nominal Output Impedance		$Z_O$		50		$\Omega$
Input Capacitance	CLKIN, 1G pin.	$C_{IN}$		5		pF
Operating Supply Current <sup>[2]</sup>	0.001 MHz, $C_L = 5\text{ pF}$ .	$I_{DD}$		0.9	2	mA
	0.008 MHz, $C_L = 5\text{ pF}$ .			0.9	2	
	40 MHz, $C_L = 5\text{ pF}$ .			15	17.2	
	100 MHz, $C_L = 5\text{ pF}$ .			35	42	
	156.25 MHz, $C_L = 5\text{ pF}$ .			52	67	
	200 MHz, $C_L = 5\text{ pF}$ .			56	80	

**Notes:**

- Nominal switching threshold is  $V_{DD}/2$ .
- $T_A = -40\text{ }^\circ\text{C}$  to  $+105\text{ }^\circ\text{C}$  unless stated otherwise.

**Table 5. DC Electrical Characteristics -  $V_{DD} = 3.3\text{ V} \pm 5\%$** 

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Operating Voltage		$V_{DD}$	3.135	3.3	3.465	V
Input High Voltage, CLKIN <sup>[1]</sup>		$V_{IH}$	$0.7 \times V_{DD}$			V
Input Low Voltage, CLKIN <sup>[1]</sup>		$V_{IL}$			$0.3 \times V_{DD}$	V
Input High Voltage, 1G		$V_{IH}$	2.1		$V_{DD}$	V
Input Low Voltage, 1G		$V_{IL}$			0.8	V
Output High Voltage	$I_{OH} = -12\text{ mA}$ .	$V_{OH}$	2.4			V
Output Low Voltage	$I_{OL} = 12\text{ mA}$ .	$V_{OL}$			0.7	V
Nominal Output Impedance		$Z_O$		50		$\Omega$
Input Capacitance	CLKIN, 1G pin.	$C_{IN}$		5		pF
Operating Supply Current <sup>[2]</sup>	0.001 MHz, $C_L = 5\text{ pF}$ .	$I_{DD}$		1.2	2.2	mA
	0.008 MHz, $C_L = 5\text{ pF}$ .			1.2	2.2	
	40 MHz, $C_L = 5\text{ pF}$ .			19	23.3	
Operating Supply Current <sup>[2]</sup>	100 MHz, $C_L = 5\text{ pF}$ .	$I_{DD}$		45	54	
	156.25 MHz, $C_L = 5\text{ pF}$ .			67	87	
	200 MHz, $C_L = 5\text{ pF}$ .			75	107	

**Notes:**

- Nominal switching threshold is  $V_{DD}/2$ .
- $T_A = -40\text{ }^\circ\text{C}$  to  $+105\text{ }^\circ\text{C}$  unless stated otherwise.

**Table 6. AC Electrical Characteristics -  $V_{DD} = 1.8\text{ V} \pm 5\%$** 

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Input Frequency			0		200	MHz
Input Slew rate			2			V/ns
Output Rise Time (5 pF load) <sup>[2]</sup>	0.36 V to 1.44 V, $C_L = 5\text{ pF}$ .	$t_{OR}$		0.65	1.2	Ns

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Output Fall Time (5 pF load) <sup>[2]</sup>	1.44 V to 0.36 V, C <sub>L</sub> = 5 pF.	t <sub>OF</sub>		0.65	1.2	Ns
Start-up Time	Part start-up time for valid outputs after VDD ramp-up.	t <sub>START-UP</sub>			3	Ms
Propagation Delay <sup>[3]</sup>		t <sub>PD</sub>	0.24		1.6	Ns
Buffer Additive Phase Jitter, RMS	156.25 MHz, Integration Range: 12 kHz – 20 MHz.	t <sub>JIT</sub>			0.06	Ps
Output to Output Skew	Rising edges at VDD/2. <sup>[1]</sup>	t <sub>SK</sub>		35	50	Ps
Device to Device Skew	Rising edges at VDD/2.				200	Ps
Output Enable Time	C <sub>L</sub> ≤ 5 pF Frequency = 25Mhz	t <sub>EN</sub>			3	Cycles
	C <sub>L</sub> ≤ 5 pF Frequency = 200Mhz	t <sub>EN</sub>			5	Cycles
Output Disable Time	C <sub>L</sub> ≤ 5 pF. Frequency = 25Mhz	t <sub>DIS</sub>			3	Cycles
	C <sub>L</sub> ≤ 5 pF Frequency = 200Mhz	t <sub>DIS</sub>			5	Cycles
Duty Cycle		t <sub>DC</sub>		50		%

**Notes:**

1. Between any 2 outputs with equal loading.
2. TA = -40 °C to +105 °C unless stated otherwise.
3. With rail to rail input clock

**Table 7. AC Electrical Characteristics - V<sub>DD</sub> = 2.5 V ±5%**

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Input Frequency			0		200	MHz
Input Slew rate			2			V/ns
Output Rise Time (5 pF load) <sup>[2]</sup>	0.5 V to 2.0 V, C <sub>L</sub> = 5 pF.	t <sub>OR</sub>		0.63	1.2	ns
Output Fall Time (5 pF load) <sup>[2]</sup>	2.0 V to 0.5 V, C <sub>L</sub> = 5 pF.	t <sub>OF</sub>		0.63	1.2	ns
Start-up Time	Part start-up time for valid outputs after V <sub>DD</sub> ramp-up.	t <sub>START-UP</sub>			3	ms
Propagation Delay <sup>[3]</sup>		t <sub>PD</sub>	0.24		1.6	ns
Buffer Additive Phase Jitter, RMS	156.25 MHz, Integration Range: 12 kHz – 20 MHz.	t <sub>JIT</sub>			0.06	ps
Output to Output Skew	Rising edges at V <sub>DD</sub> /2 <sup>[1]</sup>	t <sub>SK</sub>		35	50	ps
Device to Device Skew	Rising edges at V <sub>DD</sub> /2	t <sub>SKD</sub>			200	ps
Output Enable Time	C <sub>L</sub> ≤ 5 pF Frequency = 25Mhz	t <sub>EN</sub>			3	cycles
	C <sub>L</sub> ≤ 5 pF Frequency = 200Mhz	t <sub>EN</sub>			5	cycles
Output Disable Time	C <sub>L</sub> ≤ 5 pF. Frequency = 25Mhz	t <sub>DIS</sub>			3	cycles
	C <sub>L</sub> ≤ 5 pF Frequency = 200Mhz	t <sub>DIS</sub>			5	cycles
Duty Cycle		t <sub>DS</sub>		50		%

**Notes:**

1. Between any 2 outputs with equal loading.
2. TA = -40 °C to +105 °C unless stated otherwise.
3. With rail to rail input clock

**Table 8. AC Electrical Characteristics -  $V_{DD} = 3.3\text{ V} \pm 5\%$** 

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Input Frequency			0		200	MHz
Input Slew rate			2			V/ns
Output Rise Time (5 pF load) <sup>[2]</sup>	0.66 V to 2.64 V, CL = 5 pF.	$t_{OR}$		0.61	1.2	ns
Output Fall Time (5 pF load) <sup>[2]</sup>	2.64 V to 0.66 V, CL = 5 pF.	$t_{OF}$		0.61	1.2	ns
Start-up Time	Part start-up time for valid outputs after VDD ramp-up.	$t_{START-UP}$			3	ms
Propagation Delay <sup>[3]</sup>		$t_{PD}$	0.24		1.6	ns
Buffer Additive Phase Jitter, RMS	156.25 MHz, Integration Range: 12 kHz – 20 MHz.	$t_{JIT}$			0.05	ps
Output to Output Skew	Rising edges at $V_{DD}/2$ <sup>[1]</sup>	$t_{SK}$		35	50	ps
Device to Device Skew	Rising edges at $V_{DD}/2$ .	$t_{SKD}$			200	ps
Output Enable Time	$C_L \leq 5\text{ pF}$ Frequency = 25Mhz	$t_{EN}$			3	cycles
	$C_L \leq 5\text{ pF}$ Frequency = 200Mhz	$t_{EN}$			5	cycles
Output Disable Time	$C_L \leq 5\text{ pF}$ . Frequency = 25Mhz	$t_{DIS}$			3	cycles
	$C_L \leq 5\text{ pF}$ Frequency = 200Mhz	$t_{DIS}$			5	cycles
Duty Cycle		$t_{DC}$		50		%

**Notes:**

1. Between any 2 outputs with equal loading.
2.  $T_A = -40\text{ }^\circ\text{C}$  to  $+105\text{ }^\circ\text{C}$  unless stated otherwise.
3. With rail to rail input clock

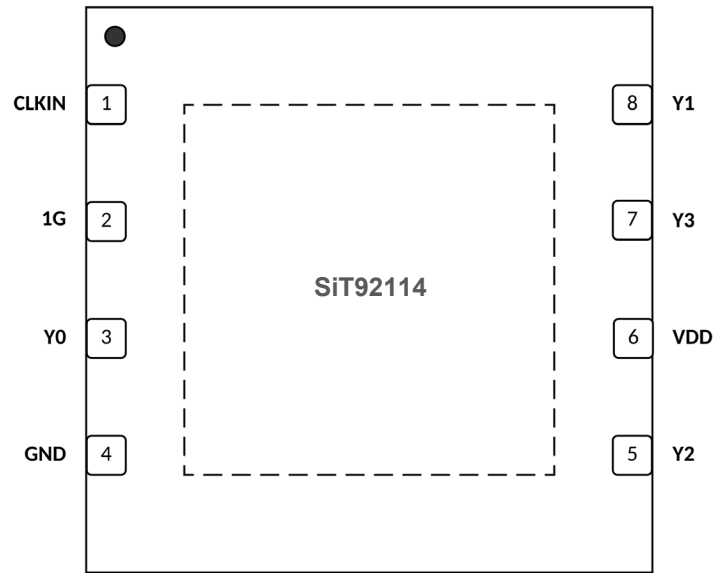
**Table 9. ESD Ratings**

Parameter	Conditions	Symbol	Min	Typ	Max	Units
ESD (Human Body Model)	AEC-Q100-002	$ESD_{HBM}$	-	2000	-	V
ESD (Charged Device Model)	AEC-Q100-011	$ESD_{CDM}$	-	500	-	V

**Table 10. Thermal Characteristics**

Package	$\Theta_{JA}$	Units
8-DFN	75	$^\circ\text{C/W}$ ; still air





**Figure 2. SiT92114 Pin Configuration**

**Table 11. Detailed Pin Description**

Pin Name	Pin Number	Functionality SiT92114
Y0	3	LVCMOS output 0
Y1	8	LVCMOS output 1
Y2	5	LVCMOS output 2
Y3	7	LVCMOS output 3
CLKIN	1	Single Ended Input Clock
1G	2	All outputs enable/disable
VDD	6	Core Supply Voltage, VDD
GND	4	Ground

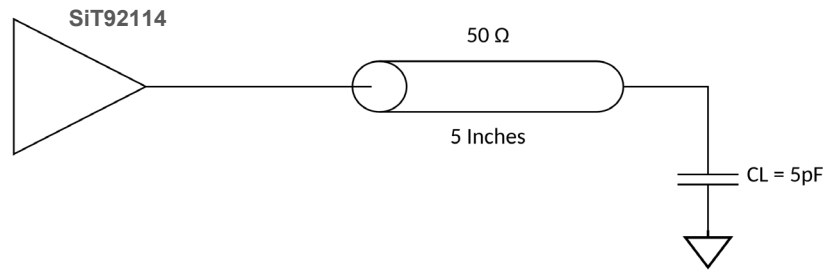
**Functional Description**

**Output Logic Tables**

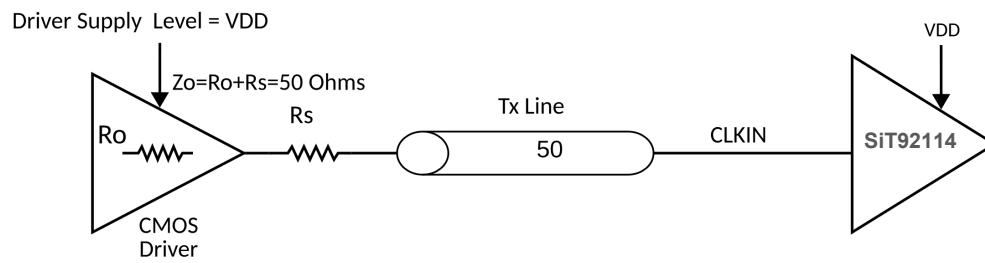
**Table 12. Output Logic Tables**

Inputs		Output
CLKIN	1G	Yn
X	L	L
L	H	L
H	H	H

### Typical Application Diagram



**Figure 3. SiT92114 Typical Application Load**



**Figure 4. Recommended input clock configuration**

### Input Clock and Power Supply Sequencing

The clock input should be available after the SiT92114 power supply is up. An example of the power up sequence is shown in [Figure 5](#).

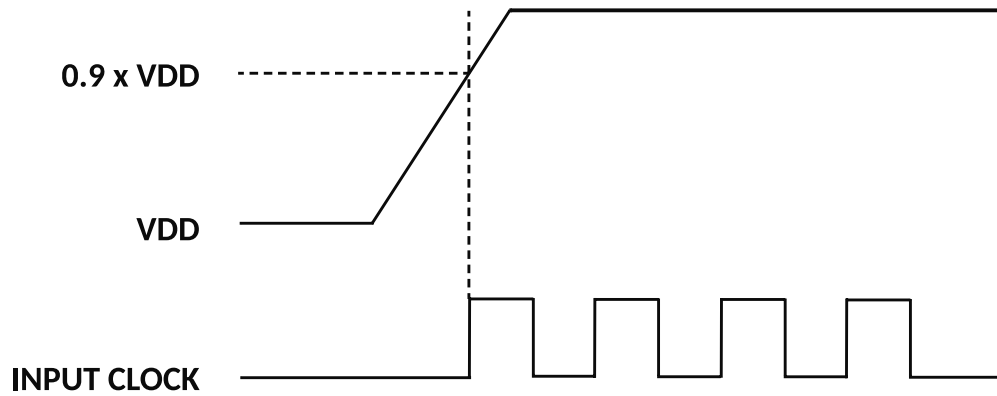
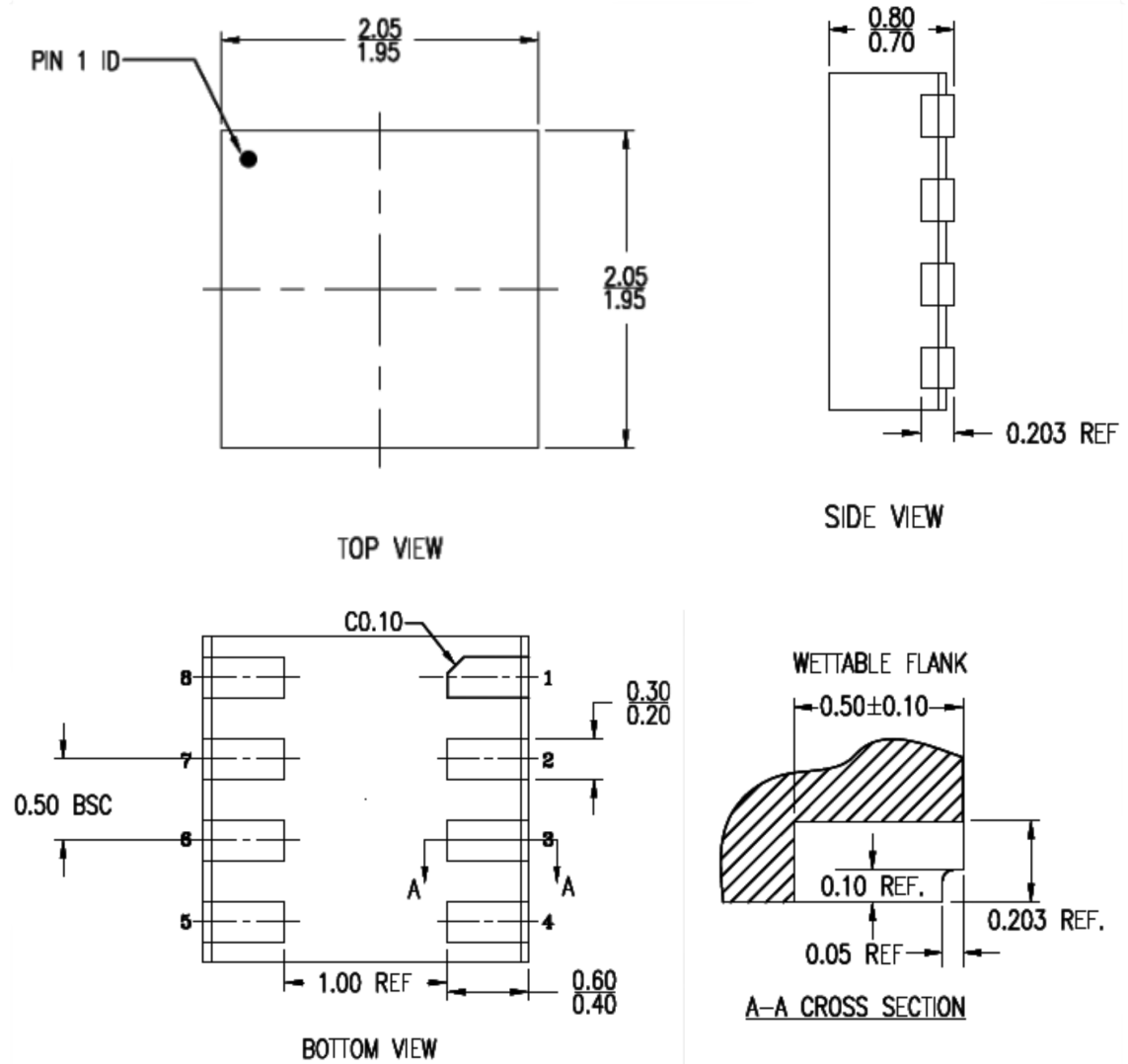


Figure 5. Input clock to VDD ramp timing requirement for SiT92114

**Package Dimensions and Patterns**



**Figure 6. SiT92114 Cross Sections**

**Note:**

1. All Dimensions and Tolerancing Conform to ANSI Y14.5M -1982
2. All Dimensions are in Millimeters (mm)

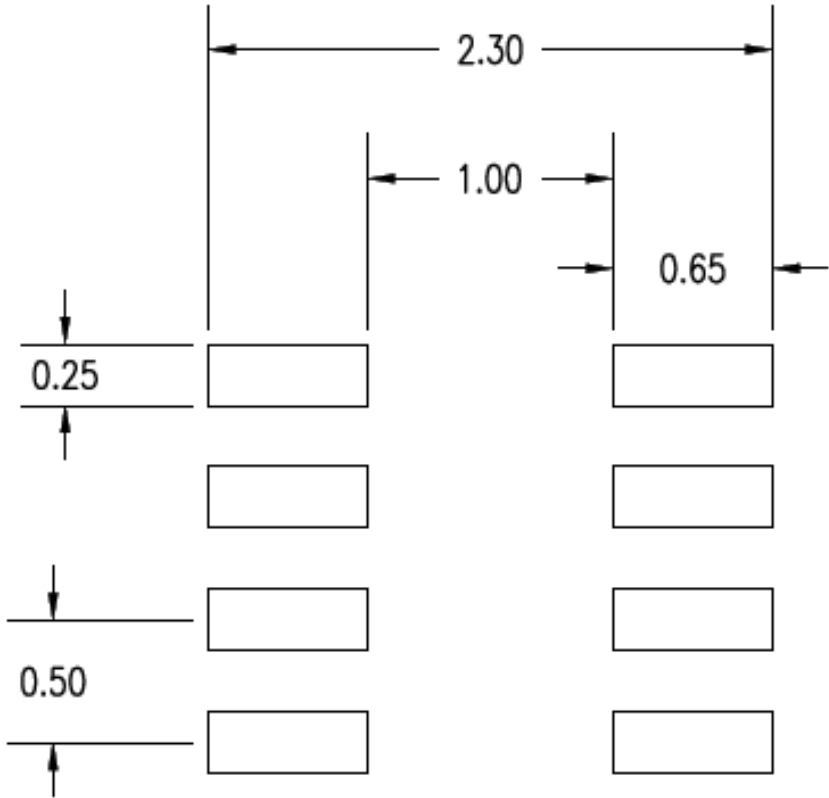


Figure 7. Recommended Land Pattern Dimension

Note:

- 1. All Dimensions are in Millimeters (mm)
- 2. All Angles are in Degrees
- 3. Land Pattern Recommendation per IPC-7351B Generic Requirement for Mount Design and Land Pattern

**Table 13. Revision History**

Revisions	Release Date	Change Summary
0.5	21-Nov-2023	Initial Release

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