General purpose demo board for 2ED21814S06F SOI gate driver evaluation

Basic demo board to test the functionality of new family of Silicon on Insulator (SOI) gate drivers

About this document

Scope and purpose

The purpose of this document is to help power electronic engineers evaluate the new family of Silicon on Insulator (SOI) gate drivers from Infineon Technologies. The general purpose board provides the right platform to test the basic functionalities of the gate driver such as PWM input-output performance, check propogation delay, source/sink current capability etc. The board can also be used to do a simple double pulse test when connected to an external load. The high switching frequency performance of SOI gate drivers can also be tested.

Intended audience

Power supply design engineers, motor control design engineers

Evaluation Board

This board will be used during design in, for evaluation and measurement of characteristics, and proof of data sheet specifications.

Note: *PCB and auxiliary circuits are NOT optimized for final customer design.*

Table 1 2ED21814S06F General Purpose Demo Board Specifications

Symbol	Parameter	Min	Max	Units
V_{CC}	Low-side supply voltage	10	20	V
V_{IN}	Bus input voltage		400	V
V_{OUT}	Switch node output voltage		420	V
I_{OUT}	Switch node output current		10	A
V_{IH}	Logic “1” input voltage	1.7	2.4	V
V_{IL}	Logic “0” input voltage	0.7	1.1	V
$t_{ON/OFF}$	Propogation delay		200	ns

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Safety precautions

Note: Please note the following warnings regarding the hazards associated with development systems.

Table 2 Safety precautions

	**Warning:** *The DC link potential of this board is up to 400 VDC. When measuring voltage waveforms by oscilloscope, high voltage differential probes must be used. Failure to do so may result in personal injury or death.*
	**Warning***: The evaluation or reference board contains DC bus capacitors which take time to discharge after removal of the main supply. Before working on the drive system, wait five minutes for capacitors to discharge to safe voltage levels. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Caution:** *The heat sink and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.*
	**Caution:** *Only personnel familiar with the drive, power electronics and associated machinery should plan, install, commission and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage.*
	**Caution:** *The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*

Table of contents

1 The board at a glance

UG-2021-15, this user guide describes the below board:

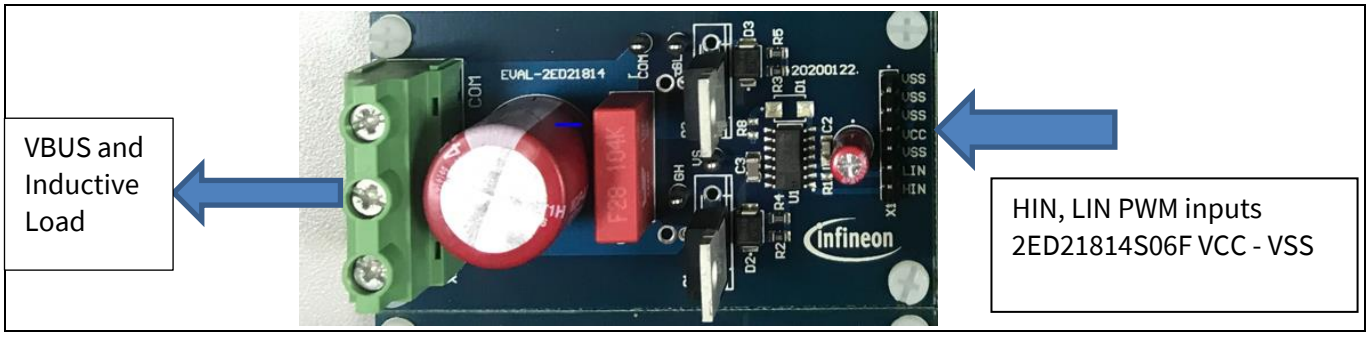

Figure 1: 2ED21814 general purpose demo board

This demo board has two high voltage MOSFETs in a half bridge configuration driven by 2ED21814S06F gate high-side, low-side gate driver. The inputs to the gate driver are provided at X1 connector and the half bridge can be loaded at X2 connector.

1.1 Delivery content

The demo board comes with the 2ED21814S06F and the IPD60R280P7 MOSFETs in half bridge configuration. It can be used to test the various parameters of the gate driver including double pulse tests, basic functionality tests and high frequency performance of the 2ED21814S06F.

1.2 Block diagram

The typical application block diagram is as below:

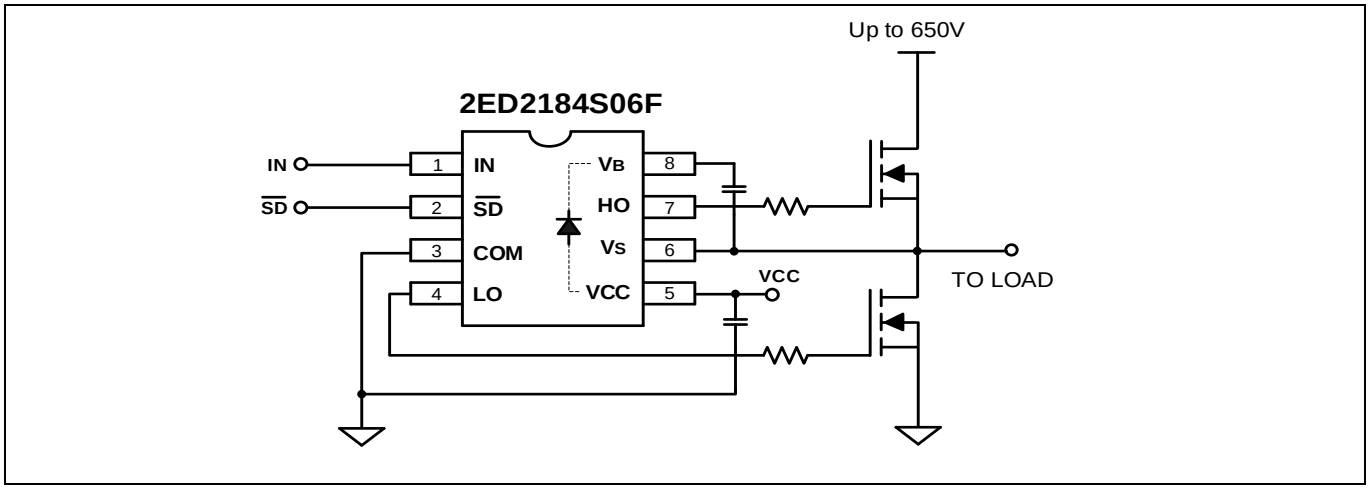

Figure 2: Functional block diagram

1.3 Main features

The demo board features new SOI gate driver IC 2ED21814S06F having:

- Unique Infineon Thin-Film-Silicon On Insulator (SOI)-technology
- Floating channel designed for bootstrap operation
- Integrated ultra-fast, low resistance bootstrap diode
- Logic operational up to –11 V on VS Pin

The board at a glance

- Negative voltage tolerance on inputs of –5 V
- Independent under voltage lockout for both channels
- Schmitt trigger inputs with hysteresis
- 3.3 V, 5 V and 15 V input logic compatible
- Maximum VCC supply voltage of 25 V
- High and low voltage pins separated for maximum creepage and clearance (2ED21814S06J version)
- Separate logic and power ground with the 2ED21814S06J version

1.4 Board parameters and technical data

The demo board is designed to operate as below:

Table 3

Symbol	Parameter	Min	Max	Units
V_{CC}	Low-side supply voltage	10	20	V
V_{IN}	Bus Input Voltage		400	V
V_{OUT}	Switch Node Output Voltage		420	V
I_{OUT}	Switch Node Output Current		10	A
V_{IH}	Logic “1” input voltage	1.7	2.4	V
V_{IL}	Logic “0” input voltage	0.7	1.1	V
$T_{ON/OFF}$	Propogation Delay		200	ns

2 System and functional description

2.1 Commissioning

The board has been tested for DC bus voltages upto 400 V. Load inductor of 1 mH, 2 mH have been used to characterize the double pulse performance.

2.2 Description of the functional blocks

The 2ED21814S06F is a high voltage, high speed power MOSFET driver with independent high and low side referenced output channels. Based on Infineon's SOI-technology there is an excellent ruggedness and noise immunity with capability to maintain operational logic at negative voltages of up to - 11 V on VS pin (V_{CC} = 15 V) on transient voltages. There are not any parasitic thyristor structures present in the device, hence no parasitic latch up may occur at all temperature and voltage conditions. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET, SiC MOSFET or IGBT in the high side configuration, which operate up to 650 V.

2.3 Example: Basic operation

The relationships between the input and output signals of the 2ED21814S06F are illustrated below in Figure 1 and Figure 4. From these figures, we can see the definitions of several timing parameters (i.e. t_{ON}, t_{OFF}, t_R, and t_F) associated with this device.

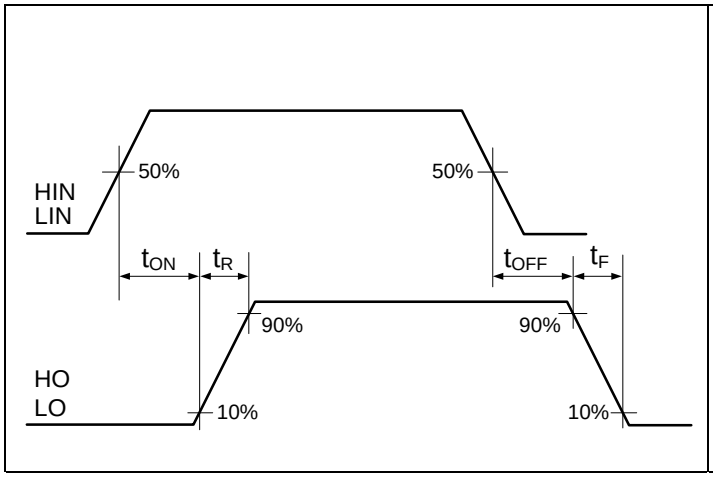

Figure 3 Switching timing diagram

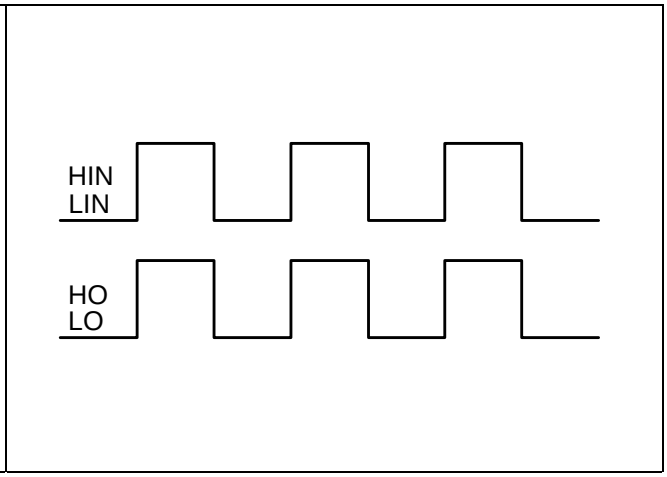

Figure 4 Input/output logic diagram

The input pins of are based on a TTL and CMOS compatible input-threshold logic that is independent of the Vcc supply voltage. With typical high threshold (V_{IH}) of 2.1 V and typical low threshold (V_{IL}) of 0.9 V, along with very little temperature variation as summarized in Figure 5, the input pins are conveniently driven with logic level PWM control signals derived from 3.3 V and 5 V digital power-controller devices. Wider hysteresis (typically 0.9 V) offers enhanced noise immunity compared to traditional TTL logic implementations, where the hysteresis is typically less than 0.5 V. 2ED218x family also features tight control of the input pin threshold voltage levels which eases system design considerations and ensures stable operation across temperature. The 2ED218x features floating input protection wherein if any of the input pin is left floating, the output of the corresponding stage is held in the low state. This is achieved using pull-down resistors on all the input pins (HIN, LIN) as shown in the block diagram. The 2ED218x family has input pins that are capable of sustaining voltages higher than the bias voltage applied on the Vcc pin of the device.

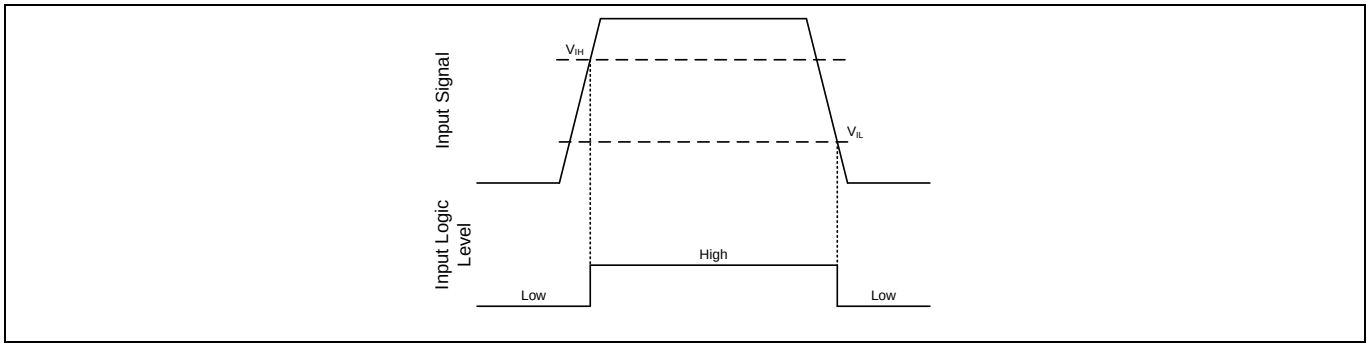

Figure 5 HIN and LIN input thresholds

2.3.1 Example: Design tips

The general-purpose board can be used for evaluating the complete 2ED218x family of gate drivers by modifying the PWM input schemes. The entire family details are as below:

Part No.	Package	Drive current source / sink	Input logic	Cross conduction prevention logic	Deadtime	Ground pins	t_{ON} / t_{OFF}
2ED2181S06F	DSO – 8	+ 2.5 A / - 2.5 A	HIN, LIN	No	None	COM	200 ns / 200 ns
2ED21814S06J	DSO – 14	+ 2.5 A / - 2.5 A				VSS / COM	
2ED2182S06F	DSO – 8	+ 2.5 A / - 2.5 A	HIN, LIN	Yes	Internal 400 ns	COM	
2ED21824S06J	DSO – 14	+ 2.5 A / - 2.5 A			Programmable 400 ns - 5000 ns	VSS / COM	
2ED2183S06F	DSO – 8	+ 2.5 A / - 2.5 A	HIN, $\overline{\text{LIN}}$	Yes	Internal 400 ns	COM	
2ED21834S06J	DSO – 14	+ 2.5 A / - 2.5 A			Programmable 400 ns - 5000 ns	VSS / COM	
2ED21814S06F	DSO – 8	+ 2.5 A / - 2.5 A	IN, $\overline{\text{SD}}$	Yes	Internal 400 ns	COM	600 ns / 200 ns
2ED218144S06J	DSO – 14	+ 2.5 A / - 2.5 A			Programmable 400 ns - 5000 ns	VSS / COM	

3 System design

3.1 Schematics

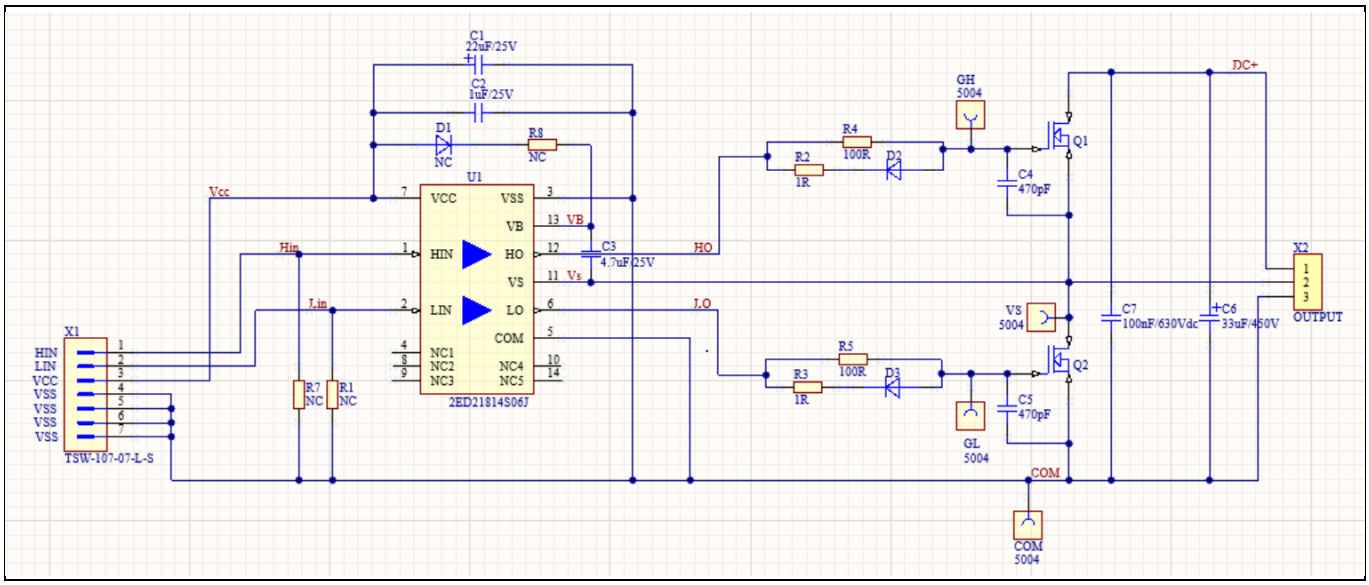

Figure 6: 2ED21814S06F demo board schematics

The schematics show the 2ED21814S06F driving a half bridge. The output can be connected to the load inductor and DC bus. The load inductor is to be connected between 2 and 3 and the DC bus positive to 1 and DC bus negative to 3 of the output connector.

The schematic shows provisions for modifying turn on and turn off dv/dt for both the high side and low side MOSFETs. Turn on dv/dt can be modified by changing R4 / R5 and turn off dv/dt can be modified by changing R2 / R3 for top and bottom MOSFETs respectively.

At X1, input to power the 2ED21814S06F is to be provided. VCC of 15 V between VCC and COM pins, HIN and LIN inputs between HIN-COM and LIN-COM pins.

3.2 Layout

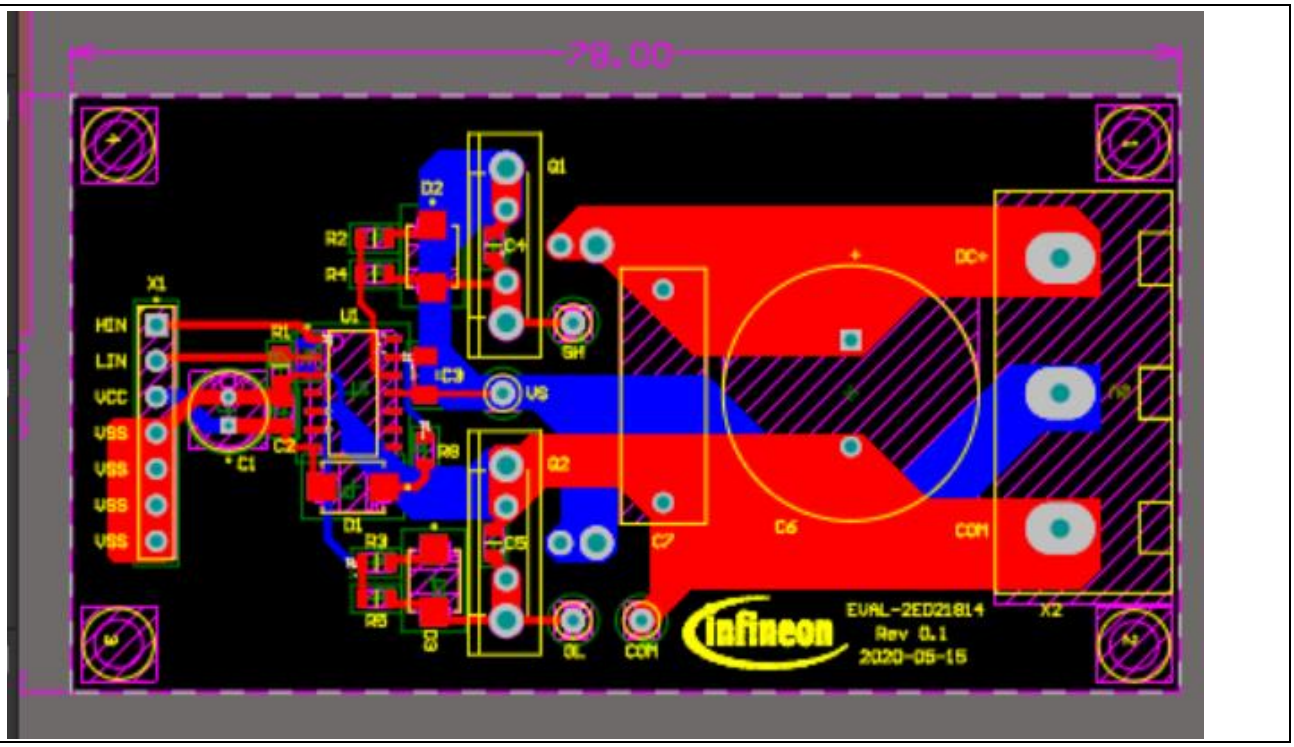

Figure 7: 2ED21814S06F demo board layout

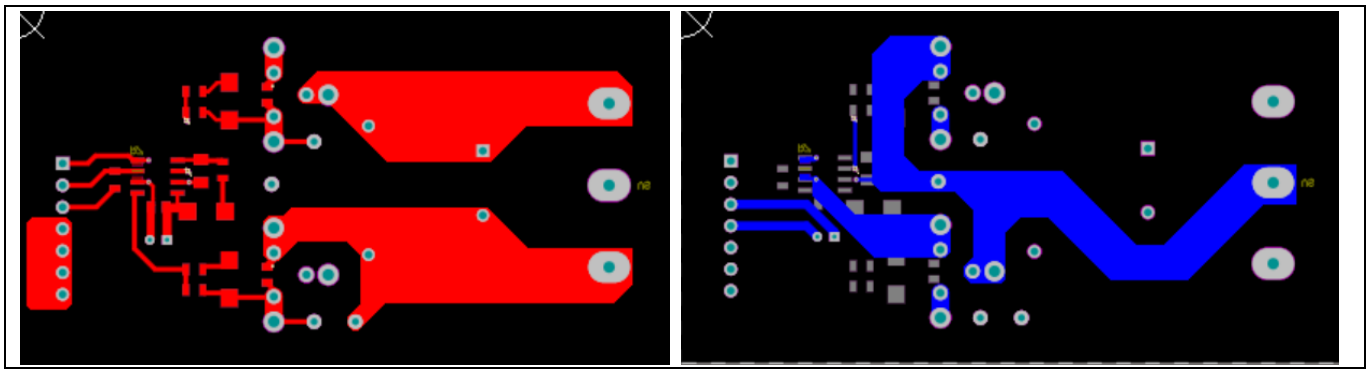

Figure 8: Top layer and bottor layer of 2ED21814S06F demo board

The board layout is as shown above. On the output side, the track thickness enable load current of around 10 A. The gate drive loop is kept to a minimum to ensure no false turn-on event takes place.

3.3 Bill of material

The complete bill of material is available on the download section of the Infineon homepage. A log-in is required to download this material.

Table 4 BOM of the most important/critical parts of the evaluation or reference board

System design

S. No.	Ref Designator	Description	Value	Manufacturer P/N
1	C1	Miniature Aluminum Electrolytic Capacitor	22uF/25V	
2	C2	Surface Mount Multilayer Ceramic Chip Capacitor	1uF/25V	
3	C3	Multilayer Ceramic Chip Capacitor	4.7uF	
4	C4, C5	Chip Monolithic Ceramic Capacitor	470pF/25V	
5	C6	Aluminum Electrolytic Capacitor, Wide Temperature Range	33uF/450V	
6	C7	EMI Suppression Capacitor	100nF/630V	
7	D2, D3	Ultrafast Power Rectifier, 1A, 200V	MURS120T3G	
8	**Q1, Q2**	**600V CoolMOS P7 Power Transistor**	**IPD60R360P7**	
9	R2, R3	Standard Thick Film Chip Resistor	1R	
10	R4, R5	Standard Thick Film Chip Resistor	100R	
11	**U1**	**High Voltage SOI Gate Driver**	**2ED21814S06F**	

Bill of Material of critical components is as above. Infineon parts are highlighted in bold. The remaining parts are generic and can be substituted with other manufacturers with same ratings.

3.4 Connector details

Table 5 Connectors

PIN	Label	Function
Input	X1	Input connector for VCC and HIN/LIN PWM
Output	X2	Output connector for VBUS and Load

4 System performance

4.1 Test points

Various test points are provided on board to measure the gate and drain voltages on the high side and low side MOSFETs.

4.2 Test results

Below test results show some of the measurements taken on the demo board.

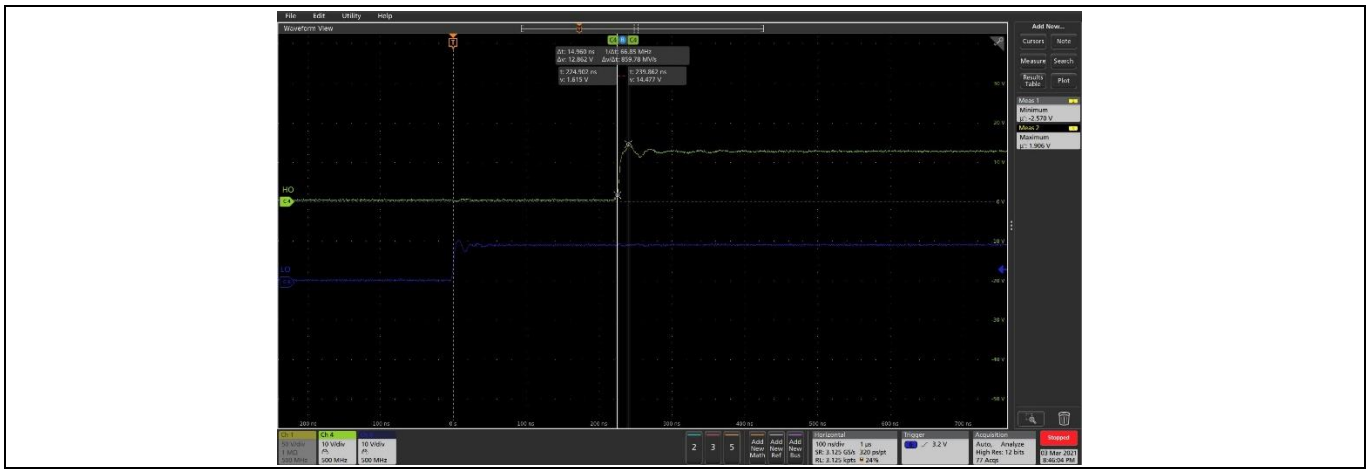

Figure 9 2ED21814S06F rise time measurement result

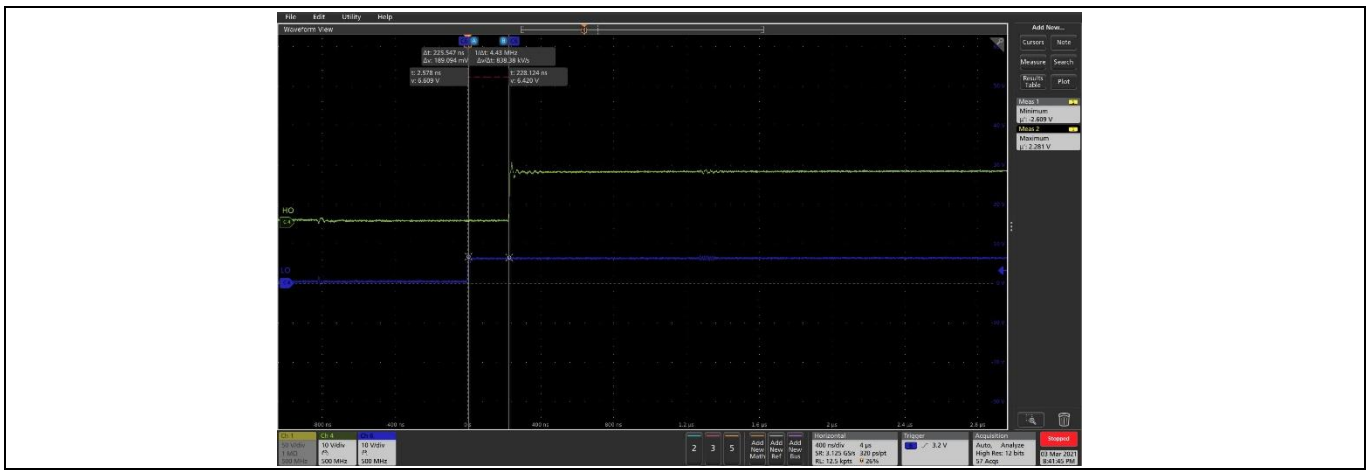

Figure 9 2ED21814S06F propogation delay measurement results

System performance

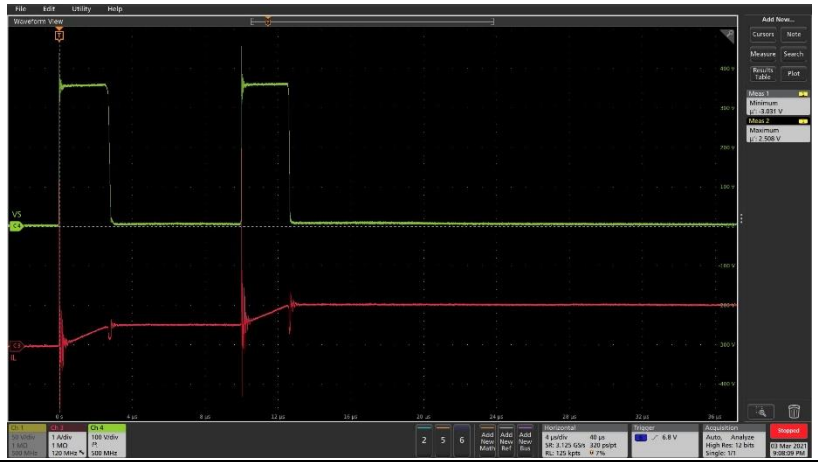

Figure 10: 2ED21814S0FS double pulse test results

5 References and appendices

5.1 Abbreviations and definitions

Table 6 Abbreviations

Abbreviation	Meaning
EMI	Electromagnetic interference

5.2 References

Several technical documents related to the use of HVICs are available at www.infineon.com; use the Site Search function and the document number to quickly locate them. Below is a short list of some of these documents.

Application Notes:
Understanding HVIC Datasheet Specifications
HV Floating MOS-Gate Driver ICs
Use Gate Charge to Design the Gate Drive Circuit for Power MOSFETs and IGBTs
Bootstrap Network Analysis: Focusing on the Integrated Bootstrap Functionality

Design Tips:
Double Pulse Testing
Using Monolithic High Voltage Gate Drivers
Alleviating High Side Latch on Problem at Power Up
Keeping the Bootstrap Capacitor Charged in Buck Converters
Managing Transients in Control IC Driven Power Stages
Simple High Side Drive Provides Fast Switching and Continuous On-Time

5.3 Additional information: Infineon online community resources

The Gate Driver community is live at Infineon.com (https://community.infineon.com/t5/Gate-Driver-IC-s/bd-p/GateDriverICs). Here the Infineon gate driver community comes to the assistance of our customers to provide technical guidance – how to use gate driver ICs, existing and new gate driver information, application information, availability of demo boards, online training materials for over 500 gate driver ICs. The Gate Driver community also serves as a repository of FAQs where the user can review solutions to common or specific issues faced in similar applications.

Register online at the community and learn the nuances of efficiently driving a power switch in any given power electronic application.

Revision history

Document version	Date of release	Description of changes
1	2021-01-10	Initial version

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