NXP Semiconductors
User Guide

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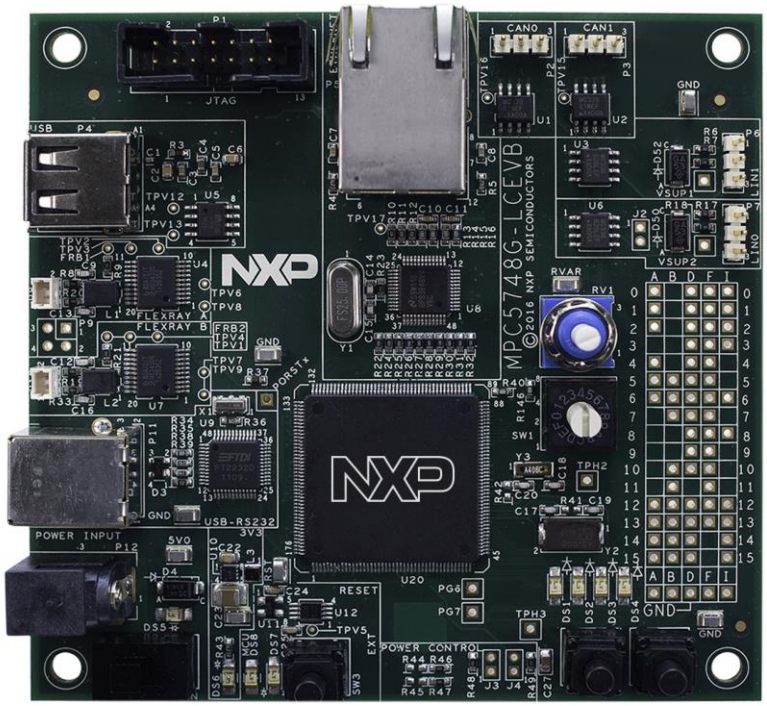


MPC5748G Low Cost EVB User Guide (MPC5748G-LCEVB)

Table of Contents

1. Introduction

This user guide details the setup and configuration of the NXP MPC5748G Low Cost Evaluation Board (hereafter referred to as the LCEVB). The LCEVB is intended to provide a mechanism for easy evaluation of the MPC5748G family of microcontrollers, and to facilitate basic hardware and software development.

Note that the LCEVB has a limited feature set compared to the main MPC574xG customer EVB and is intended for evaluation purposes. Customers moving to serious development activities are recommended to purchase the fully functional customer EVB which also has device specific daughter cards.

The LCEVB is intended for bench / laboratory use and has been designed using normal temperature specified components (+70° C).

This product contains components that may be damaged by electrostatic discharge. Observe precautions for handling electrostatic sensitive devices when using the LCEVB.

The user guide is intended to be read alongside the respective MCU documentation available at www.nxp.com and includes:

- Reference Manuals
- Product Data Sheets
- Application notes
- Device Errata

2. LCEVB Features

The LCEVB provides the following key features:

- Single 5 V DC external power supply input with on-board 3.3 V regulator. Power is supplied via a 2.1 mm barrel style power jack.
- Simple jumper less configuration (enhanced configuration is possible via 0 Ohm Resistors and optional jumpers if required).
- Master power switch and regulator status LED.
- USB Serial interface.
- 2 x High Speed CAN transceiver routed to 3-way headers.
- 2 x LIN interfaces routed to 3-way headers.
- Main clock supplied from on board crystal.
- User reset switch with reset status LED's.
- Ethernet PHY and RJ45 socket (configured for MII mode).
- USB Type A Host interface.
- 2 x FlexRay interfaces with standard 2-pin connectors.
- 14-pin JTAG connector.

- 4 user LED's wired to MCU ports.
- 2 user pushbutton switches wired to MCU ports.
- Hexadecimal encoded switch wired to 4 MCU ports.
- Simple potentiometer connected to analogue input channel.

2.1. Differences to the Customer EVB

Note that the GPIO pins used for peripherals on the LCEVB are the same as those used on the customer EVB. This ensures maximum code compatibility between the 2 boards, making it easy to migrate from one board to the other

Table 1. Customer EVB vs LCEVB features

Feature	Customer EVB	LCEVB
MCU Support	Custom MCU Daughter cards for multiple devices (socketed)	Soldered 176QFP MPC5748G
Power Supply	External 12 V	**External 5 V (Caution)**
On Board Regulators (and LED's)	5 V, 3.3 V, 1.25 V (combination of Linear and /or Switching regulators)	3.3 V Switching Regulator
Master Power Switch	Yes	Yes
Reset Control	Reset button with MCU and External Reset LED's	Reset button with MCU and External Reset LED's
USB FTDI Serial Interface	Yes	Yes
CAN Physical Interfaces	2 (routed to 0.1" headers)	2 (routed to 0.1" headers)
LIN Physical Interfaces	2 (routed to Molex headers)	2 (routed to 0.1" headers)
FlexRay Physical Interfaces	2 (routed to 0.1" headers)	2 (routed to 0.1" headers)
Ethernet Physical Interface	1 (MII and RMII Support)	1 (MII only mode)
USB Physical Interface	2 (USB Host and OTG)	1 (USB Host)
MLB Daughter card Connector	Yes	No
SAI Audio / TWRPI Connectors	Yes	No
SDHC Connector	Full Size SDHC Socket	No
Fast External Osc (FXOSC)	Daughter card Crystal * and SMA input connector	40 MHz Crystal
Slow External Osc (SXOSC)	Daughter card Crystal *	32.768 KHz Crystal
CLKOUT signals available	Yes (GPIO Matrix)	Yes (Standalone pads)
User LEDS	4	4
User Pushbutton Switches	4	2
Hex Encoded Switch	Yes	Yes
Test Potentiometer for ADC	Yes	Yes
GPIO Matrix	All Available Pins not otherwise used for peripherals	Selection of Pins available from 5 GPIO Ports
Debug	14 Pin JTAG and 50 pin Nexus	14 Pin JTAG
Configuration	Highly configurable via jumper shunts	Fixed (limited configuration via 0 ohm resistors)

* Daughter card crystals are typically 40 MHz for FXOSC and 32.768 KHz for SXOSC but may vary between daughter cards.

The figure below shows the customer EVB (left) next to the LCEVB (right).

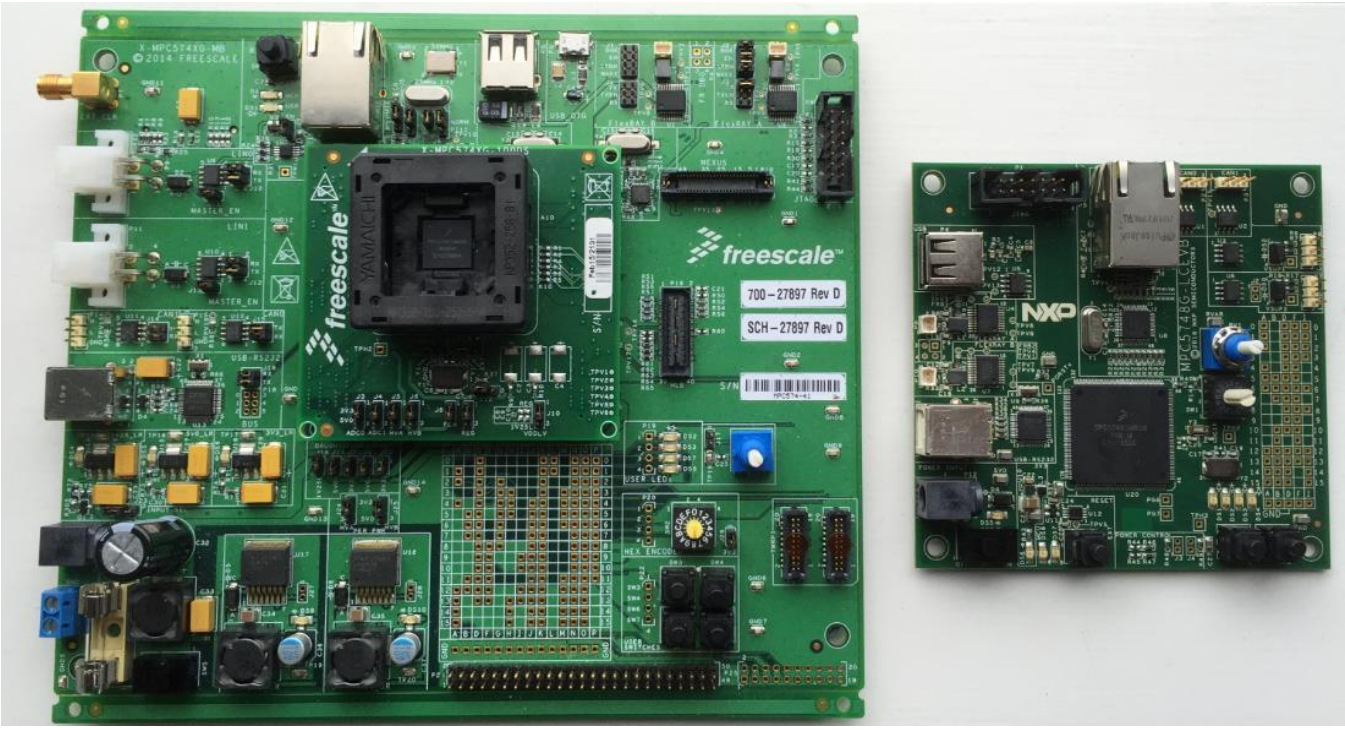


Figure 1. Customer and LCEVB side by side

3. Configuration Overview

Out of the box, there is no configuration required for the LCEVB to function. Unlike the customer EVB, the LCEVB is primarily designed for a single mode of operation with no requirement for user configuration. If you wish to have a more flexible configuration the recommendation is that the fully configurable customer EVB is purchased.

There are however some jumper footprints and zero ohm resistors populated in positions that would normally have jumper headers fitted (for example on the MCU power supply lines and tracking to the peripheral interfaces). If required these can be de-soldered to modify functionality. Any such modification is done at the full risk of the user and no support or warranty repairs will be provided for a board that has been modified. Modifications should only be attempted by appropriately trained personnel using the correct equipment and Personal Protective Apparel

The diagram below gives an overview of the functional blocks of the LCEVB

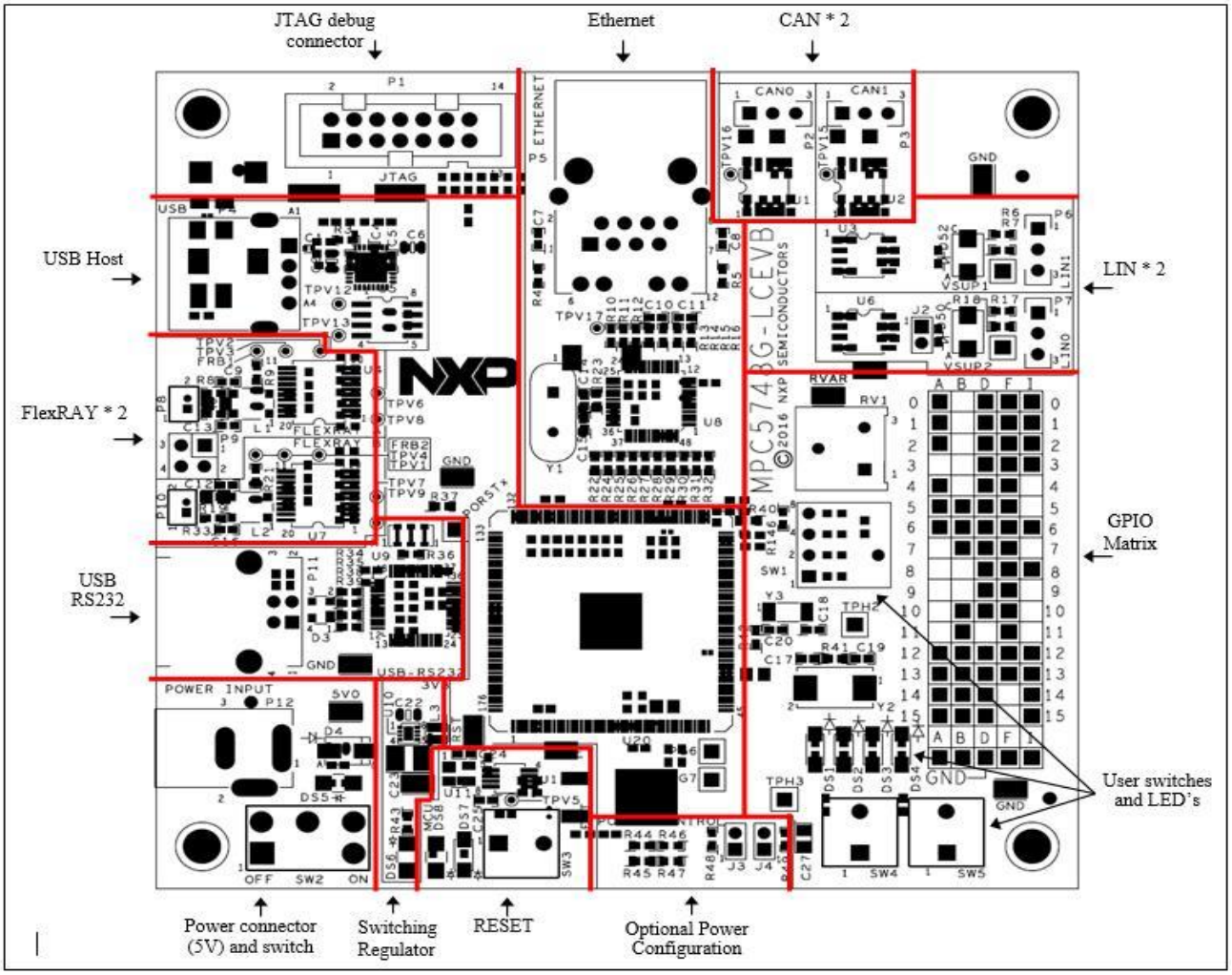


Figure 2. EVB Functional Blocks

4. Initial Setup

This section details the power, reset, clocks, and debug configuration which is the minimum configuration needed in order to power ON the LCEVB.

4.1. Power Supply Configuration

The Power supply section is located in the bottom left corner of the LCEVB

The LCEVB requires an external power supply voltage of 5 V DC, minimum 1 A. There is a single 3.3 V switching regulator on the LCEVB providing MCU and peripheral power.

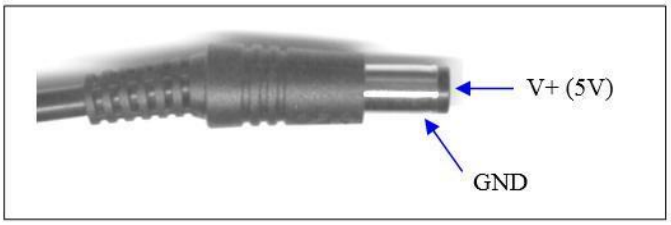
CAUTION

Connecting a power supply with a voltage greater than 5 V will result in irrecoverable board damage. Check the power supply voltage before connecting the plug to the LCEVB.

4.1.1. Power Input Connector

Power is supplied to the LCEVB via a 2.1 mm connector from the wall-plug mains adapter as shown below. Note – if a replacement or alternative adapter is used, care must be taken to ensure the 2.1 mm plug uses the correct polarization as shown below:

Figure 3. 2.1 mm Power Connector



4.1.2. Power Switch

Slide switch SW2 can be used to isolate the power supply input from the EVB voltage regulators if required.

- Moving the slide switch to the right (away from the power connector) will turn the EVB ON.
- Moving the slide switch to the left (towards the power connector) will turn the EVB OFF.

4.1.3. Power Status LED

When power is applied to the LCEVB, two green LED's adjacent to the regulator and power connector show the presence of the supply voltages as follows:

- LED DS5 – Indicates that the 5.0 V supply voltage is present
- LED DS6 – Indicates that the 3.3 V switching regulator is functioning

If no LED's are illuminated when power is supplied to the LCEVB and the power switch is in the "ON" position, the power adapter may be faulty or there may be a fault with the LCEVB. If only one LED is illuminated there may be a short in that power supply rail – check there is nothing shorting on the EVB. If you continue to have problems, contact NXP for support.

CAUTION

In the event of a short on the regulator output (in which case one of the LED's would be off or dimly illuminated), the regulator and/or the shorted component will likely be hot.

4.1.4. MCU and Peripheral Voltage Configuration

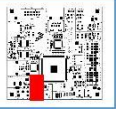
The following MCU supply rails are connected to the 3.3 V switching regulator:

- VDD_HV_ADC0
- VDD_HV_ADC1
- VDD_HV_ADC1_REF
- VDD_HV_A
- VDD_HV_B
- VDD_HV_FLA
- External Ballast Transistor Supply

Similarly all of the peripheral interfaces (or the I/O power in the peripheral interface) are supplied from 3.3 V as is the reset circuitry and the voltage sense wire on the JTAG connector.

4.2. Reset Control (SW3)

The reset circuitry is located in the bottom left quarter of the LCEVB next to the power switch



The MCU has a single bi-directional open drain Reset pin. Rather than connect multiple devices to the reset pin directly, a reset-in and reset-out buffering scheme has been implemented on the LCEVB as shown in Figure 4. The reset "in" from the reset switch (SW3) and the debug connectors are logically OR'd together using an AND gate and then connected to the buffer to provide an open-drain output.

The "reset-out" circuitry provides a buffered reset signal that can be used to drive any circuitry requiring a reset control from the MCU.

This scheme is not required if it is guaranteed that anything driving the reset pin has an open drain drive and that there is no significant output load on the MCU reset pin.

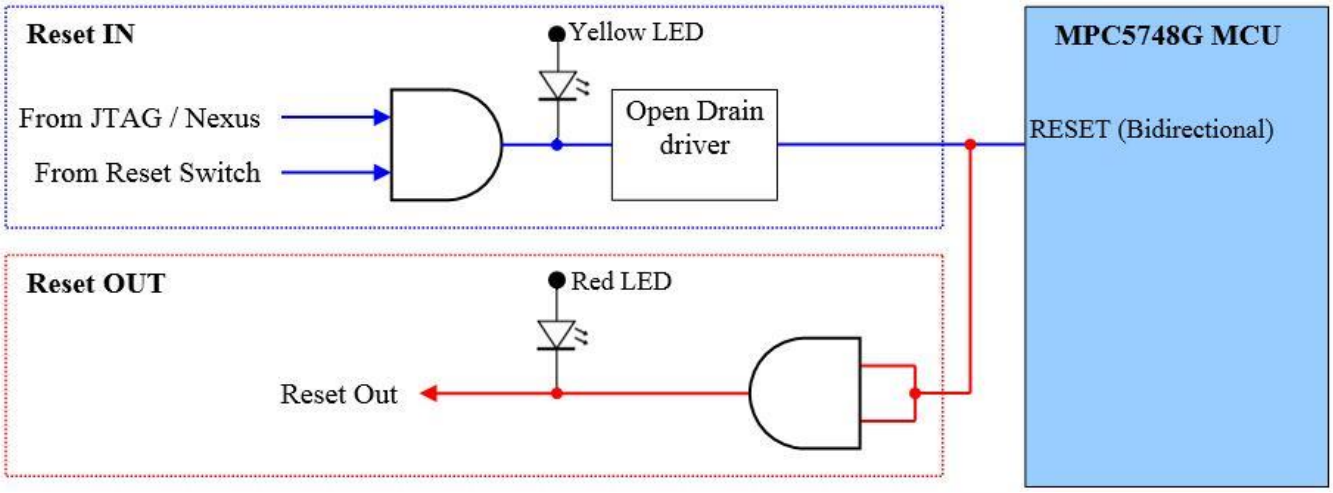


Figure 4. EVB Reset Control

4.2.1. Reset LEDs

As can be seen above, there are two reset LED's that can be used to identify the source / cause of a reset:

RED LED DS8 (titled "MCU") will illuminate if:

- The MCU issues a reset (in this condition ONLY this LED will be illuminated and LED DS1 will be off)
- There is a target reset (i.e. from the reset switch or from the debugger in which case LED DS1 will be ON)

YELLOW LED DS7 (titled "EXT") will illuminate when an external hardware device issues a reset to the MCU:

- The reset switch is pressed
- There is a reset being driven from one of the debug connectors

Table 2. Reset LED Decoding

LED DS7 (Yellow)	LED DS8 (Red)	Description
OFF	OFF	No Reset being issued from MCU or external logic
OFF	ON	MCU has issued a reset
ON	OFF	External reset issued from switch or debug BUT not being issued to MCU (check R137 has not been removed)
ON	ON	External reset issued from reset switch or debug and has been issued to MCU.

4.3. MCU Clock Configuration

There is an external 40MHz crystal connected to the MCU Fast External Oscillator (FXOSC) pins EXTAL and XTAL.

There is also a 32.768 crystal connected to the MCU Slow External Oscillator (SXOSC) pins OSC32K_EXTAL and OSC32K_XTAL. This can be used for accurate time keeping.

There are 2 pads PG6 and PG7 (located just below the MCU) on the LCEVB to facilitate measurement of the CLKOUT1 and CLKOUT0 signals.

Note – there is no external clock input on the LCEVB

4.4. Debug Connector (P1)

The JTAG debug connectors is located in the top left corner of the LCEVB

The LCEVB has a single 14-pin keyed JTAG connector for connection to an external debugger.

Before attaching or removing the debug cable from the LCEVB remove power from the EVB to prevent damage to the LCEVB or debug hardware.

4.4.1. Debug Connector Pinout

The following tables list the pinout for the JTAG connector used on the LCEVB

Table 3. 14-Pin JTAG Debug Connector Pinout

Pin No	Function	Connection		Pin No	Function	Connection
1	TDI	PC0		2	GND	GND
3	TDO	PC1		4	GND	GND
5	TCLK	PH9		6	GND	GND
7	EVTI	PL8		8	N/C	---
9	RESET	JTAG – RSTx		10	TMS	PH10
11	VREF	PER_HVA		12	GND	GND
13	RDY	---		14	JCOMP	10k Pulldown

TDI, TDO and TMS have 10K pullup resistors on the LCEVB. TCLK has a 10K pulldown (R147) to facilitate STANDBY exit without any additional code (at the sacrifice of slightly higher STANDBY current), however this can be changed to a pullup if required by removing R147 and fitting the resistor on R56.

Table 4. JTAG Pins Pull State (from MPC5748G Reference Manual)

TERMINAL TYPE	POWERUP pad state	RESET pad status	DEFAULY pad status
RESET	Strong pull-down	Strong pull-down	Weak pull-up
PORST	Weak pull-down	Weak pull-up	Weak pull-up
GPIO	High impedance	High impedance	High impedance
ANALOG	High impedance	High impedance	High impedance
EOUT0, EOUT1	High impedance	High impedance	High impedance
TCK	High impedance	Weak pull-up	Weak pull-up
TMS	High impedance	Weak pull-up	Weak pull-up
TDI	High impedance	Weak pull-up	Weak pull-up
TDO	High impedance	High impedance	High impedance

5. Communications & Memory Interfaces:

This section details the communication interface and storage peripherals that are implemented on the LCEVB.

5.1. CAN Interfaces (P2, P3)

The CAN circuitry is located on the top right edge of the LCEVB

The LCEVB incorporates two identical CAN interface circuits connected to MCU CAN0 and CAN1 using MC33901 transceivers. Both transceivers are configured for high speed operation by pulling pin 8 to GND via a 4.7 kOhm resistor. There are test points to allow the Select pin to be driven high if desired. The MC33901 is pin compatible with other CAN transceivers supporting full CAN FD data rates.

For flexibility, the CAN transceiver I/O is connected to a 0.1” header (P2 for CAN0 / P3 for CAN1) rather than using non-standard DB9 connectors. The pinout of these headers is shown below.

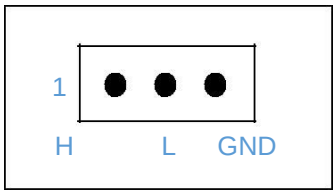


Figure 5. CAN Physical Interface Connectors

The LIN Physical interface circuits are located on the right edge of the LCEVB

5.2. LIN Interfaces (P6, P7)

The LCEVB incorporates two LIN transceiver circuits connected to MCU LIN0 and LIN1, using an NXP MC33662 transceiver. The MPC5748G LIN0 supports both master and slave modes whereas LIN1 only supports master mode.

On the LCEVB, the LIN0 transceiver is configured as slave mode by default. Master mode operation is possible by either populating a zero ohm resistor (R143) or buy fitting a jumper header (J2) – see the schematics for details. The LIN0 transceiver is hard wired for master mode. To save on board space and cost, both LIN transceivers are connected to 0.1" pitch 3x1 headers as shown below rather than the usual LIN Molex header.

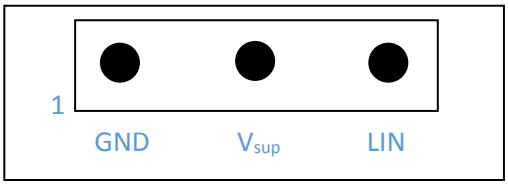


Figure 6. LIN Physical Interface Connector

Note that in order for the LIN transceiver to function, external 12v must be supplied via pin 2 of the connector

5.3. USB RS232 Serial Interface (P11)

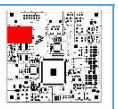
The USB RS232 interface is on the left hand edge of the board (USB Type B

The LCEVB incorporates a USB RS232 serial interface providing RS232 connectivity via a direct USB connection between the PC and the EVB. The circuit contains an FTDI FT2232D USB to Serial interface which should automatically install the drivers for two additional COM ports on your PC. Note that only one of these ports is used so you will need to try both (usually the higher numbered COM port is the active one). For more information on the USB drivers and general fault finding, consult the FTDI website at http://www.ftdichip.com/

The MCU LIN2 signals are routed to the FTDI transceiver (UART TX and RX). No handshaking signals are implemented and no board configuration is required.

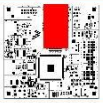
5.4. USB HOST Interface (P4)

The USB Host interface is on the top left corner of the LCEVB on the left



The LCEVB includes a Type A (Host) USB interface, routed to a USB type A female connector. The USB circuit contains a USB83340 transceiver with a MIC2026-1YM USB power switch. There is no hardware user configuration required to use the USB circuit.

5.5. Ethernet Interface (P5)



The EVB incorporates a single DP83848c Ethernet transceiver with the circuitry configured for MII mode. The transceiver is connected to a pulse J1011F21PNL RJ45 connector which includes a built-in isolation transformer. There is no hardware configuration needed.

If you require RMII mode or access to both Ethernet ports on the MPC5748G, please purchase the MPC5748G customer EVB and appropriate daughter cards.

Note that the MCU Ethernet signals are all in the VDD_HV_B domain. The Ethernet PHY will only function with 3.3 V I/O so if you have made any modifications to the EVB power domain configuration (via the zero ohm resistors), you need to ensure the VDD_HV_B domain is at 3.3 V before attempting to use the Ethernet module. If VDD_HV_B is set to 5 V, the signals routed to the Ethernet PHY (see the EVB schematics) must be left as tristate to prevent damage to the transceiver.

5.6. FlexRay (P8, P9, P10)

The LCEVB incorporates two FlexRay TJA1080TS/N interfaces connected to MCU FlexRay channels A and B and routed to two Molex 1.25 mm pitch Pico Blade shrouded headers (standard on many NXP EVB's). There is no hardware configuration required to use FlexRay.

Note that the LCEVB is supplied with a 40 MHz crystal by default. If FlexRay is configured to use the external clock source, then the crystal should be left at 40 MHz

6. User Interface (I/O)

This section details the user I/O available on the LCEVB and includes the GPIO matrix, switches, LED's and the ADC variable resistor.

6.1. GPIO Matrix

The GPIO matrix is on the right hand edge of the LCEVB

A sub-set of available GPIO pins (available pins being those not already routed to LCEVB peripherals) are available at the GPIO matrix as detailed below. The matrix provides an easy to follow, intuitive, space saving grid of 0.1" header through-hole pads. Users can solder wires, fit headers or simply insert a scope probe into the respective pad.

To use the matrix, simply read the port letter from the top or bottom row of text then the pad number from the columns on the left or right of the matrix. For example, the 1st pad available on Port B is PB5 as outlined below.

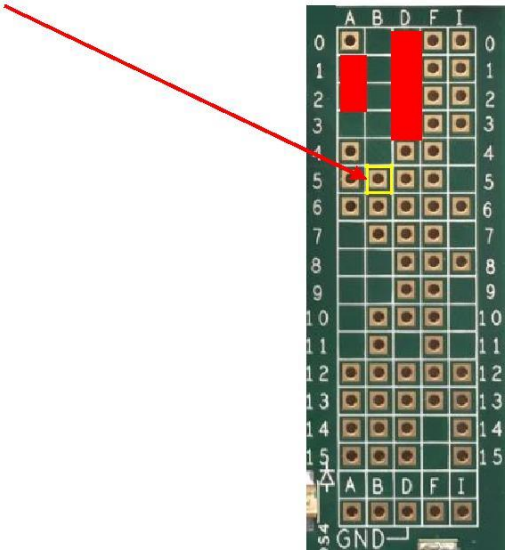


Figure 7. GPIO Matrix

If a pad is populated in the matrix, it means this is available for exclusive use as GPIO. The exception to this are the port pins detailed below which are also shared with switches or user LED's (shaded red in the matrix diagram above).

PD0, PD1, PD2, PD3 – HEX Encoder Switch
PA1, PA2 – User pushbutton Switches

If you require access to all of the available GPIO pads, the customer EVB and daughter card provides this additional functionality.

The user pushbutton switches are in the bottom right corner of the LCEVB

6.2. User Switches (SW4, SW5)

There are two active high (pulled low, driven to 3.3 V) pushbutton switches on the LCEVB connected directly to MCU GPIO ports. No configuration is required to use the switches.

SW4 is connected to port PA1 (which is also the NMI pin) and SW5 is connected to port PA2

NOTE

The MCU ports used on the user pushbutton switches are also routed to the GPIO matrix.

The hex encoder switch is located to the left of the GPIO Matrix

6.3. Hex Encoded Switch (SW1)

There is a single hex encoded 16 position rotary switch on the LCEVB. This outputs a binary encoded hex value (active high) on four MCU ports (Port D[0..3]).

Table 5. Hex Encoder Switch (SW2)

Position	HEX_SW4 (PD3)	HEX_SW3 (PD2)	HEX_SW2 (PD1)	HEX_SW1 (PD0)
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
A	1	0	1	0
B	1	0	1	1
C	1	1	0	0
D	1	1	0	1
E	1	1	1	0
F	1	1	1	1

Note that POSN 0 will ensure that no voltage is applied to the pads. This allows the pads to be used as normal GPIO (with 10K pulldown) and accessed at the respective pads on the GPIO matrix area.

6.4. User LED’s (DS1, DS2, DS3, DS4)

The user LED’s are above the user switches in the lower right corner

There are four **active low** user LED’s, DS1 to DS4, connected directly to 4 MCU ports (PG[2..5]) as shown below. No configuration is required to use the LED’s.

Table 6. Use LED’s (DS1, DS2, DS3 and DS4)

User LED	MCU Pin
DS1	PG2
DS2	PG3
DS3	PG4
DS4	PG5

6.5. ADC Input Potentiometer (RVAR, RV1)

The ADC Pot is above the hex switch to the left of the GPIO matrix

There is a small variable resistor RV1 on the LCEVB which routes a voltage between 0v and 3.3 V to MCU pin PB4. This is useful for quick ADC testing. Test point RVAR can be used to probe the voltage with a voltmeter.

Note that this circuit provides a very rough way to evaluate the ADC. There is a small current limiting series resistor network to limit the injection current to around 4.4 mA.

7. MCU Port Pin LCEVB Functions

The table below shows what each MCU pin is used for on the LCEVB.

Table 7. LCEVB 176QFP Port Pin Functions

No	Port A	Port B	Port C	Port D	Port E	Port F	Port G	Port H
0	GPIO	CAN0	JTAG	GPIO [3]	---	GPIO	Ethernet	Ethernet
1	GPIO [2]	CAN0	JTAG	GPIO [3]	---	GPIO	Ethernet	Ethernet
2	GPIO [2]	LIN0	USB1	GPIO [3]	FlexRay A	GPIO	GPIO [4,]	Ethernet
3	Ethernet	LIN0	USB1	GPIO [3]	FlexRay A	GPIO	GPIO [4]	---
4	GPIO	ADC Pot	FlexRay B	GPIO	FlexRay B	GPIO	GPIO [4]	---
5	GPIO	GPIO	FlexRay A	GPIO	FlexRay B	GPIO	GPIO [4]	---
6	GPIO	GPIO	LIN1	GPIO	---	GPIO	GPIO	---
7	Ethernet	GPIO	LIN1	GPIO	---	GPIO	GPIO	---
8	Ethernet	EXTAL32	RS232	GPIO	---	GPIO	---	---
9	Ethernet	XTAL32	RS232	GPIO	---	GPIO	---	JTAG
10	Ethernet	SAI Audio	CAN1	GPIO	---	GPIO	USB1	JTAG
11	Ethernet	GPIO	CAN1		---	GPIO	USB1	USB1
12	GPIO	GPIO	FlexRay	GPIO	Ethernet	GPIO	Ethernet	USB1
13	GPIO	GPIO	FlexRay	GPIO	Ethernet	GPIO	Ethernet	---
14	GPIO	GPIO	FlexRay	GPIO	USB1	Ethernet	USB1	---
15	GPIO	GPIO	FlexRay	GPIO	USB1	Ethernet	USB1	---

No	Port I	Port J
0	GPIO	---
1	GPIO	---
2	GPIO	---
3	GPIO	---
4	USB1	---
5	USB1	
6	GPIO	
7	USB1	
8	GPIO	
9		
10		
11	Ethernet	
12	GPIO	
13	GPIO	
14	GPIO	
15	GPIO	

Key:	
	Pin not bonded out on 176QFP package
---	Pin not accessible on LCEVB

[2] Shared with user switches

[3] Shared with Hex Encoder Switch

[4] Shared with user LED's

8. Appendix

The MPC5748G LCEVB schematics, Rev B are shown below.

MPC5748G Low Cost Evaluation Board (MPC5748G-LCEVB)

Table Of Contents:

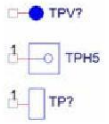
Revision Information

Rev	Date	Designer	Comments
x1	14 Apr 2015	Alasdair Robertson	Start of capture, Working version (256BGA)
x2	08 May 2015	Alasdair Robertson	Changed to 176 QFP Package and changed periperhal Matrix
x3	18 May 2015	Alasdair Robertson	Changes required for initial placement
x4	19 May 2015	Alasdair Robertson	Tidy Up, Replaced some "hard to source" components
x5	26 May 2015	Alasdair Robertson	Renumber and Back Annoted from Layout
x6	27 May 2015	Alasdair Robertson	Correction to GND on 3v3 Regulator circuit
x7	29 May 2015	Alasdair Robertson	Correction to CAN Test points
x8	31 May 2015	Alasdair Robertson	Few refdes changes after layout tweaks
x9	01 Jun 2015	Alasdair Robertson	Correction to user LED Refdes after re-number
x10	01 Jun 2015	Alasdair Robertson	DNP Jumpers. 0 Ohm resistors added accross LIN jumpers
A	11 Jun 2015	Andrew MacDonald	Prototype Manufacture Release
AX1	29 Sep 2015	Alasdair Robertson	Prodn Build changes (LIN0 default to Slave, LIN1 Master only) PN Changed to MPC5748G-LCEVB
AX2	26 Oct 2015	Alasdair Robertson	Change to JTAG Pulls to meet latest RM Spec
AX3	29 Oct 2015	Alasdair Robertson	Changed RV1 current limit resistor. SW4 / SW5 refdes swap
AX4	09 Dec 2015	Alasdair Robertson	Pull DOWN on TCLK to mitigate against STANDBY exit issue.
AX5	20 Jan 2016	Alasdair Robertson	Updated NXP Logos
B	12 Feb 2016	Alasdair Robertson	Updated NXP Logos

3 Different test points used in design:

TPVx - Through Hole Pad small
TPHx - Through Hile Pad Large (for standard 0.1" header).
Also used on IO Matrix (IOMx)

TPX - Surface Mount Wire Loop



Notes:

- All components and board processes are to be ROHS compliant
- All small capacitors are 0402 unless otherwise stated
- All resistors are 0603 5% 0.1w unless otherwise stated. All zero ohm links are 0603
- All connectors and headers are denoted Px and are 2.54mm pitch unless otherwise stated
- All jumpers are denoted Jx. Jumpers are 2mm pitch
  - Jumper default positions are shown in the schematics. For 3 way jumpers, default is always pcom 1-2.
  2 Pin jumpers generally have the "source" on pin 1.
- All switches are denoted SWx
  - All test points (SMT wire loop style) are denoted TPx
- Test point Vias (just through hole pads) are denoted TPVx

Signals (ports) have not been routed via busses as this makes it harder to determine where each signal goes.

User notes are given throughtout the schematics.
Specific PCB LAYOUT notes are detailed in ITALICS

Automotive Microcontroller Applications
East Kilbride, Scotland

NXP General Business Use

Designer: A. Robertson	Drawing Title: MPC5748G-LCEVB		
Drawn by: A. Robertson	Page Title: Index and Title Page		
Approved: A. Robertson	Size B	Document Number SCH-27897 PDF: SPF-27897	Rev B
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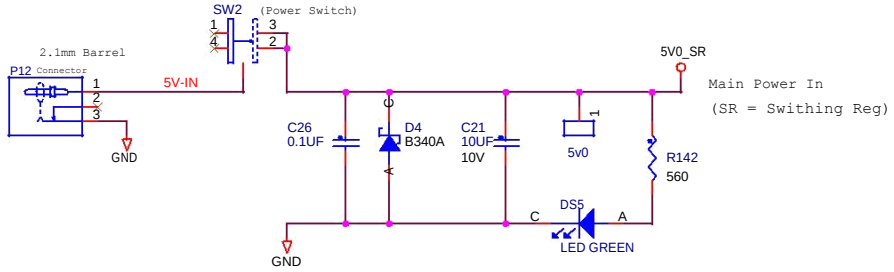
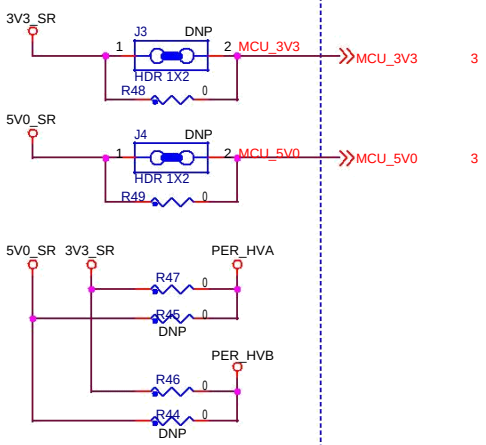
Power Input and Linear Voltage Regulators

Power Supply Input

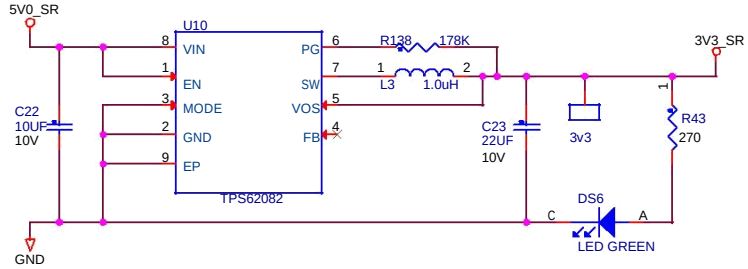


Power Control

Jumpers can be fitted to facilitate power measurements

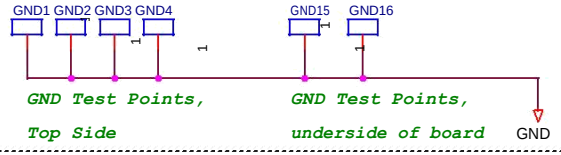


3.3v Switching Regulator



Inoput Voltage 5V, Output 3.3V at 700mA. Ripple 1.4mV, Approx 90% efficient

Test and reference points



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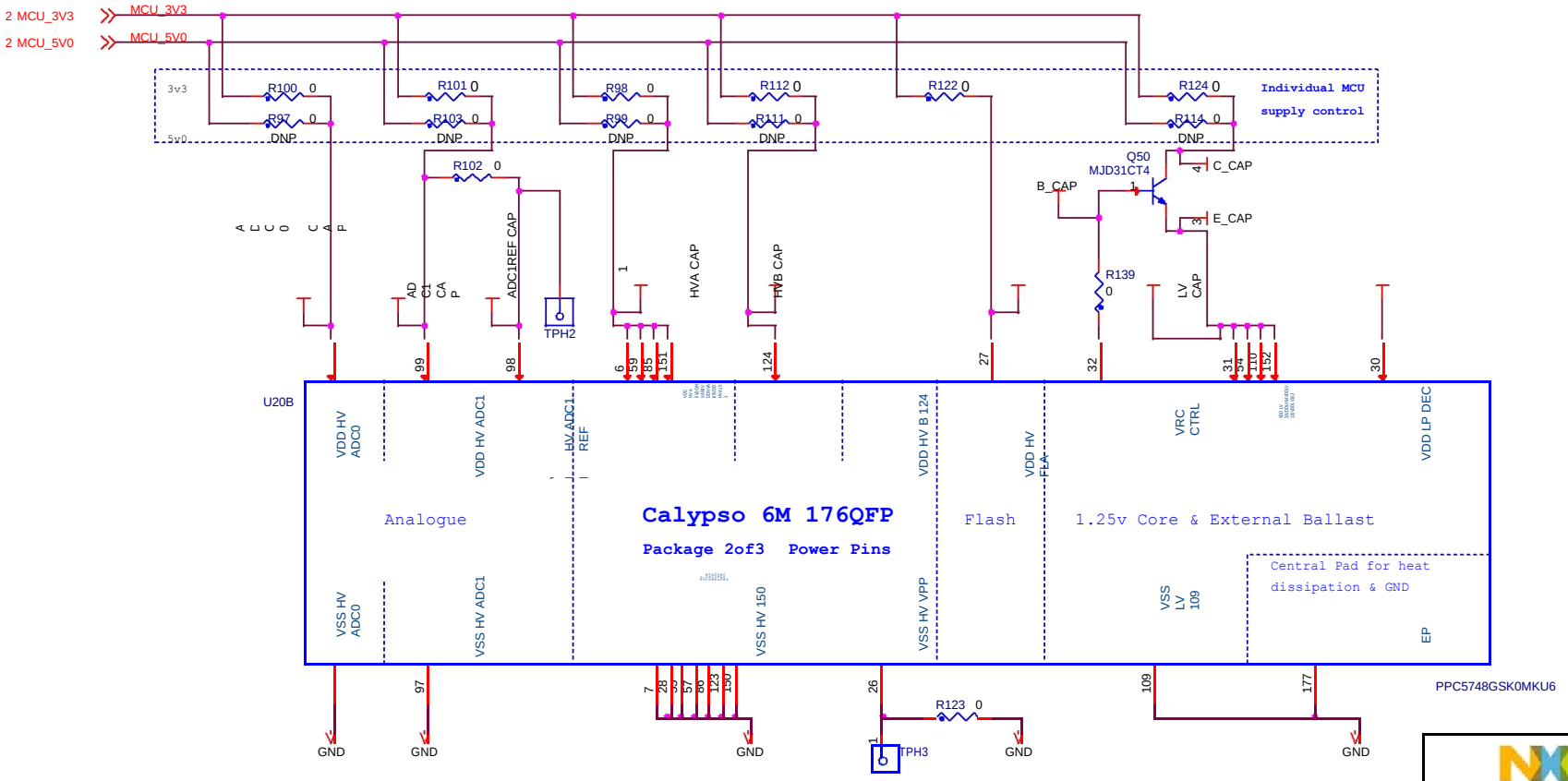
Calypso MCU Power Connections

Power Supply Contraints:
- If VDD HV A is driven from 3.3V, VDD HV FLA must also be supplied from 3.3V
- If VDD HV A is driven from 5V, the VDD HV FLA pin must be disconnected from 3.3V

- Don't attempt to over drive an analogue pad to 5V when the digital VDD HV x supply is set to 3.3V. This will trigger the ESD protectrion on that pad. For example if VDD HV A is set to 3.3V and the analogue supplies are set to 5V, you cannot drive 5V into a pad in the VDD_HV_A domain

Default Configuration:
- ALL MCU supply voltages are set to 3.3V (ADC0, ADC1, VDD HV A, VDD HV B, VDD HV C, VBallast)
- VDD_HV_FLA = External 3.3V supplied (jumper fitted)

The analogue pins can only be driven to the same voltage as the VDD HV x domain they are situated in (i.e. max 3.3V) so makes sense for the analogue supply and reference to be 3.3V



Notes on signal Grounds:

- The scheme shown has the analogue and digital grounds connected to the same plane
- This results in better ADC performance than using an analogue grond plane with single entry point (or ferrite) to digital ground plane.

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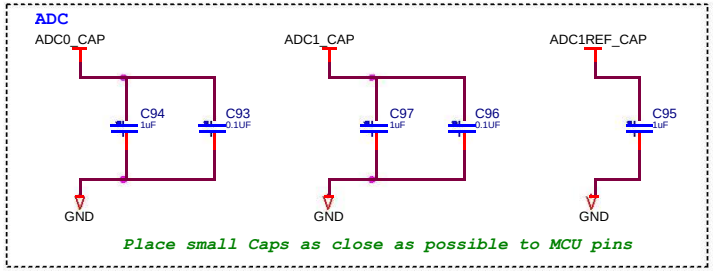
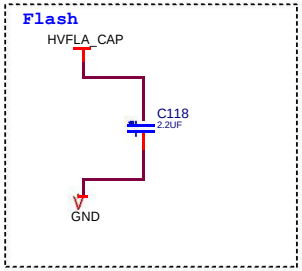
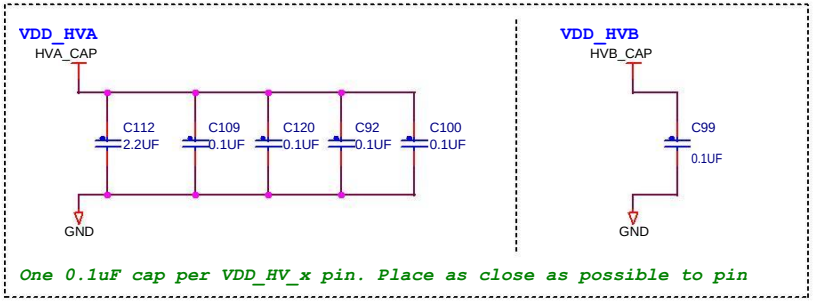
Calypso MCU Decoupling and bulk storage

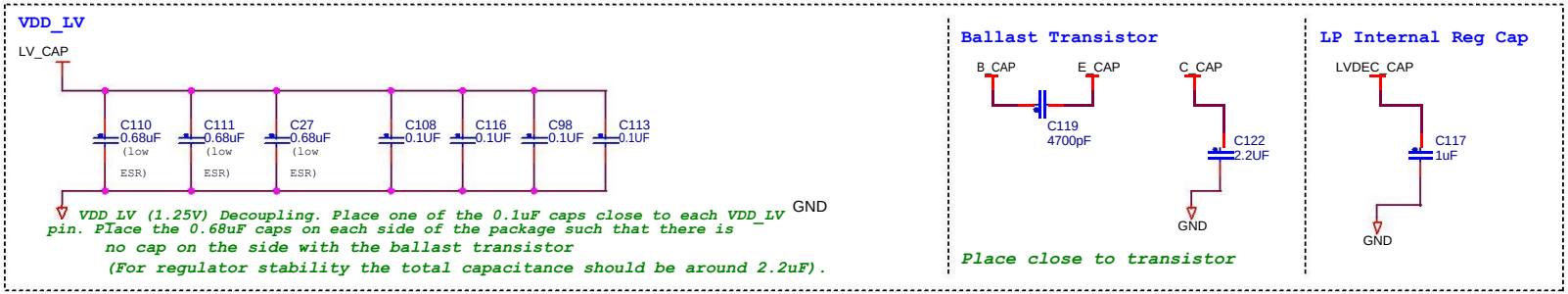




Capacitor Types:

4700pF - Ceramic X7R, 50V 10% 0402
0.1uF - Ceramic X7R, 16V 10% 0402 (Kemet C0402C104K4RAC)
0.68uF - Ceramic X7R, 16V 10% 0805 (Murata GCM219R71C684KA37)
2.2uF - Ceramic X7R, 10V 10% 0603 Low ESR (Taiyo Yuden LMK107B7225KA-TR)





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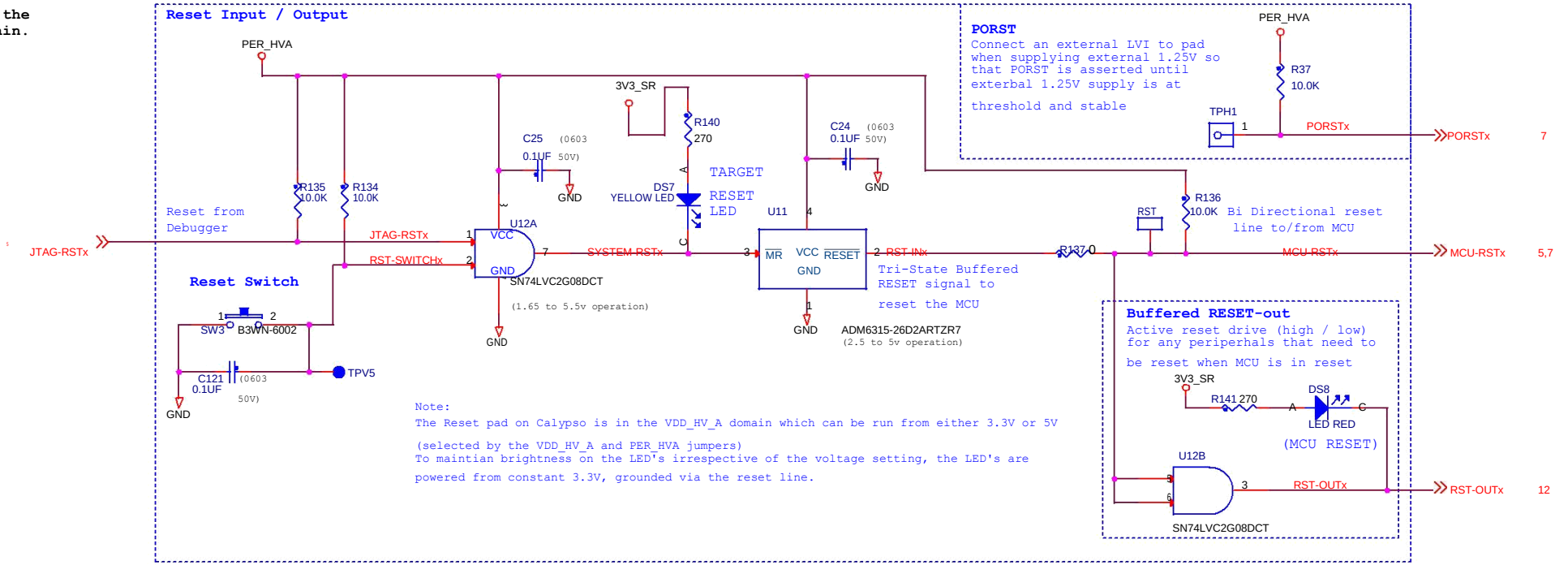
Reset and External Clock In

Reset is in the VDD_HVA domain.



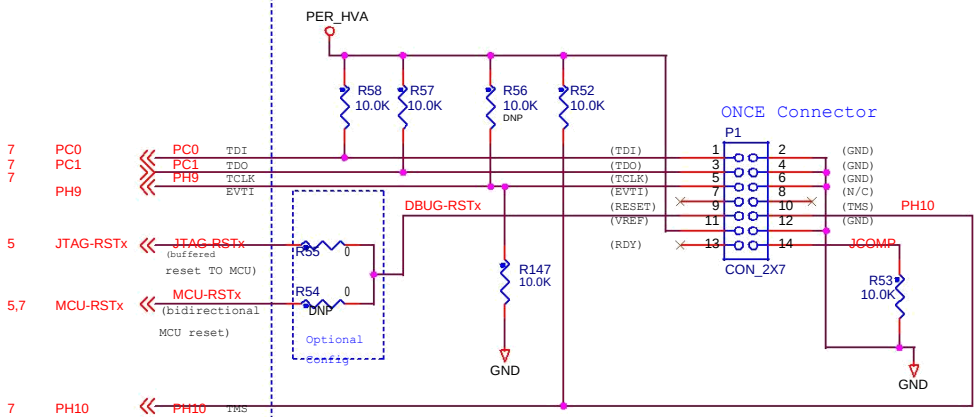


Table 13-3. Functional terminal state during power-up and reset

TERMINAL TYPE[1]	POWERUP pad state[2]	RESET pad state	DEFAULT pad state[3]	Comments
RESET	strong pull-down	strong pull-down	weak pull-up	functional reset pad.
PORST[4]	Weak pull down	Weak pull up	weak pull-up	power on reset pad.
GPIO	high impedance	high impedance	high impedance	by default, but configurable for STANDBY exit
ANALOG	high impedance	high impedance	high impedance	-
ECUT0, ECUT1	high impedance	high impedance	high impedance	
TCK	high impedance	weak pull-up	weak pull-up	-
TMS	high impedance	weak pull-up	weak pull-up	-
TDI	high impedance	weak pull-up	weak pull-up	-
TDO	high impedance	high impedance	high impedance	-
TCK_ALT	high impedance	weak pull-up	weak pull-up	-
TMS_ALT	high impedance	weak pull-up	weak pull-up	-
TDI_ALT	high impedance	weak pull-up	weak pull-up	-
TDO_ALT	high impedance	high impedance	high impedance	-

Note TCLK needs to be pulled down to allow exit from STANDBY in some corner cases

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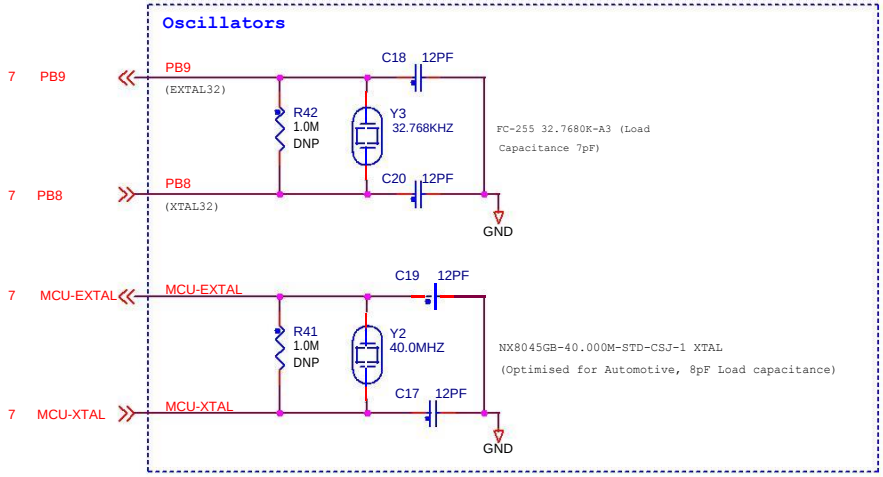
Clocks



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Calypso GPIO 1 of 2

U20A

Calypso 176QFP

Package 1of3 GPIO Pins1

Key to text colours:

- Purple - Comms Physical Interfaces
- Orange - Other Peripherals and I/O
- Blue - Debug (JTAG & Nexus)
- Black - Clock, Reset and Control
- RED - I/O Matrix and other functions (eg LED)

PA 12..15 has SPI

PD has ADC0 and ADC1

PPC5748GSK0MKU6

(WKPU2 / NMI0)	15	PA0	(GPIO)	PA0	24								
(WKPU3)	14,15	PA2	(SW1 & GPIO**)	PA1	19	PA0							
			(SW2 & GPIO)	PA2	17	PA2							
			(MII_RXCLK)	PA3	114								
	12	PA3	(GPIO)	PA4	51	PA3							
	15	PA5	(GPIO)	PA5	146	PA5	PE5						
	15	PA6	(GPIO)	PA6	147	PA6	PE6	167					
	12	PA7	(MII_RXD2)	PA7	128	PA7	PE7	168					
	12	PA8	(RMII_RXD1)	PA8	129	PA8	PE8	21					
	12	PA9	(RMII_RXD0)	PA9	130	PA9	PE9	22					
	12	PA10	(MII_COL)	PA10	131	PA10	PE10	23					
	12	PA11	(RMII_RXER)	PA11	132	PA11	PE11	25					
	15	PA12	(GPIO)	PA12	53			133	PE12	(MII_CRS)			
			(GPIO)	PA13	52	PA12	PE12	127	PE13	(MII_RXD3)	PE12	12	
			(GPIO)	PA14	50			136	PE14	(USB1_D2)			
	15	PA15	(GPIO)	PA15	48	PA15	PE15	137	PE15	(USB1_D3)	PE15	11	
	9	PB0	(CAN0_TX)	PB0	39	PB0	PF0	63	PF0	(GPIO)	PF0	15	
	9	PB1	(CAN0_RX)	PB1	40	PB1	PF1	64	PF1	(GPIO)	PF1	15	
	9	PB2	(LIN0_TX)	PB2	176	PB2	PF2	65	PF2	(GPIO)	PF2	15	
	9	PB3	(LIN0_RX)	PB3	1	PB3	PF3	66	PF3	(GPIO)	PF3	15	
			(ADC_POT)	PB4	88			67	PF4	(GPIO)			
	14	PB4	(GPIO)	PB5	91	PB4	PF4	68	PF5	(GPIO)	PF4	15	
			(GPIO)	PB6	92			69	PF6	(GPIO)			
			(GPIO)	PB7	93			70	PF7	(GPIO)			
	15	PB7	(XTAL32)	PB8	61	PB7	PF7	42	PF8	(GPIO)	PF7	15	
			(EXTAL32)	PB9	60			41	PF9	(GPIO)			
			(GPIO)	PB10	62			46	PF10	(GPIO)			
	15	PB10	(GPIO)	PB11	96	PB10	PF10	47	PF11	(GPIO)	PF10	15	
			(GPIO)	PB12	101			43	PF12	(GPIO)			
	15	PB12	(GPIO)	PB13	103	PB12	PF12	49	PF13	(GPIO)	PF12	15	
			(GPIO)	PB14	105			126	PF14	(RMII_MDIO)			
	15	PB15	(GPIO)	PB15	107	PB15	PF15	125	PF15	(RMII_RXDV)	PF15	12	
	5	PC0	(TDI)	PC0	154			122	PG0	(RMII_MDC)			
			(TDO)	PC1	149	PC0	PG0	121	PG1	(RMII_TXCLK)	PG0	12	
			(USB1_CLK)	PC2	145			16	PG2	(LED1 & GPIO)			
			(USB1_DIR)	PC3	144			15	PG3	(LED2 & GPIO)			(eMIOS E1UC_11_H)
			(FR_B_TX_EN)	PC4	159			14	PG4	(LED3 & GPIO)			
	13	PC4	(FR_A_TX)	PC5	158	PC4	PG4	13	PG5	(LED4 & GPIO)	PG4	14	(eMIOS E1UC_13_H)
	9	PC6	(LIN1_TX)	PC6	44	PC6	PG6	38	PG6	(CLKOUT1 GPIO)			1 PG6
	9	PC7	(LIN1_RX)	PC7	45	PC7	PG7	37	PG7	(CLKOUT0 GPIO)			
	10	PC8	(MSEO1_B0)	PC8	175	PC8	PG8	34					
			(MSEO1_B1)	PC9	2			33					1 PG7
	10	PC9	(CAN1_TX)	PC10	36	PC9	PG9	138	PG10	(USB1_D4)			
			(CAN1_RX)	PC11	35			139	PG11	(USB1_D5)		11	
			(FR_DBG0)	PC12	173			116	PG12	(MII_TXD2)			
			(FR_DBG1)	PC13	174			115	PG13	(MII_TXD3)			
			(FR_DBG2)	PC14	3			134	PG14	(USB1_D0)			
	13	PC14	(FR_DBG3)	PC15	4	PC14	PG14	135	PG15	(USB1_D1)	PG14	11	
	14,15	PD0	(HEX1 & GPIO)	PD0	77	PD0	PH0	117	PH0	(RMII_TXD1)	PH0	12	
	14,15	PD1	(HEX2 & GPIO)	PD1	78	PD1	PH1	118	PH1	(RMII_TXD0)	PH1	12	
			(HEX3 & GPIO)	PD2	79			119	PH2	(RMII_TXEN)			
			(HEX4 & GPIO)	PD3	80			120					
	15	PD4	(GPIO)	PD4	81	PD4	PH4	162					
	15	PD5	(GPIO)	PD5	82	PD5	PH5	163					
			(GPIO)	PD6	83			164					
	15	PD6	(GPIO)	PD7	84	PD6	PH6	165					
	15	PD8	(GPIO)	PD8	87	PD8	PH8	166					
	15	PD9	(GPIO)	PD9	94			155	PH9	(TCK)			
			(GPIO)	PD10	95	PD9	PH9	148	PH10	(TMS)	PH9	5	
								140	PH11	(USB1_D6)			
			(GPIO)	PD12	100		PH11	141	PH12	(USB1_D7)	PH11	11	
			(GPIO)	PD13	102			9					
			(GPIO)	PD14	104			10					
			(GPIO)	PD15	106			8					
	15	PD15				PD15	PH15						
	5	MCU-RSTx		MCU-RSTx	29								
	5	PORSTx		PORSTx	153	PORST							
	6	MCU-XTAL		MCU-XTAL	56	XTAL							
	6	MCU-EXTAL		MCU-EXTAL	58	EXTAL							

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Calypso GPIO 2 of 2

Key to text colours:
Purple - Comms Physical Interfaces
Orange - Other Peripherals and I/O
Blue - Debug (JTAG & Nexus)
Black - Clock, Reset and Control
RED - I/O Matrix and other functions (eg LED)
Green - I/O Matrix (dedicated)

U20C

Calypso 176QFP

Package 3of3 GPIO Pins2

15	PI0	(GPIO)	PI0	172	PI0
15	PI1	(GPIO)	PI1	171	PI1
15	PI2	(GPIO)	PI2	170	PI2
15	PI3	(GPIO)	PI3	169	PI3
11	PI4	(USB1 STP)	PI4	143	PI4
11	PI5	(USB1 NXT)	PI5	142	PI5
15	PI6	(GPIO)	PI6	11	PI6
11	PI7	(USB1 RST)	PI7	12	PI7
15	PI8		PI8	108	PI8
12	PI11	(ENET RST)	PI11	111	PI11
15	PI12	(GPIO)	PI12	112	PI12
15	PI13	(GPIO)	PI13	113	PI13
15	PI14	(GPIO)	PI14	76	PI14
15	PI15	(GPIO)	PI15	75	PI15
				74	
				73	PJ0
				72	PJ1
				71	PJ2
				5	PJ3
					PJ4

PPC5748GSK0MKU6

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CAN & LIN Physical

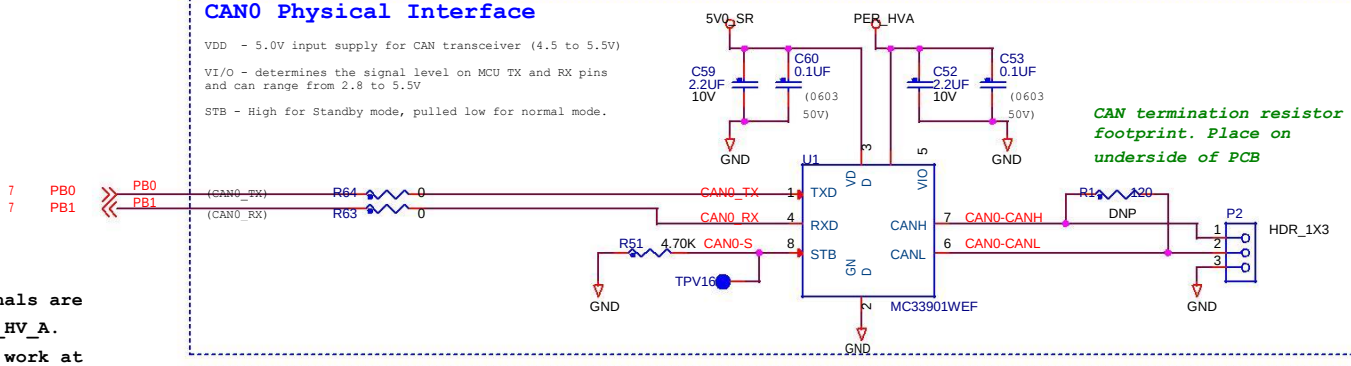
All CAN and LIN signals are in power domain VDD_HV_A.
All interfaces will work at 3.3V or 5.0V (PER_HVA)

CAN0 Physical Interface

VDD - 5.0V input supply for CAN transceiver (4.5 to 5.5V)

VI/O - determines the signal level on MCU TX and RX pins and can range from 2.8 to 5.5V

STB - High for Standby mode, pulled low for normal mode.



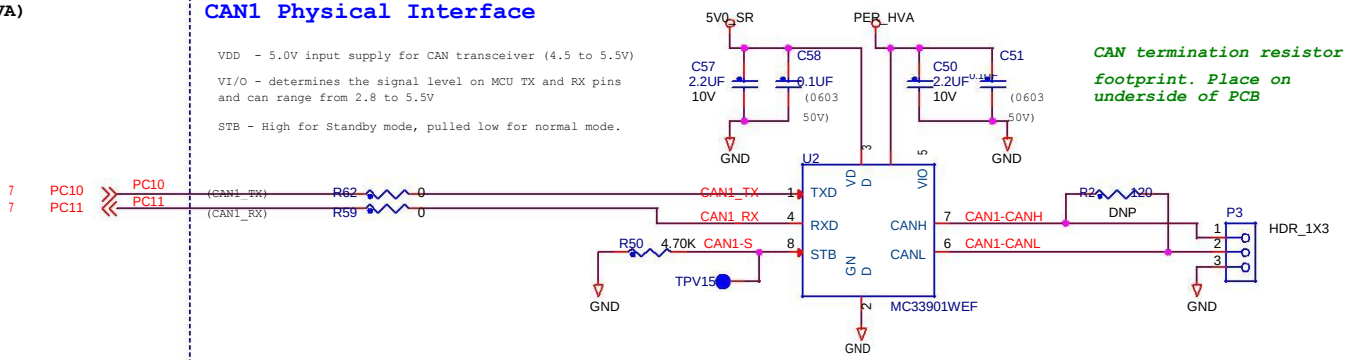
CAN termination resistor footprint. Place on underside of PCB

CAN1 Physical Interface

VDD - 5.0V input supply for CAN transceiver (4.5 to 5.5V)

VI/O - determines the signal level on MCU TX and RX pins and can range from 2.8 to 5.5V

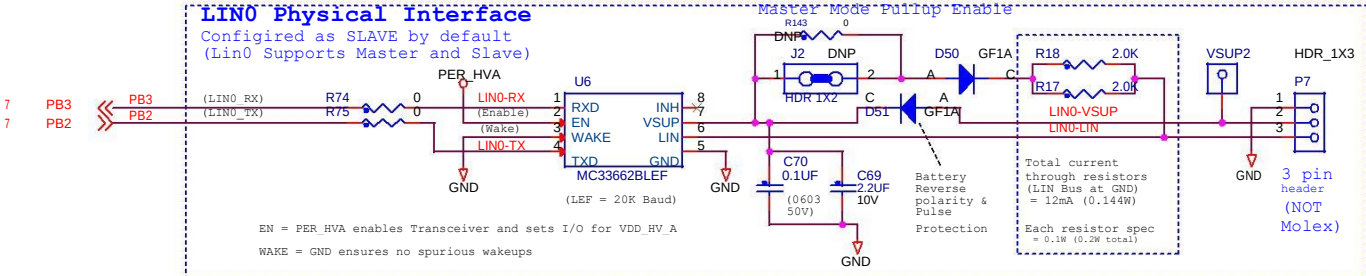
STB - High for Standby mode, pulled low for normal mode.



CAN termination resistor footprint. Place on underside of PCB

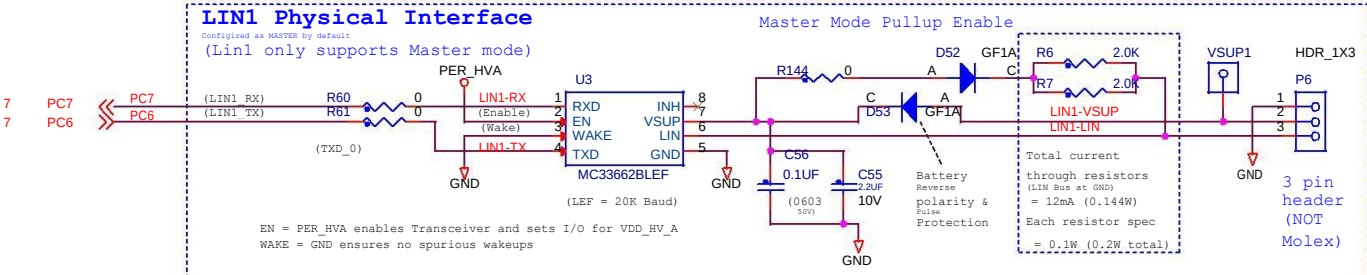
LIN0 Physical Interface

Configured as SLAVE by default
(Lin0 Supports Master and Slave)



LIN1 Physical Interface

Configured as MASTER by default
(Lin1 only supports Master mode)



MC33662LEF LIN transceiver is newer version of 33661 offering:

- Full LIN compliance (33661 no longer compliant)
- Improved ESD protection on LIN pin up to 15KV
  - Improved ESD on Wake and VSUP Pins
- Other EMC and performance improvements

See freescale.com for more details

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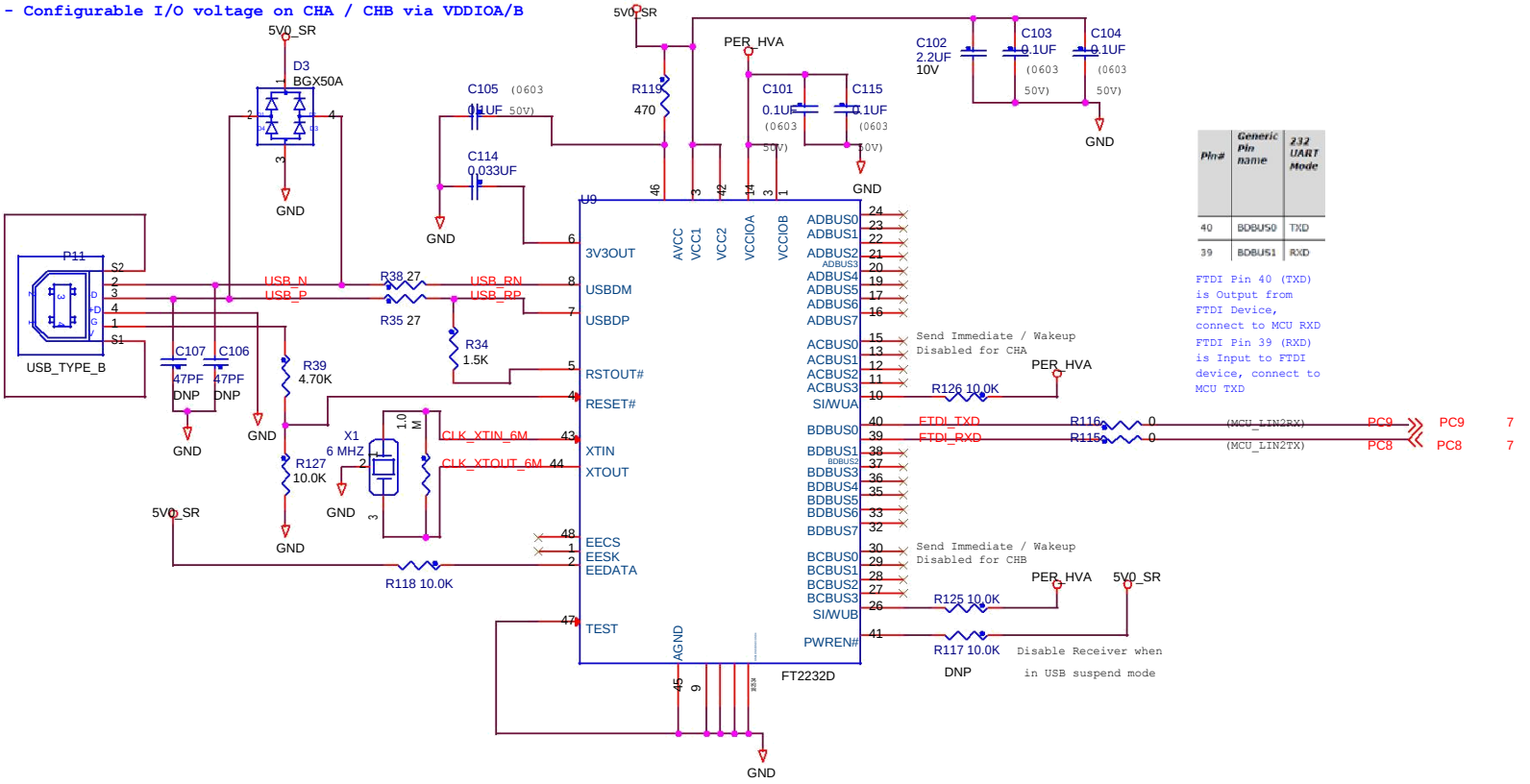
USB RS232 (serial) Interface

All Signals are in power domain VDD_HV_A.
FTDI interface will work at 3.3V or 5.0V (PER_HVA)

FTDI USB <-> Serial Interface

- Self Powered mode. No power is taken from USB
- Device efaults to Dual serial (RS232) mode i.e. RS232 on both A and B
- Configurable I/O voltage on CHA / CHB via VDDIOA/B



Pin#	Generic Pin name	232 UART Mode
40	BDBUS0	TXD
39	BDBUS1	RXD

FTDI Pin 40 (TXD) is Output from FTDI Device, connect to MCU RXD
FTDI Pin 39 (RXD) is Input to FTDI device, connect to MCU TXD

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USB (Type A Host and Type AB OTG)

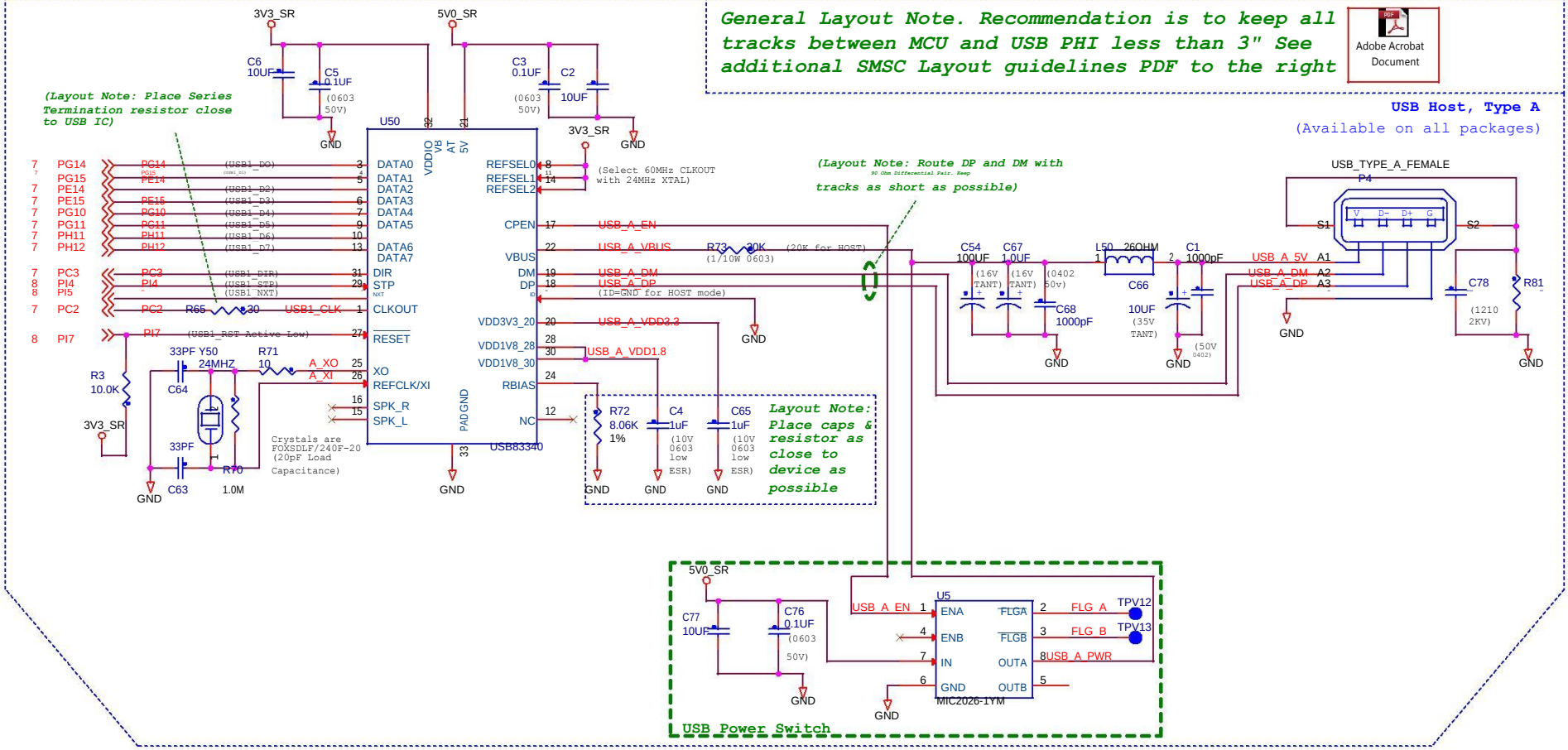
USB Signals are in power domain VDD_HV_A

The USB interface only supports 3.3V operation. All I/O signals must be 3.3V. If VDD_HVA is set to 5V, USB MCU pads must be left as tri-state with no pullups.

General Layout Note. Recommendation is to keep all tracks between MCU and USB PHI less than 3" See additional SMSC Layout guidelines PDF to the right

Adobe Acrobat Document

USB Host, Type A
(Available on all packages)



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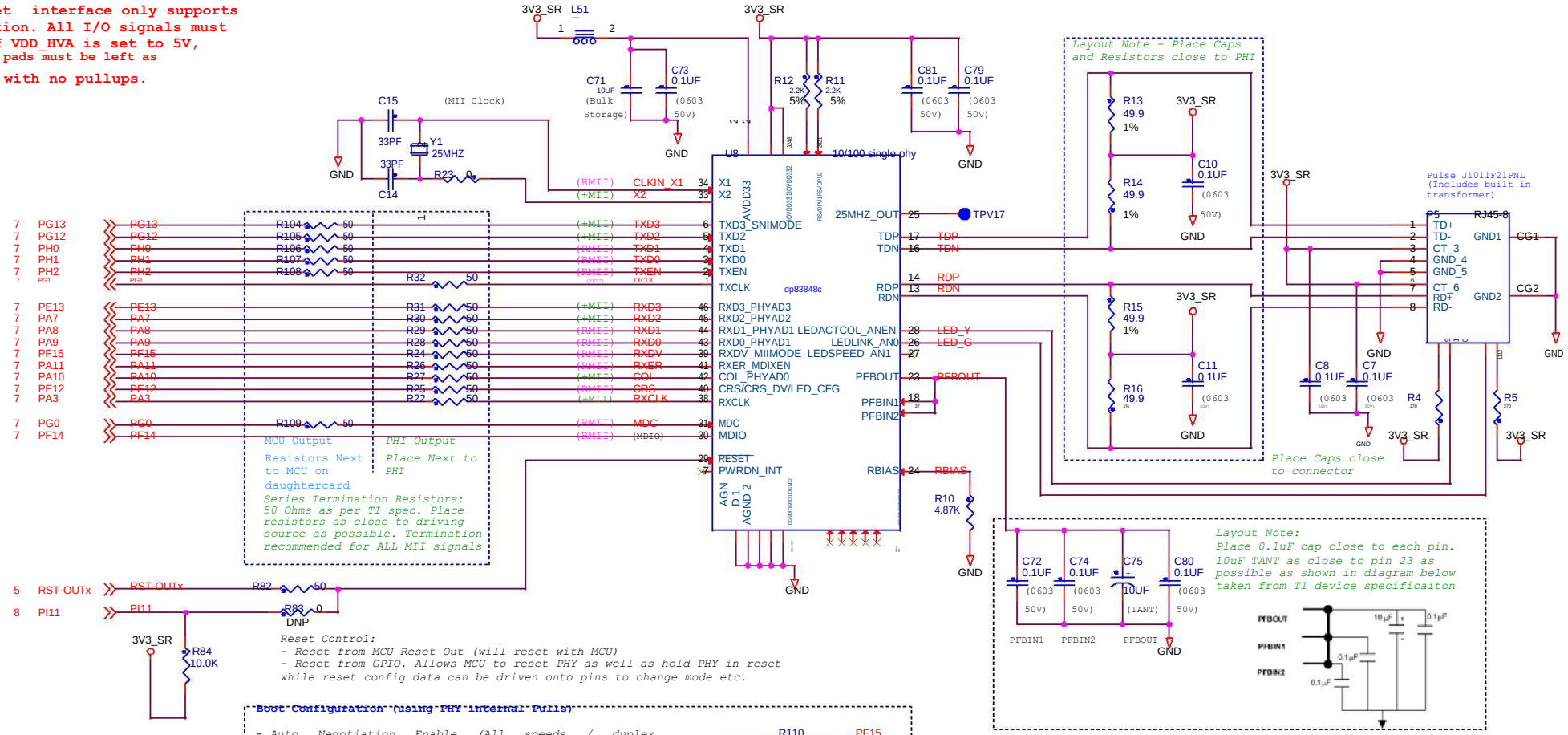
Ethernet (Configured for MII Mode)

All Ethernet Signals are in power

domain VDD_HV_B

The Ethernet interface only supports 3.3V operation. All I/O signals must be 3.3V. If VDD_HVA is set to 5V, Ethernet MCU pads must be left as tri-state with no pullups.



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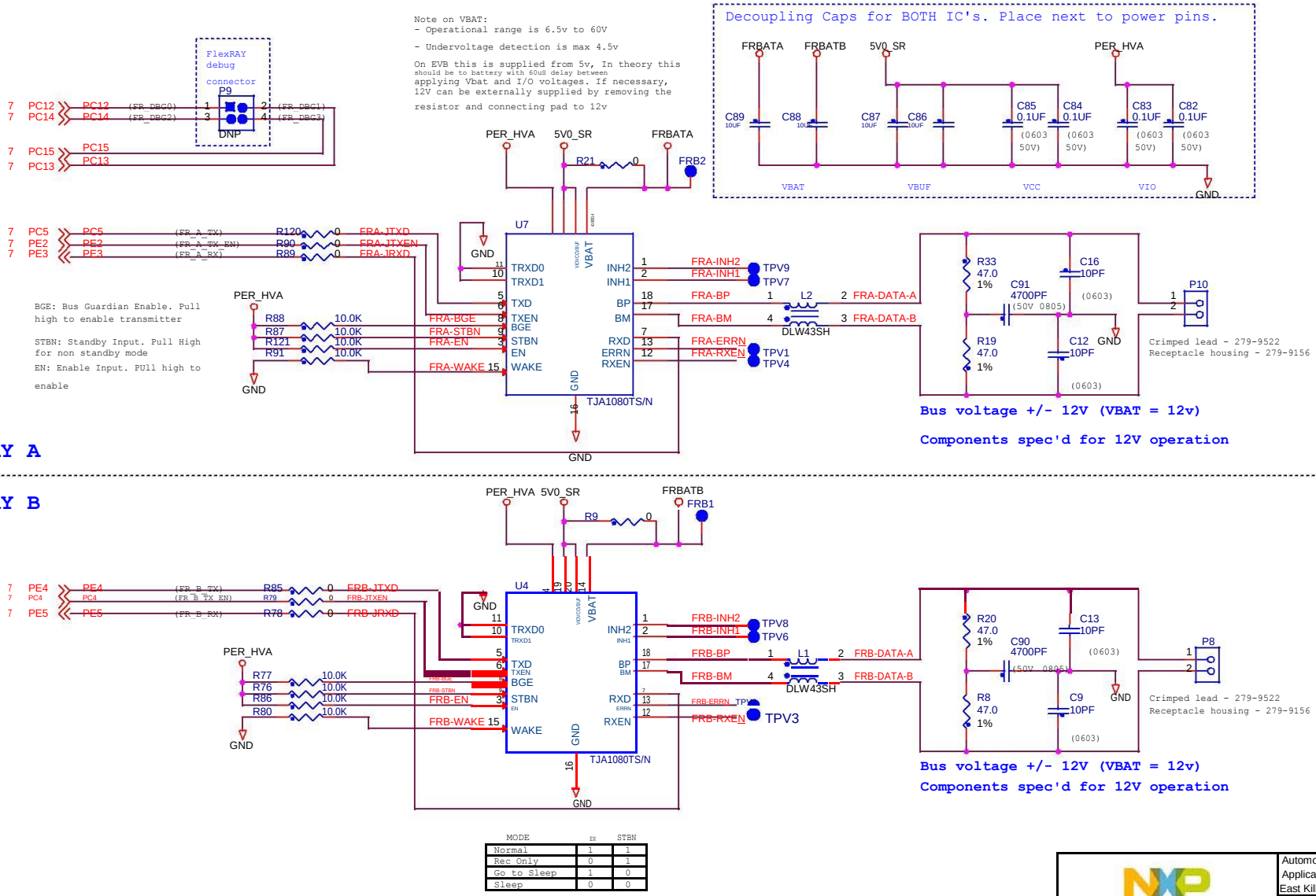
FlexRAY Physical Interface

All Signals are in power domain VDD_HV_A.

FlexRAY interface will work at 3.3V or 5.0V (PER_HVA)



MODE	EN	STBN
Normal	1	1
Rec Only	0	1
Go to Sleep	1	0
Sleep	0	0

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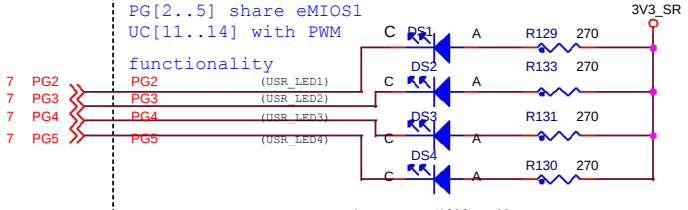
User Peripheralls (Led's, Switches and ADC Pot)

Switches are hard wired to 3.3V rather than 5V so it's not possible to drive 5V into a 3.3V pad (which would cause damage)
Similarly, the LED's are active low with 3.3v supply so can be safely coupled to pads on either 3.3V or 5V domains
The ADC input is limited to 3.3V, again to prevent driving 5V into a 3.3V pad which would cause damage

User LED's (Active Low)

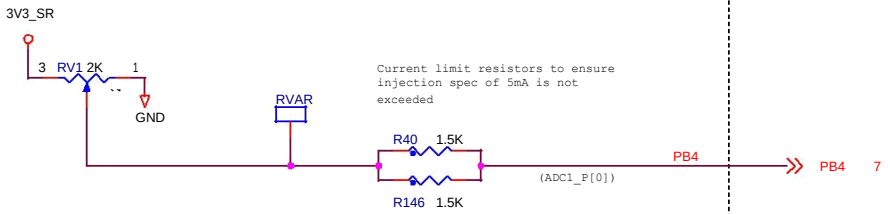
PG[2..5] share eMIOS1
UC[11..14] with PWM

functionality

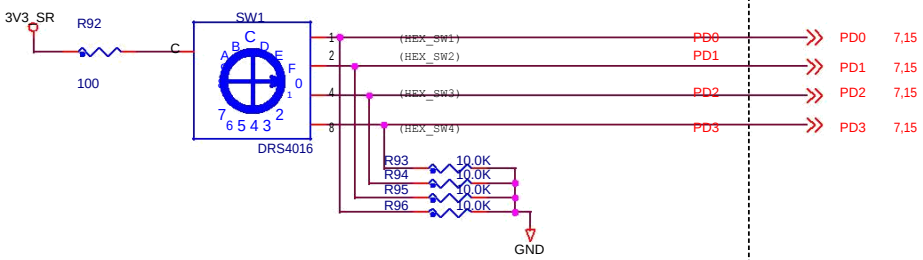


Note that LED2 and LED4 (PG3 and PG5) can be controlled in LPU RUN mode (and also have pad keepers in LPU_STANDBY)

ADC Input Pot and Test Point

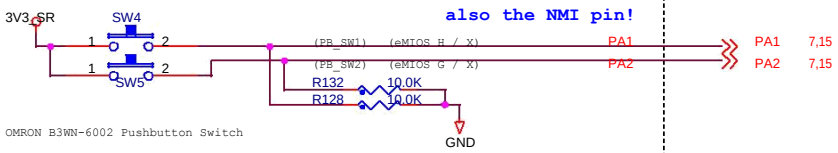


Hex Encoded Switch (Active High)



User Pushbutton Switches (Active High)

Note - PA1 is also the NMI pin!



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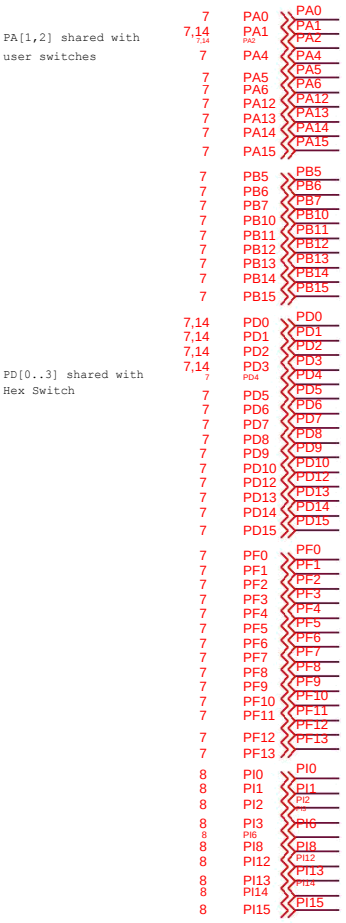
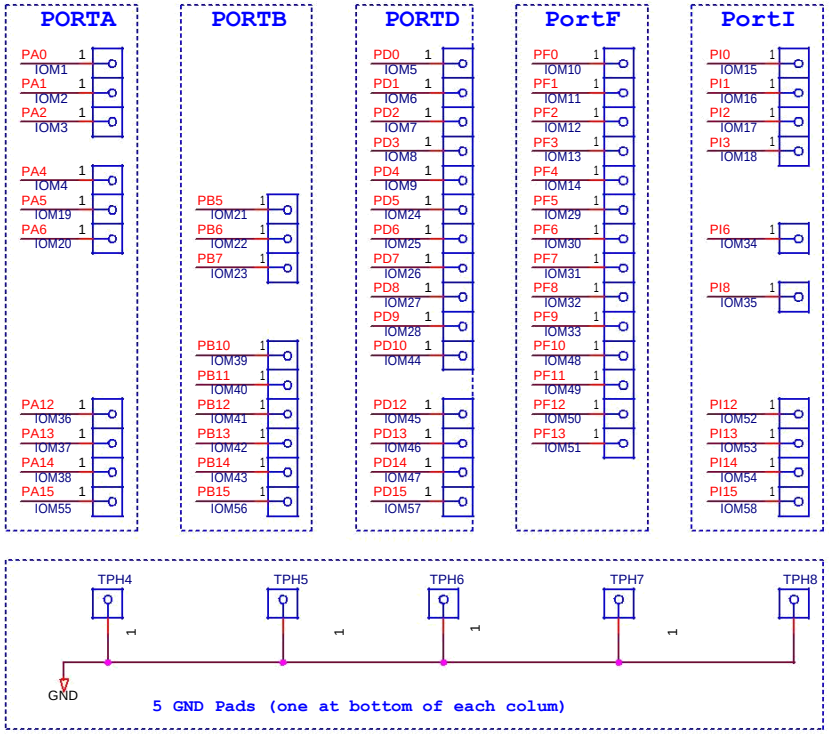
GPIO Pin Matrix

All pads are DNP (Do Not Populate) 0.1" pitch headers placed on a 0.1" grid

PA[1,2] shared with user switches

PD[0..3] shared with Hex Switch





Layout Notes:

Pads must be placed in a 5 (W) x 16(H) matrix pattern, 2.54 mm pitch

- *one column for each port*
- *16 tall (1 row for each port number from 0 to 15).*
- *GND pad at bottom of each colum*
- *After production, pads should be through hole (not solder filled)*

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9. Revision History

Date	Substantial changes
March 2016	Initial release
August 2016	Rev. 1: Updated Schematics and Board Pictures

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