LX2162A

Layerscape LX2162A/LX2122A/LX2082A Data Sheet

Rev. 1 — 08/2021

Data Sheet: Technical Data

- Arm® Cortex®-A72 cores:
  - Up to 2.0 GHz
  - Single-threaded cores with 48 KB L1 instruction cache and 32 KB L1 data cache
- Cache Coherent Interconnect Fabric
  - Up to 1300 MHz
  - 8 MB Level 3 cache with ECC and On-Chip Memory (OCM) mode
- One 72-bit (64-bit + ECC) 2.9 GT/s DDR4 SDRAM memory controllers
- Datapath acceleration architecture 2.0 (DPAA2)
  - Packet parsing, classification, and distribution (WRIOP)
  - Queue and Hardware buffer management
  - Cryptography acceleration (SEC) at up to 50 Gbps
  - Decompression/compression acceleration (DCE) at up to 88 Gbps
  - Queue Direct Memory Access (QDMA) engine
  - Management Complex (MC)
  - 2 MB Packet Express Buffer
  - L2 Switching (105 Gbps)
- 12 SerDes lanes at up to 25 Gbps
- 3x PCIe Gen3 controllers: x8, x4, x4
- Ethernet interfaces supporting IEEE 1588
  - Up to 14 Ethernet MACs
  - Support for 10G-SXGMII (USXGMII)
  - Support for SGMII (and 1000Base-KX)
  - Support for XFI, SFI, and 10GBase-KR
  - Support for 50GAUI-2 (50G) and 25GAUI (25G)
  - Support for XLAUI (and 40GBase-KR4) for 40G
  - Support for two RGMII parallel interfaces
- Additional peripheral interfaces
  - One USB 3.0 controller with integrated PHY
  - Two enhanced secure digital host controllers
  - Two Controller Area Network (CAN) modules, optionally supporting Flexible Datarate
  - Flexible Serial Peripheral Interface (FlexSPI) and three Serial Peripheral Interface (SPI) controllers
  - Eight I2C controllers
  - Four UARTs
  - Up to 101 General Purpose IOs (GPIO)
- Support for hardware virtualization and partitioning enforcement (Arm MMU-500)
- Global interrupt controller (Arm GIC-500)
- QorIQ platform trust architecture 3.0 with 256 KB on-chip RAM for trusted accesses
- Two Flextimers, one secure watchdog timer and one non-secure watchdog timer
- Debug supporting run control, data acquisition, high-speed trace, and performance/event monitoring
- Support for Voltage ID (VID) for yield improvement

Contents

1 Introduction

The QorIQ LX2162A processor is built on NXP's software-aware, core-agnostic DPAA2 architecture, which delivers scalable acceleration elements sized for application needs, unprecedented efficiency, and smarter, more capable networks. When coupled with ease-of-use facilities such as real-time monitoring and debug, virtualization, and software management utilities, the available toolkits allow for both hardware and software engineers to bring a complete solution to market faster than ever.

The device integrated multicore processor combines sixteen Arm Cortex®-A72 processor cores with high-performance data path acceleration logic and network and peripheral bus interfaces required for networking, storage, telecom/datacom, wireless infrastructure, and mil/aerospace applications.

The device processor is supported by a consistent API that provides both basic and complex manipulation of the hardware peripherals in the device, releasing the developer from the classic programming challenges of interfacing with new peripherals at the hardware level.

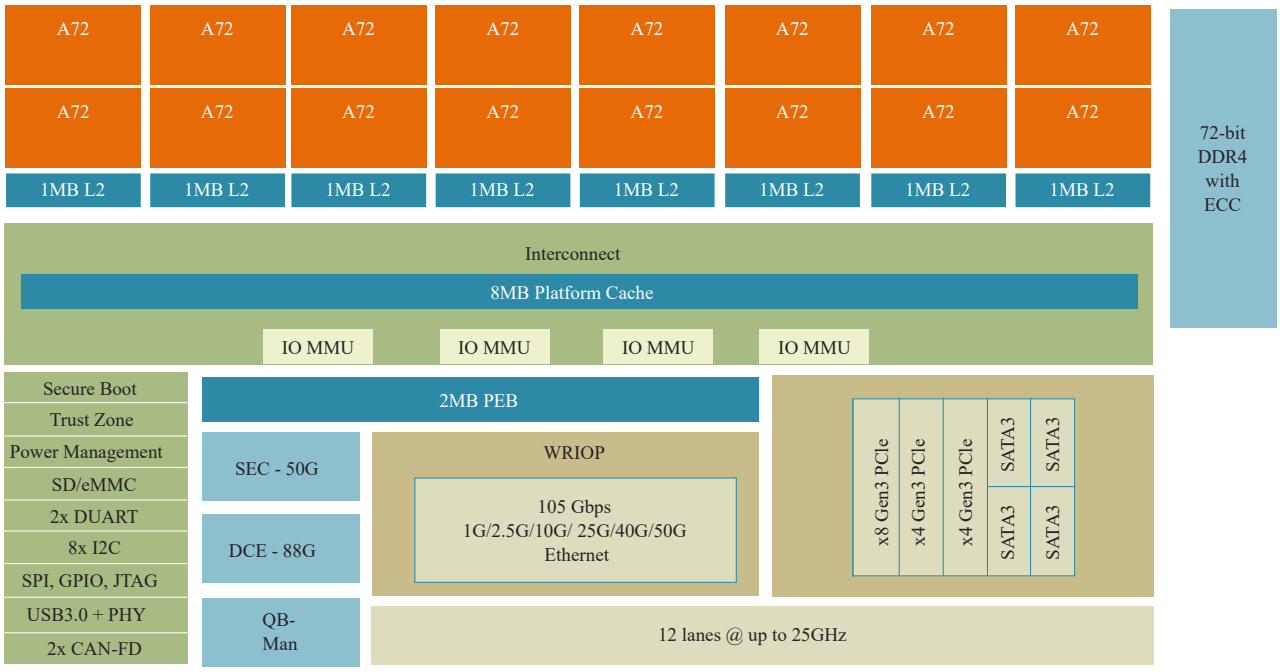


Figure 1. LX2162A Block diagram

The LX2122A integrated multicore processor combines twelve Arm® v8 A72 cores. This figure shows the major functional units within the chip.

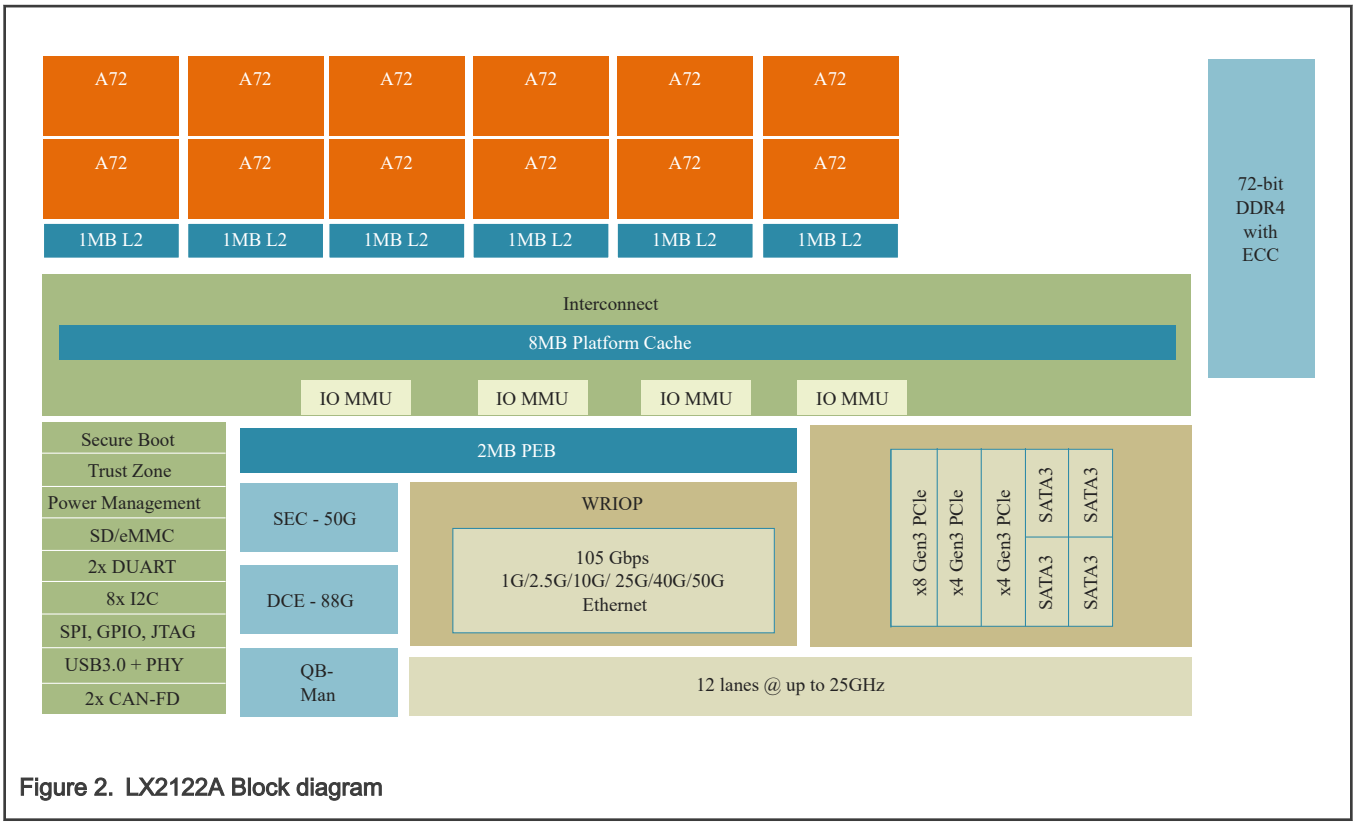


Figure 2. LX2122A Block diagram

The LX2082A integrated multicore processor combines eight Arm® v8 A72 cores. This figure shows the major functional units within the chip.

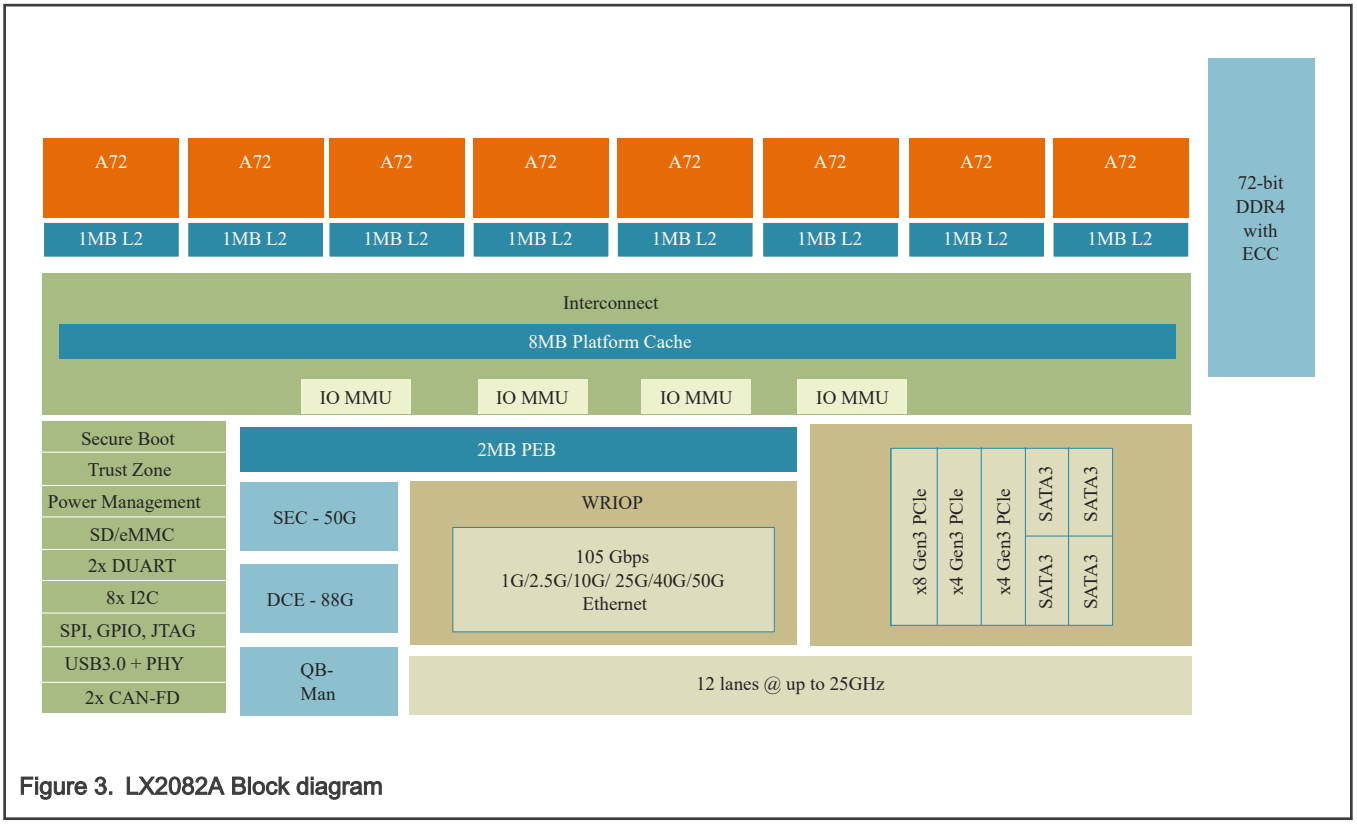


Figure 3. LX2082A Block diagram

1.1 Device selection

This table shows how to set the TEST_SEL_B and the cfg_svr[0:1] pins at power-on-reset to select between LX2162A, LX2122A, and LX2082A.

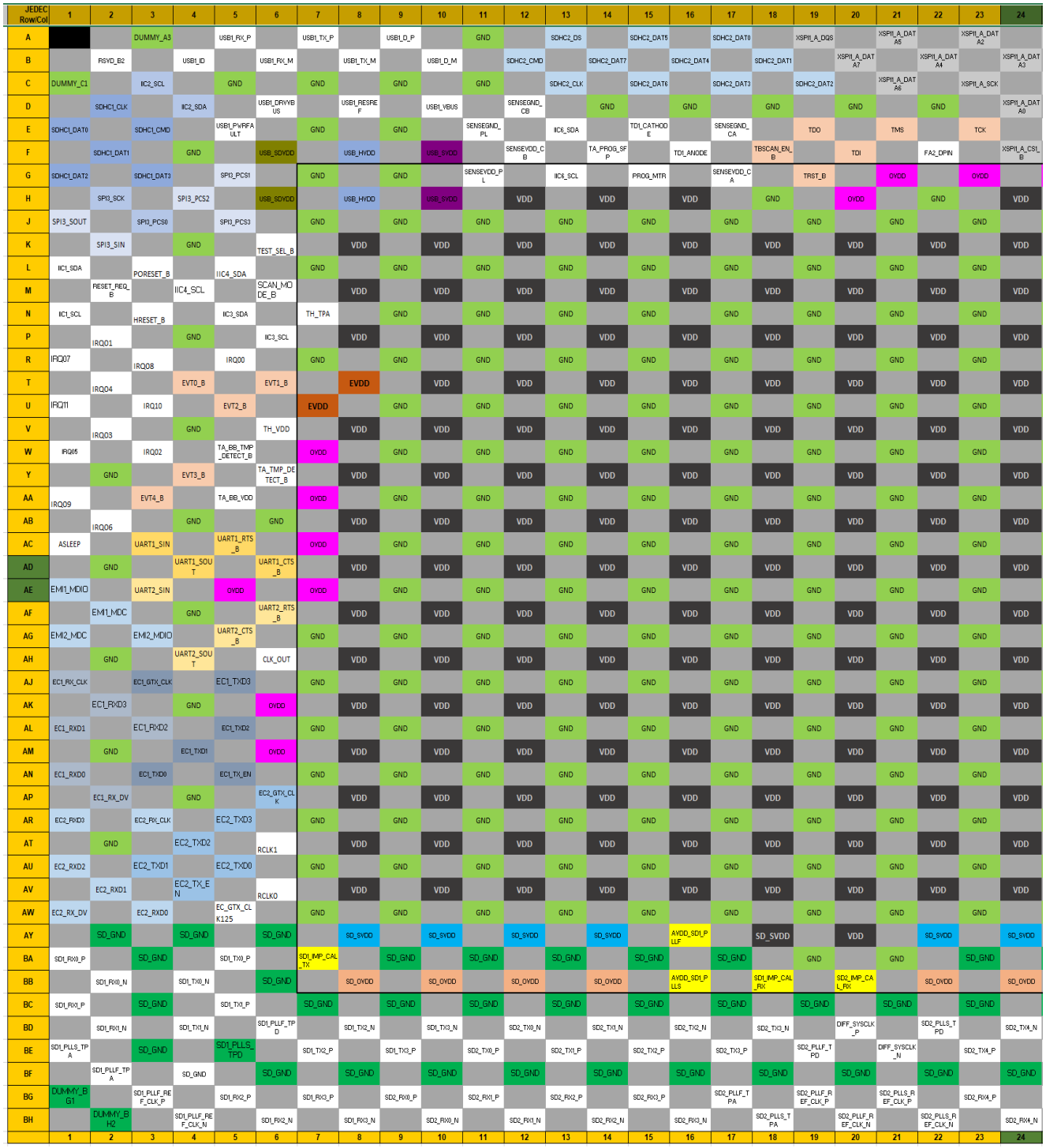
Table 1. Device Personality Selection

Personality	TEST_SEL_B	cfg_svr0 (primary signal XSPI1_A_CS0_B)	cfg_svr1 (primary signal XSPI1_A_CS1_B)
LX2162A	1	1	1
LX2122A	0	1	1
LX2082A	1	0	1

2 Pin assignments

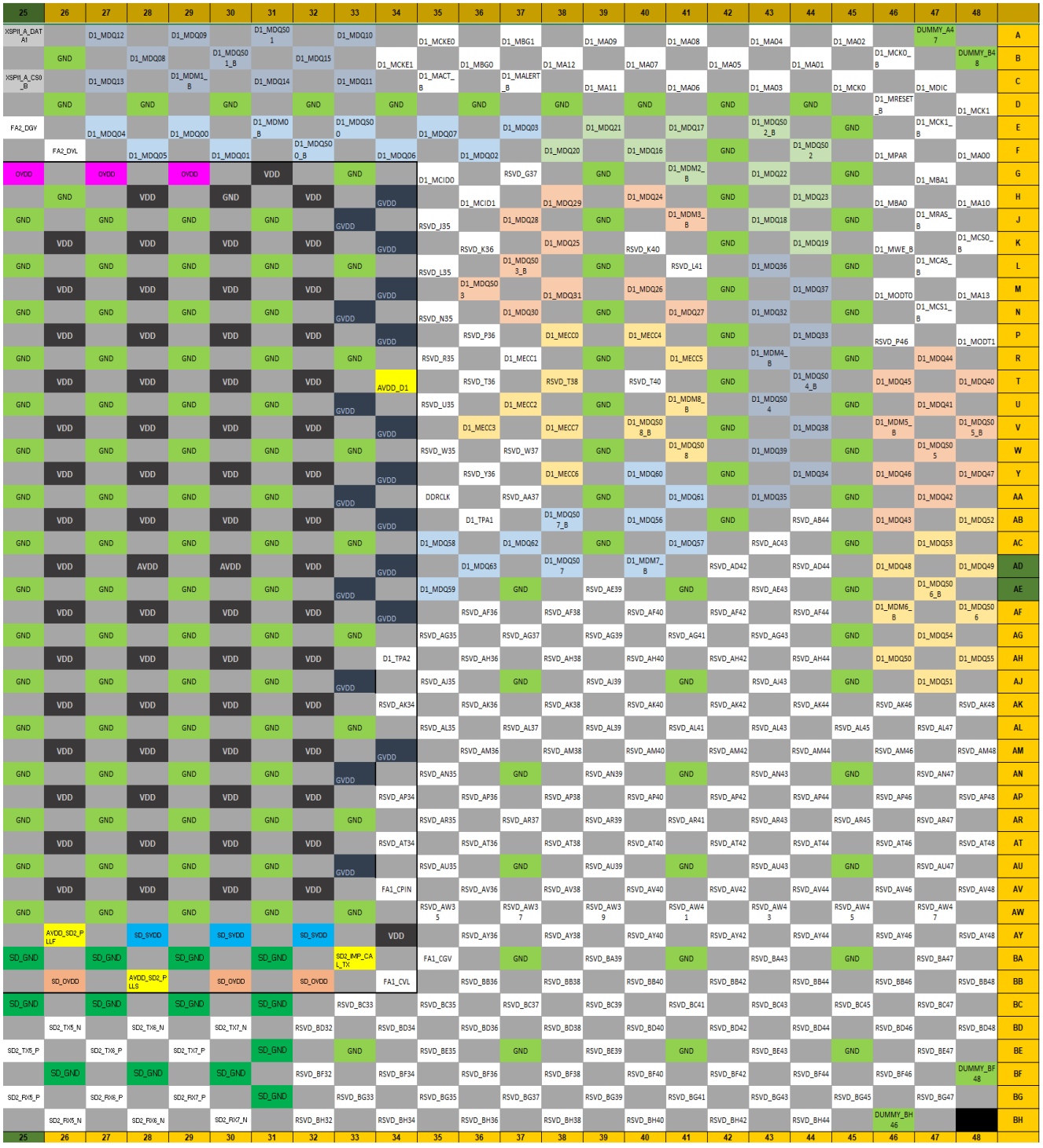
2.1 1150 ball layout diagrams

Figure 4 and Figure 5 show the left and right halves of the LX2162A ball map.



JEDEC Row/Col	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
A			DUMMY_A3		USB1_RX_P		USB1_TX_P		USB1_D_P		GND		SDHC2_DS		SDHC2_DAT5		SDHC2_DAT0		XSPI1_A_DQS		XSPI1_A_DAT A5		XSPI1_A_DAT A2	
B		RSVD_B2		USB1_ID		USB1_RX_M		USB1_TX_M		USB1_D_M		SDHC2_CMD		SDHC2_DAT7		SDHC2_DAT4		SDHC2_DAT1		XSPI1_A_DAT A7		XSPI1_A_DAT A4		XSPI1_A_DAT A3
C	DUMMY_C1		IIC2_SCL		GND		GND		GND		GND		SDHC2_CLK		SDHC2_DAT6		SDHC2_DAT3		SDHC2_DAT2		XSPI1_A_DAT A6		XSPI1_A_SCK	
D		SDHC1_CLK		IIC2_SDA		USB1_DRVVBUS		USB1_RESREF		USB1_VBUS		SENSEGND_CB		GND		GND		GND		GND		GND		XSPI1_A_DAT A0
E	SDHC1_DAT0		SDHC1_CMD		USB1_PWRFAULT		GND		GND		SENSEGND_PL		IIC6_SDA		TDI_CATHODE		SENSEGND_CA		TDO		TMS		TCK	
F		SDHC1_DAT1		GND		USB_SDVDD		USB_HVDD		USB_SVDD		SENSEVDD_CB		TA_PROG_SFP		TDI_ANODE		TBSCAN_EN_B		TDI		FA2_DPIN		XSPI1_A_CS1_B
G	SDHC1_DAT2		SDHC1_DAT3		SPI3_PCS1		GND		GND		SENSEVDD_PL		IIC6_SCL		PROG_MTR		SENSEVDD_CA		TRST_B		OVDD		OVDD	
H		SPI3_SCK		SPI3_PCS2		USB_SDVDD		USB_HVDD		USB_SVDD		VDD		VDD		VDD		GND		OVDD		GND		VDD
J	SPI3_SOUT		SPI3_PCS0		SPI3_PCS3		GND		GND		GND		GND		GND		GND		GND		GND		GND	
K		SPI3_SIN		GND		TEST_SEL_B		VDD		VDD		VDD		VDD		VDD		VDD		VDD		VDD		VDD
L	IIC1_SDA		PORESET_B		IIC4_SDA		GND		GND		GND		GND		GND		GND		GND		GND		GND	
M		RESET_REQ_B		IIC4_SCL		SCAN_MODE_B		VDD		VDD		VDD		VDD		VDD		VDD		VDD		VDD		VDD
N	IIC1_SCL		HRESET_B		IIC3_SDA		TH_TPA		GND		GND		GND		GND		GND		GND		GND		GND	
P		IRQ01		GND		IIC3_SCL		VDD		VDD		VDD		VDD		VDD		VDD		VDD		VDD		VDD
R	IRQ07		IRQ08		IRQ00		GND		GND		GND		GND		GND		GND		GND		GND		GND	
T		IRQ04		EVT0_B		EVT1_B		EVDD		VDD		VDD		VDD		VDD		VDD		VDD		VDD		VDD
U	IRQ11		IRQ10		EVT2_B		EVDD		GND		GND		GND		GND		GND		GND		GND		GND	
V		IRQ03		GND		TH_VDD		VDD		VDD		VDD		VDD		VDD		VDD		VDD		VDD		VDD
W	IRQ05		IRQ02		TA_BB_TMP_DETECT_B		OVDD		GND		GND		GND		GND		GND		GND		GND		GND	
Y		GND		EVT3_B		TA_TMP_DETECT_B		VDD		VDD		VDD		VDD		VDD		VDD		VDD		VDD		VDD
AA	IRQ09		EVT4_B		TA_BB_VDD		OVDD		GND		GND		GND		GND		GND		GND		GND		GND	
AB		IRQ06		GND		GND		VDD		VDD		VDD		VDD		VDD		VDD		VDD		VDD		VDD
AC	ASLEEP		UART1_SIN		UART1_RTS_B		OVDD		GND		GND		GND		GND		GND		GND		GND		GND	
AD		GND		UART1_SOUT		UART1_CTS_B		VDD		VDD		VDD		VDD		VDD		VDD		VDD		VDD		VDD
AE	EMI1_MDIO		UART2_SIN		OVDD		OVDD		GND		GND		GND		GND		GND		GND		GND		GND	
AF		EMI1_MDC		GND		UART2_RTS_B		VDD		VDD		VDD		VDD		VDD		VDD		VDD		VDD		VDD
AG	EMI2_MDC		EMI2_MDIO		UART2_CTS_B		GND		GND		GND		GND		GND		GND		GND		GND		GND	
AH		GND		UART2_SOUT		CLK_OUT		VDD		VDD		VDD		VDD		VDD		VDD		VDD		VDD		VDD
AJ	EC1_RX_CLK		EC1_GTX_CLK		EC1_TXD3		GND		GND		GND		GND		GND		GND		GND		GND		GND	
AK		EC1_RXD3		GND		OVDD		VDD		VDD		VDD		VDD		VDD		VDD		VDD		VDD		VDD
AL	EC1_RXD1		EC1_RXD2		EC1_TXD2		GND		GND		GND		GND		GND		GND		GND		GND		GND	
AM		GND		EC1_TXD1		OVDD		VDD		VDD		VDD		VDD		VDD		VDD		VDD		VDD		VDD
AN	EC1_RXD0		EC1_TXD0		EC1_TX_EN		GND		GND		GND		GND		GND		GND		GND		GND		GND	
AP		EC1_RX_DV		GND		EC2_GTX_CLK		VDD		VDD		VDD		VDD		VDD		VDD		VDD		VDD		VDD
AR	EC2_RXD3		EC2_RX_CLK		EC2_TXD3		GND		GND		GND		GND		GND		GND		GND		GND		GND	
AT		GND		EC2_TXD2		RCLK1		VDD		VDD		VDD		VDD		VDD		VDD		VDD		VDD		VDD
AU	EC2_RXD2		EC2_TXD1		EC2_TXD0		GND		GND		GND		GND		GND		GND		GND		GND		GND	
AV		EC2_RXD1		EC2_TX_EN		RCLK0		VDD		VDD		VDD		VDD		VDD		VDD		VDD		VDD		VDD
AW	EC2_RX_DV		EC2_RXD0		EC_GTX_CLK125		GND		GND		GND		GND		GND		GND		GND		GND		GND	
AY		SD_GND		SD_GND		SD_GND		SD_SVDD		SD_SVDD		SD_SVDD		SD_SVDD		AVDD_SDI_PLLF		SD_SVDD		VDD		SD_SVDD		SD_SVDD
BA	SD1_RX0_P		SD_GND		SD1_TX0_P		SDI_IMP_CAL_TX		SD_GND		SD_GND		SD_GND		SD_GND		SD_GND		GND		GND		SD_GND	
BB		SD1_RX0_N		SD1_TX0_N		SD_GND		SD_OVDD		SD_OVDD		SD_OVDD		SD_OVDD		AVDD_SDI_PLLS		SDI_IMP_CAL_RX		SD2_IMP_CAL_RX		SD_OVDD		SD_OVDD
BC	SD1_RX1_P		SD_GND		SD1_TX1_P		SD_GND		SD_GND		SD_GND		SD_GND		SD_GND		SD_GND		SD_GND		SD_GND		SD_GND	
BD		SD1_RX1_N		SD1_TX1_N		SD1_PLLF_TPD		SD1_TX2_N		SD1_TX3_N		SD2_TX0_N		SD2_TX1_N		SD2_TX2_N		SD2_TX3_N		DIFF_SYSCLK_P		SD2_PLLS_TPD		SD2_TX4_N
BE	SD1_PLLS_TPA		SD_GND		SD1_PLLS_TPD		SD1_TX2_P		SD1_TX3_P		SD2_TX0_P		SD2_TX1_P		SD2_TX2_P		SD2_TX3_P		SD2_PLLF_TPD		DIFF_SYSCLK_N		SD2_TX4_P	
BF		SD1_PLLF_TPA		SD_GND		SD_GND		SD_GND		SD_GND		SD_GND		SD_GND		SD_GND		SD_GND		SD_GND		SD_GND		SD_GND
BG	DUMMY_BG1		SD1_PLLF_REF_CLK_P		SD1_RX2_P		SD1_RX3_P		SD2_RX0_P		SD2_RX1_P		SD2_RX2_P		SD2_RX3_P		SD2_PLLF_TPA		SD2_PLLF_REF_CLK_P		SD2_PLLS_REF_CLK_P		SD2_RX4_P	
BH		DUMMY_BH2		SD1_PLLF_REF_CLK_N		SD1_RX2_N		SD1_RX3_N		SD2_RX0_N		SD2_RX1_N		SD2_RX2_N		SD2_RX3_N		SD2_PLLS_TPA		SD2_PLLF_REF_CLK_N		SD2_PLLS_REF_CLK_N		SD2_RX4_N
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24

Figure 4. Left half



25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	
XSPI1_A_DATA1		D1_MDQ12		D1_MDQ09		D1_MDQS01		D1_MDQ10		D1_MCKE0		D1_MBG1		D1_MA09		D1_MA08		D1_MA04		D1_MA02		DUMMY_A47		A
	GND		D1_MDQ08		D1_MDQS01_B		D1_MDQ15		D1_MCKE1		D1_MBG0		D1_MA12		D1_MA07		D1_MA05		D1_MA01		D1_MCK0_B		DUMMY_B48	B
XSPI1_A_CS0_B		D1_MDQ13		D1_MDM1_B		D1_MDQ14		D1_MDQ11		D1_MACT_B		D1_MALERT_B		D1_MA11		D1_MA06		D1_MA03		D1_MCK0		D1_MDIC		C
	GND		GND		GND		GND		GND		GND		GND		GND		GND		GND		D1_MRESET_B		D1_MCK1	D
FA2_DGV		D1_MDQ04		D1_MDQ00		D1_MDM0_B		D1_MDQS00		D1_MDQ07		D1_MDQ03		D1_MDQ21		D1_MDQ17		D1_MDQS02_B		GND		D1_MCK1_B		E
	FA2_DVL		D1_MDQ05		D1_MDQ01		D1_MDQS00_B		D1_MDQ06		D1_MDQ02		D1_MDQ20		D1_MDQ16		GND		D1_MDQS02		D1_MPAR		D1_MA00	F
OVDD		OVDD		OVDD		VDD		GND		D1_MCID0		RSVD_G37		GND		D1_MDM2_B		D1_MDQ22		GND		D1_MBA1		G
	GND		VDD		GND		VDD		GVDD		D1_MCID1		D1_MDQ29		D1_MDQ24		GND		D1_MDQ23		D1_MBA0		D1_MA10	H
GND		GND		GND		GND		GVDD		RSVD_J35		D1_MDQ28		GND		D1_MDM3_B		D1_MDQ18		GND		D1_MRAS_B		J
	VDD		VDD		VDD		VDD		GVDD		RSVD_K36		D1_MDQ25		RSVD_K40		GND		D1_MDQ19		D1_MWE_B		D1_MCS0_B	K
GND		GND		GND		GND		GND		RSVD_L35		D1_MDQS03_B		GND		RSVD_L41		D1_MDQ36		GND		D1_MCAS_B		L
	VDD		VDD		VDD		VDD		GVDD		D1_MDQS03		D1_MDQ31		D1_MDQ26		GND		D1_MDQ37		D1_MODT0		D1_MA13	M
GND		GND		GND		GND		GVDD		RSVD_N35		D1_MDQ30		GND		D1_MDQ27		D1_MDQ32		GND		D1_MCS1_B		N
	VDD		VDD		VDD		VDD		GVDD		RSVD_P36		D1_MECC0		D1_MECC4		GND		D1_MDQ33		RSVD_P46		D1_MODT1	P
GND		GND		GND		GND		GND		RSVD_R35		D1_MECC1		GND		D1_MECC5		D1_MDM4_B		GND		D1_MDQ44		R
	VDD		VDD		VDD		VDD		AVDD_D1		RSVD_T36		RSVD_T38		RSVD_T40		GND		D1_MDQS04_B		D1_MDQ45		D1_MDQ40	T
GND		GND		GND		GND		GVDD		RSVD_U35		D1_MECC2		GND		D1_MDM8_B		D1_MDQS04		GND		D1_MDQ41		U
	VDD		VDD		VDD		VDD		GVDD		D1_MECC3		D1_MECC7		D1_MDQS08_B		GND		D1_MDQ38		D1_MDM5_B		D1_MDQS05_B	V
GND		GND		GND		GND		GND		RSVD_W35		RSVD_W37		GND		D1_MDQS08		D1_MDQ39		GND		D1_MDQS05		W
	VDD		VDD		VDD		VDD		GVDD		RSVD_Y36		D1_MECC6		D1_MDQ60		GND		D1_MDQ34		D1_MDQ46		D1_MDQ47	Y
GND		GND		GND		GND		GVDD		DDRCLK		RSVD_AA37		GND		D1_MDQ61		D1_MDQ35		GND		D1_MDQ42		AA
	VDD		VDD		VDD		VDD		GVDD		D1_TPA1		D1_MDQS07_B		D1_MDQ56		GND		RSVD_AB44		D1_MDQ43		D1_MDQ52	AB
GND		GND		GND		GND		GND		D1_MDQ58		D1_MDQ62		GND		D1_MDQ57		RSVD_AC43		GND		D1_MDQ53		AC
	VDD		AVDD		AVDD		VDD		GVDD		D1_MDQ63		D1_MDQS07		D1_MDM7_B		RSVD_AD42		RSVD_AD44		D1_MDQ48		D1_MDQ49	AD
GND		GND		GND		GND		GVDD		D1_MDQ59		GND		RSVD_AE39		GND		RSVD_AE43		GND		D1_MDQS06_B		AE
	VDD		VDD		VDD		VDD		GVDD		RSVD_AF36		RSVD_AF38		RSVD_AF40		RSVD_AF42		RSVD_AF44		D1_MDM6_B		D1_MDQS06	AF
GND		GND		GND		GND		GND		RSVD_AG35		RSVD_AG37		RSVD_AG39		RSVD_AG41		RSVD_AG43		GND		D1_MDQ54		AG
	VDD		VDD		VDD		VDD		D1_TPA2		RSVD_AH36		RSVD_AH38		RSVD_AH40		RSVD_AH42		RSVD_AH44		D1_MDQ50		D1_MDQ55	AH
GND		GND		GND		GND		GVDD		RSVD_AJ35		GND		RSVD_AJ39		GND		RSVD_AJ43		GND		D1_MDQ51		AJ
	VDD		VDD		VDD		VDD		RSVD_AK34		RSVD_AK36		RSVD_AK38		RSVD_AK40		RSVD_AK42		RSVD_AK44		RSVD_AK46		RSVD_AK48	AK
GND		GND		GND		GND		GND		RSVD_AL35		RSVD_AL37		RSVD_AL39		RSVD_AL41		RSVD_AL43		RSVD_AL45		RSVD_AL47		AL
	VDD		VDD		VDD		VDD		GVDD		RSVD_AM36		RSVD_AM38		RSVD_AM40		RSVD_AM42		RSVD_AM44		RSVD_AM46		RSVD_AM48	AM
GND		GND		GND		GND		GVDD		RSVD_AN35		GND		RSVD_AN39		GND		RSVD_AN43		GND		RSVD_AN47		AN
	VDD		VDD		VDD		VDD		RSVD_AP34		RSVD_AP36		RSVD_AP38		RSVD_AP40		RSVD_AP42		RSVD_AP44		RSVD_AP46		RSVD_AP48	AP
GND		GND		GND		GND		GND		RSVD_AR35		RSVD_AR37		RSVD_AR39		RSVD_AR41		RSVD_AR43		RSVD_AR45		RSVD_AR47		AR
	VDD		VDD		VDD		VDD		RSVD_AT34		RSVD_AT36		RSVD_AT38		RSVD_AT40		RSVD_AT42		RSVD_AT44		RSVD_AT46		RSVD_AT48	AT
GND		GND		GND		GND		GVDD		RSVD_AU35		GND		RSVD_AU39		GND		RSVD_AU43		GND		RSVD_AU47		AU
	VDD		VDD		VDD		VDD		FA1_CPIN		RSVD_AV36		RSVD_AV38		RSVD_AV40		RSVD_AV42		RSVD_AV44		RSVD_AV46		RSVD_AV48	AV
GND		GND		GND		GND		GND		RSVD_AW35		RSVD_AW37		RSVD_AW39		RSVD_AW41		RSVD_AW43		RSVD_AW45		RSVD_AW47		AW
	AVDD_SD2_PLLF		SD_SVDD		SD_SVDD		SD_SVDD		VDD		RSVD_AY36		RSVD_AY38		RSVD_AY40		RSVD_AY42		RSVD_AY44		RSVD_AY46		RSVD_AY48	AY
SD_GND		SD_GND		SD_GND		SD_GND		SD2_IMP_CAL_TX		FA1_CGV		GND		RSVD_BA39		GND		RSVD_BA43		GND		RSVD_BA47		BA
	SD_OVDD		AVDD_SD2_PLLS		SD_OVDD		SD_OVDD		FA1_CVL		RSVD_BB36		RSVD_BB38		RSVD_BB40		RSVD_BB42		RSVD_BB44		RSVD_BB46		RSVD_BB48	BB
SD_GND		SD_GND		SD_GND		SD_GND		RSVD_BC33		RSVD_BC35		RSVD_BC37		RSVD_BC39		RSVD_BC41		RSVD_BC43		RSVD_BC45		RSVD_BC47		BC
	SD2_TX5_N		SD2_TX6_N		SD2_TX7_N		RSVD_BD32		RSVD_BD34		RSVD_BD36		RSVD_BD38		RSVD_BD40		RSVD_BD42		RSVD_BD44		RSVD_BD46		RSVD_BD48	BD
SD2_TX5_P		SD2_TX6_P		SD2_TX7_P		SD_GND		GND		RSVD_BE35		GND		RSVD_BE39		GND		RSVD_BE43		GND		RSVD_BE47		BE
	SD_GND		SD_GND		SD_GND		RSVD_BF32		RSVD_BF34		RSVD_BF36		RSVD_BF38		RSVD_BF40		RSVD_BF42		RSVD_BF44		RSVD_BF46		DUMMY_BF48	BF
SD2_RX5_P		SD2_RX6_P		SD2_RX7_P		SD_GND		RSVD_BG33		RSVD_BG35		RSVD_BG37		RSVD_BG39		RSVD_BG41		RSVD_BG43		RSVD_BG45		RSVD_BG47		BG
	SD2_RX5_N		SD2_RX6_N		SD2_RX7_N		RSVD_BH32		RSVD_BH34		RSVD_BH36		RSVD_BH38		RSVD_BH40		RSVD_BH42		RSVD_BH44		DUMMY_BH46			BH
25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	

Figure 5. Right half

2.2 Pinout list

This table provides the pinout listing for the LX2162A by bus. Primary functions are **bolded** in the table.

Table 2. Pinout list by bus

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
DDR SDRAM Memory Interface					
D1_MA00	Address	F48	O	GV_{DD}	---
D1_MA01	Address	B44	O	GV_{DD}	---
D1_MA02	Address	A45	O	GV_{DD}	---
D1_MA03	Address	C43	O	GV_{DD}	---
D1_MA04	Address	A43	O	GV_{DD}	---
D1_MA05	Address	B42	O	GV_{DD}	---
D1_MA06	Address	C41	O	GV_{DD}	---
D1_MA07	Address	B40	O	GV_{DD}	---
D1_MA08	Address	A41	O	GV_{DD}	---
D1_MA09	Address	A39	O	GV_{DD}	---
D1_MA10	Address	H48	O	GV_{DD}	---
D1_MA11	Address	C39	O	GV_{DD}	---
D1_MA12	Address	B38	O	GV_{DD}	---
D1_MA13	Address	M48	O	GV_{DD}	---
D1_MACT_B	Activate	C35	O	GV_{DD}	---
D1_MALERT_B	Alert	C37	I	GV_{DD}	1, 16
D1_MBA0	Bank Select	H46	O	GV_{DD}	---
D1_MBA1	Bank Select	G47	O	GV_{DD}	---
D1_MBG0	Bank Group	B36	O	GV_{DD}	---
D1_MBG1	Bank Group	A37	O	GV_{DD}	---
D1_MCAS_B	Column Address Strobe / MA[15]	L47	O	GV_{DD}	---
D1_MCK0	Clock	C45	O	GV_{DD}	---
D1_MCK1	Clock	D48	O	GV_{DD}	---
D1_MCKE0	Clock Enable	A35	O	GV_{DD}	2
D1_MCKE1	Clock Enable	B34	O	GV_{DD}	2
D1_MCK0_B	Clock Complement	B46	O	GV_{DD}	---
D1_MCK1_B	Clock Complement	E47	O	GV_{DD}	---
D1_MCS0_B	Chip Select	K48	O	GV_{DD}	---
D1_MCS1_B	Chip Select	N47	O	GV_{DD}	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
D1_MCID0	Chip ID 0	G35	O	GV_{DD}	---
D1_MCID1	Chip ID 1	H36	O	GV_{DD}	---
D1_MDIC	Driver Impedence Calibration	C47	IO	GV_{DD}	3
D1_MDM0_B/D1_MDBI0_B	Data Mask/MDBI[0]_B	E31	IO	GV_{DD}	---
D1_MDM1_B/D1_MDBI1_B	Data Mask/MDBI[1]_B	C29	IO	GV_{DD}	---
D1_MDM2_B/D1_MDBI2_B	Data Mask/MDBI[2]_B	G41	IO	GV_{DD}	---
D1_MDM3_B/D1_MDBI3_B	Data Mask/MDBI[3]_B	J41	IO	GV_{DD}	---
D1_MDM4_B/D1_MDBI4_B	Data Mask/MDBI[4]_B	R43	IO	GV_{DD}	---
D1_MDM5_B/D1_MDBI5_B	Data Mask/MDBI[5]_B	V46	IO	GV_{DD}	---
D1_MDM6_B/D1_MDBI6_B	Data Mask/MDBI[6]_B	AF46	IO	GV_{DD}	---
D1_MDM7_B/D1_MDBI7_B	Data Mask/MDBI[7]_B	AD40	IO	GV_{DD}	---
D1_MDM8_B/D1_MDBI8_B	Data Mask/MDBI[8]_B	U41	IO	GV_{DD}	---
D1_MDQ00	Data	E29	IO	GV_{DD}	---
D1_MDQ01	Data	F30	IO	GV_{DD}	---
D1_MDQ02	Data	F36	IO	GV_{DD}	---
D1_MDQ03	Data	E37	IO	GV_{DD}	---
D1_MDQ04	Data	E27	IO	GV_{DD}	---
D1_MDQ05	Data	F28	IO	GV_{DD}	---
D1_MDQ06	Data	F34	IO	GV_{DD}	---
D1_MDQ07	Data	E35	IO	GV_{DD}	---
D1_MDQ08	Data	B28	IO	GV_{DD}	---
D1_MDQ09	Data	A29	IO	GV_{DD}	---
D1_MDQ10	Data	A33	IO	GV_{DD}	---
D1_MDQ11	Data	C33	IO	GV_{DD}	---
D1_MDQ12	Data	A27	IO	GV_{DD}	---
D1_MDQ13	Data	C27	IO	GV_{DD}	---
D1_MDQ14	Data	C31	IO	GV_{DD}	---
D1_MDQ15	Data	B32	IO	GV_{DD}	---
D1_MDQ16	Data	F40	IO	GV_{DD}	---
D1_MDQ17	Data	E41	IO	GV_{DD}	---
D1_MDQ18	Data	J43	IO	GV_{DD}	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
D1_MDQ19	Data	K44	IO	GV_{DD}	---
D1_MDQ20	Data	F38	IO	GV_{DD}	---
D1_MDQ21	Data	E39	IO	GV_{DD}	---
D1_MDQ22	Data	G43	IO	GV_{DD}	---
D1_MDQ23	Data	H44	IO	GV_{DD}	---
D1_MDQ24	Data	H40	IO	GV_{DD}	---
D1_MDQ25	Data	K38	IO	GV_{DD}	---
D1_MDQ26	Data	M40	IO	GV_{DD}	---
D1_MDQ27	Data	N41	IO	GV_{DD}	---
D1_MDQ28	Data	J37	IO	GV_{DD}	---
D1_MDQ29	Data	H38	IO	GV_{DD}	---
D1_MDQ30	Data	N37	IO	GV_{DD}	---
D1_MDQ31	Data	M38	IO	GV_{DD}	---
D1_MDQ32	Data	N43	IO	GV_{DD}	---
D1_MDQ33	Data	P44	IO	GV_{DD}	---
D1_MDQ34	Data	Y44	IO	GV_{DD}	---
D1_MDQ35	Data	AA43	IO	GV_{DD}	---
D1_MDQ36	Data	L43	IO	GV_{DD}	---
D1_MDQ37	Data	M44	IO	GV_{DD}	---
D1_MDQ38	Data	V44	IO	GV_{DD}	---
D1_MDQ39	Data	W43	IO	GV_{DD}	---
D1_MDQ40	Data	T48	IO	GV_{DD}	---
D1_MDQ41	Data	U47	IO	GV_{DD}	---
D1_MDQ42	Data	AA47	IO	GV_{DD}	---
D1_MDQ43	Data	AB46	IO	GV_{DD}	---
D1_MDQ44	Data	R47	IO	GV_{DD}	---
D1_MDQ45	Data	T46	IO	GV_{DD}	---
D1_MDQ46	Data	Y46	IO	GV_{DD}	---
D1_MDQ47	Data	Y48	IO	GV_{DD}	---
D1_MDQ48	Data	AD46	IO	GV_{DD}	---
D1_MDQ49	Data	AD48	IO	GV_{DD}	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
D1_MDQ50	Data	AH46	IO	GV_{DD}	---
D1_MDQ51	Data	AJ47	IO	GV_{DD}	---
D1_MDQ52	Data	AB48	IO	GV_{DD}	---
D1_MDQ53	Data	AC47	IO	GV_{DD}	---
D1_MDQ54	Data	AG47	IO	GV_{DD}	---
D1_MDQ55	Data	AH48	IO	GV_{DD}	---
D1_MDQ56	Data	AB40	IO	GV_{DD}	---
D1_MDQ57	Data	AC41	IO	GV_{DD}	---
D1_MDQ58	Data	AC35	IO	GV_{DD}	---
D1_MDQ59	Data	AE35	IO	GV_{DD}	---
D1_MDQ60	Data	Y40	IO	GV_{DD}	---
D1_MDQ61	Data	AA41	IO	GV_{DD}	---
D1_MDQ62	Data	AC37	IO	GV_{DD}	---
D1_MDQ63	Data	AD36	IO	GV_{DD}	---
D1_MDQS00	Data Strobe	E33	IO	GV_{DD}	---
D1_MDQS01	Data Strobe	A31	IO	GV_{DD}	---
D1_MDQS02	Data Strobe	F44	IO	GV_{DD}	---
D1_MDQS03	Data Strobe	M36	IO	GV_{DD}	---
D1_MDQS04	Data Strobe	U43	IO	GV_{DD}	---
D1_MDQS05	Data Strobe	W47	IO	GV_{DD}	---
D1_MDQS06	Data Strobe	AF48	IO	GV_{DD}	---
D1_MDQS07	Data Strobe	AD38	IO	GV_{DD}	---
D1_MDQS08	Data Strobe	W41	IO	GV_{DD}	---
D1_MDQS00_B	Data Strobe	F32	IO	GV_{DD}	---
D1_MDQS01_B	Data Strobe	B30	IO	GV_{DD}	---
D1_MDQS02_B	Data Strobe	E43	IO	GV_{DD}	---
D1_MDQS03_B	Data Strobe	L37	IO	GV_{DD}	---
D1_MDQS04_B	Data Strobe	T44	IO	GV_{DD}	---
D1_MDQS05_B	Data Strobe	V48	IO	GV_{DD}	---
D1_MDQS06_B	Data Strobe	AE47	IO	GV_{DD}	---
D1_MDQS07_B	Data Strobe	AB38	IO	GV_{DD}	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
D1_MDQS08_B	Data Strobe	V40	IO	GV_{DD}	---
D1_MECC0	Error Correcting Code	P38	IO	GV_{DD}	---
D1_MECC1	Error Correcting Code	R37	IO	GV_{DD}	---
D1_MECC2	Error Correcting Code	U37	IO	GV_{DD}	---
D1_MECC3	Error Correcting Code	V36	IO	GV_{DD}	---
D1_MECC4	Error Correcting Code	P40	IO	GV_{DD}	---
D1_MECC5	Error Correcting Code	R41	IO	GV_{DD}	---
D1_MECC6	Error Correcting Code	Y38	IO	GV_{DD}	---
D1_MECC7	Error Correcting Code	V38	IO	GV_{DD}	---
D1_MODT0	On Die Termination	M46	O	GV_{DD}	2
D1_MODT1	On Die Termination / MCID[2]	P48	O	GV_{DD}	2
D1_MPAR	Address Parity Out	F46	O	GV_{DD}	---
D1_MRAS_B	Row Address Strobe / MA[16]	J47	O	GV_{DD}	---
D1_MWE_B	Write Enable / MA[14]	K46	O	GV_{DD}	---
D1_MRESET_B	Reset to DRAM	D46	IO	GV_{DD}	16
D1_TPA1	PLL Test Point Analog	AB36	-	-	---
D1_TPA2	DDR PHY Test Point Analog	AH34	-	GV_{DD}	---
I2C1					
IIC1_SCL /GPIO1_DAT03	Serial Clock	N1	IO	OV_{DD}	5, 6
IIC1_SDA /GPIO1_DAT02	Serial Data	L1	IO	OV_{DD}	5, 6
I2C2					
IIC2_SCL /GPIO1_DAT31 / FTM1_CH0 /SDHC1_CD_B	Serial Clock	C3	IO	OV_{DD}	5, 6
IIC2_SDA /GPIO1_DAT30 / FTM2_CH0 /SDHC1_WP	Serial Data	D4	IO	OV_{DD}	5, 6
I2C3					
IIC3_SCL /GPIO1_DAT29 / CAN1_TX /EVT5_B	Serial Clock	P6	IO	OV_{DD}	5, 6
IIC3_SDA /GPIO1_DAT28 / CAN1_RX /EVT6_B	Serial Data	N5	IO	OV_{DD}	5, 6
I2C4					
IIC4_SCL /GPIO1_DAT27 / CAN2_TX /EVT7_B	Serial Clock	M4	IO	OV_{DD}	5, 6

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
IIC4_SDA /GPIO1_DAT26 / CAN2_RX /EVT8_B	Serial Data	L5	IO	OV_{DD}	5, 6
I2C5					
IIC5_SCL /GPIO1_DAT25 / SDHC1_CLK_SYNC_OUT / **SPI3_SOUT**	Serial Clock	J1	IO	OV_{DD}	5, 6
IIC5_SDA /GPIO1_DAT24 / SDHC1_CLK_SYNC_IN / **SPI3_SIN**	Serial Data	K2	IO	OV_{DD}	5, 6
I2C6					
IIC6_SCL /GPIO1_DAT23 / SDHC2_CLK_SYNC_OUT	Serial Clock	G13	IO	OV_{DD}	5, 6
IIC6_SDA /GPIO1_DAT22 / SDHC2_CLK_SYNC_IN	Serial Data	E13	IO	OV_{DD}	5, 6
I2C7					
IIC7_SCL/ **SDHC2_DAT5** / GPIO2_DAT16 / XSPI1_B_DATA5	Serial Clock	A15	IO	OV_{DD}	5, 6
IIC7_SDA/ **SDHC2_DAT4** / GPIO2_DAT15 / XSPI1_B_DATA4	Serial Data	B16	IO	OV_{DD}	5, 6
I2C8					
IIC8_SCL/ **SDHC2_DAT7** / GPIO2_DAT18 / XSPI1_B_DATA7	Serial Clock	B14	IO	OV_{DD}	5, 6
IIC8_SDA/ **SDHC2_DAT6** / GPIO2_DAT17 / XSPI1_B_DATA6	Serial Data	C15	IO	OV_{DD}	5, 6
XSPI1					
XSPI1_A_CS0_B / GPIO2_DAT21 /cfg_svr0	Chip Select	C25	O	OV_{DD}	1
XSPI1_A_CS1_B / GPIO2_DAT20 /cfg_svr1	Chip Select	F24	O	OV_{DD}	1
XSPI1_A_DATA0 / GPIO2_DAT24	Data	D24	IO	OV_{DD}	---
XSPI1_A_DATA1 / GPIO2_DAT25	Data	A25	IO	OV_{DD}	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
XSPI1_A_DATA2 / GPIO2_DAT26	Data	A23	IO	OV_{DD}	---
XSPI1_A_DATA3 / GPIO2_DAT27	Data	B24	IO	OV_{DD}	---
XSPI1_A_DATA4 / GPIO2_DAT28	Data	B22	IO	OV_{DD}	---
XSPI1_A_DATA5 / GPIO2_DAT29	Data	A21	IO	OV_{DD}	---
XSPI1_A_DATA6 / GPIO2_DAT30	Data	C21	IO	OV_{DD}	---
XSPI1_A_DATA7 / GPIO2_DAT31	Data	B20	IO	OV_{DD}	---
XSPI1_A_DQS / GPIO2_DAT23	Data Strobe	A19	IO	OV_{DD}	---
XSPI1_A_SCK / GPIO2_DAT22 /cfg_eng_use0	Clock	C23	O	OV_{DD}	1
XSPI1_B_CS1_B/ **SDHC2_CMD** / GPIO2_DAT19 /SPI2_SOUT	Chip Select	B12	O	OV_{DD}	1
XSPI1_B_DATA0/ **SDHC2_DAT0** / GPIO2_DAT11 /SPI2_SIN / cfg_gpinput4	Data	A17	IO	OV_{DD}	
XSPI1_B_DATA1/ **SDHC2_DAT1** / GPIO2_DAT12 /SPI2_PCS2 / cfg_gpinput5	Data	B18	IO	OV_{DD}	
XSPI1_B_DATA2/ **SDHC2_DAT2** / GPIO2_DAT13 /SPI2_PCS1 / cfg_gpinput6	Data	C19	IO	OV_{DD}	
XSPI1_B_DATA3/ **SDHC2_DAT3** / GPIO2_DAT14 /SPI2_PCS0 / cfg_gpinput7	Data	C17	IO	OV_{DD}	
XSPI1_B_DATA4/ **SDHC2_DAT4** / GPIO2_DAT15 /IIC7_SDA	Data	B16	IO	OV_{DD}	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
XSPI1_B_DATA5/ **SDHC2_DAT5** / GPIO2_DAT16 /IIC7_SCL	Data	A15	IO	OV_{DD}	---
XSPI1_B_DATA6/ **SDHC2_DAT6** / GPIO2_DAT17 /IIC8_SDA	Data	C15	IO	OV_{DD}	---
XSPI1_B_DATA7/ **SDHC2_DAT7** / GPIO2_DAT18 /IIC8_SCL	Data	B14	IO	OV_{DD}	---
XSPI1_B_DQS/ **SDHC2_DS** / GPIO2_DAT10 /SPI2_PCS3	Data Strobe	A13	IO	OV_{DD}	---
XSPI1_B_SCK/ **SDHC2_CLK** / GPIO2_DAT09 /SPI2_SCK	Clock	C13	O	OV_{DD}	1
eSDHC 1					
SDHC1_CD_B/ **IIC2_SCL** / GPIO1_DAT31 /FTM1_CH0	Card Detect	C3	I	OV_{DD}	1
SDHC1_CLK /GPIO1_DAT16 / SPI1_SCK	Host to Card Clock	D2	O	EV_{DD}	1
SDHC1_CLK_SYNC_IN/ IIC5_SDA /GPIO1_DAT24 **SPI3_SIN**	Input Synchronous Clock	K2	I	OV_{DD}	1
SDHC1_CLK_SYNC_OUT/ IIC5_SCL /GPIO1_DAT25 / **SPI3_SOUT**	Output Synchronuous Clock	J1	O	OV_{DD}	1
SDHC1_CMD / GPIO1_DAT21 /SPI1_SOUT	Command/Response	E3	IO	EV_{DD}	5
SDHC1_CMD_DIR / GPIO1_DAT14 /**SPI3_PCS1** / SDHC1_DAT5	Command Direction	G5	O	OV_{DD}	1
SDHC1_DAT0 / GPIO1_DAT17 /SPI1_SIN / cfg_gpinput0	Data	E1	IO	EV_{DD}	5
SDHC1_DAT0_DIR / GPIO1_DAT13 /**SPI3_PCS2** / SDHC1_DAT6	DAT0 Direction	H4	O	OV_{DD}	1
SDHC1_DAT1 / GPIO1_DAT18 /SPI1_PCS2 / cfg_gpinput1	Data	F2	IO	EV_{DD}	5

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
SDHC1_DAT123_DIR / GPIO1_DAT12 /**SPI3_PCS3** / SDHC1_DAT7	DATA[1:3] Direction	J5	O	OV_{DD}	1
SDHC1_DAT2 / GPIO1_DAT19 /SPI1_PCS1 / cfg_gpinput2	Data	G1	IO	EV_{DD}	5
SDHC1_DAT3 / GPIO1_DAT20 /SPI1_PCS0 / cfg_gpinput3	Data	G3	IO	EV_{DD}	5
SDHC1_DAT4/ SDHC1_VSEL / GPIO1_DAT15 /SPI1_PCS3 / **SPI3_PCS0**	Data	J3	IO	OV_{DD}	---
SDHC1_DAT5/ SDHC1_CMD_DIR / GPIO1_DAT14 /**SPI3_PCS1**	Data	G5	IO	OV_{DD}	---
SDHC1_DAT6/ SDHC1_DAT0_DIR / GPIO1_DAT13 /**SPI3_PCS2**	Data	H4	IO	OV_{DD}	---
SDHC1_DAT7/ SDHC1_DAT123_DIR / GPIO1_DAT12 /**SPI3_PCS3**	Data	J5	IO	OV_{DD}	---
SDHC1_DS /GPIO4_DAT29 / **SPI3_SCK**	Data Strobe (eMMC HS400 mode)	H2	I	OV_{DD}	1
SDHC1_VSEL / GPIO1_DAT15 /SPI1_PCS3 / **SPI3_PCS0** /SDHC1_DAT4	SDHC Voltage Select	J3	O	OV_{DD}	1
SDHC1_WP/ **IIC2_SDA** / GPIO1_DAT30 /FTM2_CH0	Write Protect	D4	I	OV_{DD}	1
eSDHC 2					
SDHC2_CLK /GPIO2_DAT09 / SPI2_SCK /XSPI1_B_SCK	Host to Card Clock	C13	O	OV_{DD}	1
SDHC2_CLK_SYNC_IN/ **IIC6_SDA** /GPIO1_DAT22	Input Synchronous Clock	E13	I	OV_{DD}	1
SDHC2_CLK_SYNC_OUT/ **IIC6_SCL** /GPIO1_DAT23	Output Synchronuous Clock	G13	O	OV_{DD}	1
SDHC2_CMD / GPIO2_DAT19 /SPI2_SOUT / XSPI1_B_CS1_B	Command/Response	B12	IO	OV_{DD}	5

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
SDHC2_DAT0 / GPIO2_DAT11 /SPI2_SIN / XSPI1_B_DATA0 / cfg_gpinput4	Data	A17	IO	OV_{DD}	5
SDHC2_DAT1 / GPIO2_DAT12 /SPI2_PCS2 / XSPI1_B_DATA1 / cfg_gpinput5	Data	B18	IO	OV_{DD}	5
SDHC2_DAT2 / GPIO2_DAT13 /SPI2_PCS1 / XSPI1_B_DATA2 / cfg_gpinput6	Data	C19	IO	OV_{DD}	5
SDHC2_DAT3 / GPIO2_DAT14 /SPI2_PCS0 / XSPI1_B_DATA3 / cfg_gpinput7	Data	C17	IO	OV_{DD}	5
SDHC2_DAT4 / GPIO2_DAT15 /IIC7_SDA / XSPI1_B_DATA4	Data	B16	IO	OV_{DD}	5
SDHC2_DAT5 / GPIO2_DAT16 /IIC7_SCL / XSPI1_B_DATA5	Data	A15	IO	OV_{DD}	5
SDHC2_DAT6 / GPIO2_DAT17 /IIC8_SDA / XSPI1_B_DATA6	Data	C15	IO	OV_{DD}	5
SDHC2_DAT7 / GPIO2_DAT18 /IIC8_SCL / XSPI1_B_DATA7	Data	B14	IO	OV_{DD}	5
SDHC2_DS /GPIO2_DAT10 / SPI2_PCS3 /XSPI1_B_DQS	Data Strobe (eMMC HS400 mode)	A13	I	OV_{DD}	1, 11
UART 1					
UART1_CTS_B / GPIO1_DAT08 /UART3_SIN	Clear To Send	AD6	I	OV_{DD}	1
UART1_RTS_B / GPIO1_DAT09 / UART3_SOUT /cfg_eng_use1	Ready to Send	AC5	O	OV_{DD}	1
UART1_SIN /GPIO1_DAT10	Receive Data	AC3	I	OV_{DD}	1
UART1_SOUT / GPIO1_DAT11 /cfg_rcw_src1	Transmit Data	AD4	O	OV_{DD}	1
UART 2					

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
UART2_CTS_B / GPIO1_DAT04 /UART4_SIN	Clear To Send	AG5	I	OV_{DD}	1
UART2_RTS_B / GPIO1_DAT05 / UART4_SOUT /cfg_eng_use2	Ready to Send	AF6	O	OV_{DD}	1
UART2_SIN /GPIO1_DAT06	Receive Data	AE3	I	OV_{DD}	1
UART2_SOUT / GPIO1_DAT07 /cfg_rcw_src0	Transmit Data	AH4	O	OV_{DD}	1
UART 3					
UART3_SIN/ **UART1_CTS_B** / GPIO1_DAT08	Serial Input	AD6	I	OV_{DD}	1
UART3_SOUT/ **UART1_RTS_B** / GPIO1_DAT09 /cfg_eng_use1	Serial Output	AC5	O	OV_{DD}	1
UART 4					
UART4_SIN/ **UART2_CTS_B** / GPIO1_DAT04	Serial Input	AG5	I	OV_{DD}	1
UART4_SOUT/ **UART2_RTS_B** / GPIO1_DAT05 /cfg_eng_use2	Serial Output	AF6	O	OV_{DD}	1
Interrupt Controller					
IRQ00 /GPIO3_DAT00 / FTM1_CH4	External Interrupt	R5	I	OV_{DD}	1
IRQ01 /GPIO3_DAT01 / FTM2_CH4	External Interrupt	P2	I	OV_{DD}	1
IRQ02 /GPIO3_DAT02 / FTM1_CH5	External Interrupt	W3	I	OV_{DD}	1
IRQ03 /GPIO3_DAT03 / FTM2_CH5	External Interrupt	V2	I	OV_{DD}	1
IRQ04 /GPIO3_DAT04 / FTM1_CH6	External Interrupt	T2	I	OV_{DD}	1
IRQ05 /GPIO3_DAT05 / FTM2_CH6	External Interrupt	W1	I	OV_{DD}	1
IRQ06 /GPIO3_DAT06 / FTM1_CH7	External Interrupt	AB2	I	OV_{DD}	1
IRQ07 /GPIO3_DAT07 / FTM2_CH7	External Interrupt	R1	I	OV_{DD}	1

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
IRQ08 /GPIO3_DAT08	External Interrupt	R3	I	OV_{DD}	1
IRQ09 /GPIO3_DAT09	External Interrupt	AA1	I	OV_{DD}	1
IRQ10 /GPIO3_DAT10	External Interrupt	U3	I	OV_{DD}	1
IRQ11 /GPIO3_DAT11	External Interrupt	U1	I	OV_{DD}	1
Trust Architecture					
TA_BB_TMP_DETECT_B	Battery Backed Tamper Detect	W5	I	TA_BB_V_{DD}	---
TA_TMP_DETECT_B	Tamper Detect	Y6	I	OV_{DD}	---
System Control					
HRESET_B	Hard Reset	N3	IO	OV_{DD}	5, 6
PORESET_B	Power On Reset	L3	I	OV_{DD}	---
RESET_REQ_B / GPIO2_DAT08	Reset Request (POR or Hard)	M2	O	OV_{DD}	1, 18
Clocking					
DDRCLK	DDR Controller Clock	AA35	I	OV_{DD}	---
DIFF_SYSCLK_N	Differential System Clock (negative)	BE21	I	SD_SV_{DD}	---
DIFF_SYSCLK_P	Differential System Clock (positive)	BD20	I	SD_SV_{DD}	---
EC_GTX_CLK125 / GPIO4_DAT24	RGMII Reference Clock	AW5	I	OV_{DD}	1
Debug					
ASLEEP /GPIO2_DAT06 / EVT9_B /cfg_rcw_src2	Asleep	AC1	O	OV_{DD}	1, 4
CLK_OUT /GPIO2_DAT07 / FTM1_CH1 /cfg_rcw_src3	Clock Out	AH6	O	OV_{DD}	2
CLK_OUT2/ **EC1_TXD0** / GPIO4_DAT03	Clock Output	AN3	O	OV_{DD}	1
EVT0_B /GPIO3_DAT12 / FTM2_CH1	Event 0	T4	IO	OV_{DD}	7
EVT1_B /GPIO3_DAT13 / FTM1_CH2	Event 1	T6	IO	OV_{DD}	7
EVT2_B /GPIO3_DAT14 / FTM2_CH2	Event 2	U5	IO	OV_{DD}	7
EVT3_B /GPIO3_DAT15 / FTM1_CH3	Event 3	Y4	IO	OV_{DD}	7

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
EVT4_B /GPIO3_DAT16 / FTM2_CH3	Event 4	AA3	IO	OV_{DD}	7
EVT5_B/ **IIC3_SCL** / GPIO1_DAT29 /CAN1_TX	Event 5	P6	IO	OV_{DD}	---
EVT6_B/ **IIC3_SDA** / GPIO1_DAT28 /CAN1_RX	Event 6	N5	IO	OV_{DD}	---
EVT7_B/ **IIC4_SCL** / GPIO1_DAT27 /CAN2_TX	Event 7	M4	IO	OV_{DD}	---
EVT8_B/ **IIC4_SDA** / GPIO1_DAT26 /CAN2_RX	Event 8	L5	IO	OV_{DD}	---
EVT9_B/ **ASLEEP** / GPIO2_DAT06 /cfg_rcw_src2	Event 9	AC1	O	OV_{DD}	1
DFT					
SCAN_MODE_B	Internal Use Only	M6	I	OV_{DD}	8
TEST_SEL_B	Internal Use Only	K6	I	OV_{DD}	5
JTAG					
TBSCAN_EN_B	Test Boundary Scan Enable	F18	I	OV_{DD}	5
TCK	Test Clock	E23	I	OV_{DD}	---
TDI	Test Data In	F20	I	OV_{DD}	7
TDO	Test Data Out	E19	O	OV_{DD}	2
TMS	Test Mode Select	E21	I	OV_{DD}	7
TRST_B	Test Reset	G19	I	OV_{DD}	7
Analog Signals					
D1_TPA1	PLL Test Point Analog	AB36	-	-	10
D1_TPA2	DDR PHY Test Point Analog	AH34	-	GV_{DD}	10
FA1_CGV	Internal Use Only	BA35	-	-	12
FA2_DGV	Internal Use Only	E25	-	-	12
FA1_CPIN	Internal Use Only	AV34	-	-	12
FA2_DPIN	Internal Use Only	F22	-	-	12
TD1_ANODE	Thermal diode anode	F16	-	-	14
TD1_CATHODE	Thermal diode cathode	E15	-	-	14
TH_TPA	Thermal Test Point Analog	N7	-	-	10
Serdes 1					

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
SD1_IMP_CAL_RX	SerDes Receive Impedence Calibration	BB18	I	SD_SV_{DD}	9
SD1_IMP_CAL_TX	SerDes Transmit Impedance Calibration	BA7	I	SD_OV_{DD}	13
SD1_PLLF_REF_CLK	SerDes PLL Fast Reference Clock	BG3	I	SD_SV_{DD}	---
SD1_PLLF_REF_CLK_B	SerDes PLL Fast Reference Clock Complement	BH4	I	SD_SV_{DD}	---
SD1_PLLF_TPA	SerDes PLL Fast Analog Test Point	BF2	O	AVDD_SD1_PLLF	10
SD1_PLLF_TPD	SerDes PLL Fast Digital Test Point	BD6	O	SD_SV_{DD}	10
SD1_PLLS_TPA	SerDes PLL Slow Analog Test Point	BE1	O	AVDD_SD1_PLLS	10
SD1_PLLS_TPD	SerDes PLL Slow Digital Test Point	BE5	O	SD_SV_{DD}	10
SD1_RX0_N	SerDes Receive Data (negative)	BB2	I	SD_SV_{DD}	---
SD1_RX1_N	SerDes Receive Data (negative)	BD2	I	SD_SV_{DD}	---
SD1_RX2_N	SerDes Receive Data (negative)	BH6	I	SD_SV_{DD}	---
SD1_RX3_N	SerDes Receive Data (negative)	BH8	I	SD_SV_{DD}	---
SD1_RX0_P	SerDes Receive Data (positive)	BA1	I	SD_SV_{DD}	---
SD1_RX1_P	SerDes Receive Data (positive)	BC1	I	SD_SV_{DD}	---
SD1_RX2_P	SerDes Receive Data (positive)	BG5	I	SD_SV_{DD}	---
SD1_RX3_P	SerDes Receive Data (positive)	BG7	I	SD_SV_{DD}	---
SD1_TX0_N	SerDes Transmit Data (negative)	BB4	O	SD_OV_{DD}	---
SD1_TX1_N	SerDes Transmit Data (negative)	BD4	O	SD_OV_{DD}	---
SD1_TX2_N	SerDes Transmit Data (negative)	BD8	O	SD_OV_{DD}	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
SD1_TX3_N	SerDes Transmit Data (negative)	BD10	O	SD_OV_{DD}	---
SD1_TX0_P	SerDes Transmit Data (positive)	BA5	O	SD_OV_{DD}	---
SD1_TX1_P	SerDes Transmit Data (positive)	BC5	O	SD_OV_{DD}	---
SD1_TX2_P	SerDes Transmit Data (positive)	BE7	O	SD_OV_{DD}	---
SD1_TX3_P	SerDes Transmit Data (positive)	BE9	O	SD_OV_{DD}	---
Serdes 2					
SD2_IMP_CAL_RX	SerDes Receive Impedence Calibration	BB20	I	SD_SV_{DD}	9
SD2_IMP_CAL_TX	SerDes Transmit Impedance Calibration	BA33	I	SD_OV_{DD}	13
SD2_PLLF_REF_CLK	SerDes PLL Fast Reference Clock	BG19	I	SD_SV_{DD}	---
SD2_PLLF_REF_CLK_B	SerDes PLL Fast Reference Clock Complement	BH20	I	SD_SV_{DD}	---
SD2_PLLF_TPA	SerDes PLL Fast Analog Test Point	BG17	O	AVDD_SD2_PLLF	10
SD2_PLLF_TPD	SerDes PLL Fast Digital Test Point	BE19	O	SD_SV_{DD}	10
SD2_PLLS_REF_CLK	SerDes PLL Slow Reference Clock	BG21	I	SD_SV_{DD}	---
SD2_PLLS_REF_CLK_B	SerDes PLL Slow Reference Clock Complement	BH22	I	SD_SV_{DD}	---
SD2_PLLS_TPA	SerDes PLL Slow Analog Test Point	BH18	O	AVDD_SD2_PLLS	10
SD2_PLLS_TPD	SerDes PLL Slow Digital Test Point	BD22	O	SD_SV_{DD}	10
SD2_RX0_N	SerDes Receive Data (negative)	BH10	I	SD_SV_{DD}	---
SD2_RX1_N	SerDes Receive Data (negative)	BH12	I	SD_SV_{DD}	---
SD2_RX2_N	SerDes Receive Data (negative)	BH14	I	SD_SV_{DD}	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
SD2_RX3_N	SerDes Receive Data (negative)	BH16	I	SD_SV_{DD}	---
SD2_RX4_N	SerDes Receive Data (negative)	BH24	I	SD_SV_{DD}	---
SD2_RX5_N	SerDes Receive Data (negative)	BH26	I	SD_SV_{DD}	---
SD2_RX6_N	SerDes Receive Data (negative)	BH28	I	SD_SV_{DD}	---
SD2_RX7_N	SerDes Receive Data (negative)	BH30	I	SD_SV_{DD}	---
SD2_RX0_P	SerDes Receive Data (positive)	BG9	I	SD_SV_{DD}	---
SD2_RX1_P	SerDes Receive Data (positive)	BG11	I	SD_SV_{DD}	---
SD2_RX2_P	SerDes Receive Data (positive)	BG13	I	SD_SV_{DD}	---
SD2_RX3_P	SerDes Receive Data (positive)	BG15	I	SD_SV_{DD}	---
SD2_RX4_P	SerDes Receive Data (positive)	BG23	I	SD_SV_{DD}	---
SD2_RX5_P	SerDes Receive Data (positive)	BG25	I	SD_SV_{DD}	---
SD2_RX6_P	SerDes Receive Data (positive)	BG27	I	SD_SV_{DD}	---
SD2_RX7_P	SerDes Receive Data (positive)	BG29	I	SD_SV_{DD}	---
SD2_TX0_N	SerDes Transmit Data (negative)	BD12	O	SD_OV_{DD}	---
SD2_TX1_N	SerDes Transmit Data (negative)	BD14	O	SD_OV_{DD}	---
SD2_TX2_N	SerDes Transmit Data (negative)	BD16	O	SD_OV_{DD}	---
SD2_TX3_N	SerDes Transmit Data (negative)	BD18	O	SD_OV_{DD}	---
SD2_TX4_N	SerDes Transmit Data (negative)	BD24	O	SD_OV_{DD}	---
SD2_TX5_N	SerDes Transmit Data (negative)	BD26	O	SD_OV_{DD}	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
SD2_TX6_N	SerDes Transmit Data (negative)	BD28	O	SD_OV_{DD}	---
SD2_TX7_N	SerDes Transmit Data (negative)	BD30	O	SD_OV_{DD}	---
SD2_TX0_P	SerDes Transmit Data (positive)	BE11	O	SD_OV_{DD}	---
SD2_TX1_P	SerDes Transmit Data (positive)	BE13	O	SD_OV_{DD}	---
SD2_TX2_P	SerDes Transmit Data (positive)	BE15	O	SD_OV_{DD}	---
SD2_TX3_P	SerDes Transmit Data (positive)	BE17	O	SD_OV_{DD}	---
SD2_TX4_P	SerDes Transmit Data (positive)	BE23	O	SD_OV_{DD}	---
SD2_TX5_P	SerDes Transmit Data (positive)	BE25	O	SD_OV_{DD}	---
SD2_TX6_P	SerDes Transmit Data (positive)	BE27	O	SD_OV_{DD}	---
SD2_TX7_P	SerDes Transmit Data (positive)	BE29	O	SD_OV_{DD}	---
USB PHY					
USB1_D_M	USB PHY Data Minus	B10	IO	USB_HV_{DD}	---
USB1_D_P	USB PHY Data Plus	A9	IO	USB_HV_{DD}	---
USB1_DRVVBUS / GPIO4_DAT25 /cfg_soc_use	USB PHY Digital signal - Drive VBUS	D6	O	OV_{DD}	1
USB1_ID	USB PHY ID Detect	B4	I	-	---
USB1_PWRFAULT / GPIO4_DAT26	USB PHY Digital signal - Power Fault	E5	I	OV_{DD}	1
USB1_RESREF	USB PHY Impedance Calibration	D8	IO	-	15
USB1_RX_M	USB PHY 3.0 Receive Data (negative)	B6	I	USB_SV_{DD}	---
USB1_RX_P	USB PHY 3.0 Receive Data (positive)	A5	I	USB_SV_{DD}	---
USB1_TX_M	USB PHY 3.0 Transmit Data (negative)	B8	O	USB_SV_{DD}	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
USB1_TX_P	USB PHY 3.0 Transmit Data (positive)	A7	O	USB_SV_{DD}	---
USB1_VBUS	USB PHY VBUS	D10	I	-	19
Ethernet Controller 1					
EC1_GTX_CLK / GPIO4_DAT05	Transmit Clock Out	AJ3	O	OV_{DD}	1
EC1_RXD0 /GPIO4_DAT09	Receive Data	AN1	I	OV_{DD}	1
EC1_RXD1 /GPIO4_DAT08	Receive Data	AL1	I	OV_{DD}	1
EC1_RXD2 /GPIO4_DAT07	Receive Data	AL3	I	OV_{DD}	1
EC1_RXD3 /GPIO4_DAT06	Receive Data	AK2	I	OV_{DD}	1
EC1_RX_CLK /GPIO4_DAT10	Receive Clock	AJ1	I	OV_{DD}	1
EC1_RX_DV /GPIO4_DAT11	Receive Data Valid	AP2	I	OV_{DD}	1
EC1_TXD0 /GPIO4_DAT03 / CLK_OUT2	Transmit Data	AN3	O	OV_{DD}	1
EC1_TXD1 /GPIO4_DAT02	Transmit Data	AM4	O	OV_{DD}	1
EC1_TXD2 /GPIO4_DAT01	Transmit Data	AL5	O	OV_{DD}	1
EC1_TXD3 /GPIO4_DAT00	Transmit Data	AJ5	O	OV_{DD}	1
EC1_TX_EN /GPIO4_DAT04	Transmit Enable	AN5	O	OV_{DD}	1, 11
Ethernet Controller 2					
EC2_GTX_CLK / GPIO4_DAT17	Transmit Clock Out	AP6	O	OV_{DD}	1
EC2_RXD0 /GPIO4_DAT21 / TSEC_1588_TRIG_IN2	Receive Data	AW3	I	OV_{DD}	1
EC2_RXD1 /GPIO4_DAT20 / TSEC_1588_PULSE_OUT1	Receive Data	AV2	I	OV_{DD}	1
EC2_RXD2 /GPIO4_DAT19	Receive Data	AU1	I	OV_{DD}	1
EC2_RXD3 /GPIO4_DAT18	Receive Data	AR1	I	OV_{DD}	1
EC2_RX_CLK / GPIO4_DAT22 / TSEC_1588_CLK_IN	Receive Clock	AR3	I	OV_{DD}	1
EC2_RX_DV /GPIO4_DAT23 / TSEC_1588_TRIG_IN1	Receive Data Valid	AW1	I	OV_{DD}	1
EC2_TXD0 /GPIO4_DAT15 / TSEC_1588_PULSE_OUT2	Transmit Data	AU5	O	OV_{DD}	1

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
EC2_TXD1 /GPIO4_DAT14 / TSEC_1588_CLK_OUT	Transmit Data	AU3	O	OV_{DD}	1
EC2_TXD2 /GPIO4_DAT13 / TSEC_1588_ALARM_OUT1	Transmit Data	AT4	O	OV_{DD}	1
EC2_TXD3 /GPIO4_DAT12 / TSEC_1588_ALARM_OUT2	Transmit Data	AR5	O	OV_{DD}	1
EC2_TX_EN /GPIO4_DAT16	Transmit Enable	AV4	O	OV_{DD}	1, 11
Sync Ethernet ClockOut					
RCLK0	Reconstructed Clock	AV6	O	OV_{DD}	---
RCLK1	Reconstructed Clock	AT6	O	OV_{DD}	---
Ethernet Management Interface 1					
EMI1_MDC	Management Data Clock	AF2	O	OV_{DD}	---
EMI1_MDIO	Management Data In/Out	AE1	IO	OV_{DD}	---
Ethernet Management Interface 2					
EMI2_MDC	Management Data Clock	AG1	O	OV_{DD}	---
EMI2_MDIO	Management Data In/Out	AG3	IO	OV_{DD}	5, 6
General Purpose Input/Output					
GPIO1_DAT02/ **IIC1_SDA**	General Purpose Input/Output	L1	IO	OV_{DD}	---
GPIO1_DAT03/ **IIC1_SCL**	General Purpose Input/Output	N1	IO	OV_{DD}	---
GPIO1_DAT04/ **UART2_CTS_B** /UART4_SIN	General Purpose Input/Output	AG5	IO	OV_{DD}	---
GPIO1_DAT05/ **UART2_RTS_B** / UART4_SOUT /cfg_eng_use2	General Purpose Input/Output	AF6	O	OV_{DD}	1
GPIO1_DAT06/ **UART2_SIN**	General Purpose Input/Output	AE3	IO	OV_{DD}	---
GPIO1_DAT07/ **UART2_SOUT** /cfg_rcw_src0	General Purpose Input/Output	AH4	O	OV_{DD}	1
GPIO1_DAT08/ **UART1_CTS_B** /UART3_SIN	General Purpose Input/Output	AD6	IO	OV_{DD}	---
GPIO1_DAT09/ **UART1_RTS_B** / UART3_SOUT /cfg_eng_use1	General Purpose Input/Output	AC5	O	OV_{DD}	1
GPIO1_DAT10/ **UART1_SIN**	General Purpose Input/Output	AC3	IO	OV_{DD}	---
GPIO1_DAT11/ **UART1_SOUT** /cfg_rcw_src1	General Purpose Input/Output	AD4	O	OV_{DD}	1

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GPIO1_DAT12/ SDHC1_DAT123_DIR / **SPI3_PCS3** /SDHC1_DAT7	General Purpose Input/Output	J5	IO	OV_{DD}	---
GPIO1_DAT13/ SDHC1_DAT0_DIR / **SPI3_PCS2** /SDHC1_DAT6	General Purpose Input/Output	H4	IO	OV_{DD}	---
GPIO1_DAT14/ SDHC1_CMD_DIR / **SPI3_PCS1** /SDHC1_DAT5	General Purpose Input/Output	G5	IO	OV_{DD}	---
GPIO1_DAT15/ SDHC1_VSEL /SPI1_PCS3 / **SPI3_PCS0** /SDHC1_DAT4	General Purpose Input/Output	J3	IO	OV_{DD}	---
GPIO1_DAT16/ **SDHC1_CLK** / SPI1_SCK	General Purpose Input/Output	D2	IO	EV_{DD}	---
GPIO1_DAT17/ **SDHC1_DAT0** /SPI1_SIN / cfg_gpinput0	General Purpose Input/Output	E1	IO	EV_{DD}	
GPIO1_DAT18/ **SDHC1_DAT1** /SPI1_PCS2 / cfg_gpinput1	General Purpose Input/Output	F2	IO	EV_{DD}	
GPIO1_DAT19/ **SDHC1_DAT2** /SPI1_PCS1 / cfg_gpinput2	General Purpose Input/Output	G1	IO	EV_{DD}	
GPIO1_DAT20/ **SDHC1_DAT3** /SPI1_PCS0 / cfg_gpinput3	General Purpose Input/Output	G3	IO	EV_{DD}	
GPIO1_DAT21/ **SDHC1_CMD** /SPI1_SOUT	General Purpose Input/Output	E3	IO	EV_{DD}	---
GPIO1_DAT22/ **IIC6_SDA** / SDHC2_CLK_SYNC_IN	General Purpose Input/Output	E13	IO	OV_{DD}	---
GPIO1_DAT23/ **IIC6_SCL** / SDHC2_CLK_SYNC_OUT	General Purpose Input/Output	G13	IO	OV_{DD}	---
GPIO1_DAT24/ IIC5_SDA / SDHC1_CLK_SYNC_IN / **SPI3_SIN**	General Purpose Input/Output	K2	IO	OV_{DD}	---
GPIO1_DAT25/ IIC5_SCL / SDHC1_CLK_SYNC_OUT / **SPI3_SOUT**	General Purpose Input/Output	J1	IO	OV_{DD}	---
GPIO1_DAT26/ **IIC4_SDA** / CAN2_RX /EVT8_B	General Purpose Input/Output	L5	IO	OV_{DD}	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GPIO1_DAT27/ **IIC4_SCL** / CAN2_TX /EVT7_B	General Purpose Input/Output	M4	IO	OV_{DD}	---
GPIO1_DAT28/ **IIC3_SDA** / CAN1_RX /EVT6_B	General Purpose Input/Output	N5	IO	OV_{DD}	---
GPIO1_DAT29/ **IIC3_SCL** / CAN1_TX /EVT5_B	General Purpose Input/Output	P6	IO	OV_{DD}	---
GPIO1_DAT30/ **IIC2_SDA** / FTM2_CH0 /SDHC1_WP	General Purpose Input/Output	D4	IO	OV_{DD}	---
GPIO1_DAT31/ **IIC2_SCL** / FTM1_CH0 /SDHC1_CD_B	General Purpose Input/Output	C3	IO	OV_{DD}	---
GPIO2_DAT06/ **ASLEEP** / EVT9_B /cfg_rcw_src2	General Purpose Input/Output	AC1	O	OV_{DD}	1
GPIO2_DAT07/ **CLK_OUT** / FTM1_CH1 /cfg_rcw_src3	General Purpose Input/Output	AH6	O	OV_{DD}	1
GPIO2_DAT08/ **RESET_REQ_B**	General Purpose Input/Output	M2	O	OV_{DD}	1
GPIO2_DAT09/ **SDHC2_CLK** / SPI2_SCK /XSPI1_B_SCK	General Purpose Input/Output	C13	IO	OV_{DD}	---
GPIO2_DAT10/ **SDHC2_DS** / SPI2_PCS3 /XSPI1_B_DQS	General Purpose Input/Output	A13	IO	OV_{DD}	---
GPIO2_DAT11/ **SDHC2_DAT0** /SPI2_SIN / XSPI1_B_DATA0 / cfg_gpinput4	General Purpose Input/Output	A17	IO	OV_{DD}	
GPIO2_DAT12/ **SDHC2_DAT1** /SPI2_PCS2 / XSPI1_B_DATA1 / cfg_gpinput5	General Purpose Input/Output	B18	IO	OV_{DD}	
GPIO2_DAT13/ **SDHC2_DAT2** /SPI2_PCS1 / XSPI1_B_DATA2 / cfg_gpinput6	General Purpose Input/Output	C19	IO	OV_{DD}	
GPIO2_DAT14/ **SDHC2_DAT3** /SPI2_PCS0 / XSPI1_B_DATA3 / cfg_gpinput7	General Purpose Input/Output	C17	IO	OV_{DD}	
GPIO2_DAT15/ **SDHC2_DAT4** /IIC7_SDA / XSPI1_B_DATA4	General Purpose Input/Output	B16	IO	OV_{DD}	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GPIO2_DAT16/ **SDHC2_DAT5** /IIC7_SCL / XSPI1_B_DATA5	General Purpose Input/Output	A15	IO	OV_{DD}	---
GPIO2_DAT17/ **SDHC2_DAT6** /IIC8_SDA / XSPI1_B_DATA6	General Purpose Input/Output	C15	IO	OV_{DD}	---
GPIO2_DAT18/ **SDHC2_DAT7** /IIC8_SCL / XSPI1_B_DATA7	General Purpose Input/Output	B14	IO	OV_{DD}	---
GPIO2_DAT19/ **SDHC2_CMD** /SPI2_SOUT / XSPI1_B_CS1_B	General Purpose Input/Output	B12	IO	OV_{DD}	---
GPIO2_DAT20/ **XSPI1_A_CS1_B** /cfg_svr1	General Purpose Input/Output	F24	O	OV_{DD}	1
GPIO2_DAT21/ **XSPI1_A_CS0_B** /cfg_svr0	General Purpose Input/Output	C25	O	OV_{DD}	1
GPIO2_DAT22/ **XSPI1_A_SCK** /cfg_eng_use0	General Purpose Input/Output	C23	O	OV_{DD}	1
GPIO2_DAT23/ **XSPI1_A_DQS**	General Purpose Input/Output	A19	IO	OV_{DD}	---
GPIO2_DAT24/ **XSPI1_A_DATA0**	General Purpose Input/Output	D24	IO	OV_{DD}	---
GPIO2_DAT25/ **XSPI1_A_DATA1**	General Purpose Input/Output	A25	IO	OV_{DD}	---
GPIO2_DAT26/ **XSPI1_A_DATA2**	General Purpose Input/Output	A23	IO	OV_{DD}	---
GPIO2_DAT27/ **XSPI1_A_DATA3**	General Purpose Input/Output	B24	IO	OV_{DD}	---
GPIO2_DAT28/ **XSPI1_A_DATA4**	General Purpose Input/Output	B22	IO	OV_{DD}	---
GPIO2_DAT29/ **XSPI1_A_DATA5**	General Purpose Input/Output	A21	IO	OV_{DD}	---
GPIO2_DAT30/ **XSPI1_A_DATA6**	General Purpose Input/Output	C21	IO	OV_{DD}	---
GPIO2_DAT31/ **XSPI1_A_DATA7**	General Purpose Input/Output	B20	IO	OV_{DD}	---
GPIO3_DAT00/ **IRQ00** / FTM1_CH4	General Purpose Input/Output	R5	IO	OV_{DD}	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GPIO3_DAT01/ **IRQ01** / FTM2_CH4	General Purpose Input/Output	P2	IO	OV_{DD}	---
GPIO3_DAT02/ **IRQ02** / FTM1_CH5	General Purpose Input/Output	W3	IO	OV_{DD}	---
GPIO3_DAT03/ **IRQ03** / FTM2_CH5	General Purpose Input/Output	V2	IO	OV_{DD}	---
GPIO3_DAT04/ **IRQ04** / FTM1_CH6	General Purpose Input/Output	T2	IO	OV_{DD}	---
GPIO3_DAT05/ **IRQ05** / FTM2_CH6	General Purpose Input/Output	W1	IO	OV_{DD}	---
GPIO3_DAT06/ **IRQ06** / FTM1_CH7	General Purpose Input/Output	AB2	IO	OV_{DD}	---
GPIO3_DAT07/ **IRQ07** / FTM2_CH7	General Purpose Input/Output	R1	IO	OV_{DD}	---
GPIO3_DAT08/ **IRQ08**	General Purpose Input/Output	R3	IO	OV_{DD}	---
GPIO3_DAT09/ **IRQ09**	General Purpose Input/Output	AA1	IO	OV_{DD}	---
GPIO3_DAT10/ **IRQ10**	General Purpose Input/Output	U3	IO	OV_{DD}	---
GPIO3_DAT11/ **IRQ11**	General Purpose Input/Output	U1	IO	OV_{DD}	---
GPIO3_DAT12/ **EVT0_B** / FTM2_CH1	General Purpose Input/Output	T4	IO	OV_{DD}	---
GPIO3_DAT13/ **EVT1_B** / FTM1_CH2	General Purpose Input/Output	T6	IO	OV_{DD}	---
GPIO3_DAT14/ **EVT2_B** / FTM2_CH2	General Purpose Input/Output	U5	IO	OV_{DD}	---
GPIO3_DAT15/ **EVT3_B** / FTM1_CH3	General Purpose Input/Output	Y4	IO	OV_{DD}	---
GPIO3_DAT16/ **EVT4_B** / FTM2_CH3	General Purpose Input/Output	AA3	IO	OV_{DD}	---
GPIO4_DAT00/ **EC1_TXD3**	General Purpose Input/Output	AJ5	IO	OV_{DD}	---
GPIO4_DAT01/ **EC1_TXD2**	General Purpose Input/Output	AL5	IO	OV_{DD}	---
GPIO4_DAT02/ **EC1_TXD1**	General Purpose Input/Output	AM4	IO	OV_{DD}	---
GPIO4_DAT03/ **EC1_TXD0** / CLK_OUT2	General Purpose Input/Output	AN3	IO	OV_{DD}	---
GPIO4_DAT04/ **EC1_TX_EN**	General Purpose Input/Output	AN5	IO	OV_{DD}	---
GPIO4_DAT05/ **EC1_GTX_CLK**	General Purpose Input/Output	AJ3	IO	OV_{DD}	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GPIO4_DAT06/ **EC1_RXD3**	General Purpose Input/Output	AK2	IO	OV_{DD}	---
GPIO4_DAT07/ **EC1_RXD2**	General Purpose Input/Output	AL3	IO	OV_{DD}	---
GPIO4_DAT08/ **EC1_RXD1**	General Purpose Input/Output	AL1	IO	OV_{DD}	---
GPIO4_DAT09/ **EC1_RXD0**	General Purpose Input/Output	AN1	IO	OV_{DD}	---
GPIO4_DAT10/ **EC1_RX_CLK**	General Purpose Input/Output	AJ1	IO	OV_{DD}	---
GPIO4_DAT11/ **EC1_RX_DV**	General Purpose Input/Output	AP2	IO	OV_{DD}	---
GPIO4_DAT12/ **EC2_TXD3** / TSEC_1588_ALARM_OUT2	General Purpose Input/Output	AR5	IO	OV_{DD}	---
GPIO4_DAT13/ **EC2_TXD2** / TSEC_1588_ALARM_OUT1	General Purpose Input/Output	AT4	IO	OV_{DD}	---
GPIO4_DAT14/ **EC2_TXD1** / TSEC_1588_CLK_OUT	General Purpose Input/Output	AU3	IO	OV_{DD}	---
GPIO4_DAT15/ **EC2_TXD0** / TSEC_1588_PULSE_OUT2	General Purpose Input/Output	AU5	IO	OV_{DD}	---
GPIO4_DAT16/ **EC2_TX_EN**	General Purpose Input/Output	AV4	IO	OV_{DD}	---
GPIO4_DAT17/ **EC2_GTX_CLK**	General Purpose Input/Output	AP6	IO	OV_{DD}	---
GPIO4_DAT18/ **EC2_RXD3**	General Purpose Input/Output	AR1	IO	OV_{DD}	---
GPIO4_DAT19/ **EC2_RXD2**	General Purpose Input/Output	AU1	IO	OV_{DD}	---
GPIO4_DAT20/ **EC2_RXD1** / TSEC_1588_PULSE_OUT1	General Purpose Input/Output	AV2	IO	OV_{DD}	---
GPIO4_DAT21/ **EC2_RXD0** / TSEC_1588_TRIG_IN2	General Purpose Input/Output	AW3	IO	OV_{DD}	---
GPIO4_DAT22/ **EC2_RX_CLK** / TSEC_1588_CLK_IN	General Purpose Input/Output	AR3	IO	OV_{DD}	---
GPIO4_DAT23/ **EC2_RX_DV** / TSEC_1588_TRIG_IN1	General Purpose Input/Output	AW1	IO	OV_{DD}	---
GPIO4_DAT24/ **EC_GTX_CLK125**	General Purpose Input/Output	AW5	IO	OV_{DD}	---
GPIO4_DAT25/ **USB1_DRVVBUS** / cfg_soc_use	General Purpose Input/Output	D6	IO	OV_{DD}	1
GPIO4_DAT26/ **USB1_PWRFAULT**	General Purpose Input/Output	E5	IO	OV_{DD}	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GPIO4_DAT29/ SDHC1_DS / **SPI3_SCK**	General Purpose Input/Output	H2	IO	OV_{DD}	---
FlexTimer Module					
FTM1_CH0/ **IIC2_SCL** / GPIO1_DAT31 / SDHC1_CD_B	Channel 0	C3	IO	OV_{DD}	---
FTM1_CH1/ **CLK_OUT** / GPIO2_DAT07 /cfg_rcw_src3	Channel 1	AH6	O	OV_{DD}	1
FTM1_CH2/ **EVT1_B** / GPIO3_DAT13	Channel 2	T6	IO	OV_{DD}	---
FTM1_CH3/ **EVT3_B** / GPIO3_DAT15	Channel 3	Y4	IO	OV_{DD}	---
FTM1_CH4/ **IRQ00** / GPIO3_DAT00	Channel 4	R5	IO	OV_{DD}	---
FTM1_CH5/ **IRQ02** / GPIO3_DAT02	Channel 5	W3	IO	OV_{DD}	---
FTM1_CH6/ **IRQ04** / GPIO3_DAT04	Channel 6	T2	IO	OV_{DD}	---
FTM1_CH7/ **IRQ06** / GPIO3_DAT06	Channel 7	AB2	IO	OV_{DD}	---
FTM2_CH0/ **IIC2_SDA** / GPIO1_DAT30 /SDHC1_WP	Channel 0	D4	IO	OV_{DD}	---
FTM2_CH1/ **EVT0_B** / GPIO3_DAT12	Channel 1	T4	IO	OV_{DD}	---
FTM2_CH2/ **EVT2_B** / GPIO3_DAT14	Channel 2	U5	IO	OV_{DD}	---
FTM2_CH3/ **EVT4_B** / GPIO3_DAT16	Channel 3	AA3	IO	OV_{DD}	---
FTM2_CH4/ **IRQ01** / GPIO3_DAT01	Channel 4	P2	IO	OV_{DD}	---
FTM2_CH5/ **IRQ03** / GPIO3_DAT03	Channel 5	V2	IO	OV_{DD}	---
FTM2_CH6/ **IRQ05** / GPIO3_DAT05	Channel 6	W1	IO	OV_{DD}	---
FTM2_CH7/ **IRQ07** / GPIO3_DAT07	Channel 7	R1	IO	OV_{DD}	---
Controller Area Network					

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
CAN1_RX/ **IIC3_SDA** / GPIO1_DAT28 /EVT6_B	Receive Data	N5	I	OV_{DD}	1
CAN1_TX/ **IIC3_SCL** / GPIO1_DAT29 /EVT5_B	Transmit Data	P6	O	OV_{DD}	1
CAN2_RX/ **IIC4_SDA** / GPIO1_DAT26 /EVT8_B	Receive Data	L5	I	OV_{DD}	1
CAN2_TX/ **IIC4_SCL** / GPIO1_DAT27 /EVT7_B	Transmit Data	M4	O	OV_{DD}	1
Power-On-Reset Configuration					
cfg_eng_use0/ **XSPI1_A_SCK** / GPIO2_DAT22	Power-on-Reset Configuration	C23	I	OV_{DD}	1, 4
cfg_eng_use1/ **UART1_RTS_B** / GPIO1_DAT09 / UART3_SOUT	Power-on-Reset Configuration	AC5	I	OV_{DD}	1, 4
cfg_eng_use2/ **UART2_RTS_B** / GPIO1_DAT05 / UART4_SOUT	Power-on-Reset Configuration	AF6	I	OV_{DD}	1, 4
cfg_gpinput0/ **SDHC1_DAT0** / GPIO1_DAT17 /SPI1_SIN	General Input	E1	I	EV_{DD}	1, 4
cfg_gpinput1/ **SDHC1_DAT1** / GPIO1_DAT18 /SPI1_PCS2	General Input	F2	I	EV_{DD}	1, 4
cfg_gpinput2/ **SDHC1_DAT2** / GPIO1_DAT19 /SPI1_PCS1	General Input	G1	I	EV_{DD}	1, 4
cfg_gpinput3/ **SDHC1_DAT3** / GPIO1_DAT20 /SPI1_PCS0	General Input	G3	I	EV_{DD}	1, 4
cfg_gpinput4/ **SDHC2_DAT0** / GPIO2_DAT11 /SPI2_SIN / XSPI1_B_DATA0	General Input	A17	I	OV_{DD}	1, 4
cfg_gpinput5/ **SDHC2_DAT1** / GPIO2_DAT12 /SPI2_PCS2 / XSPI1_B_DATA1	General Input	B18	I	OV_{DD}	1, 4
cfg_gpinput6/ **SDHC2_DAT2** / GPIO2_DAT13 /SPI2_PCS1 / XSPI1_B_DATA2	General Input	C19	I	OV_{DD}	1, 4
cfg_gpinput7/ **SDHC2_DAT3** / GPIO2_DAT14 /SPI2_PCS0 / XSPI1_B_DATA3	General Input	C17	I	OV_{DD}	1, 4

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
cfg_rcw_src0/ **UART2_SOUT** / GPIO1_DAT07	Reset Configuration Word Source	AH4	I	OV_{DD}	1, 4
cfg_rcw_src1/ **UART1_SOUT** / GPIO1_DAT11	Reset Configuration Word Source	AD4	I	OV_{DD}	1, 4
cfg_rcw_src2/ **ASLEEP** / GPIO2_DAT06 /EVT9_B	Reset Configuration Word Source	AC1	I	OV_{DD}	1, 4
cfg_rcw_src3/ **CLK_OUT** / GPIO2_DAT07 /FTM1_CH1	Reset Configuration Word Source	AH6	I	OV_{DD}	1, 4
cfg_soc_use/ **USB1_DRVVBUS** / GPIO4_DAT25	Power-on-Reset Configuration	D6	I	OV_{DD}	1, 4
cfg_svr0/ **XSPI1_A_CS0_B** / GPIO2_DAT21	Power-on-Reset Configuration	C25	I	OV_{DD}	1, 4
cfg_svr1/ **XSPI1_A_CS1_B** / GPIO2_DAT20	Power-on-Reset Configuration	F24	I	OV_{DD}	1, 4
SPI1					
SPI1_PCS0/ **SDHC1_DAT3** / GPIO1_DAT20 /cfg_gpinput3	SPI Chip Select	G3	O	EV_{DD}	1
SPI1_PCS1/ **SDHC1_DAT2** / GPIO1_DAT19 /cfg_gpinput2	SPI Chip Select	G1	O	EV_{DD}	1
SPI1_PCS2/ **SDHC1_DAT1** / GPIO1_DAT18 /cfg_gpinput1	SPI Chip Select	F2	O	EV_{DD}	1
SPI1_PCS3/ SDHC1_VSEL / GPIO1_DAT15 /**SPI3_PCS0** / SDHC1_DAT4	SPI Chip Select	J3	O	OV_{DD}	1
SPI1_SCK/ **SDHC1_CLK** / GPIO1_DAT16	SPI Serial Clock	D2	O	EV_{DD}	1
SPI1_SIN/ **SDHC1_DAT0** / GPIO1_DAT17 /cfg_gpinput0	SPI Serial Data Input	E1	I	EV_{DD}	1
SPI1_SOUT/ **SDHC1_CMD** / GPIO1_DAT21	SPI Serial Data Output	E3	O	EV_{DD}	1
SPI2					
SPI2_PCS0/ **SDHC2_DAT3** / GPIO2_DAT14 / XSPI1_B_DATA3 / cfg_gpinput7	SPI Chip Select	C17	O	OV_{DD}	1
SPI2_PCS1/ **SDHC2_DAT2** / GPIO2_DAT13 /	SPI Chip Select	C19	O	OV_{DD}	1

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
XSPI1_B_DATA2 / cfg_gpinput6					
SPI2_PCS2/ **SDHC2_DAT1** / GPIO2_DAT12 / XSPI1_B_DATA1 / cfg_gpinput5	SPI Chip Select	B18	O	OV_{DD}	1
SPI2_PCS3/ **SDHC2_DS** / GPIO2_DAT10 / XSPI1_B_DQS	SPI Chip Select	A13	O	OV_{DD}	1
SPI2_SCK/ **SDHC2_CLK** / GPIO2_DAT09 / XSPI1_B_SCK	SPI Serial Clock	C13	O	OV_{DD}	1
SPI2_SIN/ **SDHC2_DAT0** / GPIO2_DAT11 / XSPI1_B_DATA0 / cfg_gpinput4	SPI Serial Data Input	A17	I	OV_{DD}	1
SPI2_SOUT/ **SDHC2_CMD** / GPIO2_DAT19 / XSPI1_B_CS1_B	SPI Serial Data Output	B12	O	OV_{DD}	1
SPI3					
SPI3_PCS0/ SDHC1_VSEL / GPIO1_DAT15 /SPI1_PCS3 / SDHC1_DAT4	SPI Chip Select	J3	O	OV_{DD}	1
SPI3_PCS1/ SDHC1_CMD_DIR / GPIO1_DAT14 / SDHC1_DAT5	SPI Chip Select	G5	O	OV_{DD}	1
SPI3_PCS2/ SDHC1_DAT0_DIR / GPIO1_DAT13 / SDHC1_DAT6	SPI Chip Select	H4	O	OV_{DD}	1
SPI3_PCS3/ SDHC1_DAT123_DIR / GPIO1_DAT12 / SDHC1_DAT7	SPI Chip Select	J5	O	OV_{DD}	1
SPI3_SCK/ SDHC1_DS / GPIO4_DAT29	SPI Serial Clock	H2	O	OV_{DD}	1
SPI3_SIN/ IIC5_SDA / GPIO1_DAT24 / SDHC1_CLK_SYNC_IN	SPI Serial Data Input	K2	I	OV_{DD}	1

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
SPI3_SOUT/ IIC5_SCL / GPIO1_DAT25 / SDHC1_CLK_SYNC_OUT	SPI Serial Data Output	J1	O	OV_{DD}	1
1588					
TSEC_1588_ALARM_OUT1/ **EC2_TXD2** /GPIO4_DAT13	Alarm Out	AT4	O	OV_{DD}	1
TSEC_1588_ALARM_OUT2/ **EC2_TXD3** /GPIO4_DAT12	Alarm Out	AR5	O	OV_{DD}	1
TSEC_1588_CLK_IN/ **EC2_RX_CLK** /GPIO4_DAT22	Clock Input	AR3	I	OV_{DD}	1
TSEC_1588_CLK_OUT/ **EC2_TXD1** /GPIO4_DAT14	Clock Out	AU3	O	OV_{DD}	1
TSEC_1588_PULSE_OUT1/ **EC2_RXD1** /GPIO4_DAT20	Pulse Out	AV2	O	OV_{DD}	1
TSEC_1588_PULSE_OUT2/ **EC2_TXD0** /GPIO4_DAT15	Pulse Out	AU5	O	OV_{DD}	1
TSEC_1588_TRIG_IN1/ **EC2_RX_DV** /GPIO4_DAT23	Trigger In	AW1	I	OV_{DD}	1
TSEC_1588_TRIG_IN2/ **EC2_RXD0** /GPIO4_DAT21	Trigger In	AW3	I	OV_{DD}	1
Dummy Signals					
DUMMY_A3	GND	A3	---	---	17
DUMMY_A47	GND	A47	---	---	17
DUMMY_B48	GND	B48	---	---	17
DUMMY_C1	GND	C1	---	---	17
DUMMY_BH2	SD_GND	BH2	---	---	17
DUMMY_BF48	GND	BF48	---	---	17
DUMMY_BH46	GND	BH46	---	---	17
DUMMY_BG1	SD_GND	BG1	---	---	17
Power and Ground Signals					
GND2	GND	A11	---	---	---
GND4	GND	B26	---	---	---
GND7	GND	C5	---	---	---
GND8	GND	C7	---	---	---
GND9	GND	C9	---	---	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GND10	GND	C11	---	---	---
GND11	GND	D14	---	---	---
GND12	GND	D16	---	---	---
GND13	GND	D18	---	---	---
GND14	GND	D20	---	---	---
GND15	GND	D22	---	---	---
GND16	GND	D26	---	---	---
GND17	GND	D28	---	---	---
GND18	GND	D30	---	---	---
GND19	GND	D32	---	---	---
GND20	GND	D34	---	---	---
GND21	GND	D36	---	---	---
GND22	GND	D38	---	---	---
GND23	GND	D40	---	---	---
GND24	GND	D42	---	---	---
GND25	GND	D44	---	---	---
GND26	GND	E7	---	---	---
GND27	GND	E9	---	---	---
GND28	GND	E45	---	---	---
GND29	GND	F4	---	---	---
GND30	GND	F42	---	---	---
GND31	GND	G7	---	---	---
GND32	GND	G9	---	---	---
GND33	GND	G33	---	---	---
GND34	GND	G39	---	---	---
GND35	GND	G45	---	---	---
GND36	GND	H18	---	---	---
GND37	GND	H22	---	---	---
GND38	GND	H26	---	---	---
GND39	GND	H30	---	---	---
GND40	GND	H42	---	---	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GND41	GND	J7	---	---	---
GND42	GND	J9	---	---	---
GND43	GND	J11	---	---	---
GND44	GND	J13	---	---	---
GND45	GND	J15	---	---	---
GND46	GND	J17	---	---	---
GND47	GND	J19	---	---	---
GND48	GND	J21	---	---	---
GND49	GND	J23	---	---	---
GND50	GND	J25	---	---	---
GND51	GND	J27	---	---	---
GND52	GND	J29	---	---	---
GND53	GND	J31	---	---	---
GND54	GND	J39	---	---	---
GND55	GND	J45	---	---	---
GND56	GND	K4	---	---	---
GND57	GND	K42	---	---	---
GND58	GND	L7	---	---	---
GND59	GND	L9	---	---	---
GND60	GND	L11	---	---	---
GND61	GND	L13	---	---	---
GND62	GND	L15	---	---	---
GND63	GND	L17	---	---	---
GND64	GND	L19	---	---	---
GND65	GND	L21	---	---	---
GND66	GND	L23	---	---	---
GND67	GND	L25	---	---	---
GND68	GND	L27	---	---	---
GND69	GND	L29	---	---	---
GND70	GND	L31	---	---	---
GND71	GND	L33	---	---	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GND72	GND	L39	---	---	---
GND73	GND	L45	---	---	---
GND74	GND	M42	---	---	---
GND75	GND	N9	---	---	---
GND76	GND	N11	---	---	---
GND77	GND	N13	---	---	---
GND78	GND	N15	---	---	---
GND79	GND	N17	---	---	---
GND80	GND	N19	---	---	---
GND81	GND	N21	---	---	---
GND82	GND	N23	---	---	---
GND83	GND	N25	---	---	---
GND84	GND	N27	---	---	---
GND85	GND	N29	---	---	---
GND86	GND	N31	---	---	---
GND87	GND	N39	---	---	---
GND88	GND	N45	---	---	---
GND89	GND	P4	---	---	---
GND90	GND	P42	---	---	---
GND91	GND	R7	---	---	---
GND92	GND	R9	---	---	---
GND93	GND	R11	---	---	---
GND94	GND	R13	---	---	---
GND95	GND	R15	---	---	---
GND96	GND	R17	---	---	---
GND97	GND	R19	---	---	---
GND98	GND	R21	---	---	---
GND99	GND	R23	---	---	---
GND100	GND	R25	---	---	---
GND101	GND	R27	---	---	---
GND102	GND	R29	---	---	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GND103	GND	R31	---	---	---
GND104	GND	R33	---	---	---
GND105	GND	R39	---	---	---
GND106	GND	R45	---	---	---
GND107	GND	T42	---	---	---
GND108	GND	U9	---	---	---
GND109	GND	U11	---	---	---
GND110	GND	U13	---	---	---
GND111	GND	U15	---	---	---
GND112	GND	U17	---	---	---
GND113	GND	U19	---	---	---
GND114	GND	U21	---	---	---
GND115	GND	U23	---	---	---
GND116	GND	U25	---	---	---
GND117	GND	U27	---	---	---
GND118	GND	U29	---	---	---
GND119	GND	U31	---	---	---
GND120	GND	U39	---	---	---
GND121	GND	U45	---	---	---
GND122	GND	V4	---	---	---
GND123	GND	V42	---	---	---
GND124	GND	W9	---	---	---
GND125	GND	W11	---	---	---
GND126	GND	W13	---	---	---
GND127	GND	W15	---	---	---
GND128	GND	W17	---	---	---
GND129	GND	W19	---	---	---
GND130	GND	W21	---	---	---
GND131	GND	W23	---	---	---
GND132	GND	W25	---	---	---
GND133	GND	W27	---	---	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GND134	GND	W29	---	---	---
GND135	GND	W31	---	---	---
GND136	GND	W33	---	---	---
GND137	GND	W39	---	---	---
GND138	GND	W45	---	---	---
GND139	GND	Y2	---	---	---
GND140	GND	Y42	---	---	---
GND141	GND	AA9	---	---	---
GND142	GND	AA11	---	---	---
GND143	GND	AA13	---	---	---
GND144	GND	AA15	---	---	---
GND145	GND	AA17	---	---	---
GND146	GND	AA19	---	---	---
GND147	GND	AA21	---	---	---
GND148	GND	AA23	---	---	---
GND149	GND	AA25	---	---	---
GND150	GND	AA27	---	---	---
GND151	GND	AA29	---	---	---
GND152	GND	AA31	---	---	---
GND153	GND	AA39	---	---	---
GND154	GND	AA45	---	---	---
GND155	GND	AB4	---	---	---
GND156	GND	AB6	---	---	---
GND157	GND	AB42	---	---	---
GND158	GND	AC9	---	---	---
GND159	GND	AC11	---	---	---
GND160	GND	AC13	---	---	---
GND161	GND	AC15	---	---	---
GND162	GND	AC17	---	---	---
GND163	GND	AC19	---	---	---
GND164	GND	AC21	---	---	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GND165	GND	AC23	---	---	---
GND166	GND	AC25	---	---	---
GND167	GND	AC27	---	---	---
GND168	GND	AC29	---	---	---
GND169	GND	AC31	---	---	---
GND170	GND	AC33	---	---	---
GND171	GND	AC39	---	---	---
GND172	GND	AC45	---	---	---
GND173	GND	AD2	---	---	---
GND174	GND	AE9	---	---	---
GND175	GND	AE11	---	---	---
GND176	GND	AE13	---	---	---
GND177	GND	AE15	---	---	---
GND178	GND	AE17	---	---	---
GND179	GND	AE19	---	---	---
GND180	GND	AE21	---	---	---
GND181	GND	AE23	---	---	---
GND182	GND	AE25	---	---	---
GND183	GND	AE27	---	---	---
GND184	GND	AE29	---	---	---
GND185	GND	AE31	---	---	---
GND186	GND	AE37	---	---	---
GND187	GND	AE41	---	---	---
GND188	GND	AE45	---	---	---
GND189	GND	AF4	---	---	---
GND190	GND	AG7	---	---	---
GND191	GND	AG9	---	---	---
GND192	GND	AG11	---	---	---
GND193	GND	AG13	---	---	---
GND194	GND	AG15	---	---	---
GND195	GND	AG17	---	---	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GND196	GND	AG19	---	---	---
GND197	GND	AG21	---	---	---
GND198	GND	AG23	---	---	---
GND199	GND	AG25	---	---	---
GND200	GND	AG27	---	---	---
GND201	GND	AG29	---	---	---
GND202	GND	AG31	---	---	---
GND203	GND	AG33	---	---	---
GND204	GND	AG45	---	---	---
GND205	GND	AH2	---	---	---
GND206	GND	AJ7	---	---	---
GND207	GND	AJ9	---	---	---
GND208	GND	AJ11	---	---	---
GND209	GND	AJ13	---	---	---
GND210	GND	AJ15	---	---	---
GND211	GND	AJ17	---	---	---
GND212	GND	AJ19	---	---	---
GND213	GND	AJ21	---	---	---
GND214	GND	AJ23	---	---	---
GND215	GND	AJ25	---	---	---
GND216	GND	AJ27	---	---	---
GND217	GND	AJ29	---	---	---
GND218	GND	AJ31	---	---	---
GND219	GND	AJ37	---	---	---
GND220	GND	AJ41	---	---	---
GND221	GND	AJ45	---	---	---
GND222	GND	AK4	---	---	---
GND223	GND	AL7	---	---	---
GND224	GND	AL9	---	---	---
GND225	GND	AL11	---	---	---
GND226	GND	AL13	---	---	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GND227	GND	AL15	---	---	---
GND228	GND	AL17	---	---	---
GND229	GND	AL19	---	---	---
GND230	GND	AL21	---	---	---
GND231	GND	AL23	---	---	---
GND232	GND	AL25	---	---	---
GND233	GND	AL27	---	---	---
GND234	GND	AL29	---	---	---
GND235	GND	AL31	---	---	---
GND236	GND	AL33	---	---	---
GND237	GND	AM2	---	---	---
GND238	GND	AN7	---	---	---
GND239	GND	AN9	---	---	---
GND240	GND	AN11	---	---	---
GND241	GND	AN13	---	---	---
GND242	GND	AN15	---	---	---
GND243	GND	AN17	---	---	---
GND244	GND	AN19	---	---	---
GND245	GND	AN21	---	---	---
GND246	GND	AN23	---	---	---
GND247	GND	AN25	---	---	---
GND248	GND	AN27	---	---	---
GND249	GND	AN29	---	---	---
GND250	GND	AN31	---	---	---
GND251	GND	AN37	---	---	---
GND252	GND	AN41	---	---	---
GND253	GND	AN45	---	---	---
GND254	GND	AP4	---	---	---
GND255	GND	AR7	---	---	---
GND256	GND	AR9	---	---	---
GND257	GND	AR11	---	---	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GND258	GND	AR13	---	---	---
GND259	GND	AR15	---	---	---
GND260	GND	AR17	---	---	---
GND261	GND	AR19	---	---	---
GND262	GND	AR21	---	---	---
GND263	GND	AR23	---	---	---
GND264	GND	AR25	---	---	---
GND265	GND	AR27	---	---	---
GND266	GND	AR29	---	---	---
GND267	GND	AR31	---	---	---
GND268	GND	AR33	---	---	---
GND269	GND	AT2	---	---	---
GND270	GND	AU7	---	---	---
GND271	GND	AU9	---	---	---
GND272	GND	AU11	---	---	---
GND273	GND	AU13	---	---	---
GND274	GND	AU15	---	---	---
GND275	GND	AU17	---	---	---
GND276	GND	AU19	---	---	---
GND277	GND	AU21	---	---	---
GND278	GND	AU23	---	---	---
GND279	GND	AU25	---	---	---
GND280	GND	AU27	---	---	---
GND281	GND	AU29	---	---	---
GND282	GND	AU31	---	---	---
GND283	GND	AU37	---	---	---
GND284	GND	AU41	---	---	---
GND285	GND	AU45	---	---	---
GND286	GND	AW7	---	---	---
GND287	GND	AW9	---	---	---
GND288	GND	AW11	---	---	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GND289	GND	AW13	---	---	---
GND290	GND	AW15	---	---	---
GND291	GND	AW17	---	---	---
GND292	GND	AW19	---	---	---
GND293	GND	AW21	---	---	---
GND294	GND	AW23	---	---	---
GND295	GND	AW25	---	---	---
GND296	GND	AW27	---	---	---
GND297	GND	AW29	---	---	---
GND298	GND	AW31	---	---	---
GND299	GND	AW33	---	---	---
GND300	GND	BA19	---	---	---
GND301	GND	BA21	---	---	---
GND302	GND	BA37	---	---	---
GND303	GND	BA41	---	---	---
GND304	GND	BA45	---	---	---
GND305	GND	BE33	---	---	---
GND306	GND	BE37	---	---	---
GND307	GND	BE41	---	---	---
GND308	GND	BE45	---	---	---
SENSEGND_CA	GND Sense pin	E17	---	---	---
SENSEGND_CB	GND Sense pin	D12	---	---	---
SENSEGND_PL	GND Sense pin	E11	---	---	---
SD_GND1	SerDes core logic ground	AY2	---	---	---
SD_GND2	SerDes core logic ground	AY4	---	---	---
SD_GND3	SerDes core logic ground	AY6	---	---	---
SD_GND4	SerDes core logic ground	BA3	---	---	---
SD_GND5	SerDes core logic ground	BA9	---	---	---
SD_GND6	SerDes core logic ground	BA11	---	---	---
SD_GND7	SerDes core logic ground	BA13	---	---	---
SD_GND8	SerDes core logic ground	BA15	---	---	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
SD_GND9	SerDes core logic ground	BA17	---	---	---
SD_GND10	SerDes core logic ground	BA23	---	---	---
SD_GND11	SerDes core logic ground	BA25	---	---	---
SD_GND12	SerDes core logic ground	BA27	---	---	---
SD_GND13	SerDes core logic ground	BA29	---	---	---
SD_GND14	SerDes core logic ground	BA31	---	---	---
SD_GND15	SerDes core logic ground	BB6	---	---	---
SD_GND16	SerDes core logic ground	BC3	---	---	---
SD_GND17	SerDes core logic ground	BC7	---	---	---
SD_GND18	SerDes core logic ground	BC9	---	---	---
SD_GND19	SerDes core logic ground	BC11	---	---	---
SD_GND20	SerDes core logic ground	BC13	---	---	---
SD_GND21	SerDes core logic ground	BC15	---	---	---
SD_GND22	SerDes core logic ground	BC17	---	---	---
SD_GND23	SerDes core logic ground	BC19	---	---	---
SD_GND24	SerDes core logic ground	BC21	---	---	---
SD_GND25	SerDes core logic ground	BC23	---	---	---
SD_GND26	SerDes core logic ground	BC25	---	---	---
SD_GND27	SerDes core logic ground	BC27	---	---	---
SD_GND28	SerDes core logic ground	BC29	---	---	---
SD_GND29	SerDes core logic ground	BC31	---	---	---
SD_GND30	SerDes core logic ground	BE3	---	---	---
SD_GND31	SerDes core logic ground	BE31	---	---	---
SD_GND32	SerDes core logic ground	BF4	---	---	---
SD_GND33	SerDes core logic ground	BF6	---	---	---
SD_GND34	SerDes core logic ground	BF8	---	---	---
SD_GND35	SerDes core logic ground	BF10	---	---	---
SD_GND36	SerDes core logic ground	BF12	---	---	---
SD_GND37	SerDes core logic ground	BF14	---	---	---
SD_GND38	SerDes core logic ground	BF16	---	---	---
SD_GND39	SerDes core logic ground	BF18	---	---	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
SD_GND40	SerDes core logic ground	BF20	---	---	---
SD_GND41	SerDes core logic ground	BF22	---	---	---
SD_GND42	SerDes core logic ground	BF24	---	---	---
SD_GND43	SerDes core logic ground	BF26	---	---	---
SD_GND44	SerDes core logic ground	BF28	---	---	---
SD_GND45	SerDes core logic ground	BF30	---	---	---
SD_GND47	SerDes core logic ground	BG31	---	---	---
OVDD1	General I/O supply	G21	---	OV_{DD}	---
OVDD2	General I/O supply	G23	---	OV_{DD}	---
OVDD3	General I/O supply	G25	---	OV_{DD}	---
OVDD4	General I/O supply	G27	---	OV_{DD}	---
OVDD5	General I/O supply	G29	---	OV_{DD}	---
OVDD6	General I/O supply	H20	---	OV_{DD}	---
OVDD7	General I/O supply	W7	---	OV_{DD}	---
OVDD8	General I/O supply	AA7	---	OV_{DD}	---
OVDD9	General I/O supply	AC7	---	OV_{DD}	---
OVDD10	General I/O supply	AE5	---	OV_{DD}	---
OVDD11	General I/O supply	AE7	---	OV_{DD}	---
OVDD12	General I/O supply	AK6	---	OV_{DD}	---
OVDD13	General I/O supply	AM6	---	OV_{DD}	---
EVDD1	eSDHC1 1.8V supply	T8	---	EV_{DD}	---
EVDD2	eSDHC1 1.8V supply	U7	---	EV_{DD}	---
GVDD1	DDR supply	H34	---	---	---
GVDD2	DDR supply	J33	---	---	---
GVDD3	DDR supply	K34	---	---	---
GVDD4	DDR supply	M34	---	---	---
GVDD5	DDR supply	N33	---	---	---
GVDD6	DDR supply	P34	---	---	---
GVDD7	DDR supply	U33	---	---	---
GVDD8	DDR supply	V34	---	---	---
GVDD9	DDR supply	Y34	---	---	---

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Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GVDD10	DDR supply	AA33	---	---	---
GVDD11	DDR supply	AB34	---	---	---
GVDD12	DDR supply	AD34	---	---	---
GVDD13	DDR supply	AE33	---	---	---
GVDD14	DDR supply	AF34	---	---	---
GVDD15	DDR supply	AJ33	---	---	---
GVDD16	DDR supply	AM34	---	---	---
GVDD17	DDR supply	AN33	---	---	---
GVDD18	DDR supply	AU33	---	---	---
FA1_CVL	Internal Use Only	BB34	---	FA1_CVL	12
FA2_DVL	Internal Use Only	F26	---	FA2_DVL	12
PROG_MTR	Internal Use Only	G15	---	PROG_MTR	12
TA_PROG_SFP	SFP Fuse Programming supply	F14	---	TA_PROG_SFP	---
TH_VDD	Thermal Monitor Unit supply	V6	---	TH_V_{DD}	---
VDD1	Supply for cores and platform	G31	---	V_{DD}	---
VDD2	Supply for cores and platform	H12	---	V_{DD}	---
VDD3	Supply for cores and platform	H14	---	V_{DD}	---
VDD4	Supply for cores and platform	H16	---	V_{DD}	---
VDD5	Supply for cores and platform	H24	---	V_{DD}	---
VDD6	Supply for cores and platform	H28	---	V_{DD}	---
VDD7	Supply for cores and platform	H32	---	V_{DD}	---
VDD8	Supply for cores and platform	K8	---	V_{DD}	---
VDD9	Supply for cores and platform	K10	---	V_{DD}	---
VDD10	Supply for cores and platform	K12	---	V_{DD}	---
VDD11	Supply for cores and platform	K14	---	V_{DD}	---
VDD12	Supply for cores and platform	K16	---	V_{DD}	---
VDD13	Supply for cores and platform	K18	---	V_{DD}	---
VDD14	Supply for cores and platform	K20	---	V_{DD}	---
VDD15	Supply for cores and platform	K22	---	V_{DD}	---
VDD16	Supply for cores and platform	K24	---	V_{DD}	---

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Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
VDD17	Supply for cores and platform	K26	---	V_{DD}	---
VDD18	Supply for cores and platform	K28	---	V_{DD}	---
VDD19	Supply for cores and platform	K30	---	V_{DD}	---
VDD20	Supply for cores and platform	K32	---	V_{DD}	---
VDD21	Supply for cores and platform	M8	---	V_{DD}	---
VDD22	Supply for cores and platform	M10	---	V_{DD}	---
VDD23	Supply for cores and platform	M12	---	V_{DD}	---
VDD24	Supply for cores and platform	M14	---	V_{DD}	---
VDD25	Supply for cores and platform	M16	---	V_{DD}	---
VDD26	Supply for cores and platform	M18	---	V_{DD}	---
VDD27	Supply for cores and platform	M20	---	V_{DD}	---
VDD28	Supply for cores and platform	M22	---	V_{DD}	---
VDD29	Supply for cores and platform	M24	---	V_{DD}	---
VDD30	Supply for cores and platform	M26	---	V_{DD}	---
VDD31	Supply for cores and platform	M28	---	V_{DD}	---
VDD32	Supply for cores and platform	M30	---	V_{DD}	---
VDD33	Supply for cores and platform	M32	---	V_{DD}	---
VDD34	Supply for cores and platform	P8	---	V_{DD}	---
VDD35	Supply for cores and platform	P10	---	V_{DD}	---
VDD36	Supply for cores and platform	P12	---	V_{DD}	---
VDD37	Supply for cores and platform	P14	---	V_{DD}	---
VDD38	Supply for cores and platform	P16	---	V_{DD}	---
VDD39	Supply for cores and platform	P18	---	V_{DD}	---
VDD40	Supply for cores and platform	P20	---	V_{DD}	---
VDD41	Supply for cores and platform	P22	---	V_{DD}	---
VDD42	Supply for cores and platform	P24	---	V_{DD}	---
VDD43	Supply for cores and platform	P26	---	V_{DD}	---
VDD44	Supply for cores and platform	P28	---	V_{DD}	---
VDD45	Supply for cores and platform	P30	---	V_{DD}	---
VDD46	Supply for cores and platform	P32	---	V_{DD}	---
VDD47	Supply for cores and platform	T10	---	V_{DD}	---

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Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
VDD48	Supply for cores and platform	T12	---	V_{DD}	---
VDD49	Supply for cores and platform	T14	---	V_{DD}	---
VDD50	Supply for cores and platform	T16	---	V_{DD}	---
VDD51	Supply for cores and platform	T18	---	V_{DD}	---
VDD52	Supply for cores and platform	T20	---	V_{DD}	---
VDD53	Supply for cores and platform	T22	---	V_{DD}	---
VDD54	Supply for cores and platform	T24	---	V_{DD}	---
VDD55	Supply for cores and platform	T26	---	V_{DD}	---
VDD56	Supply for cores and platform	T28	---	V_{DD}	---
VDD57	Supply for cores and platform	T30	---	V_{DD}	---
VDD58	Supply for cores and platform	T32	---	V_{DD}	---
VDD59	Supply for cores and platform	V8	---	V_{DD}	---
VDD60	Supply for cores and platform	V10	---	V_{DD}	---
VDD61	Supply for cores and platform	V12	---	V_{DD}	---
VDD62	Supply for cores and platform	V14	---	V_{DD}	---
VDD63	Supply for cores and platform	V16	---	V_{DD}	---
VDD64	Supply for cores and platform	V18	---	V_{DD}	---
VDD65	Supply for cores and platform	V20	---	V_{DD}	---
VDD66	Supply for cores and platform	V22	---	V_{DD}	---
VDD67	Supply for cores and platform	V24	---	V_{DD}	---
VDD68	Supply for cores and platform	V26	---	V_{DD}	---
VDD69	Supply for cores and platform	V28	---	V_{DD}	---
VDD70	Supply for cores and platform	V30	---	V_{DD}	---
VDD71	Supply for cores and platform	V32	---	V_{DD}	---
VDD72	Supply for cores and platform	Y8	---	V_{DD}	---
VDD73	Supply for cores and platform	Y10	---	V_{DD}	---
VDD74	Supply for cores and platform	Y12	---	V_{DD}	---
VDD75	Supply for cores and platform	Y14	---	V_{DD}	---
VDD76	Supply for cores and platform	Y16	---	V_{DD}	---
VDD77	Supply for cores and platform	Y18	---	V_{DD}	---
VDD78	Supply for cores and platform	Y20	---	V_{DD}	---

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Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
VDD79	Supply for cores and platform	Y22	---	V_{DD}	---
VDD80	Supply for cores and platform	Y24	---	V_{DD}	---
VDD81	Supply for cores and platform	Y26	---	V_{DD}	---
VDD82	Supply for cores and platform	Y28	---	V_{DD}	---
VDD83	Supply for cores and platform	Y30	---	V_{DD}	---
VDD84	Supply for cores and platform	Y32	---	V_{DD}	---
VDD85	Supply for cores and platform	AB8	---	V_{DD}	---
VDD86	Supply for cores and platform	AB10	---	V_{DD}	---
VDD87	Supply for cores and platform	AB12	---	V_{DD}	---
VDD88	Supply for cores and platform	AB14	---	V_{DD}	---
VDD89	Supply for cores and platform	AB16	---	V_{DD}	---
VDD90	Supply for cores and platform	AB18	---	V_{DD}	---
VDD91	Supply for cores and platform	AB20	---	V_{DD}	---
VDD92	Supply for cores and platform	AB22	---	V_{DD}	---
VDD93	Supply for cores and platform	AB24	---	V_{DD}	---
VDD94	Supply for cores and platform	AB26	---	V_{DD}	---
VDD95	Supply for cores and platform	AB28	---	V_{DD}	---
VDD96	Supply for cores and platform	AB30	---	V_{DD}	---
VDD97	Supply for cores and platform	AB32	---	V_{DD}	---
VDD98	Supply for cores and platform	AD8	---	V_{DD}	---
VDD99	Supply for cores and platform	AD10	---	V_{DD}	---
VDD100	Supply for cores and platform	AD12	---	V_{DD}	---
VDD101	Supply for cores and platform	AD14	---	V_{DD}	---
VDD102	Supply for cores and platform	AD16	---	V_{DD}	---
VDD103	Supply for cores and platform	AD18	---	V_{DD}	---
VDD104	Supply for cores and platform	AD20	---	V_{DD}	---
VDD105	Supply for cores and platform	AD22	---	V_{DD}	---
VDD106	Supply for cores and platform	AD24	---	V_{DD}	---
VDD107	Supply for cores and platform	AD26	---	V_{DD}	---
VDD108	Supply for cores and platform	AD32	---	V_{DD}	---
VDD109	Supply for cores and platform	AF8	---	V_{DD}	---

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Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
VDD110	Supply for cores and platform	AF10	---	V_{DD}	---
VDD111	Supply for cores and platform	AF12	---	V_{DD}	---
VDD112	Supply for cores and platform	AF14	---	V_{DD}	---
VDD113	Supply for cores and platform	AF16	---	V_{DD}	---
VDD114	Supply for cores and platform	AF18	---	V_{DD}	---
VDD115	Supply for cores and platform	AF20	---	V_{DD}	---
VDD116	Supply for cores and platform	AF22	---	V_{DD}	---
VDD117	Supply for cores and platform	AF24	---	V_{DD}	---
VDD118	Supply for cores and platform	AF26	---	V_{DD}	---
VDD119	Supply for cores and platform	AF28	---	V_{DD}	---
VDD120	Supply for cores and platform	AF30	---	V_{DD}	---
VDD121	Supply for cores and platform	AF32	---	V_{DD}	---
VDD122	Supply for cores and platform	AH8	---	V_{DD}	---
VDD123	Supply for cores and platform	AH10	---	V_{DD}	---
VDD124	Supply for cores and platform	AH12	---	V_{DD}	---
VDD125	Supply for cores and platform	AH14	---	V_{DD}	---
VDD126	Supply for cores and platform	AH16	---	V_{DD}	---
VDD127	Supply for cores and platform	AH18	---	V_{DD}	---
VDD128	Supply for cores and platform	AH20	---	V_{DD}	---
VDD129	Supply for cores and platform	AH22	---	V_{DD}	---
VDD130	Supply for cores and platform	AH24	---	V_{DD}	---
VDD131	Supply for cores and platform	AH26	---	V_{DD}	---
VDD132	Supply for cores and platform	AH28	---	V_{DD}	---
VDD133	Supply for cores and platform	AH30	---	V_{DD}	---
VDD134	Supply for cores and platform	AH32	---	V_{DD}	---
VDD135	Supply for cores and platform	AK8	---	V_{DD}	---
VDD136	Supply for cores and platform	AK10	---	V_{DD}	---
VDD137	Supply for cores and platform	AK12	---	V_{DD}	---
VDD138	Supply for cores and platform	AK14	---	V_{DD}	---
VDD139	Supply for cores and platform	AK16	---	V_{DD}	---
VDD140	Supply for cores and platform	AK18	---	V_{DD}	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
VDD141	Supply for cores and platform	AK20	---	V_{DD}	---
VDD142	Supply for cores and platform	AK22	---	V_{DD}	---
VDD143	Supply for cores and platform	AK24	---	V_{DD}	---
VDD144	Supply for cores and platform	AK26	---	V_{DD}	---
VDD145	Supply for cores and platform	AK28	---	V_{DD}	---
VDD146	Supply for cores and platform	AK30	---	V_{DD}	---
VDD147	Supply for cores and platform	AK32	---	V_{DD}	---
VDD148	Supply for cores and platform	AM8	---	V_{DD}	---
VDD149	Supply for cores and platform	AM10	---	V_{DD}	---
VDD150	Supply for cores and platform	AM12	---	V_{DD}	---
VDD151	Supply for cores and platform	AM14	---	V_{DD}	---
VDD152	Supply for cores and platform	AM16	---	V_{DD}	---
VDD153	Supply for cores and platform	AM18	---	V_{DD}	---
VDD154	Supply for cores and platform	AM20	---	V_{DD}	---
VDD155	Supply for cores and platform	AM22	---	V_{DD}	---
VDD156	Supply for cores and platform	AM24	---	V_{DD}	---
VDD157	Supply for cores and platform	AM26	---	V_{DD}	---
VDD158	Supply for cores and platform	AM28	---	V_{DD}	---
VDD159	Supply for cores and platform	AM30	---	V_{DD}	---
VDD160	Supply for cores and platform	AM32	---	V_{DD}	---
VDD161	Supply for cores and platform	AP8	---	V_{DD}	---
VDD162	Supply for cores and platform	AP10	---	V_{DD}	---
VDD163	Supply for cores and platform	AP12	---	V_{DD}	---
VDD164	Supply for cores and platform	AP14	---	V_{DD}	---
VDD165	Supply for cores and platform	AP16	---	V_{DD}	---
VDD166	Supply for cores and platform	AP18	---	V_{DD}	---
VDD167	Supply for cores and platform	AP20	---	V_{DD}	---
VDD168	Supply for cores and platform	AP22	---	V_{DD}	---
VDD169	Supply for cores and platform	AP24	---	V_{DD}	---
VDD170	Supply for cores and platform	AP26	---	V_{DD}	---
VDD171	Supply for cores and platform	AP28	---	V_{DD}	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
VDD172	Supply for cores and platform	AP30	---	V_{DD}	---
VDD173	Supply for cores and platform	AP32	---	V_{DD}	---
VDD174	Supply for cores and platform	AT8	---	V_{DD}	---
VDD175	Supply for cores and platform	AT10	---	V_{DD}	---
VDD176	Supply for cores and platform	AT12	---	V_{DD}	---
VDD177	Supply for cores and platform	AT14	---	V_{DD}	---
VDD178	Supply for cores and platform	AT16	---	V_{DD}	---
VDD179	Supply for cores and platform	AT18	---	V_{DD}	---
VDD180	Supply for cores and platform	AT20	---	V_{DD}	---
VDD181	Supply for cores and platform	AT22	---	V_{DD}	---
VDD182	Supply for cores and platform	AT24	---	V_{DD}	---
VDD183	Supply for cores and platform	AT26	---	V_{DD}	---
VDD184	Supply for cores and platform	AT28	---	V_{DD}	---
VDD185	Supply for cores and platform	AT30	---	V_{DD}	---
VDD186	Supply for cores and platform	AT32	---	V_{DD}	---
VDD187	Supply for cores and platform	AV8	---	V_{DD}	---
VDD188	Supply for cores and platform	AV10	---	V_{DD}	---
VDD189	Supply for cores and platform	AV12	---	V_{DD}	---
VDD190	Supply for cores and platform	AV14	---	V_{DD}	---
VDD191	Supply for cores and platform	AV16	---	V_{DD}	---
VDD192	Supply for cores and platform	AV18	---	V_{DD}	---
VDD193	Supply for cores and platform	AV20	---	V_{DD}	---
VDD194	Supply for cores and platform	AV22	---	V_{DD}	---
VDD195	Supply for cores and platform	AV24	---	V_{DD}	---
VDD196	Supply for cores and platform	AV26	---	V_{DD}	---
VDD197	Supply for cores and platform	AV28	---	V_{DD}	---
VDD198	Supply for cores and platform	AV30	---	V_{DD}	---
VDD199	Supply for cores and platform	AV32	---	V_{DD}	---
VDD200	Supply for cores and platform	AY20	---	V_{DD}	---
VDD201	Supply for cores and platform	AY34	---	V_{DD}	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
TA_BB_VDD	Low Power Security Monitor supply	AA5	---	$TA\_BB\_V_{DD}$	---
AVDD1	PLL analog power	AD28	---	AV_{DD}	---
AVDD2	PLL analog power	AD30	---	AV_{DD}	---
AVDD_D1	DDR PHY1 PLL supply	T34	---	AVDD_D1	---
USB_HVDD1	High voltage supply for High Speed operation	F8	---	USB_HV_{DD}	---
USB_HVDD2	High voltage supply for High Speed operation	H8	---	USB_HV_{DD}	---
USB_SDVDD1	Analog and digital high speed low voltage supply	F6	---	USB_SDV_{DD}	---
USB_SDVDD2	Analog and digital high speed low voltage supply	H6	---	USB_SDV_{DD}	---
USB_SVDD1	Analog and digital super speed low voltage supply	F10	---	USB_SV_{DD}	---
USB_SVDD2	Analog and digital super speed low voltage supply	H10	---	USB_SV_{DD}	---
AVDD_SD1_PLLF	SerDes1 Analog PLL fast supply	AY16	---	AVDD_SD1_PLLF	---
AVDD_SD1_PLLS	SerDes1 Analog PLL slow supply	BB16	---	AVDD_SD1_PLLS	---
AVDD_SD2_PLLF	SerDes2 Analog PLL fast supply	AY26	---	AVDD_SD2_PLLF	---
AVDD_SD2_PLLS	SerDes2 Analog PLL slow supply	BB28	---	AVDD_SD2_PLLS	---
SD_SVDD1	SerDes core logic supply	AY8	---	SD_SV_{DD}	---
SD_SVDD2	SerDes core logic supply	AY10	---	SD_SV_{DD}	---
SD_SVDD3	SerDes core logic supply	AY12	---	SD_SV_{DD}	---
SD_SVDD4	SerDes core logic supply	AY14	---	SD_SV_{DD}	---
SD_SVDD5	SerDes core logic supply	AY18	---	SD_SV_{DD}	---
SD_SVDD6	SerDes core logic supply	AY22	---	SD_SV_{DD}	---
SD_SVDD7	SerDes core logic supply	AY24	---	SD_SV_{DD}	---
SD_SVDD8	SerDes core logic supply	AY28	---	SD_SV_{DD}	---
SD_SVDD9	SerDes core logic supply	AY30	---	SD_SV_{DD}	---
SD_SVDD10	SerDes core logic supply	AY32	---	SD_SV_{DD}	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
SD_OVDD1	SerDes transceiver supply	BB8	---	SD_OV_{DD}	---
SD_OVDD2	SerDes transceiver supply	BB10	---	SD_OV_{DD}	---
SD_OVDD3	SerDes transceiver supply	BB12	---	SD_OV_{DD}	---
SD_OVDD4	SerDes transceiver supply	BB14	---	SD_OV_{DD}	---
SD_OVDD5	SerDes transceiver supply	BB22	---	SD_OV_{DD}	---
SD_OVDD6	SerDes transceiver supply	BB24	---	SD_OV_{DD}	---
SD_OVDD7	SerDes transceiver supply	BB26	---	SD_OV_{DD}	---
SD_OVDD8	SerDes transceiver supply	BB30	---	SD_OV_{DD}	---
SD_OVDD9	SerDes transceiver supply	BB32	---	SD_OV_{DD}	---
SENSEVDD_CA	VDD Sense pin	G17	---	SENSEVDD_CA	---
SENSEVDD_CB	VDD Sense pin	F12	---	SENSEVDD_CB	---
SENSEVDD_PL	VDD Sense pin	G11	---	SENSEVDD_PL	---
Reserved Pins					
RSVD_P46	Reserved	P46	---	---	---
RSVD_N35	Reserved	N35	---	---	---
RSVD_L41	Reserved	L41	---	---	---
RSVD_P36	Reserved	P36	---	---	---
RSVD_T36	Reserved	T36	---	---	---
RSVD_R35	Reserved	R35	---	---	---
RSVD_T38	Reserved	T38	---	---	---
RSVD_U35	Reserved	U35	---	---	---
RSVD_T40	Reserved	T40	---	---	---
RSVD_G37	Reserved	G37	---	---	---
RSVD_J35	Reserved	J35	---	---	---
RSVD_K36	Reserved	K36	---	---	---
RSVD_L35	Reserved	L35	---	---	---
RSVD_W35	Reserved	W35	---	---	---
RSVD_W37	Reserved	W37	---	---	---
RSVD_Y36	Reserved	Y36	---	---	---
RSVD_AA37	Reserved	AA37	---	---	---
RSVD_K40	Reserved	K40	---	---	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
RSVD_BH34	Reserved	BH34	---	---	---
RSVD_BH32	Reserved	BH32	---	---	---
RSVD_BF32	Reserved	BF32	---	---	---
RSVD_BG33	Reserved	BG33	---	---	---
RSVD_BH36	Reserved	BH36	---	---	---
RSVD_BH38	Reserved	BH38	---	---	---
RSVD_BD34	Reserved	BD34	---	---	---
RSVD_BD36	Reserved	BD36	---	---	---
RSVD_BD32	Reserved	BD32	---	---	---
RSVD_BE35	Reserved	BE35	---	---	---
RSVD_BC33	Reserved	BC33	---	---	---
RSVD_BF40	Reserved	BF40	---	---	---
RSVD_BH40	Reserved	BH40	---	---	---
RSVD_BH42	Reserved	BH42	---	---	---
RSVD_BH44	Reserved	BH44	---	---	---
RSVD_BC37	Reserved	BC37	---	---	---
RSVD_BC35	Reserved	BC35	---	---	---
RSVD_BD38	Reserved	BD38	---	---	---
RSVD_BB36	Reserved	BB36	---	---	---
RSVD_BG45	Reserved	BG45	---	---	---
RSVD_BG43	Reserved	BG43	---	---	---
RSVD_BF44	Reserved	BF44	---	---	---
RSVD_BC39	Reserved	BC39	---	---	---
RSVD_BC41	Reserved	BC41	---	---	---
RSVD_BB38	Reserved	BB38	---	---	---
RSVD_BB40	Reserved	BB40	---	---	---
RSVD_AY36	Reserved	AY36	---	---	---
RSVD_BD44	Reserved	BD44	---	---	---
RSVD_AW35	Reserved	AW35	---	---	---
RSVD_AT34	Reserved	AT34	---	---	---
RSVD_BE47	Reserved	BE47	---	---	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
RSVD_AW37	Reserved	AW37	---	---	---
RSVD_AT48	Reserved	AT48	---	---	---
RSVD_AK38	Reserved	AK38	---	---	---
RSVD_AP46	Reserved	AP46	---	---	---
RSVD_AM44	Reserved	AM44	---	---	---
RSVD_AT44	Reserved	AT44	---	---	---
RSVD_AJ35	Reserved	AJ35	---	---	---
RSVD_AP44	Reserved	AP44	---	---	---
RSVD_AN43	Reserved	AN43	---	---	---
RSVD_AH36	Reserved	AH36	---	---	---
RSVD_AJ39	Reserved	AJ39	---	---	---
RSVD_AH38	Reserved	AH38	---	---	---
RSVD_AK44	Reserved	AK44	---	---	---
RSVD_AR47	Reserved	AR47	---	---	---
RSVD_AP48	Reserved	AP48	---	---	---
RSVD_AK40	Reserved	AK40	---	---	---
RSVD_AN47	Reserved	AN47	---	---	---
RSVD_AK46	Reserved	AK46	---	---	---
RSVD_AF36	Reserved	AF36	---	---	---
RSVD_AK48	Reserved	AK48	---	---	---
RSVD_AG41	Reserved	AG41	---	---	---
RSVD_AG35	Reserved	AG35	---	---	---
RSVD_AM48	Reserved	AM48	---	---	---
RSVD_AL47	Reserved	AL47	---	---	---
RSVD_AG37	Reserved	AG37	---	---	---
RSVD_AC43	Reserved	AC43	---	---	---
RSVD_AE43	Reserved	AE43	---	---	---
RSVD_AD44	Reserved	AD44	---	---	---
RSVD_AD42	Reserved	AD42	---	---	---
RSVD_AB44	Reserved	AB44	---	---	---
RSVD_AF38	Reserved	AF38	---	---	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
RSVD_AF42	Reserved	AF42	---	---	---
RSVD_AF44	Reserved	AF44	---	---	---
RSVD_BC43	Reserved	BC43	---	---	---
RSVD_BB42	Reserved	BB42	---	---	---
RSVD_AV36	Reserved	AV36	---	---	---
RSVD_BD48	Reserved	BD48	---	---	---
RSVD_AY40	Reserved	AY40	---	---	---
RSVD_AU35	Reserved	AU35	---	---	---
RSVD_BC47	Reserved	BC47	---	---	---
RSVD_BB46	Reserved	BB46	---	---	---
RSVD_AV48	Reserved	AV48	---	---	---
RSVD_BF34	Reserved	BF34	---	---	---
RSVD_BF38	Reserved	BF38	---	---	---
RSVD_BE39	Reserved	BE39	---	---	---
RSVD_BF46	Reserved	BF46	---	---	---
RSVD_AM40	Reserved	AM40	---	---	---
RSVD_AL45	Reserved	AL45	---	---	---
RSVD_AJ43	Reserved	AJ43	---	---	---
RSVD_AG43	Reserved	AG43	---	---	---
RSVD_BD46	Reserved	BD46	---	---	---
RSVD_BF36	Reserved	BF36	---	---	---
RSVD_BF42	Reserved	BF42	---	---	---
RSVD_BE43	Reserved	BE43	---	---	---
RSVD_AY38	Reserved	AY38	---	---	---
RSVD_AL41	Reserved	AL41	---	---	---
RSVD_AL43	Reserved	AL43	---	---	---
RSVD_AG39	Reserved	AG39	---	---	---
RSVD_AE39	Reserved	AE39	---	---	---
RSVD_BA43	Reserved	BA43	---	---	---
RSVD_BG35	Reserved	BG35	---	---	---
RSVD_BG39	Reserved	BG39	---	---	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
RSVD_BD40	Reserved	BD40	---	---	---
RSVD_BG47	Reserved	BG47	---	---	---
RSVD_AL39	Reserved	AL39	---	---	---
RSVD_AM46	Reserved	AM46	---	---	---
RSVD_AH42	Reserved	AH42	---	---	---
RSVD_AH44	Reserved	AH44	---	---	---
RSVD_BC45	Reserved	BC45	---	---	---
RSVD_BG37	Reserved	BG37	---	---	---
RSVD_BG41	Reserved	BG41	---	---	---
RSVD_BD42	Reserved	BD42	---	---	---
RSVD_BA39	Reserved	BA39	---	---	---
RSVD_AM42	Reserved	AM42	---	---	---
RSVD_AK42	Reserved	AK42	---	---	---
RSVD_AH40	Reserved	AH40	---	---	---
RSVD_AF40	Reserved	AF40	---	---	---
RSVD_BB44	Reserved	BB44	---	---	---
RSVD_AT38	Reserved	AT38	---	---	---
RSVD_AP38	Reserved	AP38	---	---	---
RSVD_AY42	Reserved	AY42	---	---	---
RSVD_BB48	Reserved	BB48	---	---	---
RSVD_AU47	Reserved	AU47	---	---	---
RSVD_AV44	Reserved	AV44	---	---	---
RSVD_AY48	Reserved	AY48	---	---	---
RSVD_AN35	Reserved	AN35	---	---	---
RSVD_AW45	Reserved	AW45	---	---	---
RSVD_AY46	Reserved	AY46	---	---	---
RSVD_AP34	Reserved	AP34	---	---	---
RSVD_AT36	Reserved	AT36	---	---	---
RSVD_AR37	Reserved	AR37	---	---	---
RSVD_AU39	Reserved	AU39	---	---	---
RSVD_AL35	Reserved	AL35	---	---	---

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
RSVD_BA47	Reserved	BA47	---	---	---
RSVD_AY44	Reserved	AY44	---	---	---
RSVD_AP36	Reserved	AP36	---	---	---
RSVD_AR43	Reserved	AR43	---	---	---
RSVD_AR35	Reserved	AR35	---	---	---
RSVD_AR41	Reserved	AR41	---	---	---
RSVD_AM38	Reserved	AM38	---	---	---
RSVD_AM36	Reserved	AM36	---	---	---
RSVD_AK34	Reserved	AK34	---	---	---
RSVD_AN39	Reserved	AN39	---	---	---
RSVD_AL37	Reserved	AL37	---	---	---
RSVD_AK36	Reserved	AK36	---	---	---
RSVD_AW39	Reserved	AW39	---	---	---
RSVD_AV38	Reserved	AV38	---	---	---
RSVD_AW41	Reserved	AW41	---	---	---
RSVD_AV40	Reserved	AV40	---	---	---
RSVD_AV42	Reserved	AV42	---	---	---
RSVD_AR39	Reserved	AR39	---	---	---
RSVD_AV46	Reserved	AV46	---	---	---
RSVD_AT42	Reserved	AT42	---	---	---
RSVD_AW43	Reserved	AW43	---	---	---
RSVD_AT40	Reserved	AT40	---	---	---
RSVD_AW47	Reserved	AW47	---	---	---
RSVD_AU43	Reserved	AU43	---	---	---
RSVD_AP40	Reserved	AP40	---	---	---
RSVD_AP42	Reserved	AP42	---	---	---
RSVD_AT46	Reserved	AT46	---	---	---
RSVD_AR45	Reserved	AR45	---	---	---
RSVD_B2	Reserved	B2	---	---	---

1. Functionally, this pin is an output or an input, but structurally it is an I/O because it either sample configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.

Table continues on the next page...

Table 2. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
2. This output is actively driven during reset rather than being tri-stated during reset. 3. MDIC is grounded through a 240Ω precision 1% resistor. For either full or half driver strength calibration of DDR IOs, use the same MDIC resistor value of 240Ω. The memory controller register setting can be used to determine automatic calibration is done to full or half drive strength. This pin is used for automatic calibration of the DDR4 IOs. The MDIC pin must be connected to 240Ω precision 1% resistors. 4. This pin is a power-on-reset (POR) configuration pin. It has a weak internal pull-up resistor that is enabled during POR state only. The internal pull-up resistor allows the default value to be captured at POR de-assertion. This pull-up can be overpowered by an external pull-down resistor in case a change in the default value is required. See the Design Checklist for details. 5. Recommend that a weak pull-up resistor be placed on this pin to the respective power supply. Refer to the Design Checklist for details. 6. This pin is an open-drain signal. 7. This pin has a weak internal pull-up resistor that is always enabled. 8. These are test signals for factory use only and must be pulled up (100Ω to 1-kΩ) to the respective power supply for normal operation. 9. This pin requires a 200 Ω ± 1% pull-up resistor to respective power-supply. 10. Do not connect. These pins should be left floating. 11. This pin requires an external 1-kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven. 12. This pin must be pulled to GND. 13. This pin requires a 1.5 kΩ ± 1% pull-up resistor to respective power-supply. 14. These pins should be tied to ground if the diode is not utilized for temperature monitoring. 15. Attach 200 Ω ± 1% 100-ppm/C precision resistor-to-ground. Voltage range is between 0 to 250 mV. 16. Refer to the Design Checklist. 17. Dummy pins can be connected to the ground on the board. 18. Pin must **NOT** be pulled down during power-on reset. This pin may be pulled up, driven high, or if there are any externally connected devices, left in tristate. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset. 19. A 30.1 kΩ (±1%, ±100 ppm/ºC) resistor is required between the USBn_VBUS and the 5 V supply.					

2.3 Pin grouping links

2.3.1 DDR1

See the DDR1 pins.

2.3.2 I2C1

See the I2C1 pins.

2.3.3 I2C2

See the I2C2 pins.

2.3.4 I2C3

See the I2C3 pins.

2.3.5 I2C4

See the I2C4 pins.

2.3.6 I2C5

See the I2C5 pins.

2.3.7 I2C6

See the I2C6 pins.

2.3.8 I2C7

See the I2C7 pins.

2.3.9 I2C8

See the I2C8 pins.

2.3.10 XSPI1

See the XSPI1 pins.

2.3.11 ESDHC1

See the ESDHC1 pins.

2.3.12 ESDHC2

See the ESDHC2 pins.

2.3.13 UART1

See the UART1 pins.

2.3.14 UART2

See the UART2 pins.

2.3.15 UART3

See the UART3 pins.

2.3.16 UART4

See the UART4 pins.

2.3.17 Interrupt

See the Interrupt pins.

2.3.18 Trust

See the Trust pins.

2.3.19 System Control

See the System Control pins.

2.3.20 Clocking

See the Clocking pins.

2.3.21 Debug

See the Debug pins.

2.3.22 DFT

See the DFT pins.

2.3.23 JTAG

See the JTAG pins.

2.3.24 Analog Signals

See the Analog pins.

2.3.25 SerDes1

See the SerDes1 pins.

2.3.26 SerDes2

See the SerDes2 pins.

2.3.27 USB PHY

See the USB PHY pins.

2.3.28 EC1

See the EC1 pins.

2.3.29 EC2

See the EC2 pins.

2.3.30 Sync Ethernet Clockout

See the Sync Ethernet Clkout pins.

2.3.31 EMI1

See the EMI1 pins.

2.3.32 EMI2

See the EMI2 pins.

2.3.33 GPIO

See the GPIO pins.

2.3.34 FTM

See the FTM pins.

2.3.35 CAN

See the CAN pins.

2.3.36 Power-on-Reset Configuration

See the Power-on-Reset Configuration pins.

2.3.37 SPI1

See the SPI1 pins.

2.3.38 SPI2

See the SPI2 pins.

2.3.39 SPI3

See the SPI3 pins.

2.3.40 IEEE 1588

See the 1588 pins.

2.3.41 Dummy

See the Dummy pins.

2.3.42 Power and Ground

See the Power and Ground pins.

2.3.43 Reserved

See the Reserved pins.

3 Electrical characteristics

This section describes the DC and AC electrical specifications for the chip. The chip is currently targeted to these specifications, some of which are independent of the I/O cell but are included for a more complete reference. These are not purely I/O buffer design specifications.

3.1 Overall DC electrical characteristics

This section describes the ratings, conditions, and other characteristics.

3.1.1 Absolute maximum ratings

This table provides the absolute maximum ratings

Table 3. Absolute maximum ratings [5]

Characteristic	Symbol	Min	Max Value	Unit	Notes
Core and platform supply voltage	V_{DD}	-0.3	0.88	V	1
PLL supply voltage (core, platform, DDR)	AV_{DD}, AV_{DD}_D1	-0.3	1.98	V	-
SerDes analog PLL fast and PLL slow supply voltage	AV_{DD}_SD1_PLLF, AV_{DD}_SD2_PLLF, AV_{DD}_SD1_PLLS, AV_{DD}_SD2_PLLS	-0.3	0.99	V	-
SerDes 1 and SerDes 2 core logic supply	SD_SV_{DD}	-0.3	0.99	V	-
SerDes 1 and SerDes 2 transceiver supply	SD_OV_{DD}	-0.3	1.98	V	-
SFP fuse programming	TA_PROG_SFP	-0.3	1.98	V	-
Thermal monitor unit supply	TH_V_{DD}	-0.3	1.98	V	-
General I/O supply	OV_{DD}	-0.3	1.98	V	-
eSDHC1 supply (also includes some GPIO1 and SPI1 pins)	EV_{DD}	-0.3	1.8 V + 90 mV	V	-
DDR4 DRAM I/O voltage	GV_{DD}	-0.3	1.32	V	-
USB PHY 3.3V high supply voltage	USB_HV_{DD}	-0.3	3.63	V	-
USB PHY analog and digital HS supply	USB_SDV_{DD}	-0.3	0.88	V	-
USB PHY analog and digital SS supply	USB_SV_{DD}	-0.3	0.88	V	-
Low power security monitor supply	$TA\_BB\_V_{DD}$	-0.3	0.88	V	-
Input voltage for DDR4 DRAM signals	MV_{IN}	-0.3	GV_{DD} + 0.3	V	2
Input voltage for general I/O signals and interfaces powered by OV_{DD}	OV_{IN}	-0.3	OV_{DD} + 0.3	V	3, 4
Input voltage for SerDes signals	SV_{IN}	-0.4	SD_SV_{DD} + 0.3	V	4

Table continues on the next page...

Table 3. Absolute maximum ratings [5] (continued)

Characteristic	Symbol	Min	Max Value	Unit	Notes
Input voltage for USB PHY 3.3V HS signals	USB_HV_{IN}	-0.3	USB_HV_{DD} + 0.3	V	4
Input voltage for USB PHY SS signals	USB_SV_{IN}	-0.3	USB_SV_{DD} + 0.3	V	4
Input voltage for USBn_ID	USB_ID_{IN}	-0.3	1.8	V	
Input voltage for USBn_VBUS	USB_VBUS_{IN}	-0.3	3.3	V	
Input voltage for eSDHC1, GPIO1, and SPI1 signals powered by EV_{DD}	EV_{IN}	-0.3	EV_{DD} + 0.3	V	-
Storage temperature range	T_{STG}	-55	150	°C	6

1. Supply voltage specified at the voltage sense pin. Voltage input pins should be regulated to provide specified voltage at the sense pin.

2. Caution: MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

3. Caution: OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

4. (M, O, S)V_{IN}, $USBn\_SV_{IN}$, and $USBn\_HV_{IN}$ may overshoot/undershoot to a voltage and for a maximum duration as shown in the Overshoot/undershoot voltage figure at the end of this section.

5. Functional operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operations at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

6. Not to exceed 1008 hours cumulative at 150°C

3.1.2 Recommended Operating Conditions

This table provides the recommended operating conditions for this chip.

WARNING

The values shown are the recommended operating conditions and proper device operation outside these conditions is not guaranteed.

Table 4. Recommended operating conditions [6]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
VID core and platform supply voltage at boot	V_{DD}	0.850 - 30 mV	0.850	0.850 + 30 mV	V	1, 2, 3
VID core and platform supply voltage during normal operation	V_{DD}	VID - 30 mV	VID	VID + 30 mV	V	1, 2, 3
PLL supply voltage (core, platform, DDR)	AV_{DD}, AV_{DD}_D1	1.8 V - 90 mV	1.8	1.8 V + 90 mV	V	4

Table continues on the next page...

Table 4. Recommended operating conditions [6] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SerDes analog PLL fast and PLL slow supply voltage	AV_{DD}_SD1_PLLF, AV_{DD}_SD2_PLLF, AV_{DD}_SD1_PLLS, AV_{DD}_SD2_PLLS	0.9 V - 30 mV	0.9	0.9 V + 50 mV	V	-
SerDes 1 and SerDes 2 core logic supply	SD_SV_{DD}	0.9 V - 30 mV	0.9	0.9 V + 50 mV	V	-
SerDes 1 and SerDes 2 transceiver supply	SD_OV_{DD}	1.8 V - 90 mV	1.8	1.8 V + 90 mV	V	-
SFP fuse programming	TA_PROG_SFP	1.8 V - 90 mV	1.8	1.8 V + 90 mV	V	5
Thermal monitor unit supply	TH_V_{DD}	1.8 V - 90 mV	1.8	1.8 V + 90 mV	V	-
General I/O supply	OV_{DD}	1.8 V - 90 mV	1.8	1.8 V + 90 mV	V	-
eSDHC1 supply (also includes some GPIO1 and SPI1 pins)	EV_{DD}	1.8 V - 90 mV	1.8 V	1.8 V + 90 mV	V	-
DDR4 DRAM I/O voltage	GV_{DD}	1.2V - 60 mV	1.2	1.2 V + 60 mV	V	-
USB PHY 3.3V high supply voltage	USB_HV_{DD}	3.3 - 165 mV	3.3	3.3 V + 165 mV	V	-
USB PHY analog and digital HS supply	USB_SDV_{DD}	0.8 V - 30 mV	0.8	0.8 V + 50 mV	V	-
USB PHY analog and digital SS supply	USB_SV_{DD}	0.8 V - 30 mV	0.8	0.8 V + 30 mV	V	-
Low power supply monitor without battery	$TA\_BB\_V_{DD}$	VDD - 30 mV	VDD	VDD + 30 mV	V	-
Low power supply monitor with battery	$TA\_BB\_V_{DD}$	0.8 V - 30 mV	0.8	0.85 + 30 mV	V	-
Input voltage for DDR4 DRAM signals	MV_{IN}		GND to GnV_{DD}		V	-
Input voltage for general I/O signals and interfaces powered by OV_{DD}	OV_{IN}	-	GND to OV_{DD}	-	V	-
Input voltage for SerDes signals	SV_{IN}	-	-400 mV to +400 mV	-	V	-
Input voltage for USB PHY 3.3V HS signals	USB_HV_{IN}	-	GND to USB_HV_{DD}	-	V	-

Table continues on the next page...

Table 4. Recommended operating conditions [6] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Input voltage for USB PHY SS signals	USB_SV_{IN}	-	GND to USB_SVDD_{IN}	-	V	-
Input voltage for eSDHC1, GPIO1, and SPI1 signals powered by EV_{DD}	EV_{IN}	-	GND to EVDD	-	V	-
Normal operating temperature range	T_A/T_J	T_A = 5	-	T_J = 105	°C	-
Secure boot fuse programming operating temperature range	T_A/T_J	T_A = 0	-	T_J = 70	°C	5

1. Supply voltage specified at the voltage sense pin. Voltage input pins should be regulated to provide specified voltage at the sense pin.

2. Operation at 0.88V is allowable for up to 25 ms at initial power on.

3. Voltage ID (VID) operating range is between 0.775 V to 0.85 V. It is highly recommended to select a PMBus style regulator with a V_{out} range of at least 0.7 V to 0.9 V, with resolution of 12.5 mV or better.

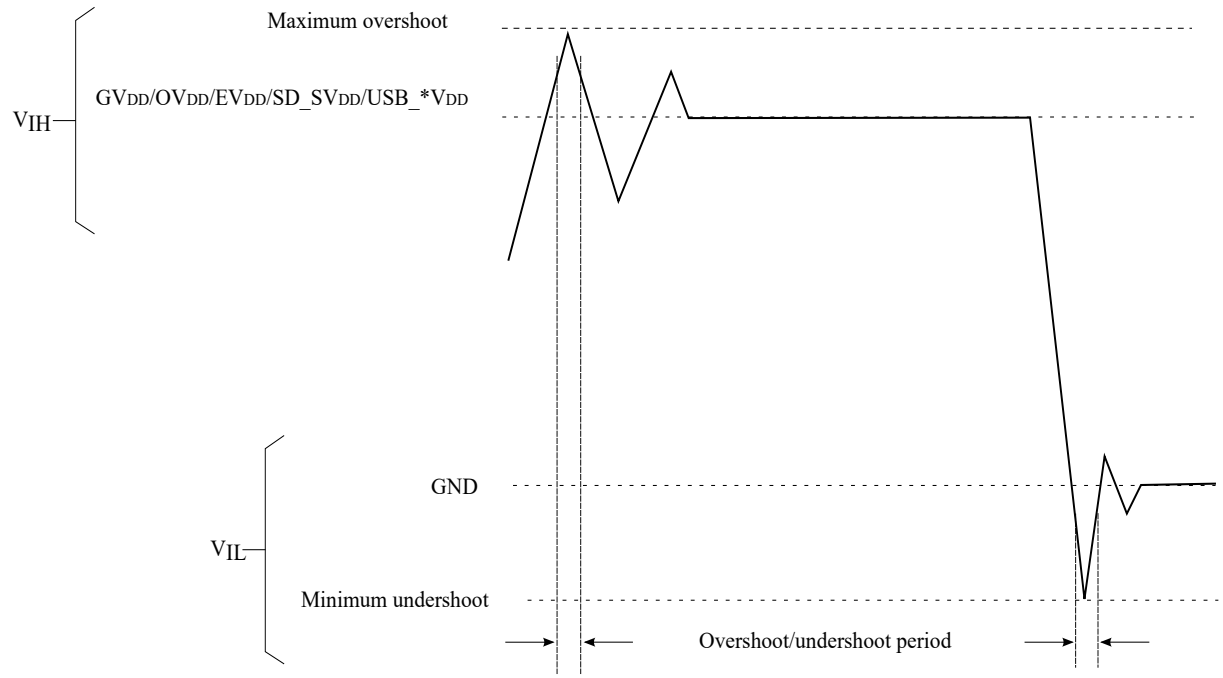
4. AV_{DD} and AV_{DD}_D1 are measured at the input to the filter and not at the pin of the device.

5. TA_PROG_SFP must be supplied 1.8V and the chip must operate in the specified fuse programming temperature range only during secure boot fuse programming. For all other operating conditions, PROG_SFP must be tied to GND, subject to the power sequencing constraints shown in Power Sequencing.

6. See Figure 6.

See the Recommended operating conditions table for actual recommended core voltage. Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in the Recommended operating conditions table. The input voltage threshold scales with respect to the associated I/O supply voltage. OVDD-based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses differential receivers referenced by the internally generated VREF signal. The DDR DQS receivers cannot be operated in single-ended fashion. The complement signal must be properly driven and cannot be grounded.

This figure shows the undershoot and overshoot voltages at the interfaces of the chip.



Note:

The overshoot/undershoot period should be less than 10% of shortest possible toggling period of the input signal or per input signal specific protocol requirement. For GPIO input signal overshoot/undershoot period, it should be less than 10% of the SYSCLK period.

Figure 6. Overshoot/undershoot voltage for GnV $_{DD}$/OV $_{DD}$/SD_SV $_{DD}$

3.1.3 Output drive capabilities

This chip provides information on the characteristics of the output driver strengths.

Table 5. Output drive capability [1, 2]

Driver Type	Minimum [1]	Typ	Maximum [2]	Supply_Voltage
General I/O signals	30	45	60	OV $_{DD}$ = 1.8V
1. Minimum values reflect estimated numbers based on best-case processed device. 2. Maximum values reflect estimated numbers based on worst-case processed device.				

3.2 General AC timing

This table provides AC timing specifications for the sections not covered under the specific interface sections.

Table 6. General AC timing specifications

Parameter	Symbol	Min	Max	Unit	Notes
Input signal rise and fall times	tR/tF	-	5	ns	1
1. Rise time refers to signal transitions from 10% to 90% of Supply; fall time refers to transitions from 90% to 10% of supply.					

3.3 Power sequencing

For power up, the following sequence should be followed:

1. During V_{DD} ramping, PORESET_B must be held low and TA_PROG_SFP must be grounded. All other power supplies (G*n*V_{DD}, OV_{DD}, EV_{DD}, USB_HV_{DD}, USB_SV_{DD}, USB_SDV_{DD}, SD_SV_{DD}, SD_OV_{DD}, $TA\_BB\_V_{DD}$, TH_V_{DD}, AV_{DD} (cores, platform, DDR), and AV_{DD}_SD*m*_PLL*n*) have no ordering requirement with respect to one another and with respect to V_{DD}. All supplies must be at their stable values within 400 ms.
2. Negate PORESET_B input as long as the required assertion/hold time has been met per the RESET initialization table.
3. For secure boot fuse programming, use the following steps:
    a. After negation of PORESET_B, drive TA_PROG_SFP = 1.80 V after a required minimum delay per Table 7.
    b. After fuse programming is completed, it is required to return TA_PROG_SFP = GND before the system is power cycled (PORESET_B assertion) or powered down (V_{DD} ramp down) per the required timing specified in Table 7. See Security fuse processor, for additional details.

NOTE

If using Trust Architecture Security Monitor battery backed features, prior to V_{DD} ramping up to 0.5 V level, ensure that SD_SV_{DD} is properly ramped and DIFF_SYSCLK_P / DIFF_SYSCLK_N is running. The clock should have a frequency of 100 MHz.

Warning

No activity other than that required for secure boot fuse programming is permitted while TA_PROG_SFP is driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while TA_PROG_SFP = GND.

Only 300,000 POR cycles are permitted per lifetime of a device. Note that this value is based on design estimates.

This figure provides the TA_PROG_SFP timing diagram.

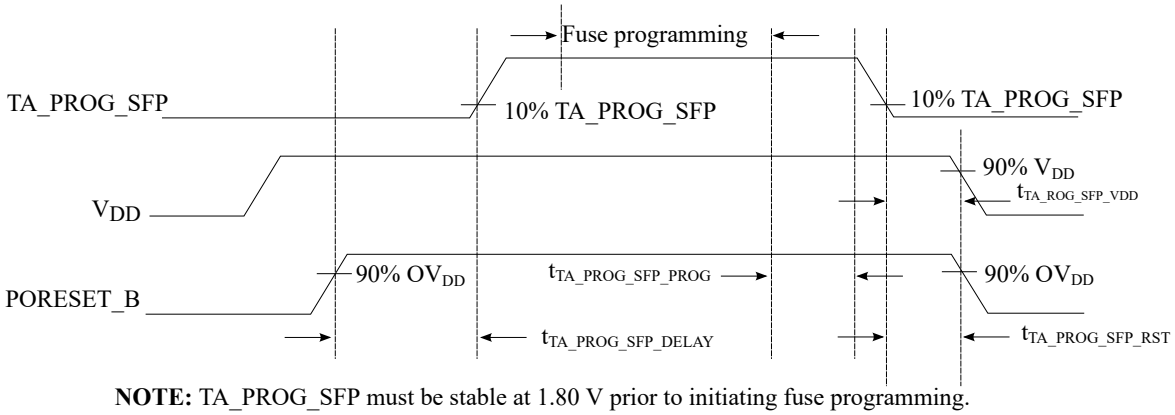


Figure 7. TA_PROG_SFP timing diagram

This table provides information on the power-down and power-up sequence parameters for TA_PROG_SFP.

Table 7. TA_PROG_SFP timing [5]

Driver type	Min	Max	Unit	Notes
$t_{TA\_PROG\_SFP\_DELAY}$	100	—	SYSCLKs	1
$t_{TA\_PROG\_SFP\_PROG}$	0	—	µs	2
$t_{TA\_PROG\_SFP\_VDD}$	0	—	µs	3
$t_{TA\_PROG\_SFP\_RST}$	0	—	µs	4

1. Delay required from the de-assertion of PORESET_B to driving TA_PROG_SFP ramp up. Delay measured from PORESET_B deassertion at 90% OV_{DD} to 10% TA_PROG_SFP ramp up.

2. Delay required from fuse programming finished to TA_PROG_SFP ramp down start. Fuse programming must complete while TA_PROG_SFP is stable at 1.80 V. No activity other than that required for secure boot fuse programming is permitted while TA_PROG_SFP driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while TA_PROG_SFP = GND. After fuse programming is completed, it is required to return TA_PROG_SFP = GND.

3. Delay required from TA_PROG_SFP ramp down complete to V_{DD} ramp down start. TA_PROG_SFP must be grounded to minimum 10% TA_PROG_SFP before V_{DD} is at 90% V_{DD}.

4. Delay required from TA_PROG_SFP ramp down complete to PORESET_B assertion. TA_PROG_SFP must be grounded to minimum 10% TA_PROG_SFP before PORESET_B assertion reaches 90% OV_{DD}.

5. Only two secure boot fuse programming events are permitted per lifetime of a device.

Warning

TA_PROG_SFP ramp up slew rate must not exceed 18,000V/s. Ramp down does not have a slew rate constraint.

3.4 Power-down requirements

The power-down cycle must complete such that power supply values are below 0.3 V before a new power-up cycle can be started.

If performing secure boot fuse programming per Power sequencing, it is required that TA_PROG_SFP = GND before the system is power cycled (PORESET_B assertion) or powered down (V_{DD} ramp down) per the required timing specified in Table 7.

NOTE

All input signals, including I/Os that are configured as inputs, driven into the chip need to monotonically increase/decrease through entire rise/fall durations.

3.5 Power characteristics

This table shows the thermal V_{DD} at 85ºC.

Table 8. Thermal V_{DD} power at 85°C

A72 frequency (MHz)	Coherency domain frequency (MHz)	Platform frequency (MHz)	DDR data rate (MHz)	Power (W)		
				LX2162A	LX2122A	LX2082A
2.0 GHz	1300	650	2900	23.9	21.6	20.1

Table continues on the next page...

Table 8. Thermal V_{DD} power at 85°C (continued)

A72 frequency (MHz)	Coherency domain frequency (MHz)	Platform frequency (MHz)	DDR data rate (MHz)	Power (W)		
				LX2162A	LX2122A	LX2082A

Notes:

1. Thermal power assumes Dhrystone running with activity factor of 60% (on all cores) and executing DMA on the platform. VDD must run at VID voltage level.

This table shows the estimated power dissipation on the TA_BB_V_{DD} supply for the LX2162A at allowable voltage levels.

Table 9. TA_BB_V_{DD} power dissipation

Supply	Maximum	Unit	Notes
TA_BB_V_{DD} (LX2xx2A off, 70°C)	36	uW	1
TA_BB_V_{DD} (LX2xx2A off, 40°C)	5	uW	1

Notes:

1. When the device is off, TA_BB_V_{DD} may be supplied by battery power to retain the Zeroizable Master Key and other trust architecture state. Board should implement a PMIC, which switches TA_BB_V_{DD} to battery when SoC powered down. See the device reference manual trust architecture chapter for more information.

3.6 Power-on ramp rate

This section describes the AC electrical specifications for the power-on ramp rate requirements. Controlling the maximum power-on ramp rate is required to avoid excess in-rush current.

This table provides the power supply ramp rate specifications.

Table 10. Power supply ramp rate

Parameter	Min	Max	Unit	Notes
Required ramp rate for all voltage supplies except those noted below	—	25	V/ms	1, 2
Required ramp rate for GV_{DD} and AV_{DD} supplies	—	5	V/ms	1, 2
Required ramp rate for TA_PROG_SFP supply	—	18	V/ms	1, 2

Notes:

1. Ramp rate is specified as a linear ramp from 10 to 90%. If non-linear (for example, exponential), the maximum rate of change from 200 to 500 mV is the most critical as this range might falsely trigger the ESD circuitry.

2. Over full recommended operating temperature range (see Recommended Operating Conditions).

3.7 Input clocks

3.7.1 USB reference clock specifications

The reference clock of the USB PHY is the DIFF_SYSCLK_P/DIFF_SYSCLK_N. Refer to Differential system clock (DIFF_SYSCLK_P/DIFF_SYSCLK_N) timing specifications.

3.7.2 Gigabit Ethernet reference clock timing

This table provides the Ethernet gigabit reference clock DC electrical characteristics with OV_{DD} = 1.8 V.

Table 11. EC_GTX_CLK125 DC electrical characteristics (OV_{DD} = 1.8 V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	—	—	V	2
Input low voltage	V_{IL}	—	—	0.3 x OV_{DD}	V	2
Input capacitance	C_{IN}	—	—	6	pF	—
Input current (V_{IN} = 0 V or V_{IN} = OV_{DD})	I_{IN}	—	—	± 50	μA	3

Notes:

1. For recommended operating conditions, see Recommended Operating Conditions.
2. The min V_{IL} and max V_{IH} values are based on the respective min and max V_{IN} values found in Recommended Operating Conditions.
3. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Recommended Operating Conditions.

This table provides the Ethernet gigabit reference clock AC timing specifications.

Table 12. EC_GTX_CLK125 AC timing specifications [1]

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
EC_GTX_CLK125 frequency	f_{G125}	125 - 100 ppm	125	125 + 100 ppm	MHz	—
EC_GTX_CLK125 cycle time	t_{G125}	-	8	-	ns	—
EC_GTX_CLK125 rise and fall time OV_{DD} = 1.8 V	t_{G125R}/t_{G125F}	—	—	0.75	ns	2
EC_GTX_CLK125 duty cycle 1000Base-T for RGMII	t_{G125H}/t_{G125}	40	—	60	%	3

Notes:

1. At recommended operating conditions with OV_{DD} = 1.8 V ± 90mV. See Recommended Operating Conditions.
2. Rise and fall times for EC_GTX_CLK125 are measured from 0.36 and 1.44 V for OV_{DD} = 1.8 V.
3. See RGMII AC timing specifications for duty cycle for the 10Base-T and 100Base-T reference clocks. The frequency of EC*n*_RX_CLK (input) should not exceed the frequency of EC_GTX_CLK125/EC*n*_TX_CLK (input) by more than 300 ppm.

3.7.3 DDR clock (DDRCLK)

This section provides the DDRCLK DC electrical characteristics and AC timing specifications.

3.7.3.1 DDRCLK DC electrical characteristics

This table provides the DDR clock (DDRCLK) DC electrical characteristics.

Table 13. DDRCLK DC electrical characteristics[3]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	—	—	V	1
Input low voltage	V_{IL}	—	—	0.3 x OV_{DD}	V	1
Input capacitance	C_{IN}	—	7	12	pF	—
Input current (V_{IN}= 0V or V_{IN} = OV_{DD})	I_{IN}	—	—	± 50	μA	2

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Recommended Operating Conditions.
2. The symbol OV_{IN}, in this case, represents the OV_{IN} symbol referenced in Recommended Operating Conditions.
3. At recommended operating conditions with OV_{DD} = 1.8 V. See Recommended Operating Conditions.

3.7.3.2 DDRCLK AC timing specifications

This table provides the DDR clock (DDRCLK) AC timing specifications.

Table 14. DDRCLK AC timing specifications[5]

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
DDRCLK frequency	f_{DDRCLK}		100		MHz	1, 2
DDRCLK frequency offset	F_{DDRCLK_OFFSET}	-300.0	—	300.0	ppm	
DDRCLK duty cycle	t_{KHK}/t_{DDRCLK}	42.5	50	57.5	%	2
DDRCLK slew rate	—	1.0	—	10	V/ns	3
DDRCLK peak period jitter	—	—	—	± 150	ps	4

Notes:

1. **Caution:** The memory controller complex PLL multiplier/ratio (RCW[MEM_PLL_RAT]) must be chosen such that the resulting DDR data rate does not exceed its respective maximum or minimum operating frequencies.
2. Measured at the rising edge and/or the falling edge at OV_{DD}/2.
3. Slew rate as measured from 0.25 x OV_{DD} to 0.75 x OV_{DD}.
4. Peak period jitter is calculated according to the JEDEC standard expression 8.22 * RMS jitter.
5. At recommended operating conditions with OV_{DD} = 1.8V. See Recommended Operating Conditions.

3.7.4 Differential system clock (DIFF_SYSCLK_P/DIFF_SYSCLK_N) timing specifications

The differential system clocking mode requires an on-board oscillator to provide reference clock input to the differential system clock pair (DIFF_SYSCLK_P/DIFF_SYSCLK_N).

This differential clock pair can be configured to provide the clock to core, platform, and USB PLLs.

This figure shows a receiver reference diagram of the differential system clock.

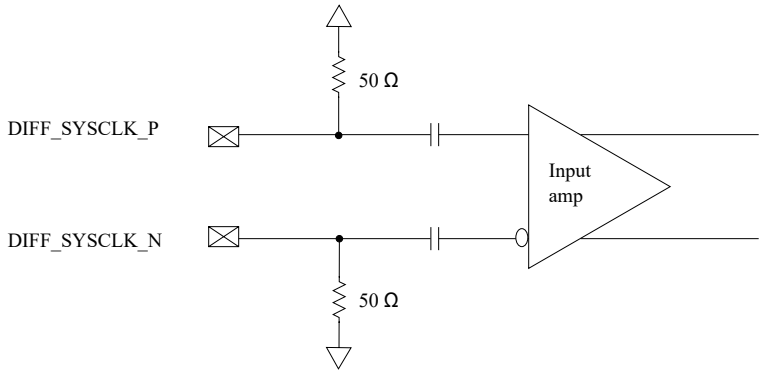


Figure 8. DIFF_SYSCLK_P/DIFF_SYSCLK_N receiver

This section provides the differential system clock DC and AC timing specifications.

3.7.4.1 Differential system clock DC electrical characteristics

For DC electrical characteristics, see DC-level requirement for SerDes reference clocks.

The differential system clock receiver's power supply voltage requirements ($SD\_SV_{DD)}$) are specified in Recommended Operating Conditions.

3.7.4.2 Differential system clock AC timing specifications

This table provides the differential system clock AC timing specificiatons.

For additional AC timing specifications, see SerDes reference clocks AC timing specifications.

Table 15. Differential System Clock AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Reference clock frequency	f_{SYSCLK}	-	100	-	MHz	-
Reference clock frequency-offset	F_{REF_OFFSET}	-300.0	-	300.0	ppm	-
Reference clock random jitter (RMS)	$JRMS_{REF\_CLK}$	-	-	2.6	ps	1, 2
Reference clock cycle-to-cycle jitter	DJ_{REF_CLK}	-	-	150.0	ps	3
Reference clock duty cycle	t_{KHK}/t_{SYSCLK}	40	-	60	%	-

1. 1.5 MHz to Nyquist frequency. For example, for 100 MHz reference clock, the Nyquist frequency is 50 MHz.

2. The peak-to-peak Rj specification is calculated at 14.069 times the RJ_{RMS} for 10^{-12} BER.

3. DJ across all frequencies.

3.7.5 Other input clocks

A description of the overall clocking of this device is available in the chip reference manual in the form of a clock subsystem block diagram. For information about the input clock requirements of functional modules sourced external of the chip, see the specific interface section.

3.8 Reset initialization timing specifications

This table provides the RESET initialization timing specifications.

Table 16. RESET initialization timing specifications

Parameter	Min	Max	Unit	Notes
Required assertion time of PORESET_B after SYSCLK/DIFF_SYSCLK and all power rails are stable	1.0	-	ms	1
Required input assertion time of HRESET_B	32.0	-	SYSCLKs	2, 3
Maximum rise/fall time of HRESET_B	-	10.0	SYSCLK	4
Maximum rise/fall time of PORESET_B	-	1	SYSCLK	4
Input setup time for POR configs with respect to negation of PORESET_B	4.0	-	SYSCLKs	2
Input hold time for all POR configs with respect to negation of PORESET_B	2.0	-	SYSCLKs	2
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of PORESET_B	-	5.0	SYSCLKs	2

1. PORESET_B must be driven asserted before the core and platform power supplies are powered up.

2. The DIFF_SYSCLK is the primary clock input for the chip.

3. The device asserts HRESET_B as an output when PORESET_B is asserted to initiate the power-on reset process. The device releases HRESET_B sometime after PORESET_B is deasserted. The exact sequence of HRESET_B deassertion is documented in the reference manual's "Power-on Reset Sequence" section.

4. The system/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

3.9 Battery-backed security monitor and tamper detect

This section describes the DC and AC electrical characteristics for the battery-backed security monitor interface, which includes the TA_BB_TMP_DETECT_B pin. It also describes the DC electrical characteristics for the TA_TMP_DETECT_B pin.

3.9.1 Battery-backed security monitor and tamper detect DC electrical characteristics

This table provides the DC electrical characteristics for the battery-backed security monitor interface (TA_BB_TMP_DETECT_B) operating at TA_BB_V_{DD}.

Table 17. Battery-backed security monitor interface DC electrical characteristics (TA_BB_V $_{DD}$ = VID) [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Input high voltage	V $_{IH}$	0.75 x TA_BB_VDD			V	2, 4
Input low voltage	V $_{IL}$		-	0.30 x TA_BB_VDD	V	2
Input current (V_{IN} = 0V or V_{IN} = TA_BB_V $_{DD}$)	I $_{IN}$	-	-	50.0	µA	3

1. For recommended operating conditions, see Recommended Operating Conditions.

2. The min V $_{IL}$ and max V $_{IH}$ values are based on the respective min and max TA_BB_V $_{IN}$ values found in Recommended Operating Conditions.

3. The symbol TA_BB_V $_{DD}$ represents the recommended operating voltage of the supply referenced in Recommended Operating Conditions.

4. If the signal falls below V_{IH}, it can cause a false trigger.

This table provides the DC electrical characteristics for the tamper detect security monitor (TA_TMP_DETECT_B) operating at OV_{DD}.

Table 18. Tamper detect monitor interface DC electrical characteristics (OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Input high voltage	V $_{IH}$	0.7 x OVDD			V	2, 4
Input low voltage	V $_{IL}$		-	0.3 x OVDD	V	2
Input current (V_{IN} = 0V or V_{IN} = OV_{IN})	I $_{IN}$	-	-	50.0	µA	3

1. For recommended operating conditions, see Recommended Operating Conditions.

2. The min V $_{IL}$ and max V $_{IH}$ values are based on the respective min and max OV $_{IN}$ values found in Recommended Operating Conditions.

3. The symbol OV $_{IN}$ represents the recommended operating voltage of the supply referenced in Recommended Operating Conditions.

4. If the signal falls below V_{IH}, it can cause a false trigger.

3.9.2 Battery-backed security monitor AC timing specifications

This table provides the AC timing specifications for the battery-backed security monitor interface.

Table 19. Battery-backed security monitor interface AC timing specifications

Parameter	Symbol	Min	Max	Unit	Notes
TA_BB_TMP_DETECT_B	t $_{TMP}$	100.0	-	ns	1

1. TA_BB_TMP_DETECT_B is asynchronous to any clock.

3.10 DDR4 SDRAM controller

This section describes the DC and AC electrical specifications for the DDR4 SDRAM controller interface. Note that the required GV_{DD}(typ) voltage is 1.2 V when interfacing to DDR4 SDRAM.

3.10.1 DDR4 SDRAM controller DC electrical characteristics

This table provides the recommended opearting conditions for the DDR SDRAM controller when interfacing to DDR4 SDRAM.

Table 20. DDR4 SDRAM interface DC electrical characteristics (GV_{DD} = 1.2V) [1, 6, 7]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	VREF + 0.085	—	V	2, 3
Input low voltage	V_{IL}	—	VREF - 0.085	V	2, 3
I/O leakage current	I_{IN}/I_{OZ}	-50	50	µA	4, 5

1. For recommended operating conditions, see Recommended Operating Conditions.
2. Input capacitance load for DQ, DQS, and DQS_B are available in the IBIS models.
3. Internal VREF is trained.
4. Refer to IBIS model for the complete output IV curve characteristics.
5. Output leakage is measured with all outputs diabled, 0 V ≤ V_{OUT} ≤ GV_{DD}. Applies to each pin.
6. GV_{DD} is expected to be within 60 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source. GV_{DD} min = 1.14 V, GV_{DD} max = 1.26 V, and GV_{DD} typ = 1.2 V.
7. VTT and VREFCA are applied directly to the DRAM device. Both VTT and VREFCA voltages must track GV_{DD}/2.

3.10.2 DDR4 SDRAM controller AC timing specifications

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR4 SDRAM.

Table 21. DDR4 SDRAM interface input AC timing specifications

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{ILAC}	-	VREF - 0.085	V	Internal VREF is trained.
AC input high voltage	V_{IHAC}	VREF + 0.085	-	V	Internal VREF is trained.

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR4 SDRAM.

Table 22. DDR4 SDRAM interface input AC timing specifications [3]

Parameter	Symbol	Min	Max	Unit	Notes
Controller Skew for MDQS-MDQ/MECC	t_{CISKEW}	-	-	ps	-
Data Rate of 1300 MT/s in DDR4		-125.0	125.0		1
Data Rate of 1600 MT/s in DDR4		-112.0	112.0		1

Table continues on the next page...

Table 22. DDR4 SDRAM interface input AC timing specifications [3] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Data Rate of 1800 MT/s in DDR4		-93.0	93.0		1
Data Rate of 2100 MT/s in DDR4		-82.0	82.0		1
Data Rate of 2400 MT/s in DDR4		-78.0	78.0		1
Data Rate of 2600 MT/s in DDR4		-74.0	74.0		1
Data Rate of 2900 MT/s in DDR4		-69.0	69.0		1
Tolerated Skew for MDQS-MDQ/MECC	t_{DISKEW}	-	-	ps	-
Data Rate of 1300 MT/s in DDR4		-250.0	250.0		2
Data Rate of 1600 MT/s in DDR4		-200.0	200.0		2
Data Rate of 1800 MT/s in DDR4		-175.0	175.0		2
Data Rate of 2100 MT/s in DDR4		-152.0	152.0		2
Data Rate of 2400 MT/s in DDR4		-130.0	130.0		2
Data Rate of 2600 MT/s in DDR4		-114.0	114.0		2
Data Rate of 2900 MT/s in DDR4		-102.0	102.0		2

1. t_{CISKEW} represents the amount of skew consumed by the controller between MDQS[n] and any corresponding bit that will be captured with MDQS[n]. This should be subtracted from the total timing budget.

2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: $t_{DISKEW} = +/-(T / 4 - abs(t_{CISKEW}))$, where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}.

3. See Figure 9.

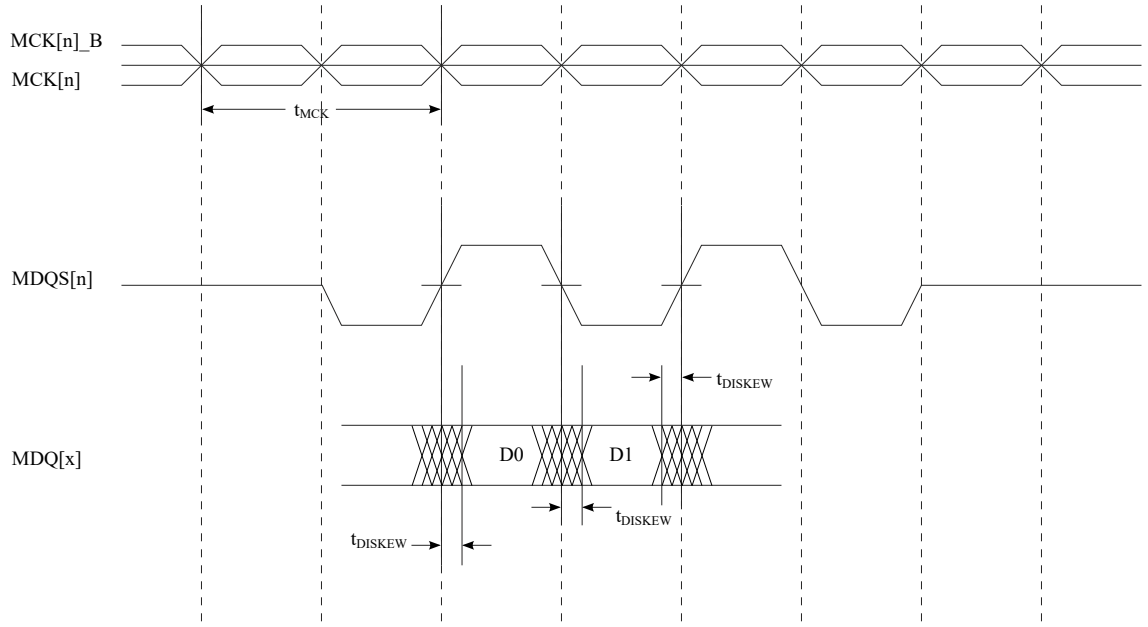


Figure 9. DDR4 SDRAM interface input timing diagram

This table contains the output AC timing targets for the DDR4 SDRAM interface.

Table 23. DDR4 SDRAM interface output AC timing specifications [6]

Parameter	Symbol	Min	Max	Unit	Notes
MCK[n] cycle time	t_{MCK}	625.0	1500.0	ps	1
ADDR/CMD/CNTL output setup with respect to MCK	t_{DDKHAS}	-	-	ps	-
Data Rate of 1300 MT/s in DDR4		606.0	-		3, 4
Data Rate of 1600 MT/s in DDR4		495.0	-		3, 4
Data Rate of 1800 MT/s in DDR4		410.0	-		3, 4
Data Rate of 2100 MT/s in DDR4		350.0	-		3, 4
Data Rate of 2400 MT/s in DDR4		321.0	-		3, 4
Data Rate of 2600 MT/s in DDR4		289.0	-		3, 4
Data Rate of 2900 MT/s in DDR4		263.0	-		3, 4
ADDR/CMD/CNTL output hold with respect to MCK	t_{DDKHAX}	-	-	ps	-
Data Rate of 1300 MT/s in DDR4		606.0	-		3, 4

Table continues on the next page...

Table 23. DDR4 SDRAM interface output AC timing specifications [6] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Data Rate of 1600 MT/s in DDR4		495.0	-		3, 4
Data Rate of 1800 MT/s in DDR4		390.0	-		3, 4
Data Rate of 2100 MT/s in DDR4		350.0	-		3, 4
Data Rate of 2400 MT/s in DDR4		321.0	-		3, 4
Data Rate of 2600 MT/s in DDR4		289.0	-		3, 4
Data Rate of 2900 MT/s in DDR4		263.0	-		3, 4
MDQ/MECC/MDM output data eye	$t_{DDKXDEYE}$	-	-	ps	-
Data Rate of 1300 MT/s in DDR4		500.0	-		4, 5
Data Rate of 1600 MT/s in DDR4		400.0	-		4, 5
Data Rate of 1800 MT/s in DDR4		350.0	-		4, 5
Data Rate of 2100 MT/s in DDR4		320.0	-		4, 5
Data Rate of 2400 MT/s in DDR4		280.0	-		4, 5
Data Rate of 2600 MT/s in DDR4		250.0	-		4, 5
Data Rate of 2900 MT/s in DDR4		225.0	-		4, 5
MDQS preamble	t_{DDKHMP}	0.9 * t_{MCK}	-	ps	4
MDQS postamble	t_{DDKHME}	0.4 * t_{MCK}	0.6 * t_{MCK}	ps	4

1. All MCK/MCK_B and MDQS/MDQS_B referenced measurements are made from the crossing of the two signals.

2. See Figure 9.

3. ADDR/CMD/CNTL includes all DDR SDRAM output signals except MCK/MCK_B, and MDQ/MECC/MDM/MDQS/MDQS_B.

4. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, tDDKHAS symbolizes DDR timing (DD) for the time tMCK memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time.

5. Available eye for data (MDQ), ECC (MECC), and data mask (MDM) outputs at the pin of the processor. Memory controller will center the strobe (MDQS) in the available data eye at the DRAM (end point) during the initialization.

6. See Figure 10.

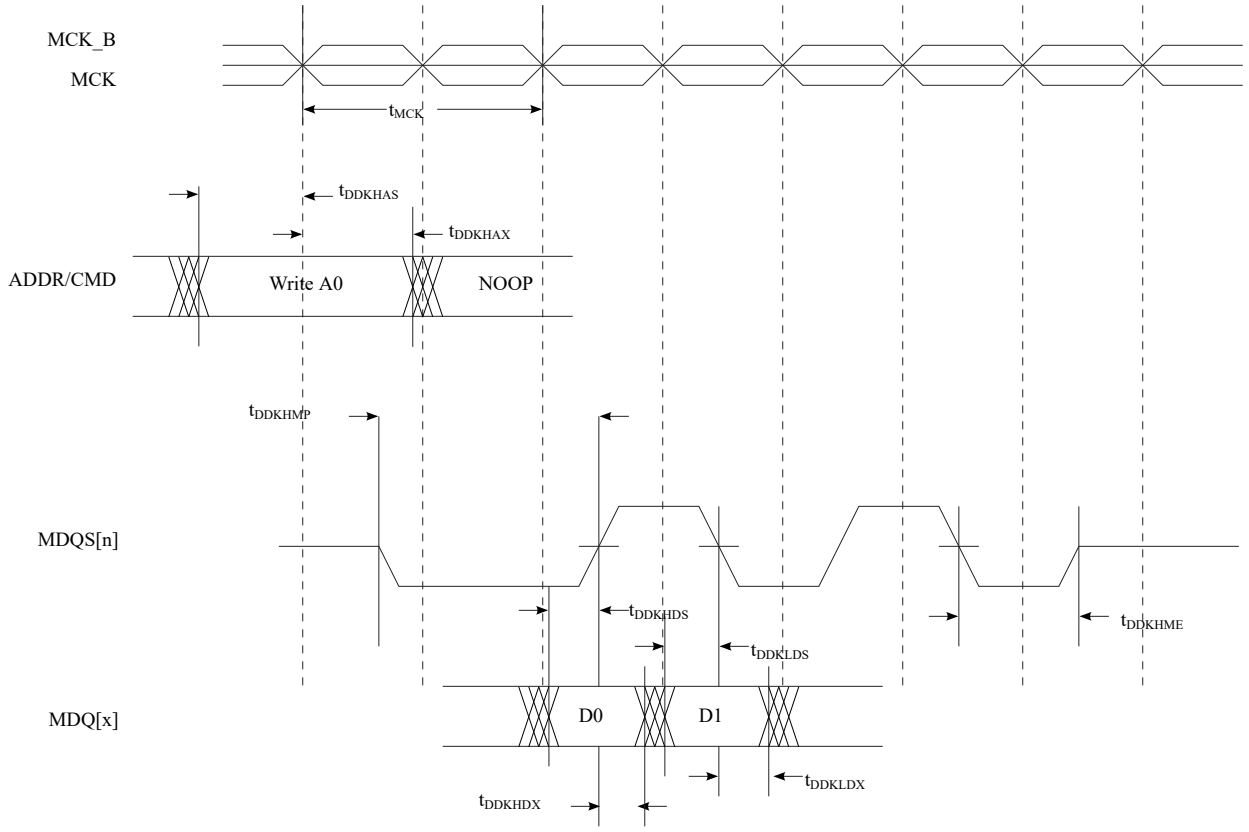


Figure 10. DDR4 SDRAM interface output timing diagram

3.11 Enhanced secure digital host controller (eSDHC)

This section describes the DC and AC electrical specifications for the eSDHC interface.

3.11.1 eSDHC DC electrical characteristics

This table provides the DC electrical characteristics for the eSDHC interface.

Table 24. eSDHC DC electrical characteristics (EV $_{DD}$/OV $_{DD}$ = 1.8V) [1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V $_{IH}$	0.7 x EV $_{DD}$/OV $_{DD}$	-	V	2
Input low voltage	V $_{IL}$	-	0.3 x EV $_{DD}$/OV $_{DD}$	V	2
Input/output leakage current	I $_{IN}$/I $_{OZ}$	-	-250/+50	µA	-
Output high voltage (I $_{OH}$ = -2mA at EV $_{DD}$/OV $_{DD}$ min)	V $_{OH}$	EV $_{DD}$/OV $_{DD}$ - 0.45	-	V	-
Output low voltage (I $_{OL}$ = 2mA at EV $_{DD}$/OV $_{DD}$ min)	V $_{OL}$	-	0.45	V	-

Table continues on the next page...

Table 24. eSDHC DC electrical characteristics (EV_{DD}/OV_{DD} = 1.8V) [1] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
1. For recommended operating conditions, see Recommended Operating Conditions. 2. The min V_{IL} and max V_{IH} values are based on the respective min and max EV_{IN}/OV_{IN} values found in Recommended Operating Conditions.					

3.11.2 eSDHC AC timing specifications

This table provides the eSDHC AC timing specifications as defined in the eSDHC clock input timing diagram.

Table 25. eSDHC AC timing specifications (full-speed mode) [1, 3, 5]

Parameter	Symbol	Min	Max	Unit	Notes
SDHC_CLK frequency SD/SDIO	f_{SHSCK}	0.0	25.0	MHz	1, 2, 3
SDHC_CLK frequency eMMC	f_{SHSCK}	0.0	26.0	MHz	1, 2, 3
SDHC_CLK clock low time	t_{SHSCKL}	10.0	-	ns	3
SDHC_CLK clock high time	t_{SHSCKH}	10.0	-	ns	3
SDHC_CLK clock rise and fall times	t_{SHSCKR}/t_{SHSCKF}	-	3.0	ns	3
Input setup times (SDHC_CMD, SDHC_DATx to SDHC_CLK)	$t_{SHSIVKH}$	2.5	-	ns	3, 4
Input hold times (SDHC_CMD, SDHC_DATx to SDHC_CLK)	$t_{SHSIXKH}$	2.5	-	ns	3
Output hold time (SDHC_CLK to SDHC_CMD, SDHC_DATx valid)	$t_{SHSKHOX}$	-3.0	-	ns	3
Output delay time (SDHC_CLK to SDHC_CMD, SDHC_DATx valid)	$t_{SHSKHOV}$	-	3.0	ns	3
1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SHKHOX} symbolizes eSDHC highspeed mode device timing (SH) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that in general, the clock reference symbol is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). 2. In full-speed mode, the clock frequency value can be 0-25MHz for an SD/SDIO card and 0-26MHz for an MMC card. 3. $C_{CARD} \leq 10$ pF, (1 card), and $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 40$ pF. 4. SDHC_SYNC_OUT/IN loop back is recommended to compensate the clock delay. In case the SDHC_SYNC_OUT/IN loopback is not used, to satisfy setup timing, one-way board-routing delay between host and card, on SDHC_CLK, SDHC_CMD, and SDHC_DATx should not exceed 1ns for any high-speed MMC card. For any high-speed or default speed mode SD card, the one-way board-routing delay between host and card, on SDHC_CLK, SDHC_CMD, and SDHC_DATx should not exceed 1.5ns. 5. See Figure 16.					

This table provides the eSDHC AC timing specifications as defined in the eSDHC clock input timing diagram.

Table 26. eSDHC AC timing specifications (high-speed mode) [1, 3, 5, 6, 7]

Parameter	Symbol	Min	Max	Unit	Notes
SDHC_CLK frequency SD/SDIO	f_{SHSCK}	0.0	50.0	MHz	1, 2, 3
SDHC_CLK frequency eMMC	f_{SHSCK}	0.0	52.0	MHz	1, 2, 3
SDHC_CLK clock low time	t_{SHSCKL}	7.0	-	ns	3
SDHC_CLK clock high time	t_{SHSCKH}	7.0	-	ns	3
SDHC_CLK clock rise and fall times	t_{SHSCKR}/t_{SHSCKF}	-	3.0	ns	3
Input setup times (SDHC_CMD, SDHC_DATx to SDHC_CLK)	$t_{SHSIVKH}$	2.5	-	ns	3, 4
Input hold times (SDHC_CMD, SDHC_DATx to SDHC_CLK)	$t_{SHSIXKH}$	2.5	-	ns	3
Output hold time (SDHC_CLK to SDHC_CMD, SDHC_DATx valid)	$t_{SHSKHOX}$	-3.0	-	ns	3
Output delay time (SDHC_CLK to SDHC_CMD, SDHC_DATx valid)	$t_{SHSKHOV}$	-	3.0	ns	3

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SHKHOX} symbolizes eSDHC highspeed mode device timing (SH) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that in general, the clock reference symbol is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

2. In high-speed mode, the clock frequency value can be 0-50MHz for an SD/SDIO card and 0-52MHz for an MMC card.

3. $C_{CARD} \leq 10$ pF, (1 card), and $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 40$ pF.

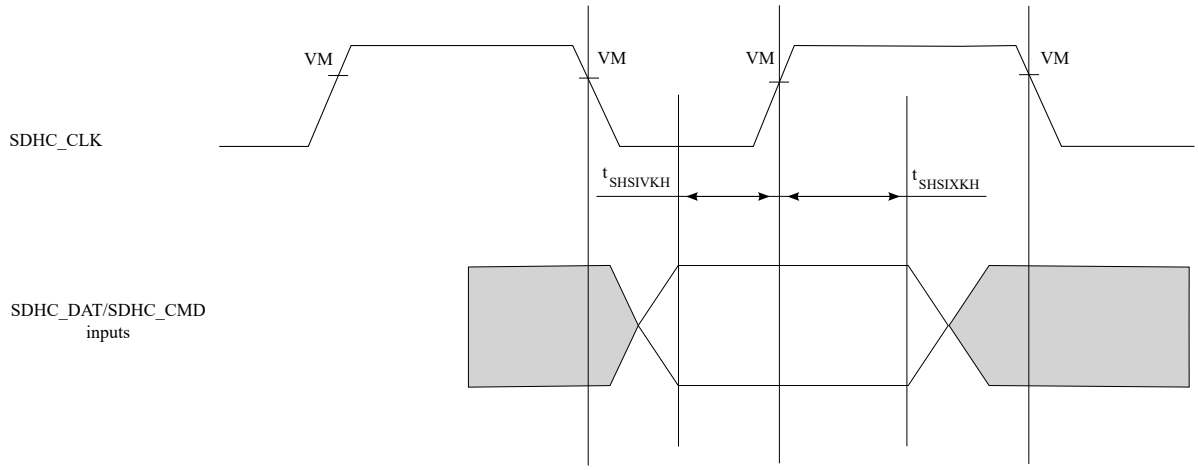
4. SDHC_SYNC_OUT/IN loop back is recommended to compensate the clock delay. In case the SDHC_SYNC_OUT/IN loopback is not used, to satisfy setup timing, one-way board-routing delay between host and card, on SDHC_CLK, SDHC_CMD, and SDHC_DATx should not exceed 1ns for any high-speed MMC card. For any high-speed or default speed mode SD card, the one-way board-routing delay between host and card, on SDHC_CLK, SDHC_CMD, and SDHC_DATx should not exceed 1.5ns.

5. See Figure 16.

6. See Figure 11.

7. See Figure 12.

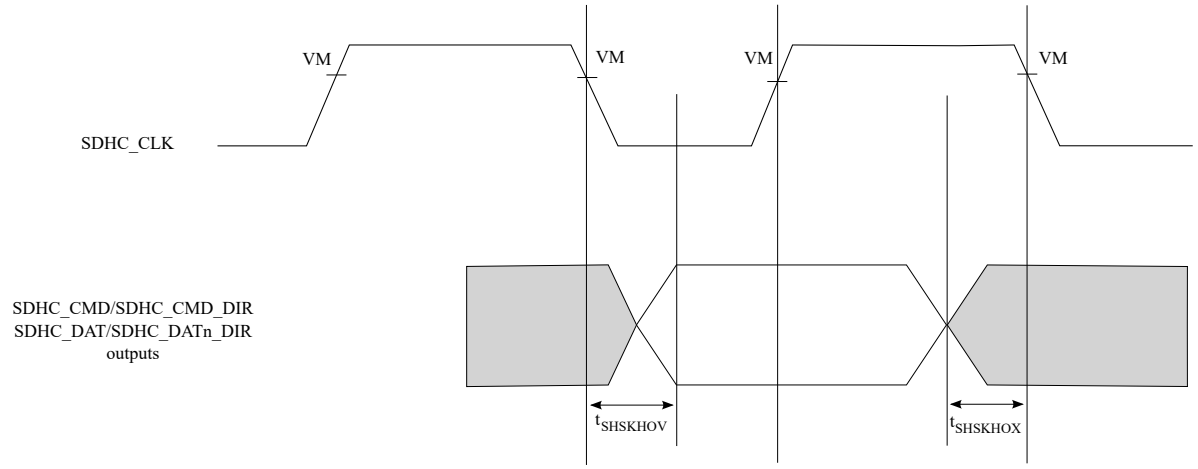
This figure provides the input AC timing diagram for high-speed mode.



VM = Midpoint Voltage (Respective supply / 2)

Figure 11. eSDHC high-speed mode input AC timing diagram

This figure provides the output AC timing diagram for high-speed mode.



VM = Midpoint Voltage (Respective supply / 2)

Figure 12. eSDHC high-speed mode output AC timing diagram

This table provides the SDHC1 and SDHC2 AC timing specifications for the DDR (1.8V) mode without voltage translator.

Table 27. SDHC1 and SDHC2 AC timing specifications (DDR (1.8V) mode without voltage translator) [1, 2, 3, 4]

Parameter	Symbol	Min	Max	Unit	Notes
SDHC_CLK duty cycle	t_{SHSCK}	47.0	53.0	%	6
SDHC_CLK frequency	f_{SHCK}		50.0	MHz	

Table continues on the next page...

Table 27. SDHC1 and SDHC2 AC timing specifications (DDR (1.8V) mode without voltage translator) [1, 2, 3, 4] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
SDHC_CLK rise and fall times	t_{SHCKR}/t_{SHCKF}		2.0	ns	
Skew between SDHC_CLK_SYNC_OUT and SDHC_CLK	t_{SHSKEW}				
SDHC1		-0.6	0.1	ns	
SDHC2		-0.275	0.275	ns	
Input setup times (SDHC_DATx to SDHC_CLK_SYNC_IN)	$t_{SHDIVKH}$	1.6		ns	5
Input hold times (SDHC_DATx to SDHC_CLK_SYNC_IN)	$t_{SHDIXKH}$	0.7		ns	5
Output hold time (SDHC_CLK to SDHC_DATx valid)	$t_{SHDKHOX}$	3.4		ns	5
Output delay time (SDHC_CLK to SDHC_DATx valid)	$t_{SHDKHOV}$		6.1	ns	5
Input setup time (SDHC_CMD to SDHC_CLK_SYNC_IN)	$t_{SHCIVKH}$	4.5		ns	5
Input hold time (SDHC_CMD to SDHC_CLK_SYNC_IN)	$t_{SHCIXKH}$	0.7		ns	5
Output hold time (SDHC_CLK to SDHC_CMD valid)	$t_{SHCKHOX}$	3.9		ns	5
Output delay time (SDHC_CLK to SDHC_CMD valid)	$t_{SHCKHOV}$		15.3	ns	5

1. $C_L = C_{BUS} + C_{HOST} + C_{CARD}$ ≤ 20 pF for MMC, ≤ 25pF for Input Data of DDR50, ≤ 30pF for Input CMD of DDR50.

2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SHKHOX} symbolizes eSDHC highspeed mode device timing (SH) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that in general, the clock reference symbol is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

3. See Figure 17.

4. See Figure 18.

5. Board skew: -0.2 to 0.2 ns

6. Characterized.

This table provides the eSDHC AC timing specifications for SDR104/eMMC HS200 mode without voltage translator.

Table 28. eSDHC AC timing specifications (SDR104/HS200 mode) [2, 3]

Parameter	Symbol	Min	Max	Unit	Notes
SDHC_CLK duty cycle	t_{SHSCK}	47.0	53.0	%	4
SDHC_CLK frequency	f_{SHCK}	-	-	MHz	-
SD/SDIO SDR104 mode		-	208.0		-
eMMC HS200 mode		-	200.0		-
SDHC_CLK rise and fall times	t_{SHCKR}/t_{SHCKF}	-	1.0	ns	1
Output hold time (SDHC_CLK to SDHC_CMD, SDHC_DATx valid)	T_{SHKHOX}	-	-	ns	-
SD/SDIO SDR104 mode		1.58	-		1
eMMC HS200 mode		1.6	-		1
Output delay time (SDHC_CLK to SDHC_CMD, SDHC_DATx valid)	T_{SHKHOV}	-	-	ns	-
SD/SDIO SDR104 mode		-	2.9		1
eMMC HS200 mode		-	3.0		1
Input data window (UI)	t_{SHIDV}	-	-	Unit interval	-
SD/SDIO SDR104 mode		0.5	-		1
eMMC HS200 mode		0.475	-		1

1. $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 15pF$.

2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SHKHOX} symbolizes eSDHC highspeed mode device timing (SH) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that in general, the clock reference symbol is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

3. See Figure 13.

4. Characterized.

This figure provides the eSDHC SDR104/HS200 mode timing diagram.

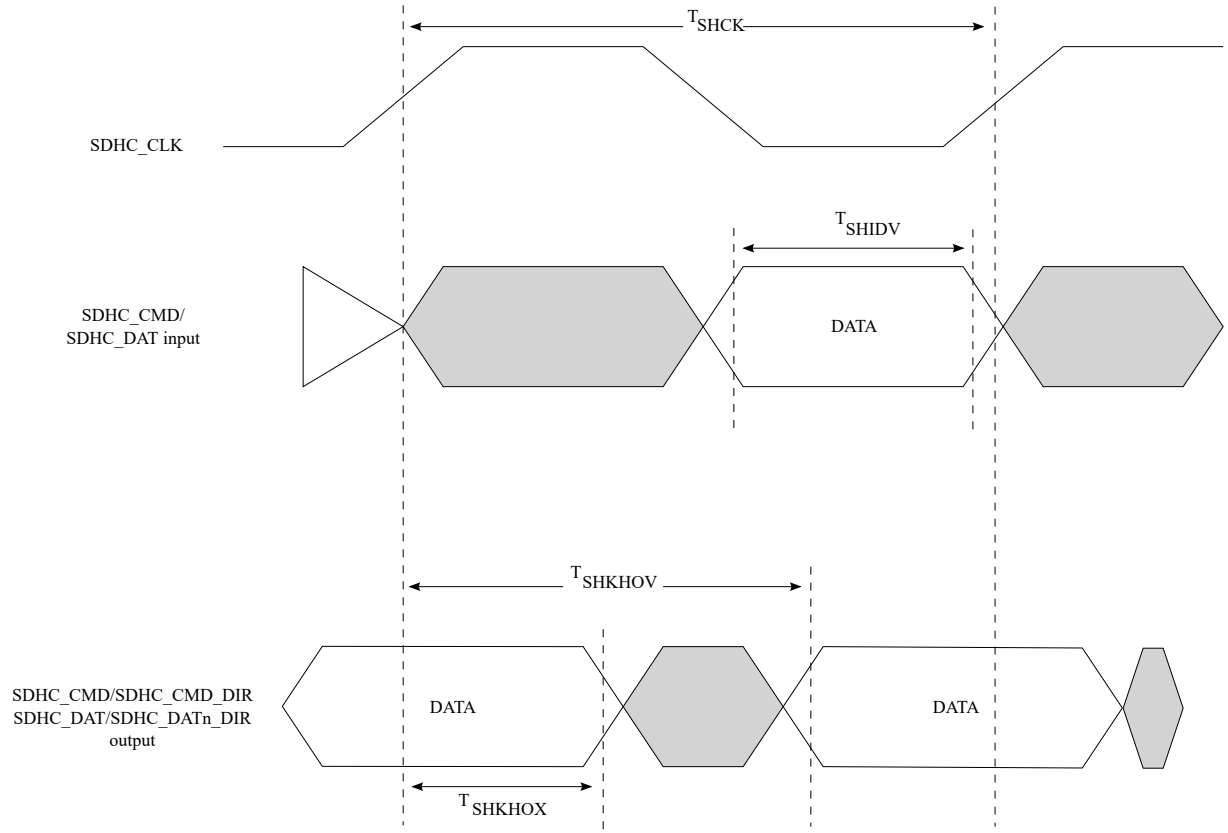


Figure 13. eSDHC SDR104/HS200 mode timing diagram

This table provides the eSDHC AC timing specifications for eMMC HS400 mode.

Table 29. eSDHC AC timing specifications (HS400 mode) [2, 3, 4, 5]

Parameter	Symbol	Min	Max	Unit	Notes
SDHC_CLK frequency	f_{SHCK}	-	200.0	MHz	-
Output hold time (SDHC_CLK to SDHC_CMD, SDHC_DATx valid)	T_{SHKHOX}	0.75	-	ns	1
Output delay time (SDHC_CLK to SDHC_CMD, SDHC_DATx valid)	T_{SHKHOV}	-	1.75	ns	1
Data valid skew to DQS	T_{SHRQV}	-	0.45	ns	1
Data hold skew to DQS	T_{SHRQHX}	-	0.45	ns	1
Command valid skew to DQS	T_{SHRQV_CMD}	-	0.45	ns	1
Command hold skew to DQS	T_{SHRQHX_CMD}	-	0.45	ns	1

Table continues on the next page...

Table 29. eSDHC AC timing specifications (HS400 mode) [2, 3, 4, 5] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
DQS pulse width	$T_{SHDSPWS}$	1.97	-	ns	1
Duty cycle distortion	t_{SHSCK_DIS}	0.0	0.3	ns	1, 6

1. $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 15pF$.

2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SHKHOX} symbolizes eSDHC highspeed mode device timing (SH) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that in general, the clock reference symbol is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

3. See Figure 14.

4. See Figure 15.

5. For HS400 without enhanced strobe (DQS) command, see Figure 13.

6. Characterized.

This figure provides the eSDHC HS400 mode input timing diagram.

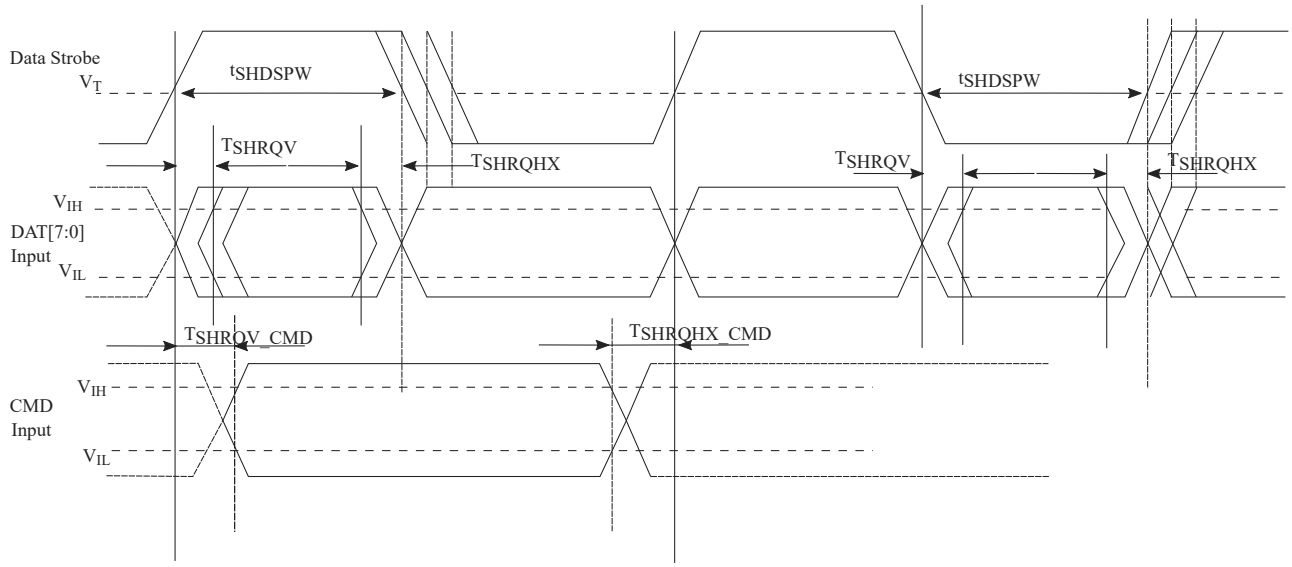


Figure 14. eSDHC HS400 mode input timing diagram

This figure provides the eSDHC HS400 mode output timing diagram.

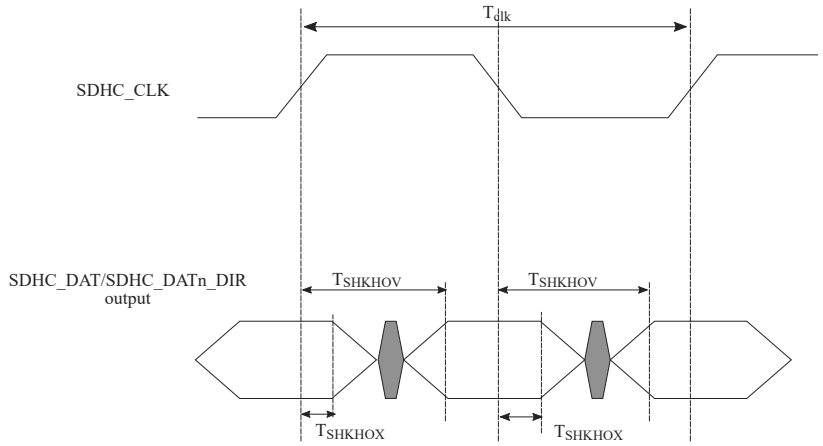


Figure 15. eSDHC HS400 mode output timing diagram

This figure provides the eSDHC clock input timing diagram.

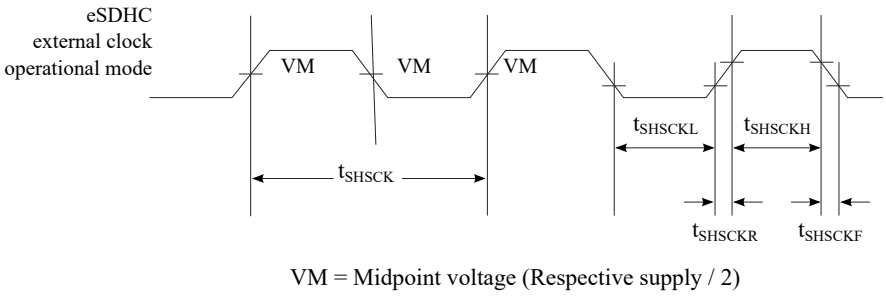


Figure 16. eSDHC clock input timing diagram

This figure provides the eSDHC DDR50/DDR mode input AC timing diagram.

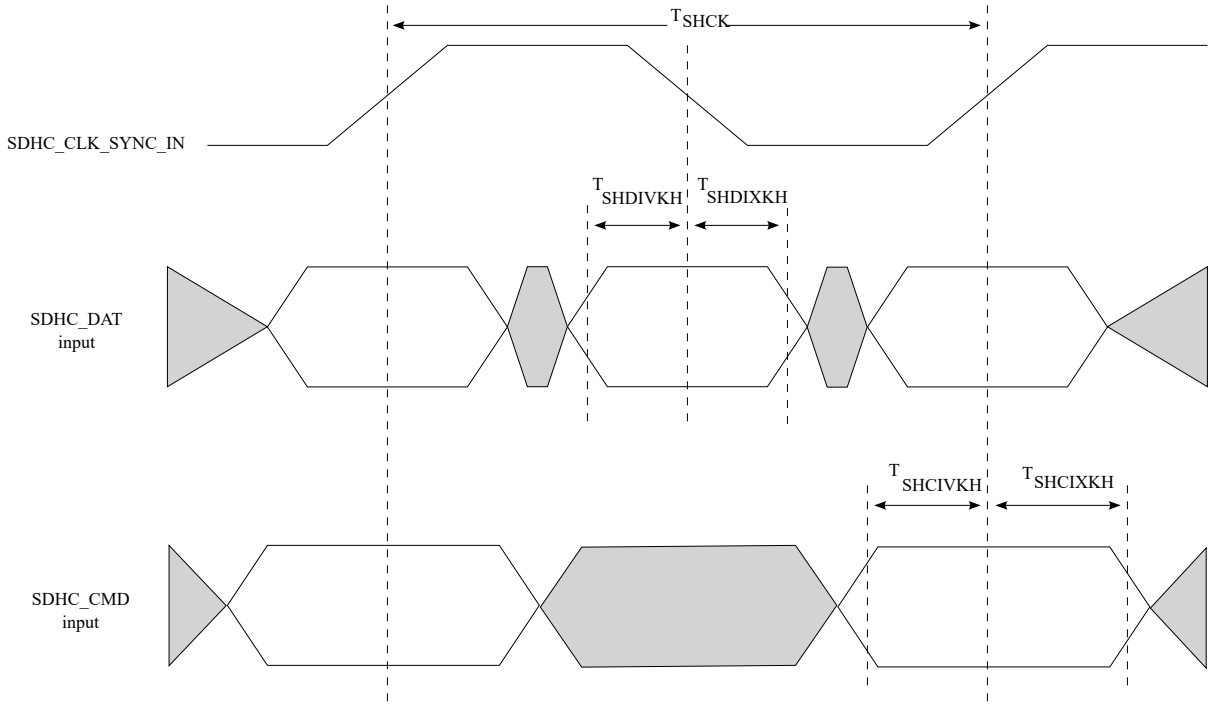


Figure 17. eSDHC DDR50/DDR mode input AC timing diagram

This figure provides the eSDHC DDR50/DDR mode output AC timing diagram.

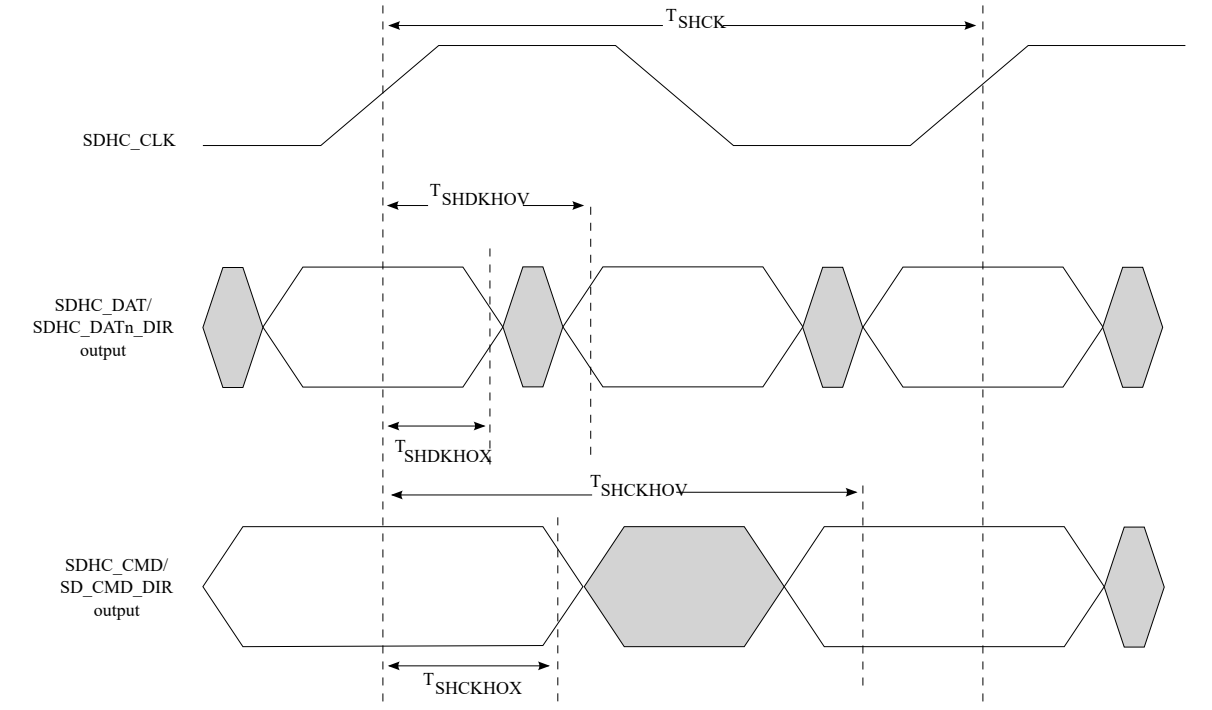


Figure 18. eSDHC DDR50/DDR mode output AC timing diagram

3.12 Universal asynchronous receiver/transmitter (UART)

3.12.1 UART DC electrical characteristics

This table provides the DC electrical characteristics for the UART interface.

Table 30. UART DC electrical characteristics (OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	2
Input current (V_{IN} = 0V or V_{IN} = OV_{DD})	I_{IN}	-	±50	μA	3
Output high voltage (I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (I_{OL} = 0.5 mA)	V_{OL}	-	0.45	V	-

1. For recommended operating conditions, see Recommended Operating Conditions.

2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Recommended Operating Conditions.

3. The symbol OV_{IN} represents the input voltage of the supply referenced in Recommended Operating Conditions.

3.12.2 UART AC timing specifications

This table provides the AC timing specifications for the UART interface.

Table 31. UART AC timing specifications

Parameter	Symbol	Min	Max	Unit	Notes
Baud rate	baud	300.0	921600.0	bits/sec	1, 2

1. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

2. The actual attainable baud rate is limited by the latency of interrupt processing.

3.13 Ethernet interface (EMI, RGMII, and IEEE Std 1588™)

This section describes the DC and AC electrical characteristics for the EMI, RGMII, and IEEE Std 1588 interfaces.

3.13.1 Ethernet management interface (EMI)

This section describes the electrical characteristics for the Ethernet management interface (EMI) interface.

The EMI1 and EMI2 interface timings are compatible with IEEE Std 802.3™ clauses 22 and 45, respectively.

3.13.1.1 EMI DC electrical characteristics

This table provides the EMI DC electrical characteristics.

Table 32. EMI DC electrical characteristics (OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	2
Input current (V_{IN} = 0 or V_{IN} = OV_{IN})	I_{IN}	-	±50	μA	3
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-

1. For recommended operating conditions, see Recommended Operating Conditions.

2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Recommended Operating Conditions.

3. The symbol OV_{IN} represents the input voltage of the supply referenced in Recommended Operating Conditions.

3.13.1.2 EMI AC timing specifications

This table provides the EMI AC timing specifications.

Table 33. EMI AC timing specifications [4, 5, 6]

Parameter	Symbol	Min	Max	Unit	Notes
MDC frequency	f_{MDC}	-	5.0	MHz	1
MDC clock pulse width high	t_{MDCH}	80.0	-	ns	-
MDC to MDIO delay	t_{MDKHDX}	Y x t_{enet_clk} - 3	Y x t_{enet_clk} + 3	ns	2, 3
MDIO to MDC setup time	t_{MDDVKH}	8.0	-	ns	-
MDIO to MDC hold time	t_{MDDXKH}	0	-	ns	

1. This parameter is dependent on the Ethernet clock frequency. The MDIO_CFG [MDIO_CLK_DIV] field determines the clock frequency of the MgmtClk Clock EC_MDC.

2. t_{enet_clk} is the Ethernet clock period x 2.

3. MDIO timing is configurable by programming the EMDIO_CFG register fields. The default value of Y = 5. Y is the value determined by EMDIO_CFG[NEG], EMDIO_CFG[MDIO_HOLD], and MDIO[EHOLD]. The easiest way is to program NEG=1, then MDIO is driven at negative edge of MDC, satisfying both setup and hold time requirement of Ethernet PHY.

4. The symbols used for timing specifications follow these patterns: $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time tMDC from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the tMDC clock reference (K) going to the high (H) state or setup time.

5. Assumes a maximum load of 338 pF.

6. See Figure 19.

This figure shows the Ethernet management interface timing diagram.

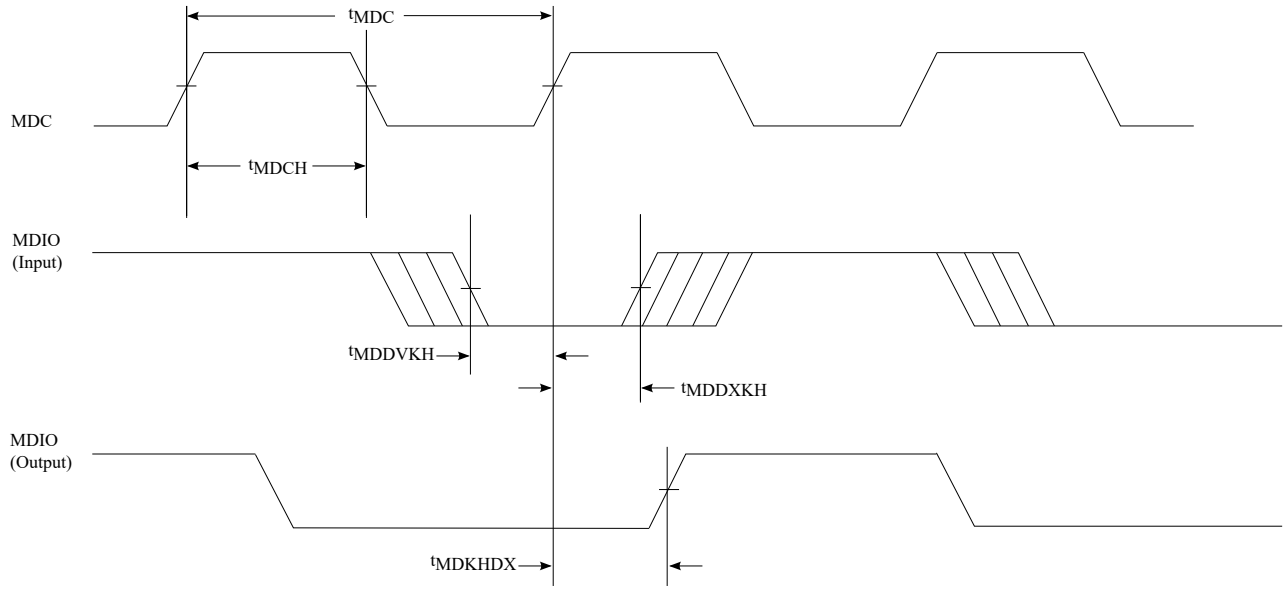


Figure 19. Ethernet management interface timing diagram

3.13.2 Reduced media-independent interface (RGMII)

3.13.2.1 RGMII DC electrical characteristics

This table provides the DC electrical characteristics for the RGMII interface.

Table 34. RGMII DC electrical characteristics (OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	2
Input current (V_{IN}=0 or V_{IN} = OV_{IN})	I_{IN}	-	±50	μA	3
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	3
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	3

1. For recommended operating conditions, see Recommended Operating Conditions.

2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Recommended Operating Conditions.

3. The symbol OV_{DD} represents the recommended operating voltage of the supply referenced in Recommended Operating Conditions.

3.13.2.2 RGMII AC timing specifications

This table provides the RGMII AC timing specifications.

Table 35. RGMII AC timing specifications [7, 8]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Data to clock output skew (at transmitter)	t_{SKRGT_TX}	-500.0	0.0	500.0	ps	1
Data to clock input skew (at receiver)	t_{SKRGT_RX}	1.0	-	2.6	ns	2
Clock period duration	t_{RGT}	7.2	8.0	8.8	ns	3
Duty cycle for 10BASE-T and 100BASE-TX	t_{RGTH}/t_{RGT}	40.0	50.0	60.0	%	3, 4
Duty cycle for Gigabit	t_{RGTH}/t_{RGT}	45.0	50.0	55.0	%	-
Rise time (20%-80%) OV_{DD} = 1.8V	t_{RGTR}	-	-	0.75	ns	5, 6
Fall time (20%-80%) OV_{DD} = 1.8V	t_{RGTF}	-	-	0.75	ns	5, 6

1. The frequency of ECn_RX_CLK (input) should not exceed the frequency of ECn_GTX_CLK (output) by more than 300 ppm.

2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal. Many PHY vendors already incorporate the necessary delay inside their device. If so, additional PCB delay is probably not needed.

3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.

4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three tRGT of the lowest speed transitioned between.

5. Applies to inputs and outputs.

6. The system/board must be designed to ensure this input requirement to the chip is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

7. In general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII timing. Note that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).

8. See Figure 20.

NOTE

NXP guarantees timings generated from the MAC. Board designers must ensure delays needed at the PHY or the MAC.

This figure shows the RGMII AC timing and multiplexing diagrams.

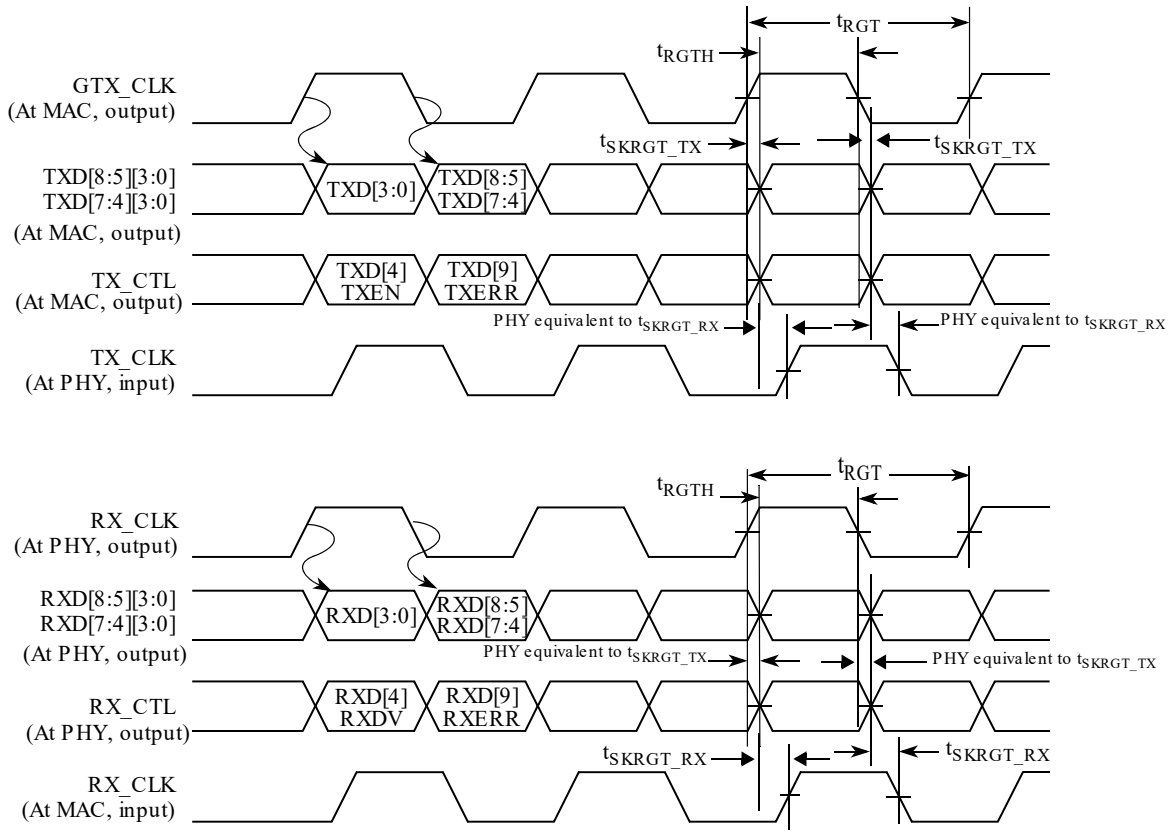


Figure 20. RGMII AC timing and multiplexing diagrams

3.13.3 IEEE 1588

3.13.3.1 IEEE 1588 DC electrical characteristics

This table provides the IEEE 1588 DC electrical characteristics.

Table 36. IEEE 1588 DC electrical characteristics (OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	2
Input current (V_{IN} = 0 or V_{IN} = OV_{DD})	I_{IN}	-	±50	μA	3
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-

Table continues on the next page...

Table 36. IEEE 1588 DC electrical characteristics (OV_{DD} = 1.8V) [1] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
1. For recommended operating conditions, see Recommended Operating Conditions. 2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Recommended Operating Conditions. 3. The symbol OV_{IN} represents the input voltage of the supply referenced in Recommended Operating Conditions.					

3.13.3.2 IEEE 1588 AC timing specifications

This table provides the AC timing specifications for the IEEE 1588 interface.

Table 37. IEEE 1588 AC timing specifications [2, 3]

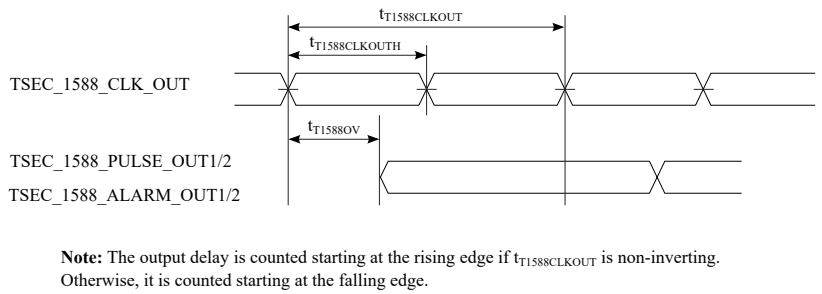
Parameter	Symbol	Min	Typ	Max	Unit	Notes
TSEC_1588_CLK_IN clock period	$t_{1588CLK}$	6.0	-		ns	-
TSEC_1588_CLK_IN duty cycle	$t_{T1588CLKH}/t_{T1588CLK}$	40.0	50.0	60.0	%	-
TSEC_1588_CLK_IN peak-to-peak jitter	$t_{T1588CLKINJ}$	-	-	250.0	ps	-
Rise time TSEC_1588_CLK_IN (20% to 80%)	$t_{T1588CLKINR}$	1.0	-	2.0	ns	-
Fall time TSEC_1588_CLK_IN (80% to 20%)	$t_{T1588CLKINF}$	1.0	-	2.0	ns	-
TSEC_1588_CLK_OUT clock period	$t_{T1588CLKOUT}$	2 x $t_{1588CLK}$	-	-	ns	-
TSEC_1588_CLK_OUT duty cycle	$t_{T1588CLKOTH}/t_{T1588CLKOUT}$	30.0	50.0	70.0	%	-
TSEC_1588_PULSE_OUT1/2, TSEC_1588_ALARM_OUT1/2	$t_{T1588OV}$	0.5	-	4.0	ns	-
TSEC_1588_TRIG_IN1/2 pulse width	$t_{T1588TRIGH}$	2 x $t_{1588CLK}$	-	-	ns	1

Table continues on the next page...

Table 37. IEEE 1588 AC timing specifications [2, 3] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
1. This needs to be at least two times the clock period of the clock selected by TMR_CTRL[CKSEL]. See the chip reference manual for a description of TMR_CTRL registers. 2. See Figure 21. 3. See Figure 22.						

This figure shows the data and command output AC timing diagram.



Note: The output delay is counted starting at the rising edge if $t_{T1588CLKOUT}$ is non-inverting. Otherwise, it is counted starting at the falling edge.

Figure 21. IEEE 1588 output AC timing

This figure shows the data and command input AC timing diagram.

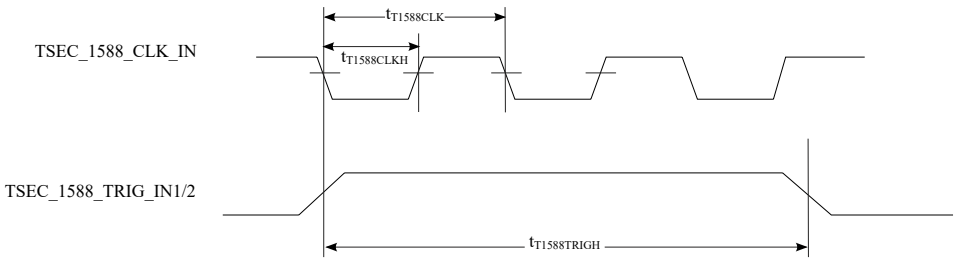


Figure 22. IEEE 1588 input AC timing

3.14 General purpose input/output (GPIO)

3.14.1 GPIO DC electrical characteristics

This table provides the DC electrical characteristics for the GPIO interface.

Table 38. GPIO DC electrical characteristics (OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	2

Table continues on the next page...

Table 38. GPIO DC electrical characteristics (OV_{DD} = 1.8V) [1] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Input current (V_{IN} = 0V or V_{IN}= OV_{DD})	I_{IN}	-	±50	μA	3
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-

1. For recommended operating conditions, see Recommended Operating Conditions.

2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Recommended Operating Conditions.

3. The symbol OV_{IN} represents the input voltage of the supply referenced in Recommended Operating Conditions.

3.14.2 GPIO AC timing specifications

This table provides the GPIO input and output AC timing specifications.

Table 39. GPIO AC timing specifications [2]

Parameter	Symbol	Min	Max	Unit	Notes
GPIO inputs-minimum pulse width	t_{PIWID}	20.0	-	ns	1

1. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs must be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

2. See Figure 23.

The figure below provides the AC test load for the GPIO.

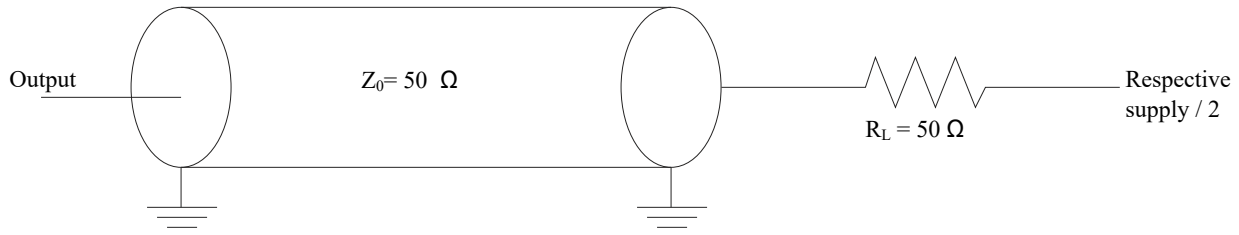


Figure 23. GPIO AC test load

3.15 Flextimer interface

3.15.1 Flextimer DC electrical characteristics

This table provides the DC electrical characteristics for the Flextimer interface.

Table 40. Flextimer DC electrical characteristics (OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	2
Input current (V_{IN} = 0V or V_{IN}= OV_{DD})	I_{IN}	-	±50	μA	3
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-

1. For recommended operating conditions, see Recommended Operating Conditions.

2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Recommended Operating Conditions.

3. The symbol OV_{IN} represents the input voltage of the supply referenced in Recommended Operating Conditions.

3.15.2 Flextimer AC timing specifications

This table provides the Flextimer input and output AC timing specifications.

Table 41. Flextimer AC timing specifications [2]

Parameter	Symbol	Min	Max	Unit	Notes
Flextimer inputs-minimum pulse width	t_{PIWID}	20.0	-	ns	1

1. Flextimer inputs and outputs are asynchronous to any visible clock. Flextimer outputs must be synchronized before use by any external synchronous logic. Flextimer inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

2. See Figure 24.

The figure below provides the AC test load for the Flextimer.

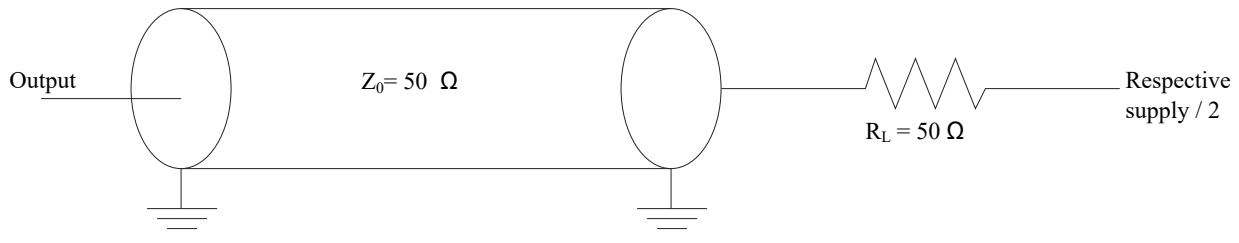


Figure 24. Flextimer AC test load

3.16 Generic interrupt controller (GIC)

3.16.1 GIC DC electrical characteristics

This table provides the DC electrical characteristics for the GIC interface.

Table 42. GIC DC electrical characteristics (OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	2
Input current (V_{IN} = 0V or V_{IN}= OV_{DD})	I_{IN}	-	±50	μA	3
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-

1. For recommended operating conditions, see Recommended Operating Conditions.

2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Recommended Operating Conditions.

3. The symbol OV_{IN} represents the input voltage of the supply referenced in Recommended Operating Conditions.

3.16.2 GIC AC timing specifications

This table provides the GIC input and output AC timing specifications.

Table 43. GIC AC timing specifications

Parameter	Symbol	Min	Max	Unit	Notes
GIC inputs-minimum pulse width	t_{PIWID}	3.0	-	SYSCLKs	1

1. GIC inputs and outputs are asynchronous to any visible clock. GIC outputs must be synchronized before use by any external synchronous logic. GIC inputs are required to be valid for at least tPIWID ns to ensure proper operation when working in edge triggered mode.

3.17 I2C

3.17.1 I2C DC electrical characteristics

This table provides the DC electrical characteristics for the I^2C interface.

Table 44. I^2C DC electrical characteristics (OV_{DD} = 1.8V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	2

Table continues on the next page...

Table 44. I²C DC electrical characteristics (OV_{DD} = 1.8V)[1] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Output low voltage (OV_{DD} = min, IOL = 2 mA, OV_{DD} ≤ 2V)	V_{OL}	0.0	0.36	V	-
Pulse width of spikes that must be suppressed by the input filter	t_{I2KHKL}	0.0	50.0	ns	3
Input current each I/O pin (input voltage is between 0.1 x OV_{DD} (min) and 0.9 x OV_{DD} (max))	I_I	-	±50	µA	4
Capacitance for each I/O pin	C_I	-	10.0	pF	-

1. For recommended operating conditions, see Recommended Operating Conditions.

2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Recommended Operating Conditions.

3. See the chip reference manual for information about the digital filter used.

4. I/O pins obstruct the SDA and SCL lines if the supply is switched off.

3.17.2 I2C AC timing specifications

This table provides the AC timing specifications for the I² C interface.

Table 45. I²C AC timing specifications [3, 4, 5]

Parameter	Symbol	Standard Mode		Fast Mode		Unit	Notes
		Min	Max	Min	Max		
Max. Frequency	f_{I2C}		100	-	400.0	kHz	-
Low period of the SCL clock	t_{I2CL}	4.7		1.3	-	µs	-
High period of the SCL clock	t_{I2CH}	4		0.6	-	µs	-
Setup time for a repeated START condition	t_{I2SVKH}	4.7		0.6	-	µs	-
Hold time (repeated) START condition	t_{I2SXKL}	4		0.6	-	µs	-
Setup time	t_{I2DVKH}	250		100.0	-	ns	1
Input hold time	t_{I2DXKL}	0.0		0.0	-	µs	2
Master output delay time	t_{I2OVKL}		3.45		0.9	µs	3
Input setup time for STOP condition	t_{I2PVKH}	4	-	0.6	-	µs	-

Table continues on the next page...

Table 45. I²C AC timing specifications [3, 4, 5] (continued)

Parameter	Symbol	Standard Mode		Fast Mode		Unit	Notes
		Min	Max	Min	Max		
Bus free time between a STOP and START condition	t_{I2KHDX}	4.7		1.3	-	µs	-
Capacitive load for each bus line	Cb		400.0	-	400.0	pF	4

1. A Fast-mode I²C-bus device can be used in a Standard-modeI²C-bus system, but the requirement of Setup time of 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line max rise time + data Setup Time = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line is released.

2. A device must internally provide a hold time of at least 300 ns for I2Cx_SDA signal to bridge the undefined region of the falling edge of I2Cx_SCL.

3. The maximum t_{I2OVKL} has to be met only if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.

4. Cb = Total capacitance of one bus line in pF

5. The symbols used for timing specifications herein follow these patterns: $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I2C timing (I2) for the time that the data with respect to the START condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I2C timing (I2) for the time that the data with respect to the STOP condition (P) reaches the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time.

6. See Figure 25.

7. See Figure 26.

This figure shows the AC test load for the I²C.

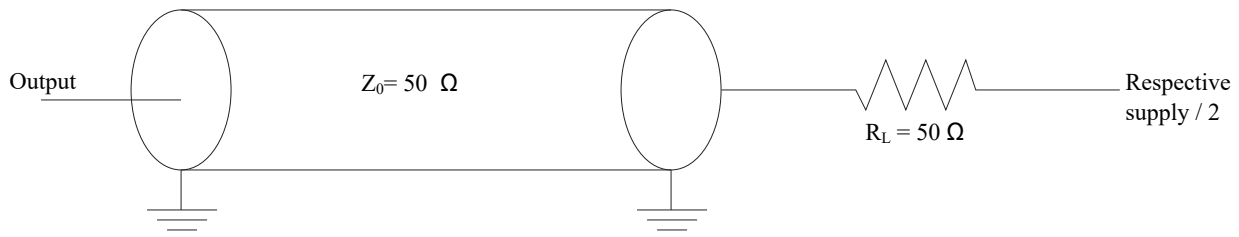


Figure 25. I²C AC test load

This figure shows the AC timing diagram for the I²C bus.

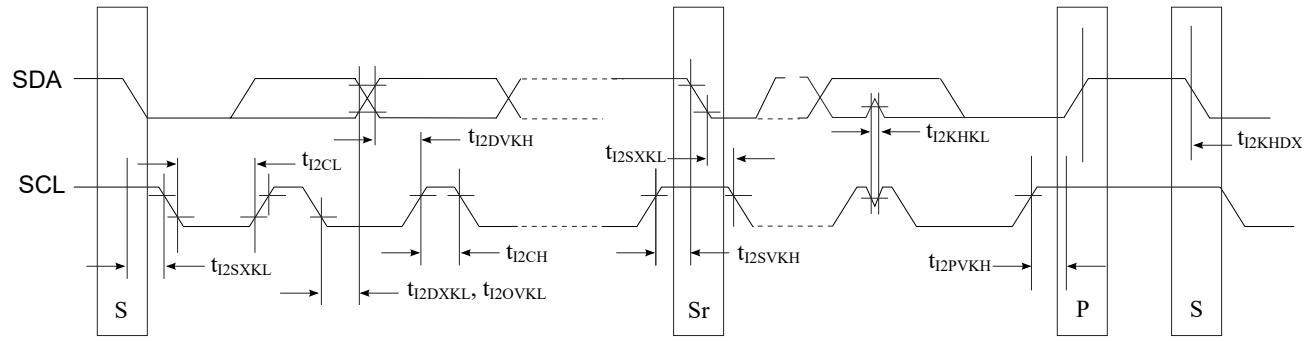


Figure 26. I²C bus AC timing diagram

3.18 JTAG

This section describes the DC and AC electrical specifications for the JTAG (IEEE 1149.1) interface.

3.18.1 JTAG DC electrical characteristics

This table provides the DC electrical characteristics for the JTAG (IEEE 1149.1) interface.

Table 46. JTAG DC electrical characteristics (OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	2
Input current (V_{IN} = 0V or V_{IN} = OV_{DD})	I_{IN}	-	-100/+50	µA	3
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-

1. For recommended operating conditions, see Recommended Operating Conditions.

2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Recommended Operating Conditions.

3. The symbol OV_{IN} represents the input voltage of the supply referenced in Recommended Operating Conditions.

3.18.2 JTAG AC timing specifications

This table provides the JTAG AC timing specifications as defined in Figure 27, Figure 28, Figure 29, and Figure 30.

Table 47. JTAG AC timing specifications [3, 4, 5, 6, 7]

Parameter	Symbol	Min	Max	Unit	Notes
JTAG external clock frequency of operation	F_{JTG}	0	25	MHz	-

Table continues on the next page...

Table 47. JTAG AC timing specifications [3, 4, 5, 6, 7] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
JTAG external clock cycle time	t_{JTG}	40	-	ns	-
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	20	-	ns	-
JTAG external clock rise and fall times	t_{JTGR}/t_{JTGF}	0.0	2.0	ns	-
TRST_B assert time	t_{TRST}	25.0	-	ns	1
Input setup times	t_{JTDVKH}	6	-	ns	-
Input hold times	t_{JTDXKH}	10.0	-	ns	-
Output valid times: boundary-scan data	t_{JTKLDV}	-	20.0	ns	2
Output valid times: TDO	t_{JTKLDV}	-	14	ns	2
Output hold times	t_{JTKLDX}	0.0	-	ns	2

1. TRST_B is an asynchronous level sensitive signal. The setup time is for test purposes only.

2. All outputs are measured from the midpoint voltage of the falling edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

3. The symbols used for timing specifications follow these patterns: t(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the tJTG clock reference (K) going to the high (H) state or setup time. Also, tJTDXKH symbolizes JTAG timing (JT) with respect to the time data input signals (D) reaching the invalid state (X) relative to the tJTG clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular function. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

4. See Figure 27.

5. See Figure 28.

6. See Figure 29.

7. See Figure 30.

This figure shows the AC test load for TDO and the boundary-scan outputs of the device.

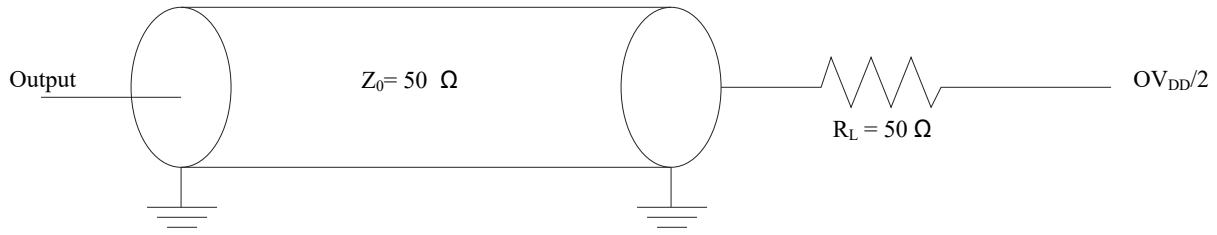


Figure 27. AC test load for the JTAG interface

This figure shows the JTAG clock input timing diagram.

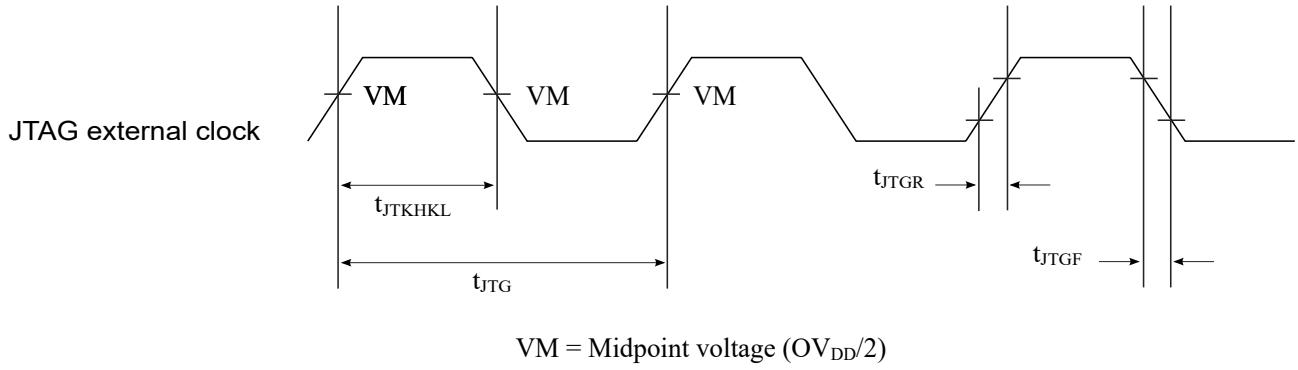


Figure 28. JTAG clock input timing diagram

This figure shows the TRST_B timing diagram.

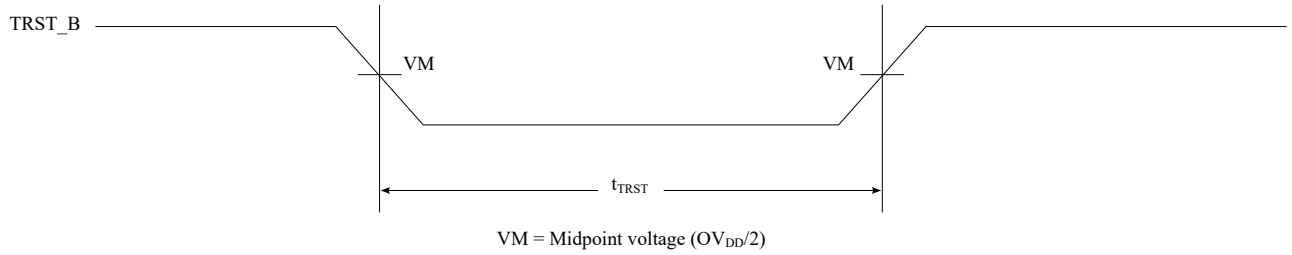


Figure 29. TRST_B timing diagram

This figure shows the boundary-scan timing diagram.

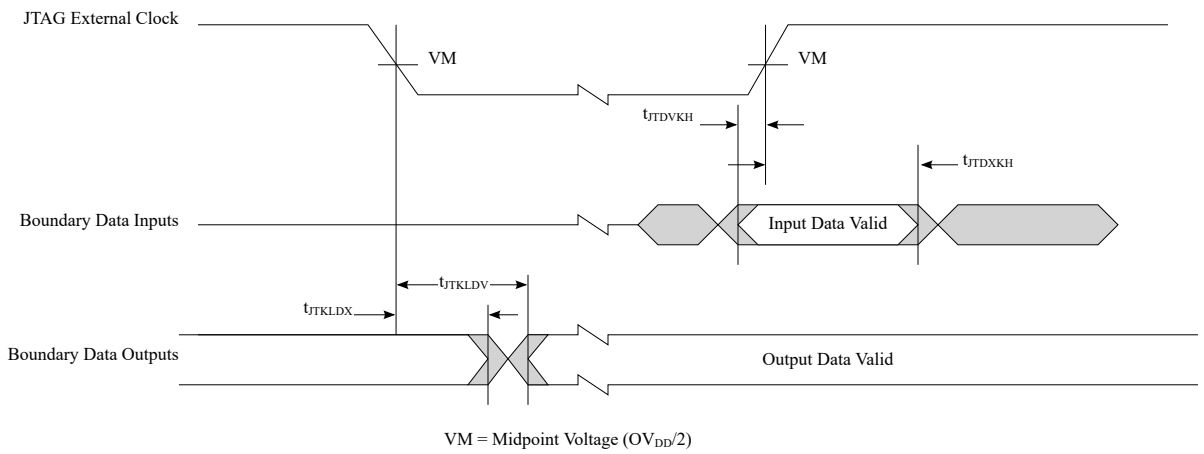


Figure 30. Boundary-scan timing diagram

3.19 Flex serial peripheral interface (FlexSPI)

3.19.1 FlexSPI DC electrical characteristics

This table provides the DC electrical characteristics for the FlexSPI interface.

Table 48. FlexSPI DC electrical characteristics (OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	2
Input current (0V ≤ V_{IN} ≤ OV_{DD})	I_{IN}	-	±50	μA	3
Output high voltage (I_{OH} = -100 μA)	V_{OH}	0.85xOV_{DD}	-	V	-
Output low voltage (I_{OL} = 100 μA)	V_{OL}	-	0.15xOV_{DD}	V	-

1. For recommended operating conditions, see Recommended Operating Conditions.

2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Recommended Operating Conditions.

3. The symbol OV_{IN} represents the input voltage of the supply referenced in Recommended Operating Conditions.

3.19.2 FlexSPI AC timing specifications

This table provides the FlexSPI timing in SDR mode where FlexSPIn_MCR0[RXCLKSRC] = 0x0

Table 49. SDR mode with FlexSPIn_MCR0[RXCLKSRC] = 0x0 [2, 3, 4]

Parameter	Symbol	Min	Max	Unit	Notes
Clock frequency	F_{SCK}	-	100.0	MHz	-
Duty cycle	T_{LOW}/T_{HIGH}	45	55	%	6
CS output hold time	$t_{FSKHOX2}$	FLSHxyCR1[TCSH] * T - 0.15	-	ns	1, 5
CS output delay	$t_{FSKHOV2}$	((FLSHxyCR1[TCSS]+ 0.5) * T) - 5.15	-	ns	1, 5
Setup time for incoming data-without DQS	t_{FSIVKH}	2.4	-	ns	5
Hold time for incoming data without DQS	t_{FSIXKH}	1.05	-	ns	-
Output data delay	t_{FSKHOV}		2.35	ns	-
Output data hold	t_{FSKHOX}	-1.35	-	ns	-

1. Refer the FLSHxyCR1 QorIQ LXxxxxARM for more details, where x: A or B, y: 1 or 2
2. See Figure 32.
3. See Figure 33.
4. See Figure 34.
5. T = FlexSPI clock period
6. Characterized.

This table provides the FlexSPI timing in SDR mode where FlexSPIn_MCR0[RXCLKSRC] =0x1 or 0x2

Table 50. SDR mode with FlexSPIn_MCR0[RXCLKSRC] = 0x1 or 0x2 [2, 3, 4]

Parameter	Symbol	Min	Max	Unit	Notes
Clock frequency	F_{SCK}	-	100.0	MHz	-
Duty cycle	T_{LOW}/T_{HIGH}	45	55	%	6
CS output hold time	$t_{FSKHOX2}$	FLSHxyCR1[TCSH] * T - 0.15	-	ns	1, 5
CS output delay	$t_{FSKHOV2}$	((FLSHxyCR1[TCSS] + 0.5) * T) - 5.15	-	ns	1, 5
Setup time for incoming data-without DQS	t_{FSIVKH}	2.4	-	ns	-
Hold time for incoming data without DQS	t_{FSIXKH}	1.05	-	ns	-

Table continues on the next page...

Table 50. SDR mode with FlexSPIn_MCR0[RXCLKSRC] = 0x1 or 0x2 [2, 3, 4] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Output data delay	t_{FSKHOV}		2.35	ns	-
Output data hold	t_{FSKHOX}	-1.35	-	ns	-

1. Refer the FLSHxyCR1 QorIQ LXxxxxARM for more details, where x: A or B, y: 1 or 2
2. See Figure 32.
3. See Figure 33.
4. See Figure 34.
5. T = FlexSPI clock period
6. Characterized.

This table provides the FlexSPI timing in DDR mode where FlexSPIn_MCR0[RXCLKSRC] =0x1 or 0x2.

Table 51. DDR mode with FlexSPIn_MCR0[RXCLKSRC] = 0x1, or 0x2 [4, 5, 6]

Parameter	Symbol	Min	Max	Unit	Notes
Clock frequency	F_{SCK}	-	75	MHz	-
Duty cycle	T_{LOW}/T_{HIGH}	47	53	%	8
CS output hold time	$t_{FSKHOX2}$	((FLSHxyCR1[TCSH]+ 0.5) * T/2) - 0.61	-	ns	1, 7
CS output delay	$t_{FSKHOV2}$	((FLSHxyCR1[TCSS]+ 0.5) * T/2) - 5.15	-	ns	1, 7
Data Valid Window	t_{FSIDVW}	0.3	-	UI	2, 3
Output data delay	t_{FSKHOV}/ tFSKLOV	-	3.94	ns	-
Output data hold	t_{FSKHOX}/ tFSKLOX	3.0	-	ns	-

1. Refer the FLSHxyCR1 QorIQ LXxxxxARM for more details, where x: A or B, y: 1 or 2
2. For DDR, Unit Internval (UI) is half of period. For example, 5 ns for 100 MHz
3. See "Data Learning Feature" section in QorIQ LXxxxxARM for details
4. See Figure 32.
5. See Figure 33.
6. See Figure 35.
7. T = FlexSPI clock period
8. Characterized.

This table provides the FlexSPI timing in DDR mode where FlexSPIn_MCR0[RXCLKSRC] =0x3.

Table 52. DDR mode with FlexSPIn_MCR0[RXCLKSRC] = 0x3 [2, 3, 4, 5]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Clock frequency	F_{SCK}	-	-	200	MHz	-
Duty cycle	T_{LOW}/T_{HIGH}	45	-	55	%	9
CS output hold time	$t_{FSKHOX2}$	((FLSHxyCR1[TCSH]+ 0.5) * T/2) - 0.61	-	-	ns	1, 6
CS output delay	$t_{FSKHOV2}$	((FLSHxyCR1[TCSH]+ 0.5) * T/2) - 5.15	-	-	ns	1, 6
DQS to data skew	t_{FSIVKH}/ tFSIVKL	-		0.6	ns	7, 8
DQS to data hold skew	$t_{FSIIVKH}$/ tFSIIVKL	-		0.9	ns	7, 8
Output data delay	t_{FSKHOV}/ tFSKLOV	-	-	1.7	ns	8
Output data hold	t_{FSKHOX}/ tFSKLOX	0.87	-	-	ns	-

1. Refer the FLSHxyCR1 QorIQ LXxxxxARM for more details, where x: A or B, y: 1 or 2
2. See Figure 32.
3. See Figure 33.
4. See Figure 35.
5. See Figure 31.
6. T = FlexSPI clock period
7. When DLLxCR = 0x0000_1100, where x: A or B.
8. The routine skew between XSPI clock/DQS to XSPI data lines must be less than 85 ps.
9. Characterized.

This figure shows the FlexSPI data input timing in DDR mode with an external DQS.

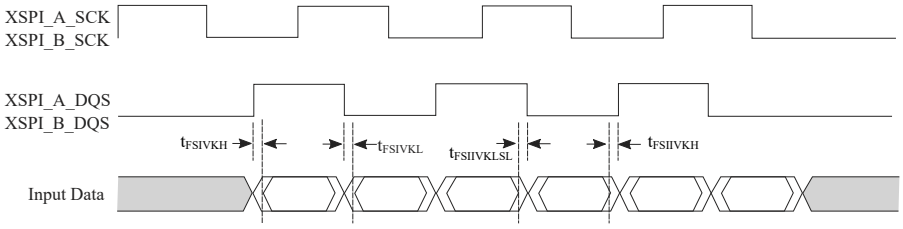


Figure 31. FlexSPI input AC timing-DDR mode with an external DQS

This figure shows the AC test load for the FlexSPI interface.

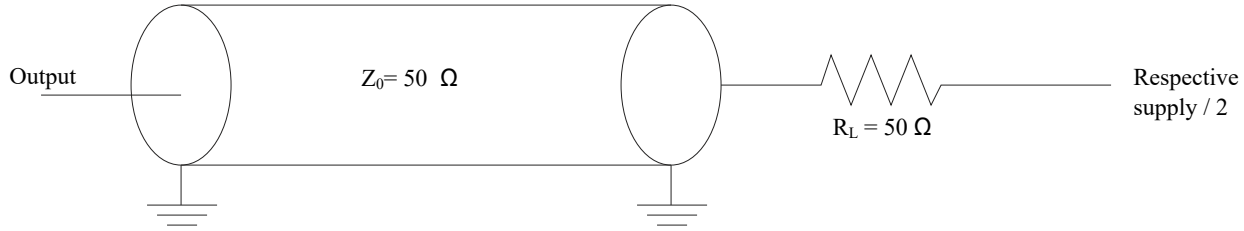


Figure 32. AC test load for FlexSPI

This figure shows the FlexSPI clock input timing diagram.

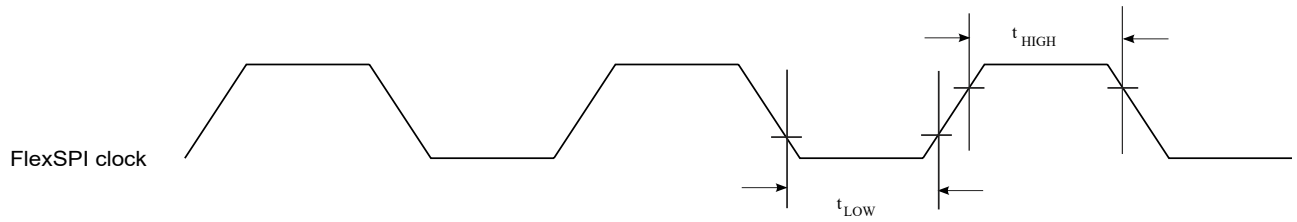


Figure 33. FlexSPI clock input timing diagram

This figure shows the FlexSPI AC timing diagram for SDR mode.

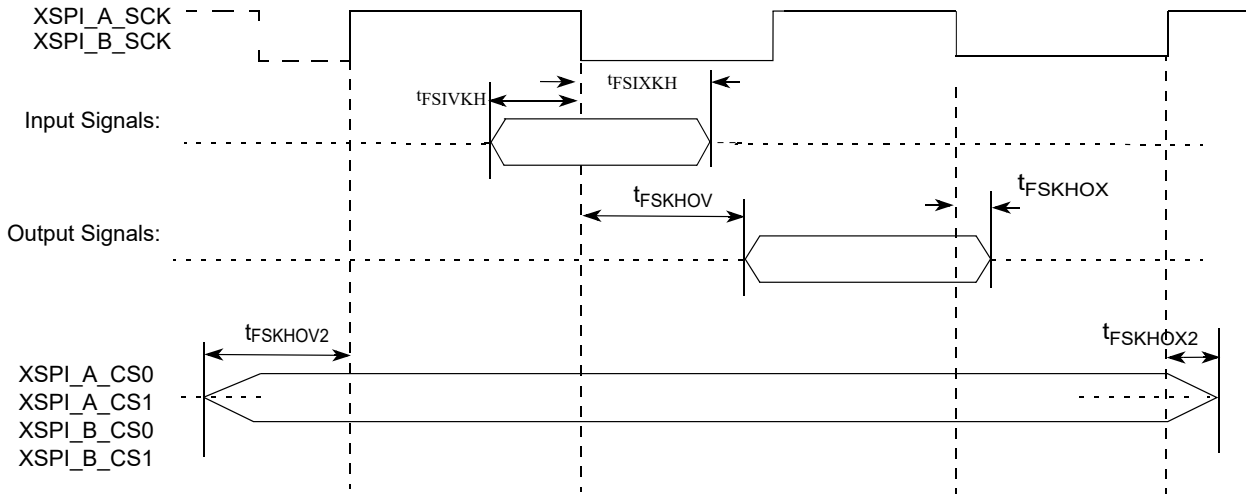


Figure 34. FlexSPI SDR mode AC timing diagram

This figure shows the FlexSPI AC timing diagram for DDR mode 1 and 2.

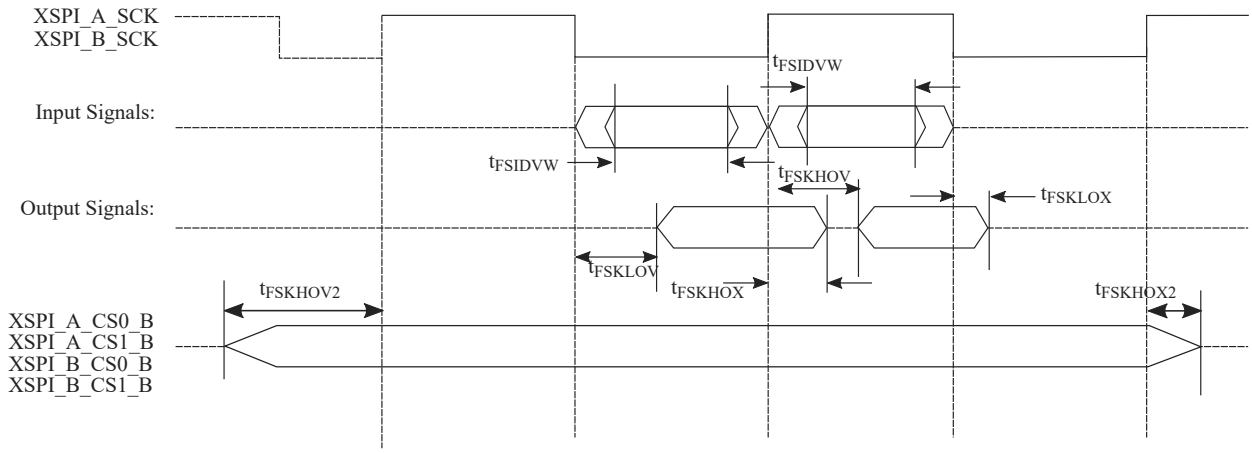


Figure 35. FlexSPI DDR mode 1 and 2 AC timing diagram

3.20 Serial peripheral interface (SPI)

3.20.1 SPI DC electrical characteristics

This table provides the DC electrical characteristics for the SPI interface when operating with a single master device.

Table 53. SPI DC electrical characteristics (OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	2

Table continues on the next page...

Table 53. SPI DC electrical characteristics (OV_{DD} = 1.8V) [1] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	2
Input current (V_{IN} = 0V or V_{IN} = OV_{DD})	I_{IN}	-	±50	μA	3
Output high voltage (I_{OH} = -100 μA)	V_{OH}	0.85xOV_{DD}	-	V	-
Output low voltage (I_{OL} = 100 μA)	V_{OL}	-	0.15xOV_{DD}	V	-

1. For recommended operating conditions, see Recommended Operating Conditions.

2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Recommended Operating Conditions.

3. The symbol OV_{IN} represents the input voltage of the supply referenced in Recommended Operating Conditions.

3.20.2 SPI AC timing specifications

This table provides the SPI timing specifications when operating with a single master device.

Table 54. SPI AC timing specifications [5, 6]

Parameter	Symbol	Min	Max	Unit	Notes
SCK cycle time	t_{SCK}	20	-	ns	
SCK clock pulse width	t_{SDC}	40.0	60.0	%	
CS to SCK delay	t_{CSC}	tp*2 - 2.16	-	ns	1, 2, 3
After SCK delay	t_{ASC}	tp*2 + 0.42	-	ns	1, 4, 5
Data setup time for inputs	t_{NIIVKH}	9.0	-	ns	1
Data hold time for inputs	t_{NIIXKH}	0.0	-	ns	1
Data valid (after SCK edge) for outputs	t_{NIKHOV}	-	5.0	ns	1
Data hold time for outputs	t_{NIKHOX}	0.0	-	ns	1

1. Master mode

2. Refer the CTARx register in QorIQ LX2162ARM for more details. The tCSC = tp*(Delay Scaler Value)*CTARx[PCSSCK] - 2.16, where the Delay Scaler Value comes from Table Delay Scaler Encoding. For example, the tCSC = tp*4*3 - 2.16 when CTARx[PCSSCK] = 0b01, CTARx[CSSCK]=0b0001

3. tp is the input clock period for the SPI controller.

4. Refer the CTARx register in QorIQ LX2162ARM for more details. The tASC = tp * (Delay Scaler Value) * CTARx[PASC] + 0.42, where the Delay Scaler Value comes from Table Delay Scaler Encoding. For example, the tASC = tp * 8 * 3 + 0.42 when CTARx[PASC] = 0b01, CTARx[ASC]=0b0010

5. See Figure 36.

6. See Figure 37.

This figure shows the SPI timing master when CPHA = 0.

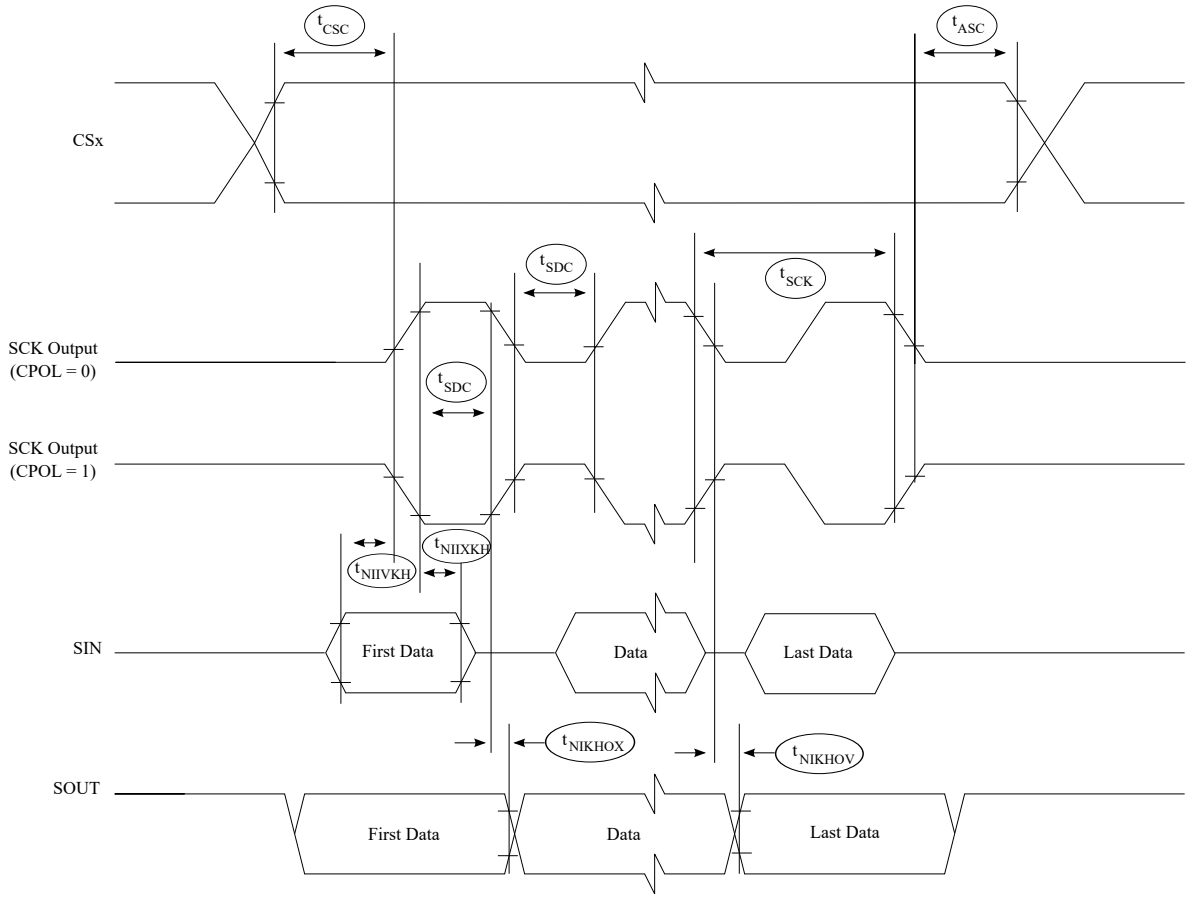


Figure 36. SPI timing master, CPHA = 0

This figure shows the SPI timing master when CPHA = 1.

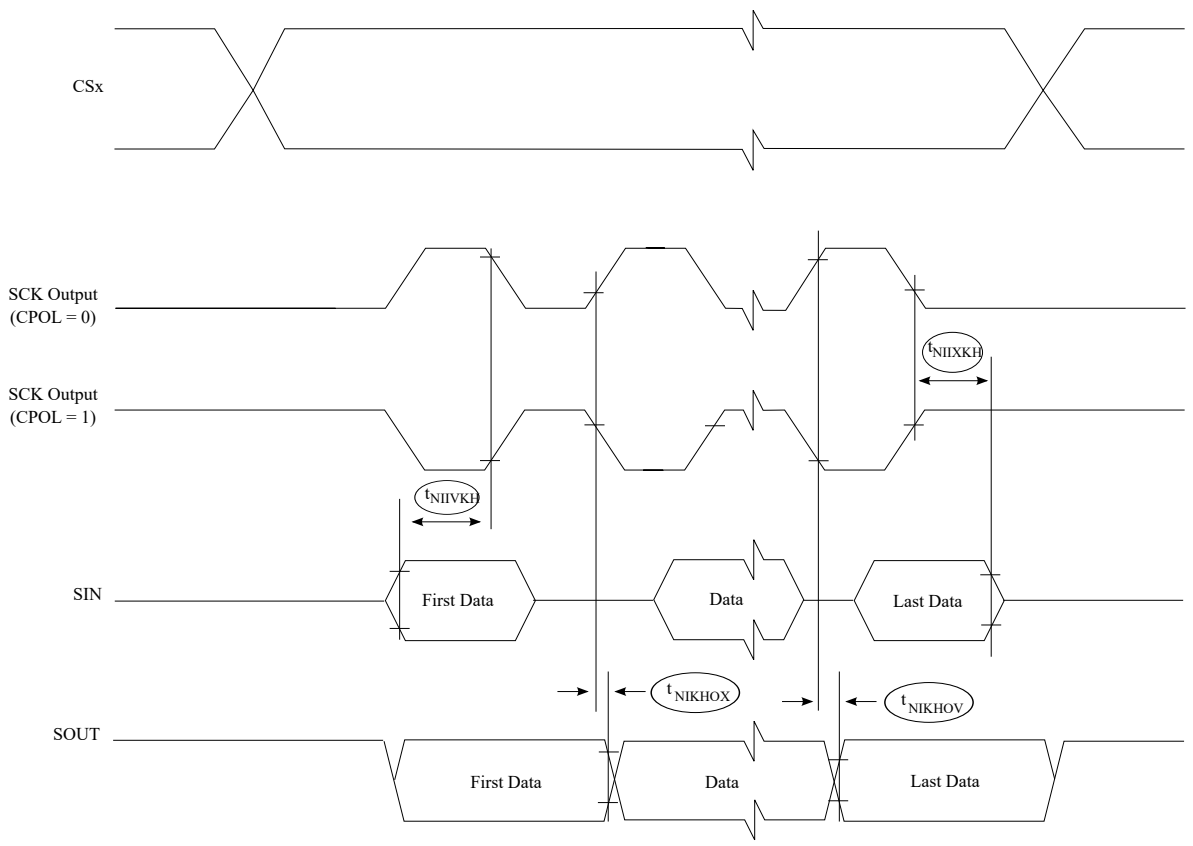


Figure 37. SPI timing master, CPHA = 1

3.21 Universal serial bus 3.0 (USB)

This section describes the specification for the on-chip Super Speed (SS) USB 3.0 PHY signals. For High Speed (HS), Full Speed (FS) , and Low Speed (LS) specifications of the USB PHY signals, see Chapter 7 in the Universal Serial Bus Revision 2.0 Specification for more information.

3.21.1 USB 3.0 DC electrical characteristics

This table provides the USB 3.0 transmitter DC electrical characteristics at package pins.

Table 55. USB 3.0 transmitter DC electrical characteristics (USB_HV_{DD} = 3.3 V, USB_SV_{DD} = 0.8 V)

Parameter	Symbol	Min	Typ	Max	Unit
Differential output voltage	$V_{tx\text{-}diff\text{-}pp}$	800.0	1000.0	1200.0	$mV_{p\text{-}p}$
Low power differential output voltage	$V_{tx\text{-}diff\text{-}pp\text{-}low}$	400.0	-	1200.0	$mV_{p\text{-}p}$
Transmit de-emphasis	$V_{tx\text{-}de\text{-}ratio}$	3.0	-	4.0	dB
Differential impedance	Z_{diffTX}	72.0	100.0	120.0	Ω

Table continues on the next page...

Table 55. USB 3.0 transmitter DC electrical characteristics (USB_HV$_{DD}$ = 3.3 V, USB_SV$_{DD}$ = 0.8 V) (continued)

Parameter	Symbol	Min	Typ	Max	Unit
Transmit common mode impedance	R_{TX-DC}	18.0	-	30.0	Ω
Absolute DC common mode voltage between U1 and U0	$T_{TX-CM-DC-ACTIVEIDLE-DELTA}$	-	-	200.0	mV
DC electrical idle differential output voltage	$V_{TX-IDLE-DIFF-DC}$	0.0	-	10.0	mV

This table provides the USB 3.0 receiver DC electrical characteristics at the receiver package pins.

Table 56. USB 3.0 receiver DC electrical characteristics (USB_HV$_{DD}$ = 3.3 V, USB_SV$_{DD}$ = 0.8 V)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential receiver input impedance	$R_{RX-DIFF-DC}$	72.0	100.0	120.0	Ω	-
Receiver DC common mode impedance	R_{RX-DC}	18.0	-	30.0	Ω	-
DC input CM input impedance for V > 0 during reset or power down	$Z_{RX-HIGH-IMP-DC}$	25000.0	-	-	Ω	-
LFPS detect threshold	$V_{TRX-IDLE-DET-DC-DIFFpp}$	100.0	-	300.0	mV	1
1. Below the minimum is noise. Must wake up above the maximum.						

3.21.2 USB 3.0 AC timing specifications

This table provides the USB 3.0 transmitter AC timing specifications at package pins.

Table 57. USB 3.0 transmitter AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Speed	f_{USB}	-	5.0	-	Gb/s	-
Transmitter eye	T_{TX-EYE}	0.625	-	-	UI	-
Unit Interval	UI	199.94	200.0	200.06	ps	1
AC coupling capacitor	AC_{CAP}	75.0	-	200.0	nF	-
1. UI does not account for SSC-caused variations.						

This table provides the USB 3.0 receiver AC timing specifications at the receiver package pins.

Table 58. USB 3.0 receiver AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval	UI	199.94	200.0	200.06	ps	1
1. UI does not account for SSC-caused variations.						

This table provides the key LFPS electrical specifications at the transmitter.

Table 59. LFPS electrical specifications at the transmitter [2]

Parameter	Symbol	Min	Max	Unit	Notes
Period	t_{Period}	20.0	100.0	ns	-
Peak-to-peak differential amplitude	$V_{tx\text{-}diff\text{-}pp\text{-}lfps}$	800.0	1200.0	mV	-
Rise/fall time	$t_{rise/fall}$	-	4.0	ns	1
Duty cycle	DC_{LFPS}	40.0	60.0	%	1, 2
1. Measured at compliance TP1. See the Transmit normative setup figure below for details. 2. See Figure 38.					

This figure shows the transmit normative setup with reference channel as per USB 3.0 specifications.

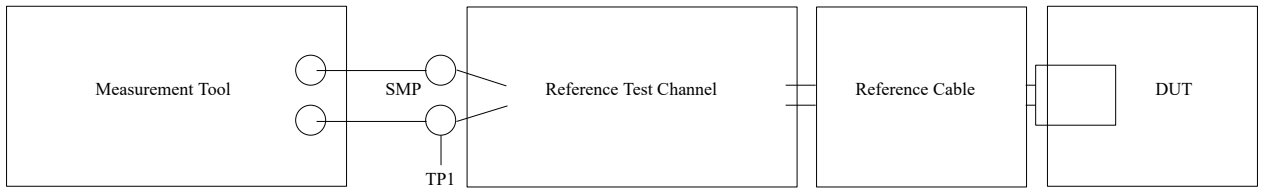


Figure 38. Transmit normative setup

3.22 Controller Automatic Network interface (CAN)

3.22.1 CAN DC electrical chracteristics

This table provides the DC electrical characteristics for CAN-FD pins operating at OV_{DD} = 1.8 V.

Table 60. DC electrical characteristics for CAN-FD (OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	2
Input current (VIN = 0 V or VIN= OV_{DD})	I_{IN}	-	±50	µA	3

Table continues on the next page...

Table 60. DC electrical characteristics for CAN-FD (OV_{DD} = 1.8V) [1] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Output high voltage (OV_{DD} = min, IOH = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (OV_{DD} = min, IOL = -0.5 mA)	V_{OL}	-	0.4	V	-

1. For recommended operating conditions, see Recommended Operating Conditions.

2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Recommended Operating Conditions.

3. The symbol OV_{IN} represents the input voltage of the supply referenced in Recommended Operating Conditions.

3.22.2 CAN AC electrical characteristics

This table provides the CAN-FD AC timing specifications.

Table 61. CAN-FD AC timing specifications [1]

Parameter	Min	Max	Unit
Baud rate	10.0	8000.0	kbps

1. See Figure 39.

This figure provides the CAN-FD AC test load.

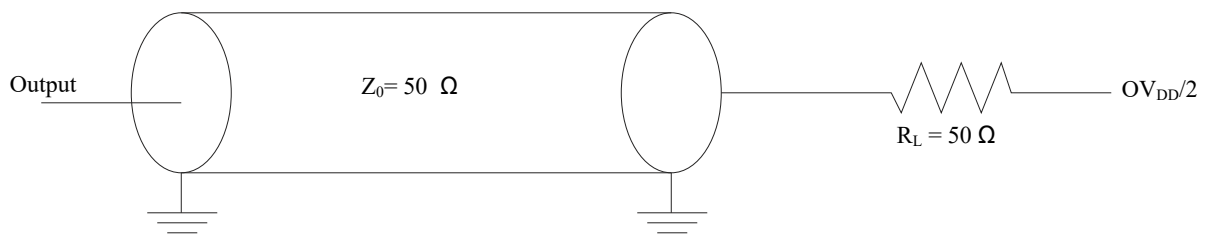


Figure 39. FlexCAN AC test load

3.23 High-speed serial interfaces (HSSI)

The chip features a Serializer/Deserializer (SerDes) interface to be used for high-speed serial interconnect applications. The SerDes interface can be used for PCI Express, SGMII, 1000Base-KX, USXGMII, XFI, SFI, 10GBase-KR, 25GAUI, 50GAUI-2, XLAUI, and serial ATA (SATA) data transfers.

This section describes the most common portion of the SerDes DC electrical specifications: the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter (Tx) and receiver (Rx) reference circuits are also described.

3.23.1 Signal terms definitions

The SerDes uses differential signaling to transfer data across the serial link. This section defines the terms that are used in the description and specification of differential signals.

This figure shows how the signals are defined. For illustration purposes only, one SerDes lane is used in the description. This figure shows the waveform for either a transmitter output (SD_TX*n*_P and SD_TX*n*_N) or a receiver input (SD_RX*n*_P and SD_RX*n*_N). Each signal swings between A volts and B volts where A > B.

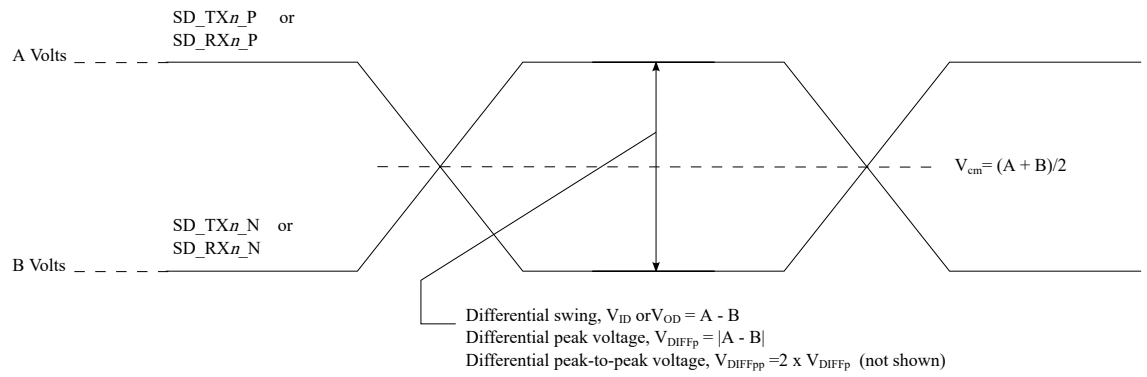


Figure 40. Differential voltage definitions for transmitter or receiver

Using this waveform, the definitions are as described in the following list. To simplify the illustration, the definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment:

Single-Ended Swing — The transmitter output signals and the receiver input signals SD_TX*n*_P, SD_TX*n*_N, SD_RX*n*_P and SD_RX*n*_N each have a peak-to-peak swing of A - B volts. This is also referred to as each signal wire's single-ended swing.

Differential Output Voltage, V_{OD} (or Differential Output Swing) — The differential output voltage (or swing) of the transmitter, V_{OD}, is defined as the difference of the two complementary output voltages: $V_{SD\_TX\ n\_}P$ - $V_{SD\_TXn\_N}$. The V_{OD} value can be either positive or negative.

Differential Input Voltage, V_{ID} (or Differential Input Swing) — The differential input voltage (or swing) of the receiver, V_{ID}, is defined as the difference of the two complementary input voltages: $V_{SD\_RXn\_P}$- $V_{SD\_RXn\_N}$. The V_{ID} value can be either positive or negative.

Differential Peak Voltage, V_{DIFFp} — The peak value of the differential transmitter output signal or the differential receiver input signal is defined as the differential peak voltage, V_{DIFFp} = |A - B| volts.

Differential Peak-to-Peak, $V_{DIFFp-p}$ — Because the differential output signal of the transmitter and the differential input signal of the receiver each range from A - B to -(A - B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p}$ = 2 x V_{DIFFp} = 2 x |(A - B)| volts, which is twice the differential swing in amplitude, or twice the differential peak. For example, the output differential peak-to-peak voltage can also be calculated as $V_{TX-DIFFp-p}$ = 2 x |V_{OD}|.

Differential Waveform — The differential waveform is constructed by subtracting the inverting signal (SD_TX*n*_N, for example) from the non-inverting signal (SD_TX*n*_P, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. See Figure 45 as an example for differential waveform.

Common Mode Voltage, V_{cm} — The common mode voltage is equal to half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, V_{cm_out} = ($V_{SD\_TXn\_P}$ + $V_{SD\_TXn\_N}$) ÷ 2 = (A + B) ÷ 2, which is the arithmetic mean of the two complementary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. It may be different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset on some occasions.

To illustrate these definitions using real values, consider the example of a current mode logic (CML) transmitter that has a common mode voltage of 2.25 V and outputs, TD and TD_B. If these outputs have a swing from 2.0 V to 2.5 V, the peak-to-peak voltage swing of each signal (TD or TD_B) is 500 mV p-p, which is referred to as the single-ended swing for each signal. Because the differential signaling environment is fully symmetrical in this example, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and -500 mV. In other words, V_{OD} is 500 mV in one phase and -500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

3.23.2 SerDes reference clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD1_PLLF_REF_CLK/SD1_PLLF_REF_CLK_B for SerDes 1 and SD2_PLLF_REF_CLK/SD2_PLLF_REF_CLK_B and SD2_PLLS_REF_CLK/SD2_PLLS_REF_CLK_B for SerDes 2.

SerDes 1-2 may be used for various combinations of the following IP blocks based on the RCW Configuration field SRDS_PRTCLn:

- SerDes 1: SGMII, PCIe, USXGMII/XFI/SFI, 50GE, 40GE, 25GE
- SerDes 2: SGMII, PCIe, USXGMII/XFI/SFI, SATA

The following sections describe the SerDes reference clock requirements and provide application information.

3.23.2.1 SerDes spread-spectrum clock source recommendations

SD*n*_REF_CLK*n*_P and SD*n*_REF_CLK*n*_N are designed to work with spread-spectrum clocking for the PCI Express protocol only with the spreading specification defined in Table 62. When using spread-spectrum clocking for PCI Express, both ends of the link partners should use the same reference clock. For best results, a source without significant unintended modulation must be used.

The SerDes transmitter does not support spread-spectrum clocking for the SATA protocol. The SerDes receiver does support spread-spectrum clocking on receive, which means the SerDes receiver can receive data correctly from a SATA serial link partner using spread-spectrum clocking.

Spread-spectrum clocking cannot be used if the same SerDes reference clock is shared with other non-spread-spectrum-supported protocols. For example, if spread-spectrum clocking is desired on a SerDes reference clock for the PCI Express protocol and the same reference clock is used for any other protocol, such as SATA or SGMII because of the SerDes lane usage mapping option, spread-spectrum clocking cannot be used at all.

This table provides the source recommendations for SerDes spread-spectrum clocking.

Table 62. SerDes spread-spectrum clock source recommendations [1]

Parameter	Min	Max	Unit	Notes
Frequency modulation	30	33	kHz	—
Frequency spread	+0	-0.5	%	2

Notes:

1. At recommended operating conditions. See Recommended Operating Conditions.
2. Only down-spreading is allowed.

3.23.2.2 SerDes reference clock receiver characteristics

This figure shows a receiver reference diagram of the SerDes reference clocks.

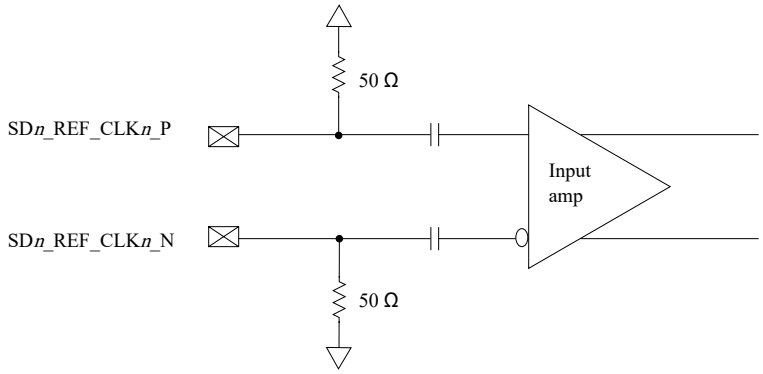


Figure 41. Receiver of SerDes reference clocks

3.23.2.3 DC-level requirement for SerDes reference clocks

The DC level requirement for the SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs, as described below.

Differential mode:

- The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-to-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing of less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
- For an external DC-coupled connection, as described in SerDes reference clock receiver characteristics, the maximum average current requirements sets the requirement for average voltage (common mode voltage) as between 100 mV and 400 mV. Figure 42 shows the SerDes reference clock input requirement for DC-coupled connection scheme.

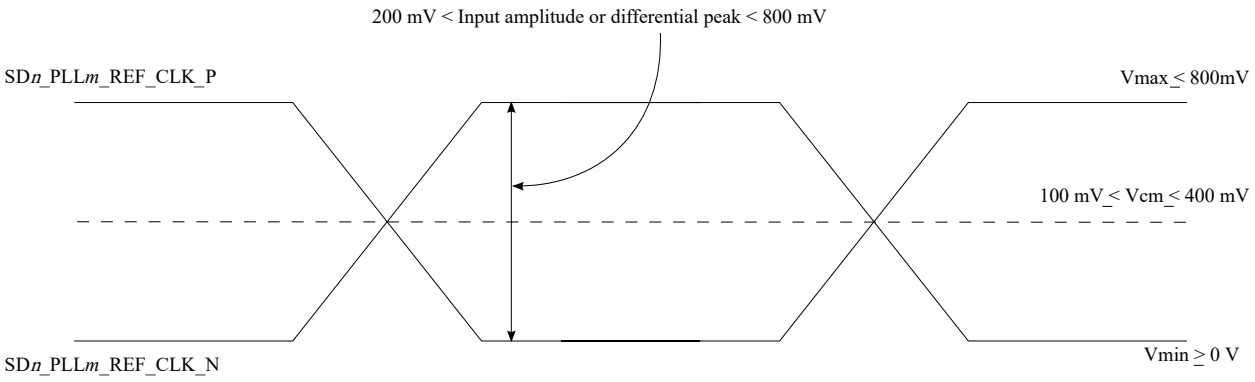


Figure 42. Differential reference clock input DC requirements (external DC-coupled)

- For an external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Because the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different common mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SD_GND. Each signal wire of the differential inputs is allowed to swing below and above the common mode voltage (SD_GND). Figure 43 shows the SerDes reference clock input requirement for AC-coupled connection scheme.

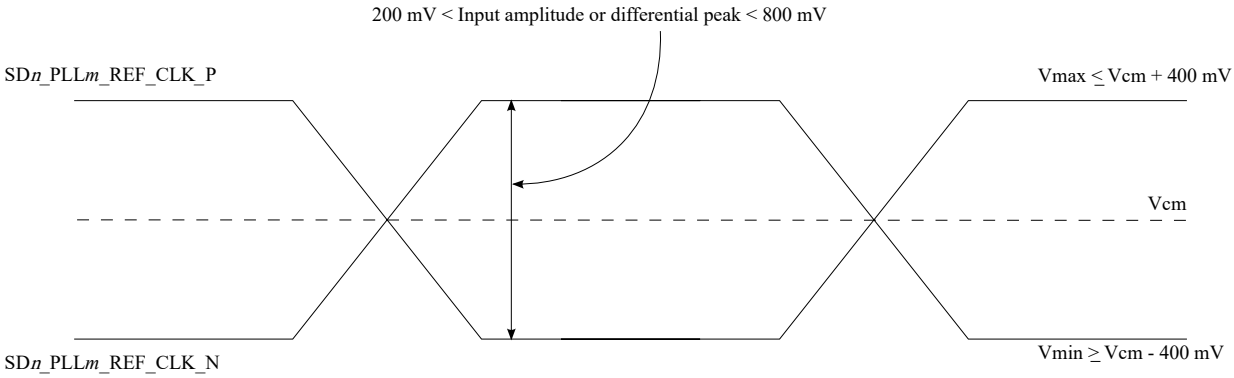


Figure 43. Differential reference clock input DC requirements (external AC-coupled)

Single-ended mode:

- The reference clock can also be single-ended. The SDn_REF_CLKn_P input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-to-peak (from V_{MIN} to V_{MAX}) with SDn_REF_CLKn_N either left unconnected or tied to ground.
- The SDn_REF_CLKn_P input average voltage must be between 200 and 400 mV. Figure 44 shows the SerDes reference clock input requirement for single-ended signaling mode.
- To meet the input amplitude requirement, the reference clock inputs may need to be DC- or AC-coupled externally. For the best noise performance, the reference of the clock could be DC- or AC-coupled into the unused phase (SDn_REF_CLKn_N) through the same source impedance as the clock input (SDn_REF_CLKn_P) in use.

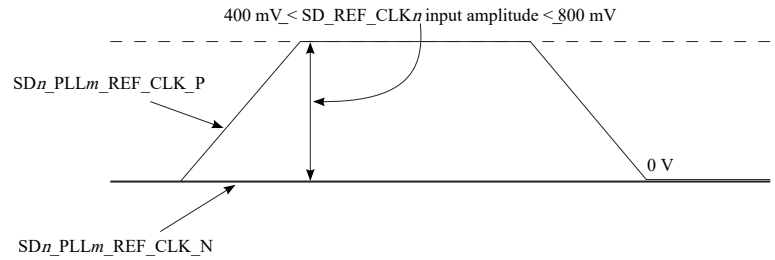


Figure 44. Single-ended reference clock input DC requirements

3.23.2.4 SerDes reference clocks AC timing specifications

For protocols with data rates up to 5 Gb/s where there is not reference clock jitter specification (ex: SGMII), use the PCIe 2.5G clock jitter requirements.

For protocols with data rates greater than 5 Gb/s and less than 8 Gb/s where there is no reference clock jitter specification, use the PCIe 5G clock jitter requirements.

For protocols with data rates greater than 8 Gb/s and less than 16 Gb/s where there is no reference clock jitter specification (ex: XLAUI, USXGMII-10.3125G), use the PCIe 8G or XFI clock jitter requirements.

For protocols with data rates greater than 16 Gb/s where there is no reference clock jitter specification (ex: 25GAUI/50GAUI-2 use the PCIe 16G clock jitter requirements).

Use the protocol's reference clock frequency tolerance specification (ex: +/-100 ppm for SGMII/USXGMII/XFI/SFI/10GBaseKR/1000Base-KX/XLAUI/25GAUI/50GAUI-2 and +/-300 ppm for PCIe).

This table defines the AC requirements for SerDes reference clocks for PCI Express. SerDes reference clocks need to be verified by the customer's application design.

Table 63. SDn_PLLm_REF_CLK_P and SDn_PLLm_REF_CLK_N input clock requirements for PCI Express

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SDn_PLLm_REF_CLK_P/ SDn_PLLm_REF_CLK_N frequency range	t_{CLK_REF}	-	100/125	-	MHz	-
SDn_PLLm_REF_CLK_P/ SDn_PLLm_REF_CLK_N clock frequency tolerance	t_{CLK_TOL}	-300.0	-	300.0	ppm	1
SDn_PLLm_REF_CLK_P/ SDn_PLLm_REF_CLK_N reference clock duty cycle	t_{CLK_DUTY}	40.0	50.0	60.0	%	2
PCIe 2.5G SDn_PLLm_REF_CLK_P/ SDn_PLLm_REF_CLK_N max deterministic peak-to-peak jitter at 10^{-6} BER	t_{CLK_DJ}	-	-	42.0	ps P-P	3, 4
PCIe 2.5G SDn_PLLm_REF_CLK_P/ SDn_PLLm_REF_CLK_N total reference clock jitter at 10^{-6} BER	t_{CLK_TJ}	-	-	86.0	ps P-P	3, 4
PCIe 5G SDn_PLLm_REF_CLK_P/ SDn_PLLm_REF_CLK_N 10 kHz to 1.5 MHz RMS jitter	$t_{REFCLK-LF-RMS}$	-	-	3.0	ps RMS	5
PCIe 5G SDn_PLLm_REF_CLK_P/ SDn_PLLm_REF_CLK_N > 1.5 MHz to Nyquist RMS jitter	$t_{REFCLK-HF-RMS}$	-	-	3.1	ps RMS	5
PCIe 8G SDn_PLLm_REF_CLK_P/ SDn_PLLm_REF_CLK_N RMS reference clock jitter	$t_{REFCLK-RMS-DC}$	-	-	1.0	ps RMS	6
SDn_PLLm_REF_CLK_P/ SDn_PLLm_REF_CLK_N rising/ falling edge rate	t_{CLKRR}/ t_{CLKFR}	0.6	-	4.0	V/ns	7, 8
Differential input high voltage	V_{IH}	150.0	-	-	mV	2
Differential input low voltage	V_{IL}	-	-	-150.0	mV	2
Rising edge rate (SDn_PLLm_REF_CLK_P) to falling edge rate	Rise-Fall matching	-	-	20.0	%	9, 10, 11

Table continues on the next page...

Table 63. SDn_PLLm_REF_CLK_P and SDn_PLLm_REF_CLK_N input clock requirements for PCI Express (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
(SDn_PLLm_REF_CLK_N) matching						

1. For PCI Express (2.5, 5, and 8 GT/s).

2. Measurement taken from differential waveform.

3. Limits from PCI Express CEM Rev 2.0.

4. For PCI Express 2.5 GT/s

5. For PCI Express 5 GT/s

6. For PCI Express 8 GT/s

7. Measured from -150 mV to +150 mV on the differential waveform (derived from SDn_PLLm_REF_CLK_P minus SDn_PLLm_REF_CLK_N). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing.

8. See Figure 45.

9. Measurement taken from single-ended waveform.

10. Matching applies to rising edge for SDn_PLLm_REF_CLK_P and falling edge rate for SDn_PLLm_REF_CLK_N. It is measured using a +/- 75 mV window centered on the median cross point where SDn_PLLm_REF_CLK_P rising meets SDn_PLLm_REF_CLK_N falling. The median cross point is used to calculate the voltage thresholds that the oscilloscope uses for the edge rate calculations. The rise edge rate of SDn_PLLm_REF_CLK_P must be compared to the fall edge rate of SDn_PLLm_REF_CLK_N, the maximum allowed difference should not exceed 20% of the slowest edge rate.

11. See Figure 46.

This figure shows the differential measurement points for rise and fall time.

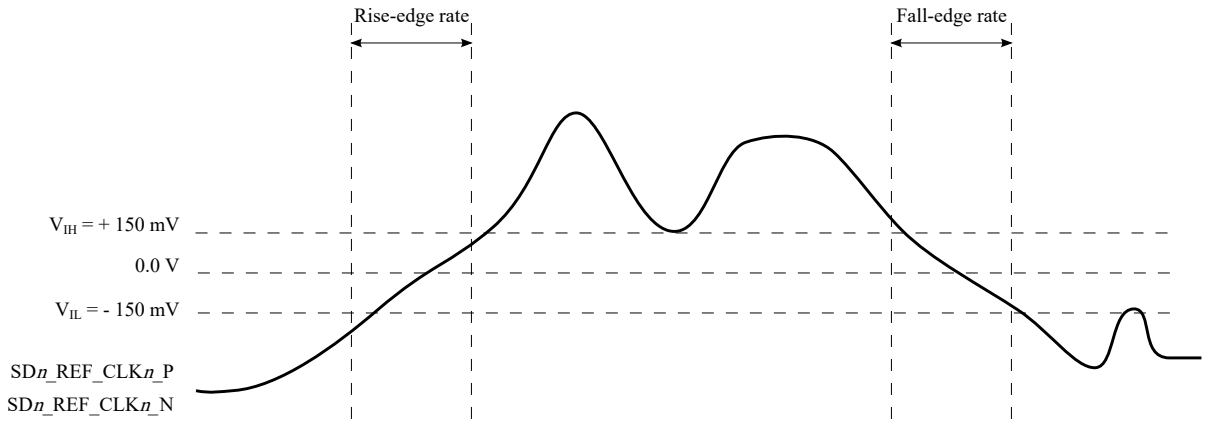


Figure 45. Differential measurement points for rise and fall time

This figure shows the single-ended measurement points for rise and fall time matching.

Figure 46. Single-ended measurement points for rise and fall time matching

This table defines the AC requirements for SerDes reference clocks for XFI, XLAUI, 25GAUI, and 50GAUI-2. SerDes reference clocks need to be verified by the customer's application design.

Table 64. SDn_PLLm_REF_CLK_P and SDn_PLLm_REF_CLK_N input clock requirements for XFI , SFI, XLAUI, and 50GAUI-2/25GAUI

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Frequency range	t_{CLK_REF}	-	156.25/ 161.1328125	-	MHz	-
Clock frequency tolerance	t_{CLK_TOL}	-100.0	-	100.0	ppm	-
Reference clock duty cycle	t_{CLK_DUTY}	40.0	50.0	60.0	%	1
Single side band noise at 1 kHz	at 1 kHz	-	-	-85.0	dBC/ Hz	2
Single side band noise at 10 kHz	at 10 kHz	-	-	-108.0	dBC/ Hz	2
Single side band noise at 100 kHz	at 100 kHz	-	-	-128.0	dBC/ Hz	2
Single side band noise at 1 MHz	at 1 MHz	-	-	-138.0	dBC/ Hz	2
Single side band noise at 10 MHz	at 10 MHz	-	-	-138.0	dBC/ Hz	2
Random jitter (1.2 MHz to 15 MHz)	t_{CLK_RJ}	-	-	0.8	ps	-
Total reference clock jitter at 10^{-12} BER (1.2 MHz to 15 MHz)	t_{CLK_TJ}	-	-	11.0	ps	-
Spurious noise (1.2 MHz to 15 MHz)	NA	-	-	-75.0	dBC	-
1. Measurement taken from differential waveform.						

Table continues on the next page...

Table 64. SDn_PLLm_REF_CLK_P and SDn_PLLm_REF_CLK_N input clock requirements for XFI , SFI, XLAUI, and 50GAUI-2/25GAUI (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
2. Per XFP specification, Rev 4.5, the Module Jitter Generation spec at XFI optical output is 10mUI (RMS) and 100 mUI (p-p). In the CDR mode, the host is contributing 7 mUI (RMS) and 50 mUI (p-p) jitter.						

3.23.3 SerDes transmitter and receiver reference circuits

This figure shows the reference circuits for SerDes data lane's transmitter and receiver.

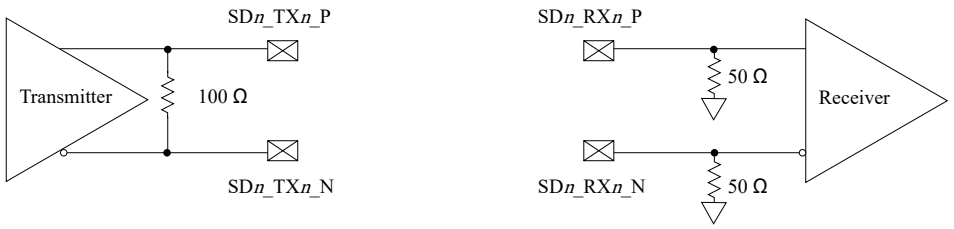


Figure 47. SerDes transmitter and receiver reference circuits

The DC and AC specifications of the SerDes data lanes are defined in each interface protocol section below based on the application usage:

- PCI Express
- SATA
- SGMII
- USXGMII
- XFI
- SFI
- 50GAUI-2, 25G-AUI
- XLAUI
- 40GBase-KR

Note that an external AC-coupling capacitor is required for the above serial transmission protocols with the capacitor value defined in the specification of each protocol section.

3.23.4 PCI Express

3.23.4.1 Clocking dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 ppm of each other at all times. This is specified to allow bit rate clock sources with a ±300 ppm tolerance.

3.23.4.2 PCI Express clocking requirements for SDn_PLLF_REF_CLK and SDn_PLLS_REF_CLK

SerDes 1 and SerDes 2 SD[1:2]_PLLF_REF_CLK/SD[1:2]_PLLF_REF_CLK_B and SerDes 2 SD2_PLLS_REF_CLK/ SD2_PLLS_REF_CLK_B may be used for various SerDes PCI Express configurations based on the RCW Configuration field SRDS_PRTCL. PCI Express is supported on SerDes 1 and 2.

For more information on these specifications, see SerDes reference clocks.

3.23.4.3 PCI Express DC electrical characteristics

This section describes the PCI Express DC physical layer transmitter specifications for 2.5 GT/s, 5 GT/s, and 8 GT/s.

This table defines the PCI Express 1.0 (2.5 GT/s) DC electrical characteristics for the differential output at all transmitters. The parameters are specified at the component pins.

Table 65. PCI Express 1.0 (2.5 GT/s) differential transmitter output DC electrical characteristics (SD_OV $_{DD}$ = 1.8V) [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential peak-to-peak output voltage	$V_{TX-DIFFP-P}$	800.0	1000.0	1200.0	mV	2
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO}$	3.0	3.5	4.0	dB	3
DC differential transmitter impedance	$Z_{TX-DIFF-DC}$	80.0	100.0	120.0	Ω	4
Transmitter DC impedance	Z_{TX-DC}	40.0	50.0	60.0	Ω	5

1. For recommended operating conditions, see Recommended Operating Conditions.
2. $V_{TX\_DIFFp-p} = 2 \times | V_{TX-D+} - V_{TX-D-} |$
3. Ratio of $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition.
4. Transmitter DC differential mode low impedance
5. Required transmitter D+ as well as D- DC Impedance during all states.

This table defines the DC electrical characteristics for the PCI Express 1.0 (2.5 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 66. PCI Express 1.0 (2.5 GT/s) differential receiver input DC electrical characteristics (SD_SV $_{DD}$ = 0.9V) [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential peak-to-peak voltage	$V_{RX-DIFFP-P}$	175.0	1000.0	1200.0	mV	2, 3
DC differential input impedance	$Z_{RX-DIFF-DC}$	80.0	100.0	120.0	Ω	4, 5
DC input impedance	Z_{RX-DC}	40.0	50.0	60.0	Ω	6, 3, 5
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50.0	-	-	kΩ	7, 8
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65.0	-	175.0	mV	9, 3

1. For recommended operating conditions, see Recommended Operating Conditions.
2. $V_{RX\_DIFFp-p} = 2 \times | V_{RX-D+} - V_{RX-D-} |$
3. Measured at the package pins with a test load of 50Ω to GND on each pin.

Table continues on the next page...

Table 66. PCI Express 1.0 (2.5 GT/s) differential receiver input DC electrical characteristics (SD_SV $_{DD}$ = 0.9V) [1] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
4. Receiver DC differential mode impedance. 5. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all configured lanes on a port. 6. Required receiver D+ as well as D- DC impedance (50 ± 20% tolerance). 7. Required receiver D+ as well as D- DC impedance when the receiver terminations do not have power. 8. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300mV above the receiver ground. 9. $V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p} = 2 \times \lvert V_{RX\text{-}D+} - V_{RX\text{-}D-} \rvert$						

This table defines the PCI Express 2.0 (5 GT/s) DC electrical characteristics for the differential output at all transmitters. The parameters are specified at the component pins.

Table 67. PCI Express 2.0 (5 GT/s) differential transmitter output DC electrical characteristics (SD_OV $_{DD}$ = 1.8V) [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential peak-to-peak output voltage	$V_{TX\text{-}DIFFP\text{-}P}$	800.0	1000.0	1200.0	mV	2
Low power differential peak-peak output voltage	$V_{TX\text{-}DIFFP\text{-}P\text{-}LOW}$	400.0	500.0	1200.0	mV	2
De-emphasized differential output voltage (ratio)	$V_{TX\text{-}DE\text{-}RATIO\text{-}3.5dB}$	3.0	3.5	4.0	dB	3
De-emphasized differential output voltage (ratio)	$V_{TX\text{-}DE\text{-}RATIO\text{-}6.0dB}$	5.5	6.0	6.5	dB	3
DC differential transmitter impedance	$Z_{TX\text{-}DIFF\text{-}DC}$	80.0	100.0	120.0	Ω	4
Transmitter DC impedance	$Z_{TX\text{-}DC}$	40.0	50.0	60.0	Ω	5
1. For recommended operating conditions, see Recommended Operating Conditions. 2. $V_{TX\_DIFFp\text{-}p} = 2 \times \lvert V_{TX\text{-}D+} - V_{TX\text{-}D-} \rvert$ 3. Ratio of $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition. 4. Transmitter DC differential mode low impedance 5. Required transmitter D+ as well as D- DC Impedance during all states.						

This table defines the DC electrical characteristics for the PCI Express 2.0 (5 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 68. PCI Express 2.0 (5 GT/s) differential receiver input DC electrical characteristics (SD_SV $_{DD}$ = 0.9V) [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential peak-to-peak voltage	$V_{RX-DIFFP-P}$	120.0	1000.0	1200.0	mV	2, 3
DC differential input impedance	$Z_{RX-DIFF-DC}$	80.0	100.0	120.0	Ω	4, 5
DC input impedance	Z_{RX-DC}	40.0	50.0	60.0	Ω	6, 3, 5
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50.0	-	-	kΩ	7, 8
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65.0	-	175.0	mV	9, 3

1. For recommended operating conditions, see Recommended Operating Conditions.

2. $V_{RX\_DIFFp-p} = 2 \times | V_{RX-D+} - V_{RX-D-} |$

3. Measured at the package pins with a test load of 50Ω to GND on each pin.

4. Receiver DC differential mode impedance.

5. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all configured lanes on a port.

6. Required receiver D+ as well as D- DC impedance (50 ± 20% tolerance).

7. Required receiver D+ as well as D- DC impedance when the receiver terminations do not have power.

8. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300mV above the receiver ground.

9. $V_{RX-IDLE-DET-DIFFp-p} = 2 \times | V_{RX-D+} - V_{RX-D-} |$

This table defines the PCI Express 3.0 (8 GT/s) DC electrical characteristics for the differential output at all transmitters. The parameters are specified at the component pins.

Table 69. PCI Express 3.0 (8 GT/s) differential transmitter output DC electrical characteristics (SD_OV $_{DD}$ = 1.8V) [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Full swing transmitter voltage with no TX Eq	$V_{TX-FS-NO-EQ}$	800.0	-	1300.0	mVp-p	2
Reduced swing transmitter voltage with no TX Eq	$V_{TX-RS-NO-EQ}$	400.0	-	1300.0	mV	2
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-3.5dB}$	3.0	3.5	4.0	dB	3

Table continues on the next page...

Table 69. PCI Express 3.0 (8 GT/s) differential transmitter output DC electrical characteristics (SD_OV $_{DD}$ = 1.8V) [1] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-6.0dB}$	5.5	6.0	6.5	dB	3
Minimum swing during EIEOS for full swing	$V_{TX-EIEOS-FS}$	250.0	-	-	mVp-p	4
Minimum swing during EIEOS for reduced swing	$V_{TX-EIEOS-RS}$	232.0	-	-	mVp-p	4
DC differential transmitter impedance	$Z_{TX-DIFF-DC}$	80.0	100.0	120.0	Ω	5
Transmitter DC impedance	Z_{TX-DC}	40.0	50.0	60.0	Ω	6

1. For recommended operating conditions, see Recommended Operating Conditions.

2. Voltage measurements for $V_{TX-FS-NO-EQ}$ and $V_{TX-RS-NO-EQ}$ are made using the 64-zeroes/64-ones pattern in the compliance pattern.

3. Ratio of $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition.

4. Voltage limits comprehend both full swing and reduced swing modes. The transmitter must reject any changes that would violate this specification. The maximum level is covered in the $V_{TX-FS-NO-EQ}$ measurement which represents the maximum peak voltage the transmitter can drive. The $V_{TX-EIEOS-FS}$ and $V_{TX-EIEOS-RS}$ voltage limits are imposed to guarantee the EIEOS threshold of 175 mV_{P-P} at the receiver pin. This parameter is measured using the actual EIEOS pattern that is part of the compliance pattern and then removing the ISI contribution of the breakout channel.

5. Transmitter DC differential mode low impedance

6. Required transmitter D+ as well as D- DC Impedance during all states.

This table defines the DC electrical characteristics for the PCI Express 3.0 (8 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 70. PCI Express 3.0 (8 GT/s) differential receiver input DC electrical characteristics (SD_SV $_{DD}$ = 0.9V) [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
DC differential input impedance	$Z_{RX-DIFF-DC}$	80.0	100.0	120.0	Ω	2, 3
DC input impedance	Z_{RX-DC}	40.0	50.0	60.0	Ω	4, 5, 3
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50.0	-	-	kΩ	6, 7
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65.0	-	175.0	mV	8, 5

Table continues on the next page...

Table 70. PCI Express 3.0 (8 GT/s) differential receiver input DC electrical characteristics (SD_SV $_{DD}$ = 0.9V) [1] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Generator launch voltage	$V_{RX-LAUNCH-8G}$	-	800.0	-	mV	9
Eye height (-20dB channel)	$V_{RX-SV-8G}$	25.0	-	-	mV	10
Eye height (-12dB channel)	$V_{RX-SV-8G}$	50.0	-	-	mV	10
Eye height (-3dB channel)	$V_{RX-SV-8G}$	200.0	-	-	mV	10

1. For recommended operating conditions, see Recommended Operating Conditions.

2. Receiver DC differential mode impedance.

3. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all configured lanes on a port.

4. Required receiver D+ as well as D- DC impedance (50 ± 20% tolerance).

5. Measured at the package pins with a test load of 50Ω to GND on each pin.

6. Required receiver D+ as well as D- DC impedance when the receiver terminations do not have power.

7. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300mV above the receiver ground.

8. $V_{RX-IDLE-DET-DIFFp-p} = 2 \times | V_{RX-D+} - V_{RX-D-} |$

9. Measured at TP1 per PCI Express base specification Rev 3.0.

10. Measured at TP2 per PCI Express base specification Rev 3.0. $V_{RX-SV-8G}$ is tested at three different voltages to ensure the receiver device under test is capable of equalizing over a range of channel loss profiles. In the parameter names, "SV" refers to stressed voltage. $V_{RX-SV-8G}$ is referenced to TP2P and is obtained after post-processing data is captured at TP2.

3.23.4.4 PCI Express AC timing specifications

This section describes the PCI Express AC physical layer transmitter specifications for 2.5 GT/s, 5 GT/s, and 8 GT/s.

This table defines the PCI Express 1.0 (2.5 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The ACtiming specifications do not include RefClk jitter.

Table 71. PCI Express 1.0 (2.5 GT/s) differential transmitter output AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval	UI	399.88	400.0	400.12	ps	1
Minimum transmitter eye width	T_{TX-EYE}	0.75	-	-	UI	2, 3, 4, 5

Table continues on the next page...

Table 71. PCI Express 1.0 (2.5 GT/s) differential transmitter output AC timing specifications (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Maximum time between the jitter median and maximum deviation from the median	$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	-	-	0.125	UI	6, 3, 4, 5
AC coupling capacitor	C_{TX}	75.0	-	200.0	nF	7, 8

1. Each UI is 400 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.

2. The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER}$ = 1 -T_{TX-EYE} = 0.25 UI. Does not include spread-spectrum or REFCLK jitter. Includes devices random jitter at 10^{-12}.

3. Specified at the measurement point into a timing and voltage test load and measured over any 250 consecutive transmitter Uis.

4. A T_{TX-EYE} - 0.75 UI provides for a a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.25 UI for the transmitter collected over any 250 consecutive transmitter Uis. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total transmitter budget collected over any 250 consecutive transmitter UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.

5. See Figure 48.

6. Jiiter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p}$ = 0 V) in relation to a recovered transmitter UI. A recovered transmitter UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the transmitter UI.

7. All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself.

8. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required.

This table defines the AC timing specifications for the PCI Express 1.0 (2.5 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 72. PCI Express 1.0 (2.5 GT/s) differential receiver input AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval	UI	399.88	400.0	400.12	ps	1
Minimum receiver eye width	T_{RX-EYE}	0.4	-	-	UI	2, 3, 4
Maximum time between the jitter median and maximum deviation from the median	$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	-	-	0.3	UI	3, 4, 5

1. Each UI is 400 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.

2. The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as $T_{RX-MAX-JITTER}$ = 1 - T_{RX-EYE} = 0.6 UI.

Table continues on the next page...

Table 72. PCI Express 1.0 (2.5 GT/s) differential receiver input AC timing specifications (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
3. Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0 V) in relation to a recovered transmitter UI. A recovered transmitter UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the transmitter UI. 4. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive transmitter UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the receiver and transmitter are not derived from the same reference clock, the transmitter UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram. 5. It is recommended that the recovered transmitter UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.						

This table defines the PCI Express 2.0 (5 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 73. PCI Express 2.0 (5 GT/s) differential transmitter output AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval	UI	199.94	200.0	200.06	ps	1
Minimum transmitter eye width	T_{TX-EYE}	0.75	-	-	UI	2, 3, 4, 5
Transmitter deterministic jitter > 1.5 MHz	$T_{TX-HF-DJ-DD}$	-	-	0.15	UI	-
Transmitter RMS jitter < 1.5 MHz	$T_{TX-LF-RMS}$	-	3.0	-	ps	6
AC coupling capacitor	C_{TX}	75.0	-	200.0	nF	7, 8
1. Each UI is 200 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations. 2. The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER}$ = 1 -T_{TX-EYE} = 0.25 UI. Does not include spread-spectrum or REFCLK jitter. Includes devices random jitter at 10^{-12}. 3. Specified at the measurement point into a timing and voltage test load and measured over any 250 consecutive transmitter Uis. 4. A T_{TX-EYE} - 0.75 UI provides for a a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.25 UI for the transmitter collected over any 250 consecutive transmitter Uis. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total transmitter budget collected over any 250 consecutive transmitter UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. 5. See Figure 48. 6. Reference input clock RMS jitter (< 1.5 MHz) at pin < 1 ps.						

Table continues on the next page...

Table 73. PCI Express 2.0 (5 GT/s) differential transmitter output AC timing specifications (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
7. All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. 8. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required.						

This table defines the AC timing specifications for the PCI Express 2.0 (5 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 74. PCI Express 2.0 (5 GT/s) differential receiver input AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval	UI	199.4	200.0	200.06	ps	1
Max receiver inherent timing error	$T_{RX-TJ-CC}$	-	-	0.4	UI	-
Max receiver inherent deterministic timing error	$T_{RX-DJ-DD-CC}$	-	-	0.3	UI	-
1. Each UI is 200 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.						

This table defines the PCI Express 3.0 (8 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 75. PCI Express 3.0 (8 GT/s) differential transmitter output AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval	UI	124.9625	125.0	125.0375	ps	1
AC coupling capacitor	C_{TX}	176.0	-	265.0	nF	2, 3
Transmitter uncorrelated total jitter	T_{TX-UTJ}	-	-	31.25	ps p-p	-
Transmitter uncorrelated deterministic jitter	$T_{TX-UDJ-DD}$	-	-	12.0	ps p-p	-
Total uncorrelated pulse width jitter (PWJ)	$T_{TX-UPW-TJ}$	-	-	24.0	ps p-p	4, 5
Deterministic data dependent jitter (DjDD) uncorrelated pulse width jitter (PWJ)	$T_{TX-UPW-DJDD}$	-	-	10.0	ps p-p	4, 5
Data-dependent jitter	T_{TX-DDJ}	-	-	18.0	ps p-p	4, 5, 6
1. Each UI is 125 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.						

Table continues on the next page...

Table 75. PCI Express 3.0 (8 GT/s) differential transmitter output AC timing specifications (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
2. All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. 3. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required. 4. Measured with optimized preset value after de-embedding to transmitter pin. 5. PWJ parameters shall be measured after data-dependent jitter (DDJ) separation. 6. The AC specifications do not include Refclk jitter						

This table defines the AC timing specifications for the PCI Express 3.0 (8 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 76. PCI Express 3.0 (8 GT/s) differential receiver input AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval	UI	124.9625	125.0	125.0375	ps	1, 2
Eye width at TP2P	$T_{RX-SV-8G}$	0.3	-	0.35	UI	2
Differential mode interference	$V_{RX-SV-DIFF-8G}$	14.0	-	-	mV	3
Sinusoidal jitter at 100 MHz	$T_{RX-SV-SJ-8G}$	-	-	0.1	UI p-p	4, 5
Random jitter	$T_{RX-SV-RJ-8G}$	-	-	2.0	ps RMS	6, 5
1. Each UI is 125 ps ± 300 ppm. UI does not account for spreadspectrum clock dictated variations. 2. T_{RX-SV} is referenced to TP2P and is obtained after post-processing data is captured at TP2. T_{RX-SV} includes the effects of applying the behavioral receiver model and receiver behavioral equalization. 3. Frequency = 2.1GHz. $V_{RX-SV-DIFF-8G}$ voltage may need to be adjusted over a wide range for the different loss calibration channels. 4. Fixed at 100 MHz. The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency. 5. See Figure 49. 6. Random jitter spectrally flat before filtering. Random jitter (Rj) is applied over the following range: The low frequency limit may be between 1.5 and 10 MHz, and the upper limit is 1.0 GHz. Rj may be adjusted to meet the 0.3 UI value for $T_{RX-SV-8G}$.						

The AC timing and voltage parameters must be verified at the measurement point. The package pins of the device must be connected to the test/measurement load within 0.2 inches of that load, as shown in the following figure. Note that the allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D- not being exactly matched in length at the package pin boundary. If the vendor does not explicitly state where the measurement point is located, the measurement point is assumed to be the D+ and Dpackage pins.

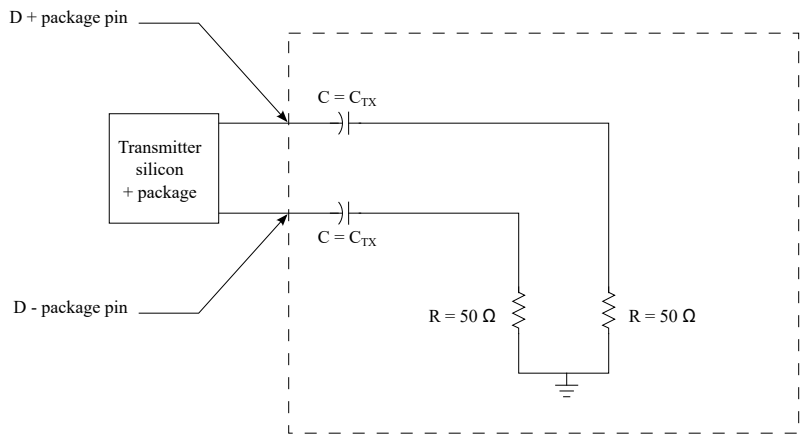


Figure 48. Test and measurement load

This figure shows the swept sinusoidal jitter mask.

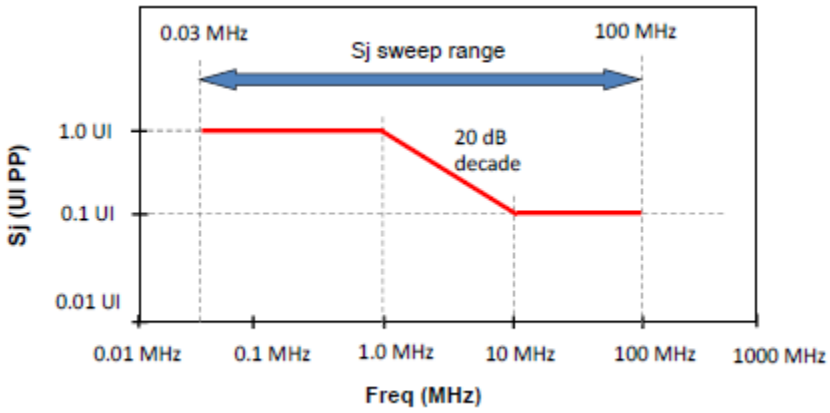


Figure 49. Swept sinusoidal jitter mask

3.23.5 Serial ATA (SATA)

3.23.5.1 SATA DC electrical characteristics

This table provides the differential transmitter output DC characteristics for the SATAinterface at Gen1i/1m or 1.5 Gbits/s transmission.

Table 77. SATA Gen 1i/1m 1.5G transmitter DC electrical characteristics (SD_OV $_{DD}$ = 1.8V) [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Transmitter differential output voltage	V SATA_TXDIFF	400.0	500.0	600.0	mV p-p	Terminated by a 50Ω load.

Table continues on the next page...

Table 77. SATA Gen 1i/1m 1.5G transmitter DC electrical characteristics (SD_OV $_{DD}$ = 1.8V) [1] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Transmitter differential pair impedance	Z SATA_TXDIFFIM	85.0	100.0	115.0	Ω	DC impedance.
1. For recommended operating conditions, see Recommended Operating Conditions. 2. Terminated by a 50Ω load. 3. DC impedance.						

This table provides the Gen1i/1m or 1.5 Gbits/s differential receiver input DC characteristics for the SATA interface.

Table 78. SATA Gen 1i/1m 1.5G receiver input DC electrical characteristics (SD_SV $_{DD}$ = 0.9V) [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential input voltage	V SATA_RXDIFF	240.0	500.0	600.0	mV p-p	2
Differential receiver input impedance	Z SATA_RXSEIM	85.0	100.0	115.0	Ω	3
OOB signal detection threshold	V SATA_OOB	50.0	120.0	240.0	mV p-p	-
1. For recommended operating conditions, see Recommended Operating Conditions. 2. Voltage relative to common of either signal comprising a differential pair. 3. DC impedance.						

This table provides the differential transmitter output DC characteristics for the SATA interface at Gen2i/2m or 3.0 Gbits/s transmission.

Table 79. SATA Gen 2i/2m 3G transmitter DC electrical characteristics (SD_OV $_{DD}$ = 1.8V) [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Transmitter differential output voltage	V SATA_TXDIFF	400.0	-	700.0	mV p-p	Terminated by a 50Ω load.
Transmitter differential pair impedance	Z SATA_TXDIFFIM	85.0	100.0	115.0	Ω	DC impedance.
1. For recommended operating conditions, see Recommended Operating Conditions. 2. Terminated by a 50Ω load. 3. DC impedance.						

This table provides the Gen2i/2m or 3 Gbits/s differential receiver input DC characteristics for the SATA interface.

Table 80. SATA Gen 2i/2m 3G receiver input DC electrical characteristics (SD_SV $_{DD}$ = 0.9V) [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential input voltage	V SATA_RXDIFF	240.0	-	750.0	mV p-p	2
Differential receiver input impedance	Z SATA_RXSEIM	85.0	100.0	115.0	Ω	3
OOB signal detection threshold	V SATA_OOB	75.0	120.0	240.0	mV p-p	-

1. For recommended operating conditions, see Recommended Operating Conditions.
2. Voltage relative to common of either signal comprising a differential pair.
3. DC impedance.

This table provides the differential transmitter output DC characteristics for the SATA interface at Gen 3i transmission.

Table 81. SATA Gen 3i transmitter DC electrical characteristics (SD_OV $_{DD}$ = 1.8V) [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Transmitter differential output voltage	V SATA_TXDIFF	240.0	-	900.0	mV p-p	Terminated by a 50Ω load.
Transmitter differential pair impedance	Z SATA_TXDIFFIM	85.0	100.0	115.0	Ω	DC impedance.

1. For recommended operating conditions, see Recommended Operating Conditions.
2. Terminated by a 50Ω load.
3. DC impedance.

This table provides the Gen 3i differential receiver input DC characteristics for the SATAinterface.

Table 82. SATA Gen 3i receiver input DC electrical characteristics (SD_SV $_{DD}$ = 0.9V) [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential input voltage	V SATA_RXDIFF	240.0	-	1000.0	mV p-p	2
Differential receiver input impedance	Z SATA_RXSEIM	85.0	100.0	115.0	Ω	3

Table continues on the next page...

Table 82. SATA Gen 3i receiver input DC electrical characteristics (SD_SV $_{DD}$ = 0.9V) [1] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
OOB signal detection threshold	V $_{SATA\_OOB}$	75.0	120.0	200.0	mV p-p	-

1. For recommended operating conditions, see Recommended Operating Conditions.

2. Voltage relative to common of either signal comprising a differential pair.

3. DC impedance.

3.23.5.2 SATA AC timing specifications

This table provides the AC requirements for the SATA reference clock. These requirements must be guaranteed by the customer's application design.

Table 83. SATA reference clock input requirements

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SDn_REF_CLKn_P/ SDn_REF_CLKn_N frequency range	t $_{CLK\_REF}$	-	100 / 125	-	MHz	1
SDn_REF_CLK *z*_P/ SDn_REF_CLKn_N frequency tolerance	t $_{CLK\_TOL}$	-350.0	-	350.0	ppm	-
SDn_REF_CLKn_P/ SDn_REF_CLKn_N reference clock duty cycle	t $_{CLK\_DUTY}$	40	50	60	%	2
SDn_REF_CLKn_P/ SDn_REF_CLKn_N cycle-to-cycle clock jitter (period jitter)	t $_{CLK\_CJ}$	-	-	100.0	ps	3
SDn_REF_CLKn_P/ SDn_REF_CLKn_N total reference clock jitter, phase jitter (peak-to-peak)	t $_{CLK\_PJ}$	-50.0	-	50.0	-	3, 4, 5

1. **Caution:** Only 100 MHz and 125 MHz have been tested. In-between values do not work correctly with the rest of the system.

2. Measurement taken from differential waveform.

3. At RefClk input.

4. In a frequency band from 150 kHz to 15 MHz at BER of 10 $^{-12}$.

5. Total peak-to-peak deterministic jitter must be less than or equal to 50 ps.

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen 1i/1m or 1.5 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

Table 84. Gen 1i/1m 1.5 G transmitter AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval	UI	666.4333	666.6667	670.2333	-	-
Channel speed	t_{CH_SPEED}	-	1.5	-	Gbps	-
Total jitter, data-data 5 UI	$U_{SATA\_TXTJ5UI}$	-	-	0.355	UI p-p	1
Total jitter, data-data 250 UI	$U_{SATA\_TXTJ250UI}$	-	-	0.47	UI p-p	1
Deterministic jitter, data-data 5 UI	$U_{SATA\_TXDJ5UI}$	-	-	0.175	UI p-p	1
Deterministic jitter, data-data 250 UI	$U_{SATA\_TXDJ250UI}$	-	-	0.22	UI p-p	1
1. Measured at transmitter output pins peak-to-peak phase variation; random data pattern.						

This table provides the Gen1i/1m or 1.5 Gbits/s differential receiver input AC characteristics for the SATA interface. The AC timing specifications do not include RefClk jitter.

Table 85. Gen 1i/1m 1.5 G receiver AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval	UI	666.4333	666.6667	670.2333	-	-
Total jitter, data-data 5 UI	$U_{SATA\_RXTJ5UI}$	-	-	0.43	UI p-p	Measured at the receiver.
Total jitter, data-data 250 UI	$U_{SATA\_RXTJ250UI}$	-	-	0.6	UI p-p	Measured at the receiver.
Deterministic jitter, data-data 5 UI	$U_{SATA\_RXDJ5UI}$	-	-	0.25	UI p-p	Measured at the receiver.
Deterministic jitter, data-data 250 UI	$U_{SATA\_RXDJ250UI}$	-	-	0.35	UI p-p	Measured at the receiver.

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen 2i/2m or 3.0 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

Table 86. Gen 2i/2m 3 G transmitter AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval	UI	333.2167	333.3333	335.1167	-	-
Channel speed	t_{CH_SPEED}	-	3.0	-	Gbps	-
Total jitter, $f_{C3DB} = f_{BAUD} \div 500$	$U_{SATA\_TXTJfB/500}$	-	-	0.37	UI p-p	1
Total jitter, $f_{C3DB} = f_{BAUD} \div 1667$	$U_{SATA\_TXTJfB/1667}$	-	-	0.55	UI p-p	1
Deterministic jitter, $f_{C3DB} = f_{BAUD} \div 500$	$U_{SATA\_TXTJfB/500}$	-	-	0.19	UI p-p	1
Deterministic jitter, $f_{C3DB} = f_{BAUD} \div 1667$	$U_{SATA\_TXTJfB/1667}$	-	-	0.35	UI p-p	1
1. Measured at transmitter output pins peak-to-peak phase variation; random data pattern.						

This table provides the differential receiver input AC characteristics for the SATA interface at Gen2i/2m or 3.0 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

Table 87. Gen 2i/2m 3 G receiver AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval	UI	333.2167	333.3333	335.1167	-	-
Total jitter, $f_{C3DB} = f_{BAUD} \div 500$	$U_{SATA\_RXTJfB/500}$	-	-	0.6	UI p-p	Measured at the receiver.
Total jitter, $f_{C3DB} = f_{BAUD} \div 1667$	$U_{SATA\_RXTJfB/1667}$	-	-	0.65	UI p-p	Measured at the receiver.
Deterministic jitter, $f_{C3DB} = f_{BAUD} \div 500$	$U_{SATA\_RXTJfB/500}$	-	-	0.42	UI p-p	Measured at the receiver.
Deterministic jitter, $f_{C3DB} = f_{BAUD} \div 1667$	$U_{SATA\_RXTJfB/1667}$	-	-	0.35	UI p-p	Measured at the receiver.

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen 3i transmission. The AC timing specifications do not include RefClk jitter.

Table 88. Gen 3i transmitter AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit
Unit Interval	UI	166.6083	167.6667	167.5583	-
Channel speed	t_{CH_SPEED}	-	6.0	-	Gbps
Total jitter before and after compliance interconnect channel	J_T	-	-	0.52	UI p-p
Random jitter before compliance interconnect channel	J_R	-	-	0.18	UI p-p

This table provides the differential receiver input AC characteristics for the SATA interface at Gen 3i transmission The AC timing specifications do not include RefClk jitter.

Table 89. Gen 3i receiver AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit
Unit Interval	UI	166.6083	167.6667	167.5583	-
Total jitter before and after compliance interconnect channel	J_T	-	-	0.6	UI p-p
Random jitter before compliance interconnect channel	J_R	-	-	0.18	UI p-p

3.23.6 SGMII interface

Each SGMII port features a 4-wire AC-coupled serial link from the SerDes interface of the chip, as shown in Figure 50, where C_{TX} is the external (on board) AC-coupled capacitor. Each SerDes transmitter differential pair features 100-Ω output impedance. Each input of the SerDes receiver differential pair features 50-Ω on-die termination to XGND*n*. The reference circuit of the SerDes transmitter and receiver is shown in figure *SerDes transmitter and receiver reference circuits*.

3.23.6.1 SGMII clocking requirements for SDn_REF_CLK1_P and SDn_REF_CLK1_N

When operating in SGMII mode, a SerDes reference clock is required on SDn_REF_CLK[1:2]_P and SDn_REF_CLK[1:2]_N pins. Both SerDes 1 and SerDes 2 may be used for SGMII configurations based on the RCW Configuration field SRDS_PRTCL.

For more information on these specifications, see SerDes reference clocks.

3.23.6.2 SGMII DC electrical characteristics

This table describes the SGMII SerDes transmitter AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SDn_TXn_P and SDn_TXn_N), as shown in the SGMII transmitter DC measurement circuit figure below.

Table 90. SGMII DC transmitter electrical characteristics (SD_OV_{DD} = 1.8V) [1, 12, 13]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output high voltage	V_{OH}	-	-	1.5 x $\lvert V_{OD} \rvert_{-max}$	mV	2

Table continues on the next page...

Table 90. SGMII DC transmitter electrical characteristics (SD_OV $_{DD}$ = 1.8V) [1, 12, 13] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output low voltage	V_{OL}	$\|V_{OD}\|_{-min}/2$	-	-	mV	2
Output differential voltage	$\|V_{OD}\|$	320.0	500.0	725.0	mV	3, 4, 5
Output differential voltage	$\|V_{OD}\|$	293.8	459.0	665.6	mV	3, 4, 6
Output differential voltage	$\|V_{OD}\|$	266.9	417.0	604.7	mV	3, 4, 7
Output differential voltage	$\|V_{OD}\|$	240.6	376.0	545.2	mV	3, 4, 8
Output differential voltage	$\|V_{OD}\|$	213.1	333.0	482.9	mV	3, 4, 9
Output differential voltage	$\|V_{OD}\|$	186.9	292.0	423.4	mV	3, 4, 10
Output differential voltage	$\|V_{OD}\|$	160.0	250.0	362.5	mV	3, 4, 11
Output impedance (differential)	R_O	80.0	100.0	120.0	Ω	-

1. For recommended operating conditions, see Recommended Operating Conditions.

2. This does not align to DC-coupled SGMII.

3. $|V_{OD}| = |V_{SD\_TXn\_P} - V_{SD\_TXn\_N}|$. $|V_{OD}|$ is also referred to as output differential peak voltage. $V_{TX\text{-}DIFFp\text{-}p} = 2 \times |V_{OD}|$.

4. The $|V_{OD}|$ value shown in Typ column is based on the condition of SD_OVDD-Typ, no common mode offset variation. SerDes transmitter is terminated with 100-Ω differential load between SDn_TXn_P and SDn_TXn_N.

5. TECR0[AMP_RED]=0b000000

6. TECR0[AMP_RED]=0b000001

7. TECR0[AMP_RED]=0b000011

8. TECR0[AMP_RED]=0b000010

9. TECR0[AMP_RED]=0b000110 (default)

10. TECR0[AMP_RED]=0b000111

11. TECR0[AMP_RED]=0b010000

12. See Figure 50.

13. See Figure 51.

This figure shows an example of a 4-wire AC-coupled SGMII serial link connection.

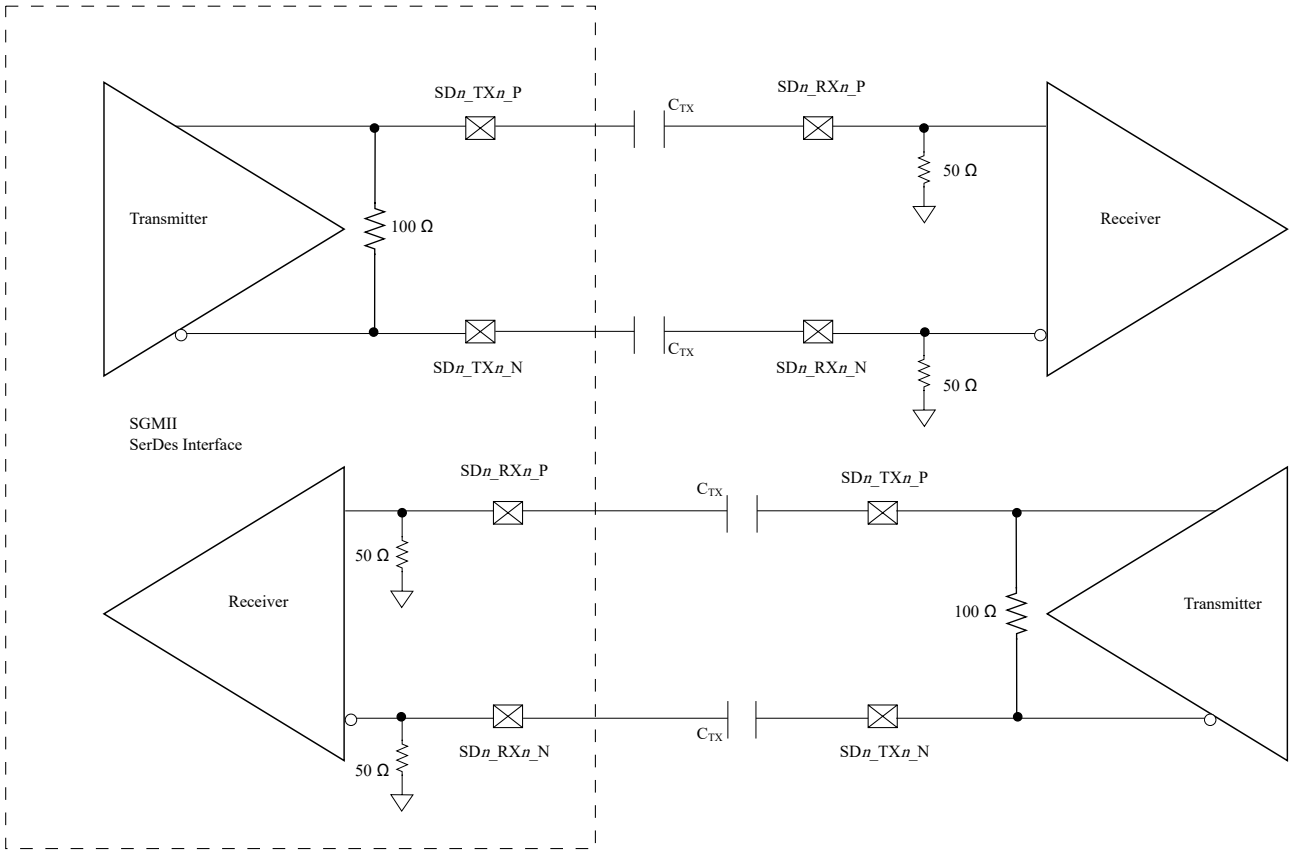


Figure 50. 4-wire AC-coupled SGMII serial link connection example

This figure shows the SGMII transmitter DC measurement circuit.

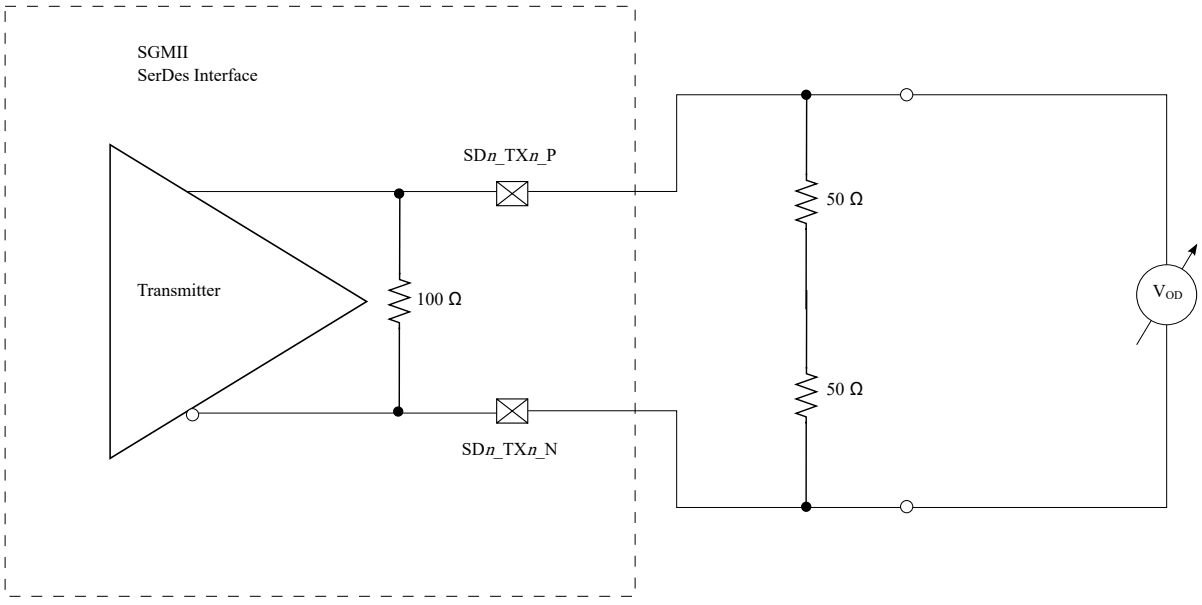


Figure 51. SGMII transmitter DC measurement circuit

This table lists the SGMII DC receiver electrical characteristics. Source synchronousclocking is not supported. Clock is recovered from the data.

Table 91. SGMII DC receiver electrical characteristics (SD_SV $_{DD}$ = 0.9V) [1]

Parameter	Symbol	Min	Max	Unit	Notes
DC input voltage range	V_{IN}	N/A	N/A	-	2
Input differential voltage (REIDL_TH = 001, default)	$V_{RX\_DIFFp\text{-}p}$	100.0	1200.0	mV	3, 4
Input differential voltage (REIDL_TH = 100)	$V_{RX\_DIFFp\text{-}p}$	175.0	1200.0	mV	3, 4
Loss of signal threshold (REIDL_TH = 001, default)	V_{LOS}	30.0	100.0	mV	5, 4
Loss of signal threshold (REIDL_TH = 100)	V_{LOS}	65.0	175.0	mV	5, 4
Receiver differential input impedance	Z_{RX_DIFF}	80.0	120.0	Ω	-

1. For recommended operating conditions, see Recommended Operating Conditions.
2. Input must be externally AC coupled.
3. $V_{RX\_DIFFp\text{-}p}$ is also referred to as peak-to-peak input differential voltage.
4. The REIDL_TH shown in the table referes to the chip's SRDSxLNmGCR1[REIDL_TH] bit field.
5. The concept of this parameter is equivalent to the electrical idle detect threshold parameter in PCI Express.

3.23.6.3 SGMII AC timing specifications

This table provides the SGMII transmit AC timing specifications. A source synchronous clock is not supported. The AC timing specifications do not include RefClk jitter.

Table 92. SGMII transmitter AC timing specifications [4]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic jitter	J_D	-	-	0.17	UI p-p	-
Total jitter	J_T	-	-	0.35	UI p-p	1
Unit interval: 1.25 GBaud (SGMII)	UI	800-100ppm	800.0	800+100ppm	ps	2
AC coupling capacitor	C_{TX}	10.0	-	200.0	nF	3

1. See Figure 53.
2. Each UI is 800 ps ± 100 ppm or 320 ps ± 100 ppm.
3. The external AC coupling capacitor is required. It is recommended that it be placed near the device transmitter output.
4. See Figure 52.

Transmitter and receiver AC characteristics are measured at the transmitter outputs (SDn_TXn_P and SDn_TXn_N) or at the receiver inputs (SDn_RXn_P and SDn_RXn_N) respectively, as shown in this figure.

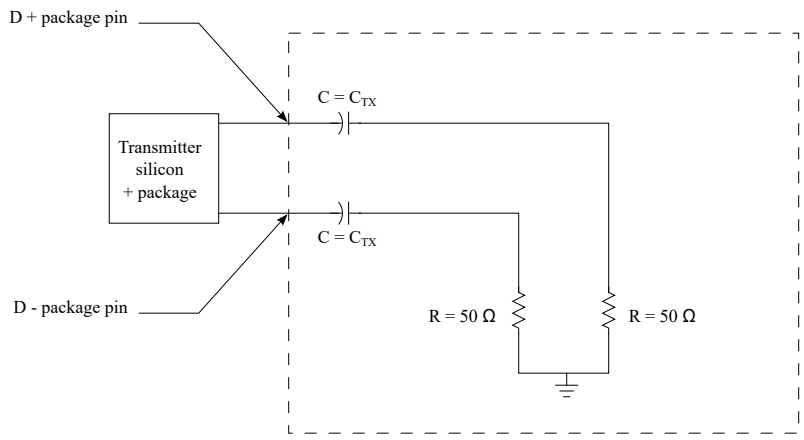


Figure 52. SGMII AC test/measurement load

This table provides the SGMII receiver AC timing specifications. TheAC timing specifications do not include RefClk jitter. Source synchronous clocking is notsupported. Clock is recovered from the data.

Table 93. SGMII receiver AC timing specifications [3]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic jitter tolerance	J_D	-	-	0.37	UI p-p	1
Combined deterministic and random jitter tolerance	J_{DR}	-	-	0.55	UI p-p	1
Total jitter tolerance	J_T	-	-	0.65	UI p-p	1, 2, 3
Unit interval: 1.25 GBaud (SGMII)	UI	800-100ppm	800.0	800+100ppm	ps	1
Bit error ratio	BER	-	-	10^{-12}	-	-

1. Measured at receiver.

2. Total jitter is composed of three components: deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of the Single-frequency sinusoidal jitter limits figure shown below. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

3. See Figure 53.

The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the unshaded region of this figure.

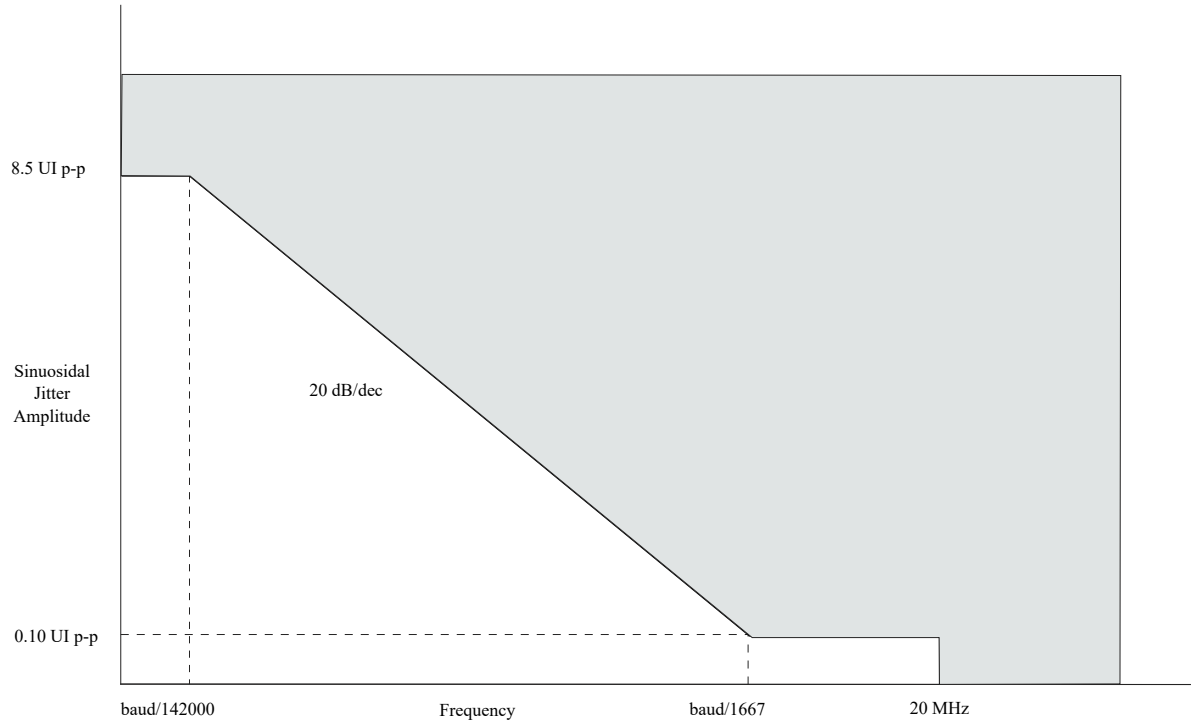


Figure 53. Single-frequency sinusoidal jitter limits

3.23.7 XFI

3.23.7.1 XFI clocking requirements for SD*n*_REF_CLK*n*_P and SD*n*_REF_CLK*n*_N

SerDes 1 and SerDes 2 (SD1_REF_CLK[1:2]_P and SD1_REF_CLK[1:2]_N and SD2_REF_CLK[1:2]_P and SD2_REF_CLK[1:2]_N) may be used for SerDes XFI configurations based on the RCW Configuration field SRDS_PRTCL.

For more information on these specifications, see SerDes reference clocks.

3.23.7.2 XFI DC electrical characteristics

This table defines the XFI transmitter DC electrical characteristics.

Table 94. XFI transmitter DC electrical characteristics (SD_OV $_{DD}$ = 1.8V) [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output differential voltage	$V_{TX-DIFF}$	360.0	-	770.0	mV	LNmTECR0[EQ_AMP_RED]= 000111
De-emphasized differential output voltage (ratio at 1.14dB)	$V_{TX-DE-RATIO-1.14dB}$	0.6	1.1	1.6	dB	LNmTECR0[EQ_POST1Q]= 00011

Table continues on the next page...

Table 94. XFI transmitter DC electrical characteristics (SD_OV $_{DD}$ = 1.8V) [1] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
De-emphasized differential output voltage (ratio at 3.5dB)	$V_{TX-DE-RATIO-3.5dB}$	3.0	3.5	4.0	dB	LNmTECR0[EQ_POST1Q]= 01000
De-emphasized differential output voltage (ratio at 4.66dB)	$V_{TX-DE-RATIO-4.66dB}$	4.1	4.6	5.1	dB	LNmTECR0[EQ_POST1Q]= 01010
De-emphasized differential output voltage (ratio at 6.0dB)	$V_{TX-DE-RATIO-6.0dB}$	5.5	6.0	6.5	dB	LNmTECR0[EQ_POST1Q]= 01100
De-emphasized differential output voltage (ratio at 9.5dB)	$V_{TX-DE-RATIO-9.5dB}$	9.0	9.5	10.0	dB	LNmTECR0[EQ_POST1Q]= 10000
Differential resistance	T_{RD}	80.0	100.0	120.0	Ω	-

1. For recommended operating conditions, see Recommended Operating Conditions.
2. LNmTECR0[EQ_AMP_RED]= 000111
3. LNmTECR0[EQ_POST1Q]= 00011
4. LNmTECR0[EQ_POST1Q]= 01000
5. LNmTECR0[EQ_POST1Q]= 01010
6. LNmTECR0[EQ_POST1Q]= 01100
7. LNmTECR0[EQ_POST1Q]= 10000

This table defines the XFI receiver DC electrical characteristics.

Table 95. XFI receiver DC electrical characteristics (SD_SV $_{DD}$ = 0.9V) [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential resistance	R_{RD}	80.0	100.0	120.0	Ω	-
Input differential voltage	$V_{RX-DIFF}$	110.0	-	1050.0	mV	Measured at receiver.

1. For recommended operating conditions, see Recommended Operating Conditions.
2. Measured at receiver.

3.23.7.3 XFI AC timing specifications

This table defines the XFI transmitter AC timing specifications. RefClk jitter is not included.

Table 96. XFI transmitter AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit
Transmitter baud Rate	T_{BAUD}	10.3125-100ppm	10.3125	10.3125+100ppm	Gb/s
Unit Interval	UI	-	96.96	-	ps
Deterministic jitter	D_J	-	-	0.15	UI p-p
Total jitter tolerance	T_J	-	-	0.3	UI p-p

This table defines the XFI receiver AC timing specifications. RefClk jitter is not included.

Table 97. XFI receiver AC timing specifications [3]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval	UI	-	96.96	-	ps	-
Receiver baud rate	R_{BAUD}	10.3125-100ppm	10.3125	10.3125+100ppm	Gb/s	-
Total non-EQJ jitter	$T_{NON-EQJ}$	-	-	0.45	UI p-p	1
Total jitter tolerance	T_J	-	-	0.65	UI p-p	1, 2

1. The total jitter (TJ) consists of Random Jitter (RJ), Duty Cycle Distortion (DCD), Periodic Jitter (PJ), and Inter-Symbol Interference (ISI). Non-EQJ jitter can include duty cycle distortion (DCD), random jitter (RJ), and periodic jitter (PJ). Non-EQJ jitter is uncorrelated to the primary data stream with exception of the DCD and so cannot be equalized by the receiver under test. It can exhibit a wide spectrum. Non - EQJ = TJ - ISI = RJ + DCD + PJ.

2. The XFI channel has a loss budget of 9.6 dB @5.5GHz. The channel loss including connector @ 5.5GHz is 6dB. The channel crosstalk and reflection margin is 3.6dB. Manual tuning of TX Equalization and amplitude will be required for performance optimization.

3. See Figure 54.

This figure shows the sinusoidal jitter tolerance of XFI receiver.

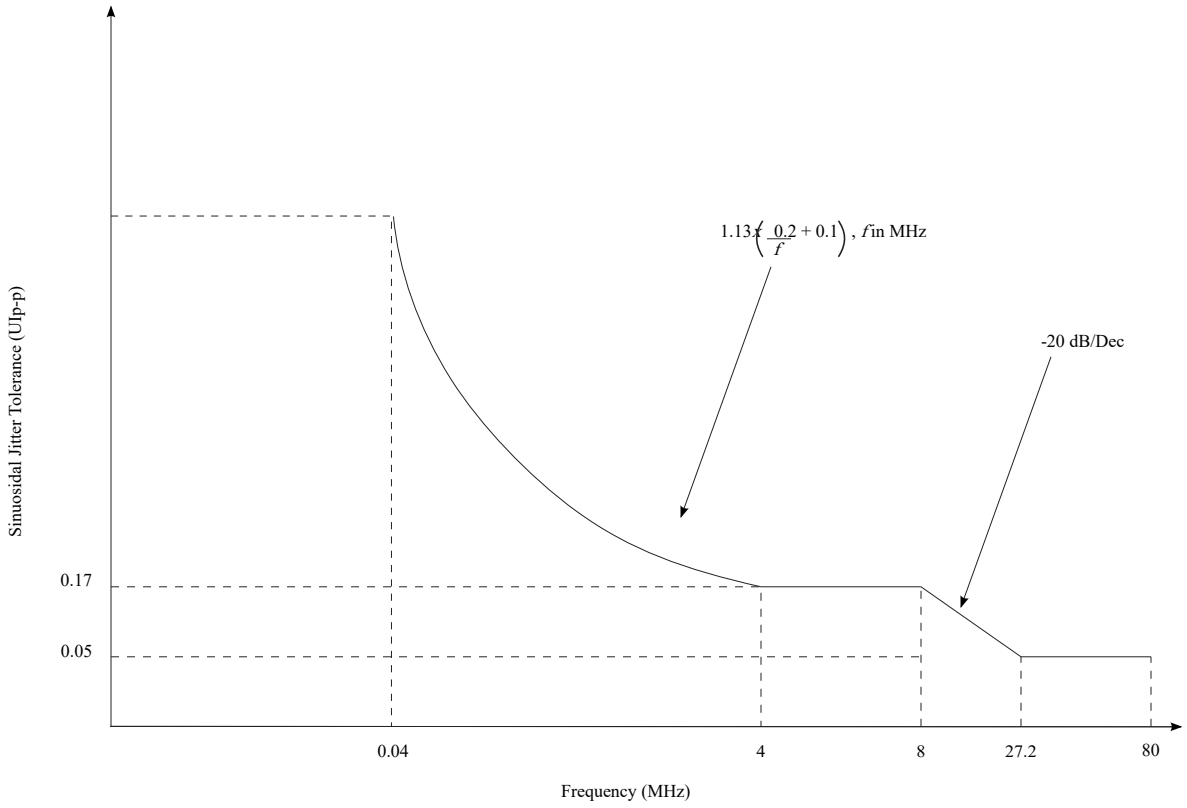


Figure 54. XFI host receiver input sinusoidal jitter tolerance

3.23.8 SFI

3.23.8.1 SFI DC electrical characteristics

This table defines the SFI+ transmitter DC electrical characteristics.

Table 98. SFI+ host transmitter DC electrical characteristics (SD_OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output differential voltage	$V_{TX-DIFF}$	190	-	700	mV_{p-p}	2
De-emphasized differential output voltage (ratio at 1.14dB)	$V_{TX-DE-RATIO-1.14dB}$	0.6	1.1	1.6	dB	3
De-emphasized differential output voltage (ratio at 3.5dB)	$V_{TX-DE-RATIO-3.5dB}$	3	3.5	4	dB	4

Table continues on the next page...

Table 98. SFI+ host transmitter DC electrical characteristics (SD_OV_{DD} = 1.8V) [1] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
De-emphasized differential output voltage (ratio at 4.66dB)	$V_{TX-DE-RATIO-4.66dB}$	4.1	4.6	5.1	dB	5
De-emphasized differential output voltage (ratio at 6.0dB)	$V_{TX-DE-RATIO-6.0dB}$	5.5	6.0	6.5	dB	6
De-emphasized differential output voltage (ratio at 9.5dB)	$V_{TX-DE-RATIO-9.5dB}$	9	9.5	10	dB	7
Differential resistance	T_{RD}	80	100	120	Ω	-

1. For recommended operating conditions, see Recommended Operating Conditions.
2. LNmTECR0[EQ_AMP_RED]= 000111
3. LNmTECR0[EQ_POST1Q]= 00011
4. LNmTECR0[EQ_POST1Q]= 01000
5. LNmTECR0[EQ_POST1Q]= 01010
6. LNmTECR0[EQ_POST1Q]= 01100
7. LNmTECR0[EQ_POST1Q]= 10000

This table defines the SFI+ host receiver DC electrical characteristics.

Table 99. SFI+ host receiver DC electrical characteristics (SD_SV_{DD} = 0.9V) [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential resistance	R_{RD}	80		120	Ω	-
Input differential voltage	$V_{RX-DIFF}$	300	-	850	mV_{p-p}	-

1. For recommended operating conditions, see Recommended Operating Conditions.

3.23.8.2 SFI AC timing specifications

This table defines the SFI+ host transmitter AC timing specifications.

Table 100. SFI+ host transmitter AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit
Transmitter baud Rate	T_{BAUD}	10.3125-100ppm	10.3125	10.3125+100ppm	Gb/s
Unit Interval	UI	-	96.96	-	ps
Data dependent jitter	DDJ	-	-	0.1	UI p-p

Table continues on the next page...

Table 100. SFI+ host transmitter AC timing specifications (continued)

Parameter	Symbol	Min	Typ	Max	Unit
Data dependent pulse width shrinkage	DDPWS			0.055	UI p-p
Uncorrelated jitter	UJ			0.023	UI (RMS)
Total jitter tolerance	T_J	-	-	0.28	UI p-p

1. Duty cycle distortion (DCD) and Pulse Width Shrinkage (DDPWS) are components of DDJ. DDJ is the range (max-min) of the timing variations.

2. The AC specifications do not include Refclk jitter.

This table defines the SFI+ host receiver AC timing specifications.

Table 101. SFI+ host receiver AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval	UI	-	96.96	-	ps	-
Receiver baud rate	R_{BAUD}	10.3125-100ppm	10.3125	10.3125+100ppm	Gb/s	-
99% jitter	J2			0.42		1
Pulse width shrinkage jitter	DDPWS	-	-	0.3	UI p-p	2
Total jitter	T_J	-	-	0.7	UI p-p	

1. The 99% jitter is per SFF-8431 Rev4.1 and includes sinusoidal jitter, per Figure 55.

2. In practice the test implementer may trade DDPWS with other pulse width shrinkage from the sinusoidal interferer per SFF-8431 Rev4.1.

3. The SFI total channel Link Budget when measured with Host Compliance board is 9.0 dB @5.5GHz. The channel loss including connector measured with Host Compliance board @ 5.5GHz is 6.5dB. The penalty for reflections and other impairments is 2.5dB. Manual tuning of TX Equalization and amplitude will be required for performance optimization.

4. The AC specifications do not include Refclk jitter.

This figure shows the sinusoidal jitter tolerance of SFI receiver.

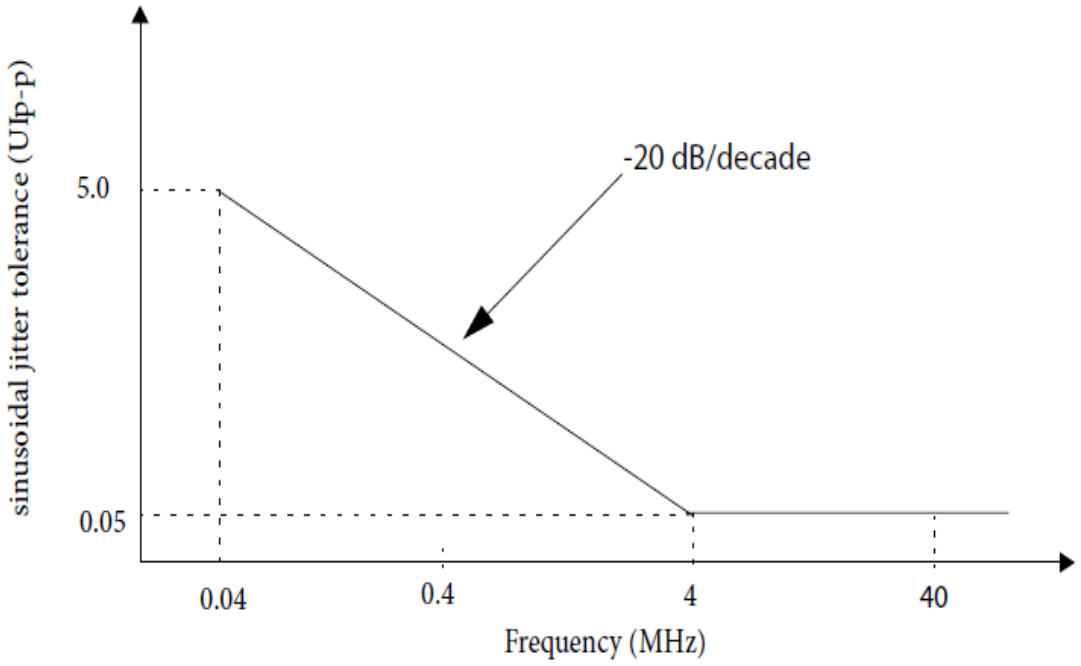


Figure 55. SFI+ SR and LR host receiver input datacom sinusoidal jitter tolerance

3.23.9 SFP+ direct attach copper

SFP+ Direct Attach Copper is supported for passive copper cable compliant per SFF-8472.

3.23.9.1 SFP+ direct attach copper DC electrical characteristics

The SFP+ host supporting direct attach cables must meet transmitter output DC specifications in Table 98 at reference point B per SFF-8472. In addition, the SFP+ host transmitter must meet the specifications in the table below.

This table defines the SFP+ host transmitter ouput DC specifications.

Table 102. SFP+ host transmitter output DC electrical characteristics at B for Cu (SD_OV_{DD} = 1.8V) [1]

Parameters - B	Symbol	Min	Typ	Max	Unit
Voltage modulation amplitude (p-p)	VMA	300			mV
Transmitter Qsq	Qsq	63.1			
Output AC common mode voltage				12.0	mV (RMS)
Host output TWDPc	TWDPc			10.7	dBe

1. For recommended operating conditions, see Recommended Operating Conditions.

2. Qsq = 1/RN if the one level and zero level noises are identical. RN is relative noise per SFF-8472.

3. Host electrical output measured with LRM 14 taps FFE and 5 taps DFE Equalizer with PRBS9 for copper direct attach stressor.

4. The TWDPc is the host transmitter penalty for copper cable stressor.

The SFP+ host supporting direct attach cables must meet the receiver output DC specifications in Table 99.

3.23.9.2 SFP+ direct attach AC timing specifications

The SFP+ host supporting direct attach cables must meet the transmitter output AC specifications in Table 100 at reference point B per SFF-8472.

The SFP+ host supporting direct attach cables must meet the AC specifications in Table 101 in at reference point B per SFF-8472. In addition, the SFP+ host receiver must meet required 1×10^{-12} BER when tested with the stressed signal described per SFF-847.

3.23.10 1000Base-KX

3.23.10.1 1000Base-KX DC electrical characteristics

This table describes the 1000Base-KX SerDes transmitter DC specification at TP1 per IEEE Std 802.3-2015. Transmitter DC characteristics are measured at the transmitter outputs (SDn_TXn_P and SDn_TXn_N).

Table 103. 1000Base-KX transmitter DC electrical characteristics (SD_OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output differential voltage	$V_{TX-DIFFp-p}$	800.0	-	1600.0	mV	2
Differential resistance	T_{RD}	80.0	100.0	120.0	Ω	-
1. For recommended operating conditions, see Recommended Operating Conditions. 2. SRDSxLNmTECR0[AMP_RED]=00_0000						

This tableprovides the 1000Base-KX receiver DC timing specifications.

Table 104. 1000Base-KX receiver DC electrical characteristics (SD_SV_{DD} = 0.9V) [1]

Parameter	Symbol	Min	Max	Unit
Input differential voltage	$V_{RX-DIFFp-p}$	-	1600.0	mV
Differential resistance	T_{RDIN}	80.0	120.0	Ω
1. For recommended operating conditions, see Recommended Operating Conditions.				

3.23.10.2 1000Base-KX AC timing specifications

This table defines the 1000Base-KX transmitter AC timing specifications.

Table 105. 1000Base-KX transmitter AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Baud rate	T_{BAUD}	1.25-100ppm	1.25	1.25+100ppm	Gb/s	-
Uncorrelated high probability jitter/ Random Jitter	T_{UHPJ} / T_{RJ}	-	-	0.15	UI p-p	-
Deterministic jitter tolerance	T_{DJ}	-	-	0.1	UI p-p	-
Total jitter tolerance	T_{TJ}	-	-	0.25	UI p-p	1

Table continues on the next page...

Table 105. 1000Base-KX transmitter AC timing specifications (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
1. Total jitter is specified at a BER of 10^{-12}.						

This table defines the 1000Base-KX receiver AC timing specifications.

Table 106. 1000Base-KX receiver AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Baud rate	R_{BAUD}	1.25-100ppm	1.25	1.25+100ppm	Gb/s	-
Total jitter tolerance	R_{TJ}	-	-	Per IEEE 802.3ap-clause 70.	UI p-p	1
Random jitter	R_{RJ}	-	-	0.15	UI p-p	2
Sinusoidal jitter (maximum)	R_{SJ-max}	-	-	0.1	UI p-p	1
1. The receiver interference tolerance level of this parameter shall be measured as described in Annex 69A of the IEEE Std 802.3ap-2007. 2. Random jitter is specified at a BER of 10^{-12}.						

3.23.11 10GBase-KR

3.23.11.1 10GBase-KR clocking requirements for SD*n*_REF_CLK*n* and SD*n*_REF_CLK*n*_B

Only SerDes 1 and SerDes 2 may be used for SerDes 10GBase-KR configurations based on the RCW Configuration field SRDS_PRTCL.

For more information on these specifications, see SerDes reference clocks .

3.23.11.2 10GBase-KR DC electrical characteristics

This table defines the 10GBase-KR transmitter DC electrical characteristics.

Table 107. 10GBase-KR transmitter DC electrical characteristics (SD_OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output differential voltage	$V_{TX-DIFF}$	800.0	-	1200.0	mV	2
De-emphasized differential output voltage (ratio at 1.14dB)	$V_{TX-DE-RATIO-1.14dB}$	0.6	1.1	1.6	dB	3
De-emphasized differential output voltage (ratio at 3.5dB)	$V_{TX-DE-RATIO-3.5dB}$	3.0	3.5	4.0	dB	4

Table continues on the next page...

Table 107. 10GBase-KR transmitter DC electrical characteristics (SD_OV $_{DD}$ = 1.8V) [1] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
De-emphasized differential output voltage (ratio at 4.66dB)	$V_{TX-DE-RATIO-4.66dB}$	4.1	4.6	5.1	dB	5
De-emphasized differential output voltage (ratio at 6.0dB)	$V_{TX-DE-RATIO-6.0dB}$	5.5	6.0	6.5	dB	6
De-emphasized differential output voltage (ratio at 9.5dB)	$V_{TX-DE-RATIO-9.5dB}$	9.0	9.5	10.0	dB	7
Differential resistance	T_{RD}	80.0	100.0	120.0	Ω	-

1. For recommended operating conditions, see Recommended Operating Conditions.
2. LNmTECR0[EQ_AMP_RED]= 000000
3. LNmTECR0[EQ_POST1Q]= 00011
4. LNmTECR0[EQ_POST1Q]= 01000
5. LNmTECR0[EQ_POST1Q]= 01010
6. LNmTECR0[EQ_POST1Q]= 01100
7. LNmTECR0[EQ_POST1Q]= 10000

This table defines the 10GBase-KR receiver DC electrical characteristics.

Table 108. 10GBase-KR receiver DC electrical characteristics (SD_SV $_{DD}$ = 0.9V) [1]

Parameter	Symbol	Min	Max	Unit
Input differential voltage	$V_{RX-DIFF}$	-	1200.0	mV
Differential resistance	R_{RD}	80.0	120.0	Ω

1. For recommended operating conditions, see Recommended Operating Conditions.

3.23.11.3 10GBase-KR AC timing specifications

This table defines the 10GBase-KR transmitter AC timing specifications. RefClk jitter is not included.

Table 109. 10GBase-KR transmitter AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit
Transmitter baud rate	T_{BAUD}	10.3125 - 100 ppm	10.3125	10.3125 + 100 ppm	GBd
Deterministic jitter	T_DJ	-	-	0.15	UI p-p
Total jitter	T_TJ	-	-	0.3	UI p-p

This table defines the 10GBase-KR receiver AC timing specifications. RefClk jitter is not included.

Table 110. 10GBase-KR receiver AC timing specifications [3]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Receiver baud rate	R_{BAUD}	10.3125 - 100 ppm	10.3125	10.3125 + 100 ppm	GBd	-
Total jitter	T_J	-	-	1.0	UI p-p	1, 2
Random jitter	R_J	-	-	0.13	UI p-p	1
Sinusoidal jitter, maximum	S_{J-max}	-	-	0.115	UI p-p	1
Duty cycle distortion	D_{CD}	-	-	0.035	UI p-p	1

1. The AC specifications do not include Refclk jitter.
2. The total applied Jitter Tj = ISI + Rj + DCD + Sj-max, where ISI is jitter due to frequency dependent loss.
3. TX equalization and amplitude tuning is through software for performance optimization, as in NXP provided SDKs.

3.23.12 25GAUI and 50GAUI-2

The IEEE Std 802.3-2015 100 Gb/s Attachment Unit Interface (CAUI-4) is intended for use as a chip-to-chip or a chip-to-module interface. The LX2162A supports 25GAUI (single lane @ 25.78125 GBaud) and 50GAUI-2 (2 lanes, each running @ 25.78125 GBaud).

3.23.12.1 25GAUI/50GAUI-2 DC electrical characteristics

This table defines the 25GAUI/50GAUI-2 transmitter DC electrical characteristics.

Table 111. 25GAUI/50GAUI-2 transmitter DC electrical characteristics (SD_OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Typ	Max	Unit
Differential peak-to-peak output voltage	$V_{TX-DIFF}$			1200.0	mV
Differential peak-to-peak output voltage transmitter disabled	$V_{TX-DIS-DIFF}$	0.0	-	30.0	mV
DC common mode voltage	V_{CM}	0.0	-	1.9	V
Output waveform steady state voltage	V_f	0.4	-	0.6	V
Output waveforem linear fit pulse peak	$V_{P(k)}$	0.71 * V_f	-	-	V
Differential resistance	$Z_{TX-DIFF-DC}$	80.0	100.0	120.0	Ω

1. For recommended operating conditions, see Recommended Operating Conditions.

This table defines the 25GAUI/50GAUI-2 receiver DC electrical characteristics.

Table 112. 25GAUI/50GAUI-2 receiver DC electrical characteristics (SD_SV $_{DD}$ = 0.9V) [1]

Parameter	Symbol	Min	Max	Unit
Differential resistance	$Z_{RX-DIFF-DC}$	80.0	120.0	Ω
1. For recommended operating conditions, see Recommended Operating Conditions.				

3.23.12.2 25GAUI/50GAUI-2 AC timing characteristics

This table defines the 25GAUI/50GAUI-2 transmitter AC timing specifications.

Table 113. 25GAUI/50GAUI-2 transmitter AC timing specifications [1, 2]

Parameter	Symbol	Min	Typ	Max	Unit
Transmitter baud Rate	T_{BAUD}	25.78125-100ppm	25.78125	25.78125+100ppm	Gb/s
AC common mode output voltage RMS	V_{CM}	-	-	0.012	V
Bounded uncorrelated jitter	T_{BUJ}			0.1	UI p-p
Even-odd jitter	T_{EOJ}	-	-	0.035	UI
Total uncorrelated jitter	$T_{TU\ J}$	-	-	0.26	UI p-p
Signal-to-noise-and-distortion ratio	SINAD	27.0	-	-	dB
1. See Figure 56.					
2. See Figure 57.					

This figure shows the applied sinusoidal jitter tolerance of the 25GAUI/50GAUI-2 receiver.

Frequency range	Sinusoidal jitter, peak-to-peak (UI)
$f < 100$ kHz	Not specified
100 kHz $< f \leq 10$ MHz	$5 \times 10^5 / f$
10 MHz $< f <$ 10 LB[a]	0.05

Figure 56. 25GAUI/50GAUI-2 receiver applied sinusoidal jitter

This figure provides the ISI channel loss profile.

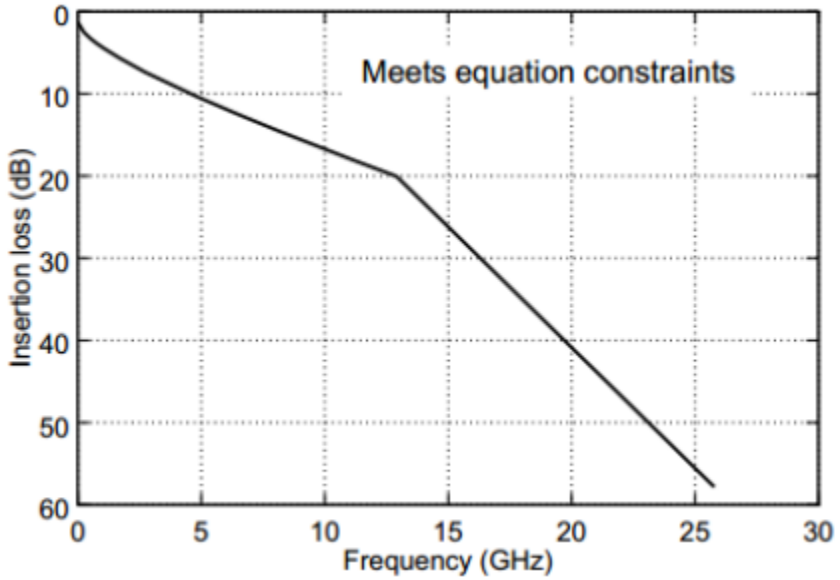


Figure 57. 25GAUI/50GAUI-2 chip-to-chip channel insertion

3.23.13 USXGMII interface (USXGMII)

3.23.13.1 USXGMII DC electrical characteristics

This table defines the 10G-SXGMII transmitter DC electrical characteristics.

Table 114. 10G-SXGMII transmitter DC electrical characteristics (SD_OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Typ	Max	Unit
Output differential voltage	$V_{TX-DIFF}$	800.0	-	1200.0	mV
De-emphasized differential output voltage (ratio at 1.14dB)	$V_{TX-DE-RATIO-1.14dB}$	0.6	1.1	1.6	dB
De-emphasized differential output voltage (ratio at 3.5dB)	$V_{TX-DE-RATIO-3.5dB}$	3.0	3.5	4.0	dB
De-emphasized differential output voltage (ratio at 4.66dB)	$V_{TX-DE-RATIO-4.66dB}$	4.1	4.6	5.1	dB
De-emphasized differential output voltage (ratio at 6.0dB)	$V_{TX-DE-RATIO-6.0dB}$	5.5	6.0	6.5	dB
De-emphasized differential output voltage (ratio at 9.5dB)	$V_{TX-DE-RATIO-9.5dB}$	9.0	9.5	10.0	dB
Differential resistance	T_{RD}	80.0	100.0	120.0	Ω

1. For recommended operating conditions, see Recommended Operating Conditions.

This table defines the 10G-SXGMIIreceiver DC electrical characteristics.

Table 115. 10G-SXGMII receiver DC electrical characteristics (SD_SV $_{DD}$ = 0.9V) [1]

Parameter	Symbol	Min	Max	Unit
Input differential voltage	$V_{RX-DIFF}$	-	1200.0	mV
Differential resistance	R_{RD}	80.0	120.0	Ω
1. For recommended operating conditions, see Recommended Operating Conditions.				

3.23.13.2 USXGMII AC timing characteristics

This table defines the 10G-SXGMIItransmitter AC timing specifications. RefClk jitter is not included.

Table 116. 10G-SXGMII transmitter AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit
Transmitter baud rate	T_{BAUD}	10.3125 - 100 ppm	10.3125	10.3125 + 100 ppm	GBd
Uncorrelated high probability jitter/ Random Jitter	T_{UHPJ}/T_{RJ}	-	-	0.15	UI p-p
Deterministic jitter	D_J	-	-	0.15	UI p-p
Total jitter	T_J	-	-	0.3	UI p-p

This table defines the 10G-SXGMIIreceiver AC timing specifications. RefClk jitter is not included.

Table 117. 10G-SXGMII receiver AC timing specifications [3]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Receiver baud rate	R_{BAUD}	10.3125 - 100 ppm	10.3125	10.3125 + 100 ppm	GBd	-
Total jitter	T_J	-	-	1.0	UI p-p	1, 2
Random jitter	R_J	-	-	0.13	UI p-p	1
Sinusoidal jitter, maximum	S_{J-max}	-	-	0.115	UI p-p	1
Duty cycle distortion	D_{CD}	-	-	0.035	UI p-p	1

1. The AC specifications do not include Refclk jitter.
2. The total applied Jitter Tj = ISI + Rj + DCD + Sj-max, where ISI is jitter due to frequency dependent loss.
3. TX equalization and amplitude tuning is through software for performance optimization, as in NXP provided SDKs.

3.23.14 XLAUI interface (XLAUI)

The XLAUI standard achieves 40 Gbps with four 10.3125 Gbps lanes.

3.23.14.1 XLAUI DC electrical characteristics

This table defines the XLAUI transmitter DC electrical characteristics. The parameters are specified at the transmitter compliance point per IEEE Std 802.3-2015.

Table 118. XLAUI transmitter DC electrical characteristics (SD_OV $_{DD}$ = 1.8V) [1]

Parameter	Symbol	Min	Typ	Max	Unit
Differential peak-to-peak output voltage	$V_{TX-DIFF}$			760.0	mV p-p
De-emphasis		4.4	-	7.0	dB
Differential resistance	$Z_{TX-DIFF-DC}$	80.0	100.0	120.0	Ω
1. For recommended operating conditions, see Recommended Operating Conditions.					

This table defines the XLAUI receiver DC electrical characteristics. The parameters are specified per IEEE 802.3-2015.

Table 119. XLAUI receiver DC electrical characteristics (SD_SV $_{DD}$ = 0.9V) [1]

Parameter	Symbol	Min	Typ	Max	Unit
Differential input voltage	V_{IN}	85.0		850.0	mV p-p
Differential receive input impedance	V_{IN}	80.0	100.0	120.0	Ohm
1. For recommended operating conditions, see Recommended Operating Conditions.					

3.23.14.2 XLAUI AC timing characteristics

This table defines the XLAUItransmitter AC timing specifications.The parameters are specified per IEEE 802.3-2015. The AC timing specifications do not include RefClk jitter.

Table 120. XLAUI transmitter AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit
Deterministic jitter eye mask (far end)	J_D			0.17	UI p-p
Total jitter eye mask (far end)	J_T	-	-	0.32	UI p-p
Transmitter baud rate	T_{BAUD}	10.3125-100ppm	10.3125	10.3125+100ppm	Gb/s

This table defines the XLAUIreceiver AC timing specifications.The parameters are specified per IEEE 802.3-2015. The AC timing specifications do not include RefClk jitter.

Table 121. XLAUI receiver AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit
Input AC common-mode voltage tolerance		20.0	-	-	RMS

Table continues on the next page...

Table 121. XLAUI receiver AC timing specifications (continued)

Parameter	Symbol	Min	Typ	Max	Unit
Deterministic jitter tolerance	J_D	0.42			UI p-p
Total jitter tolerance	J_T	0.62	-		UI p-p
Bit error ratio	BER	-	10^{-12}	-	-
Receiver baud rate	R_{BAUD}	10.3125-100ppm	10.3125	10.3125+100ppm	Gb/s

3.23.15 SerDes Recovered Clock Outputs

The RCLK[0:1] pins provide the recovered clocks from SerDes lanes running Ethernet protocols (SGMII 1G, XFI, USXGMII, 50GAUI-2, 25GAUI, and XLAUI) on SerDes 1 and SerDes 2.

3.23.15.1 SerDes 1 and 2 receive recovered clocks DC electrical characteristics

This table provides the DC electrical characteristics for the recovered clock output.

Table 122. RCLK DC electrical characteristics (OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Max	Unit	Notes
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	2
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	2

1. For recommended operating conditions, see Recommended Operating Conditions.

2. The symbol OV_{DD} represents the recommended operating voltage of the supply referenced in Recommended Operating Conditions.

3.23.15.2 SerDes 1 and 2 receive recovered clocks AC timing characteristics

This table provides the AC electrical characteristics of the recovered clock output.

Table 123. RCLK AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
RCLK frequency	f_{RCLK}	0.0	-	161.1328125	MHz	-
RCLK pulse width	t_{RCLKPW}	40.0	50.0	60.0	%	-
LP filter < 1 MHz RCLK peak-to-peak jitter	TJ_{pk-pk}	-	-	30	ps	1
	DJ_{pk-pk}	-	-	10	ps	

1. Values listed for RCLK peak-to-peak jitter represent the jitter generation limits without any input data jitter or input PLL reference clock jitter. It is recommended that system designers use RCLK with an external jitter cleaning PLL when intending to use RCLK as a reference clock for the system. Jitter calculations for such a system should include the quoted RCLK

Table continues on the next page...

Table 123. RCLK AC timing specifications (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
peak-to-peak jitter, the system's SerDes PLL reference clock jitter, and the system's receiver input data jitter. Determination of both the SerDes PLL reference clock peak-to-peak jitter and the receiver peak-to-peak input data jitter should include the use of a low pass filter with a bandwidth of 1 MHz with a roll off of at least 20 dB per decade.						

4 Hardware design considerations

4.1 Clock ranges

This table provides the clocking specifications for the processor core, coherency domain, platform, memory, and DCE.

Table 124. Processor, platform, and memory clocking specifications

Characteristic	Maximum processor core frequency		Unit	Notes
	2000 MHz			
	Min	Max		
Core cluster group PLL frequency	700	2000	MHz	
Core frequency	175	2000	MHz	1
Coherency Domain frequency	1000	1300	MHz	
Platform clock frequency	500	650	MHz	1
Memory bus clock	650	1450	MHz	1, 2
Decompression/compression acceleration engine (DCE) frequency	300	400	MHz	

Notes:

1. **Caution:** The coherency domain clock to SYSCLK ratio and core to SYSCLK ratio settings must be chosen such that the resulting SYSCLK frequency, core frequency, coherency domain and platform clock frequency do not exceed their respective maximum or minimum operating frequencies.

2. The memory bus clock speed is half the DDR4 data rate.

4.2 Platform clock requirements for Ethernet

This table shows the minimum platform clock frequency required to run Ethernet at different speeds.

Table 125. Platform clocking restrictions

Ethernet Speed	Platform clock requirement
10G	516 MHz
25G	645 MHz
40G	261 MHz
50G	350 MHz

4.3 Platform clock requirement for PCIe

PCIe3 is capable of x8/x4/x2/1 and SR-IOV. PCIe1 and PCIe4 are capable of x4/x2/x1 and do not support SR-IOV.

This table shows the PCIe speed/width capability based on the platform clock. There is no speed/width limitation when the platform clock runs at 533 MHz or higher. If the platform clock is less than 533 MHz, PCIe3 will have limited speed or width.

Table 126. Platform clock requirement for the PCIe controllers

PCIe controllers	Platform clock requirement	Max speed, width
PCIe3	533 MHz and higher	No limitation - Gen 3 rate at x8 width
	Less than 533 MHz	Gen 1/Gen 2 rate at x8 width or Gen 3 at x4 width
PCIe1, PCIe4	533 MHz and higher	No limitation - Gen 3 rate at x4 width
	Less than 533 MHz	

4.4 Power supply design

For additional details on the power supply design, see the applicable chip design checklist.

4.4.1 Voltage ID (VID) controllable supply

To guarantee performance and power specifications, a specific method of selecting the optimum voltage-level must be implemented when the chip is used. As part of the chip's boot process, software must read the VID efuse values stored in the Fuse Status register (FUSESR) and then configure the external voltage regulator based on this information. This method requires a point of load voltage regulator for each chip.

NOTE

During the power-on reset process, the fuse values are read and stored in the FUSESR. It is expected that the chip's boot code reads the FUSESR value very early in the boot sequence and updates the regulator accordingly.

The default voltage regulator setting that is safe for the system to boot is the recommended operating V_{DD} at boot of 0.850 V. It is highly recommended to select a regulator with a Vout range of at least 0.7 V to 0.9 V, with a resolution of 12.5 mV or better, when implementing a VID solution.

The table below lists the valid VID efuse values that will be programmed at the factory for this chip.

Table 127. Fuse Status Register (DCFG_CCSR_FUSESR)

Binary value of DA_V / DA_ALT_V	V_{DD} voltage
00000	default (0.850 V)
00010	0.775 V
10000	0.800 V
10010	0.825 V
10100	0.850 V
All other values	Reserved

For additional information on VID, see the chip reference manual.

5 Thermal

This table shows the thermal rating for the chip.

Table 128. Package thermal characteristics

Rating	Symbol	Value	Unit	Notes
Junction to case thermal resistance	$R_{\Theta JC}$	0.45	°C/W	1

Notes:

1. Junction-to-Case thermal resistance is determined using an isothermal cold plate heat extraction through the top side of the package. Case temperature is the surface temperature at the package lid's geometric centre.

5.1 Recommended thermal model

Information about Flotherm models of the package or thermal data not available in this document can be obtained from your local NXP sales office.

5.2 Temperature diode

The chip has temperature diodes that can be used to monitor its temperature by using an external temperature monitoring device (such as NXP SA56004x).

The following are the specifications of the chip's on-board temperature diodes:

Operating range: 14 - 240 µA

The ideality factor over temperature range 85Cº to 105Cº, n = 1.022 ± 0.003, with approximate error +/- 1.5 Cº and approximate error under +/- 3 Cº for temperature range 0 Cº to 85Cº and 105 Cº to 125Cº.

5.3 Thermal management information

This section provides thermal management information for the flip-chip, plastic-ball, grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design-the heat sink, airflow, and thermal interface material.

The recommended attachment method to the heat sink is illustrated in Figure 58. The heat sink should be attached to the printed-circuit board with the spring force centered over the lid. This spring force should not exceed 47 pounds force (209 Newton).

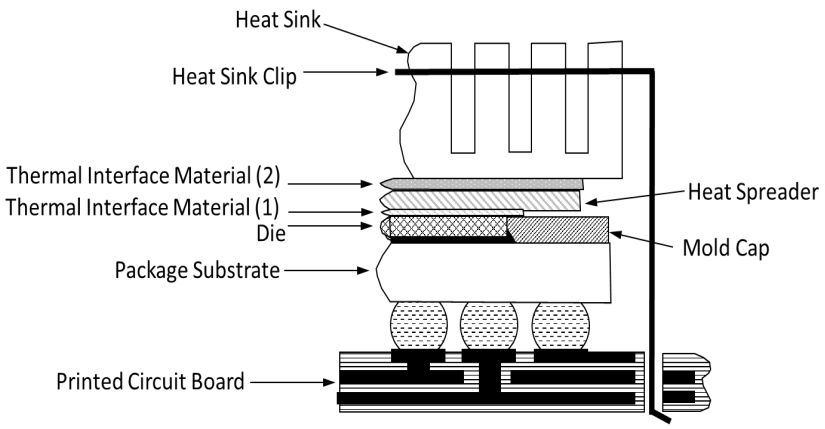


Figure 58. Package exploded, cross-sectional view-FC-PBGA (w/ Lid)

The system board designer can choose between several types of heat sinks to place on the device. There are several commercially-available thermal interfaces to choose from in the industry. Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

5.3.1 Thermal interface materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. The performance of thermal interface materials improves with increasing contact pressure; this performance characteristic chart is generally provided by the thermal interface vendor. The recommended method of mounting heat sinks on the package is by means of a spring clip attachment to the printed-circuit board (see Figure 58).

The system board designer can choose among several types of commercially available thermal interface materials.

6 Package information

6.1 Package parameters for the FC-PBGA

The package parameters are as provided in the following list.

- Package: 1150 I/O, 23 x 23 x 2.07 mm, lidded FC-PBGA
- BGA pitch: 0.65 mm checkerboard grid
- Case outline number: 98ASA01554D

6.2 Mechanical dimensions of the FC-PBGA

These figures show the mechanical dimensions and bottom surface nomenclature of the chip.

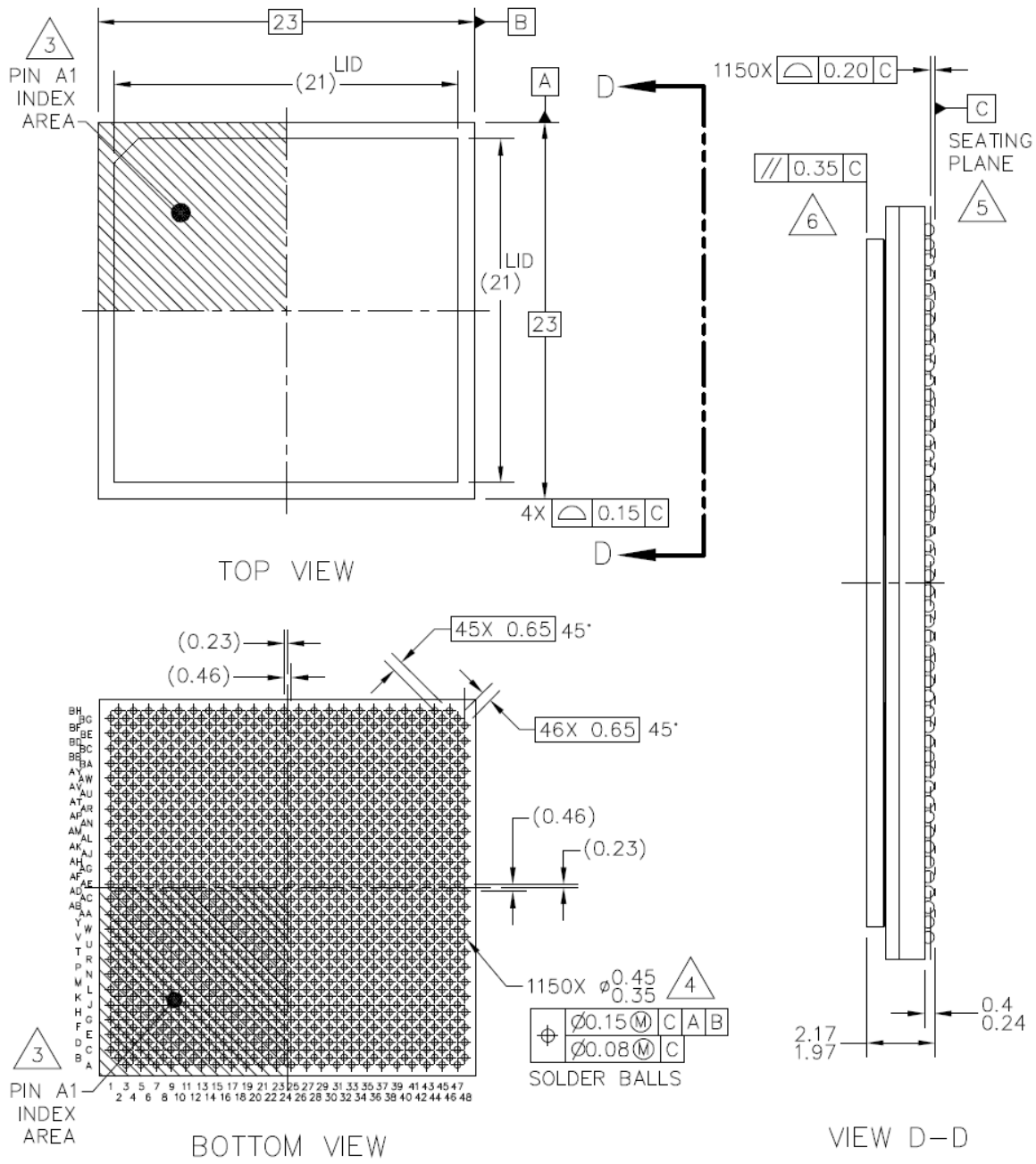
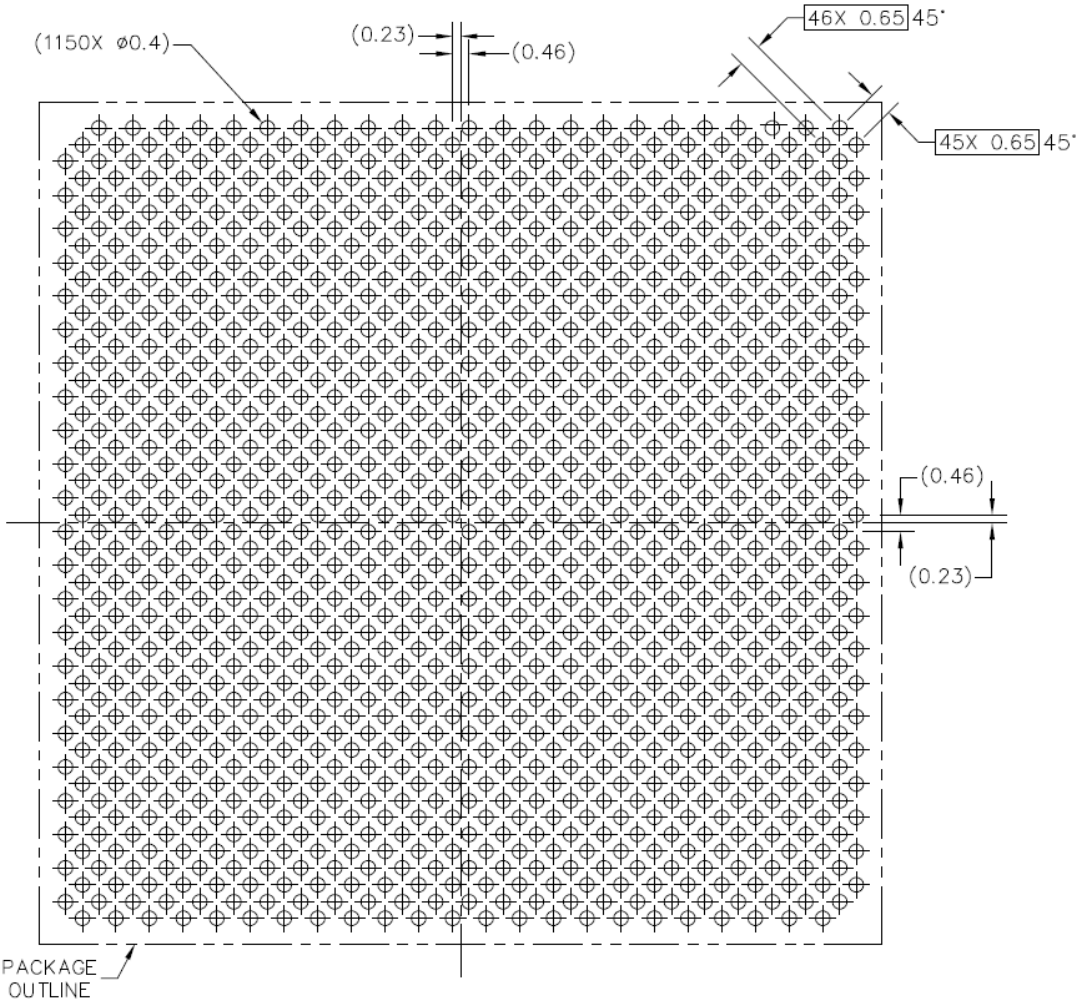


Figure 59. Mechanical dimensions of the FC-PBGA (1 of 4)

H–FC–PBGA–1150 I/O
23 X 23 X 2.07 PKG, 0.65 PITCH

SOT2055–1



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DATE: 28 OCT 2020

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01554D	REVISION: X4	PAGE: 2

Figure 60. Mechanical dimensions of the FC-PBGA (2 of 4)

H–FC–PBGA–1150 I/O
23 X 23 X 2.07 PKG, 0.65 PITCH

SOT2055–1

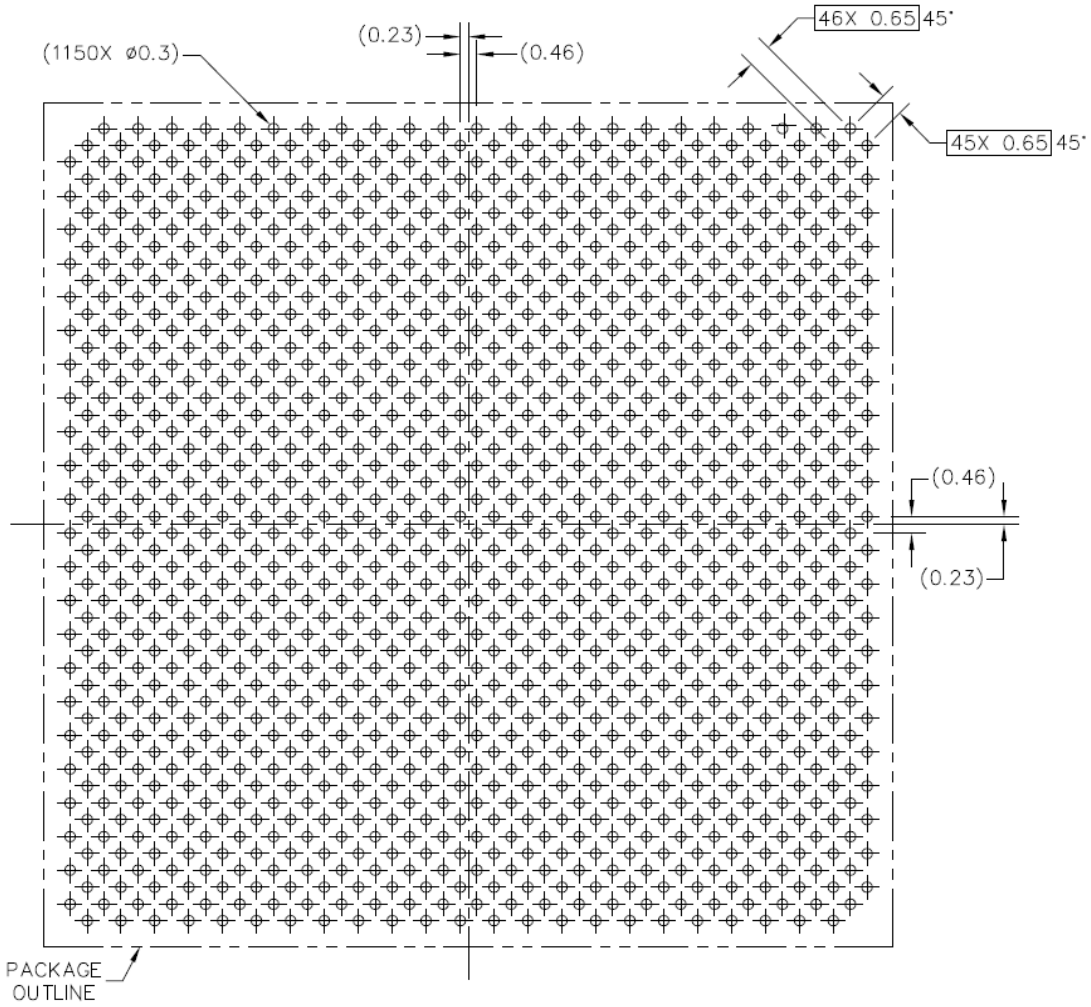

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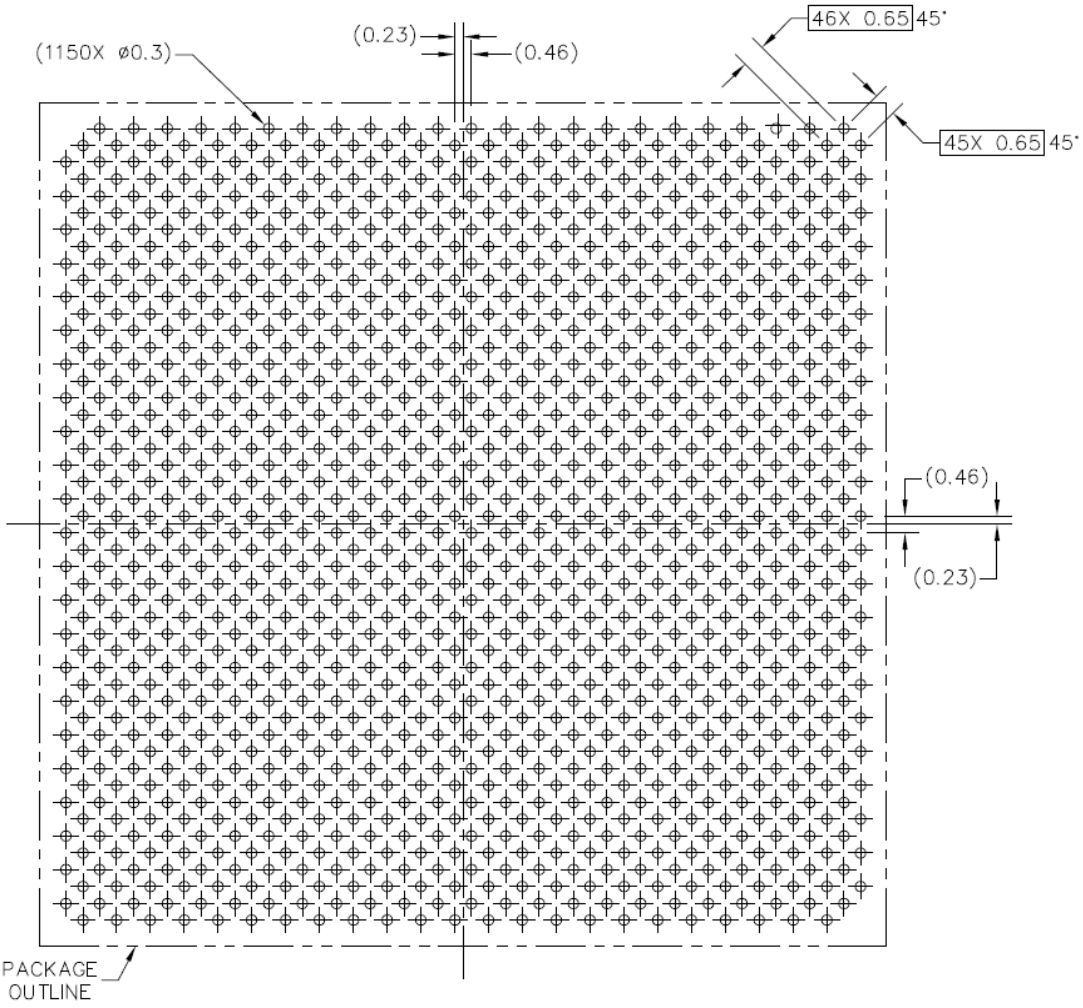
Figure 61. Mechanical dimensions of the FC-PBGA (3 of 4)

H–FC–PBGA–1150 I/O
23 X 23 X 2.07 PKG, 0.65 PITCH

SOT2055–1



RECOMMENDED STENCIL THICKNESS 0.1 MM

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DATE: 28 OCT 2020

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01554D	REVISION: X4	PAGE: 4

Figure 62. Mechanical dimensions of the FC-PBGA (4 of 4)

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
7. LID OVERHANG ON SUBSTRATE NOT ALLOWED.

7 Security fuse processor

This chip implements the QorIQ platform's trust architecture, supporting capabilities such as secure boot. Use of the trust architecture features is dependent on programming fuses in the Security Fuse Processor (SFP). The details of the trust architecture and SFP can be found in the chip reference manual.

To program SFP fuses, the user is required to supply 1.80 V to the TA_PROG_SFP pin per Power sequencing. TA_PROG_SFP should only be powered for the duration of the fuse programming cycle, with a per device limit of two fuse programming cycles. All other times TA_PROG_SFP should be connected to GND. The sequencing requirements for raising and lowering TA_PROG_SFP are shown in Figure 7. To ensure device reliability, fuse programming must be performed within the recommended fuse programming temperature range per Recommended Operating Conditions.

NOTE

Users not implementing the QorIQ platform's trust architecture features should connect TA_PROG_SFP to GND.

8 Ordering information

Contact your local NXP sales office or regional marketing team for order information.

8.1 Part numbering nomenclature

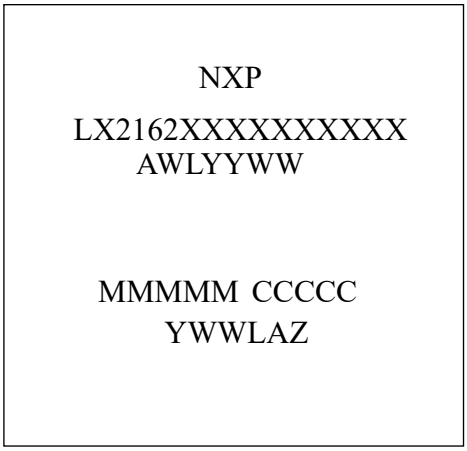
This table provides the NXP Layerscape platform part numbering nomenclature.

Table 129. Part numbering nomenclature

Process Generation	Tier	Number of Cores	Derivative	Temp Range	Enabled Options	Package Type	CPU Frequency, DDR Data Rate	Die Revision
LX = 16FFC production PLX = 16FFC prototype	2 = mid	08 = 8 12 = 12 16 = 16	2 = small package version	P = Prototype R = Indoor specification	C = SEC enabled, CAN-FD enabled E = SEC enabled, CAN 2.0b enabled (no CAN-FD support) N = SEC disabled, CAN 2.0b enabled (no CAN-FD support)	8 = 23x23mm FC PBGA pb-free C4/C5	2029 = 2000 MHz, 2900 MT/s	B = Rev 2.0

8.2 Part marking

Parts are marked as in the example shown in this figure.



FC-PBGA

Legend:
LX2162XXXXXXXXXX is the part marking on the die.
AWLYYWW is the test traceability code.
MMMMM is the mask number.
CCCCC is the country code.
YWWLAZ is the assembly traceability code.

Figure 63. Part marking for FC-PBGA chip

9 Revision history

This table summarizes revisions to this document.

Table 130. Revision history

Revision	Date	Description
1	08/2021	• Updated Figure 14 to show VIH/VIL instead of VOH/VOL and CMD/DATA input instead of CMD/DATA output. • Updated I2C AC timing specifications to add standard mode • Removed tDDKHCS and TDDKHCX from Figure 10 • In the Pinout list: — Added note 16 to D1_MRESET_B. — Updated notes 9 and 13 to add the resistor precision. • Updated note 4 in Table 90 to change XnVDD to SD_OVDD.
0	02/2021	Initial release

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Date of release: 08/2021

Document identifier: LX2162A