YAMAR
EVB Manual

DCB1M Evaluation Board Manual

1. Overview

The DCB1M evaluation board (EVB) allows easy testing of the DCB1M device in a system. Multiple DCB1M EVBs can communicate over a vehicle's DC powerline using one of the selected protocols: UART, SPI, DMX512, RDM and I²C.

Figure 1 presents the EVB. This manual describes how to use and interface with the EVB. The DCB1M data sheet is a reference to this document.

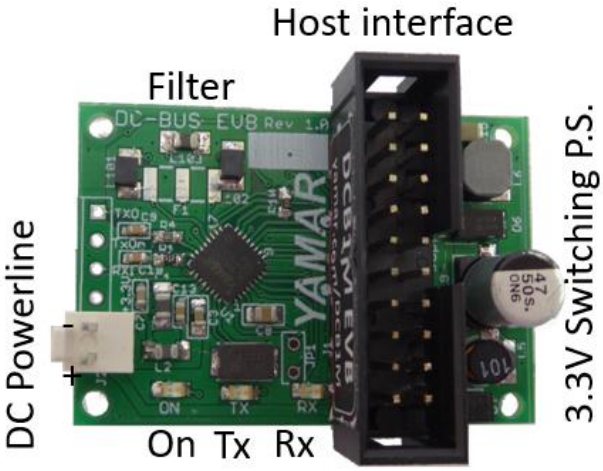

Figure 1 - DCB1M EVB

2. DCB1M EVB Description

2.1 Block Diagram Description

The EVB contains all the required hardware for the DCB1M device operation such as a line protection network, filter, 16MHz crystal, and a 3.3V switching power supply. The board is a physical layer of UART, SPI, DMX512, RDM, or I²C selected protocol over DC power lines at data rates of up to 1.4Mbit/s. The EVB connects directly to a host controller (ECU) through its TX and RX pins connected to HDI and HDO pins in the J1 Host connector. The EVB block diagram is depicted in Figure 2. When the HDC pin is low, the data from the ECU is used to configure the DCB1M registers for the desired communication frequency and other parameters as described in the DCB1M datasheet.

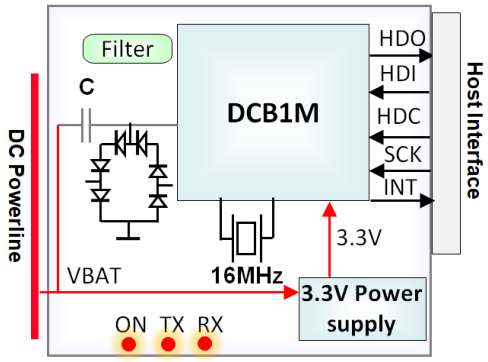

Figure 2 - DCB1M EVB Blocks

The received data signal from the DC powerline passes through a protection network into the DCB1M device. The DCB1M decodes the data and outputs it on the HDO pin of the Host interface connector.

On the transmitter side, data from the ECU is transferred to the DCB1M via HDI pin. The DCB1M process the data. If arbitration is enabled, powerline arbitration is performed based on configured arbitration ID, and then TX data is coded with error correction codes and framed. The frame is modulated at the selected carrier frequency to the TXO pin that drives the DC powerline via the protection network and a coupling capacitor.

The built-in switching power supply provides the 3.3V voltage required for the DCB1M operation. The power supply operates in a wide input voltage range between 10V and 36V. The EVB current consumption is in the range of 30mA depending on the supply input voltage (powerline voltage).

The DCB1M internal registers, as described in the DCB1M datasheet determine the EVB operation conditions such as carrier frequency. The Code level and host Interface type are determined either by resistors on the Code_SEL0, Code_SEL1 IF_SEL0, and IF_SEL1 resistors setting on the PCB (see Figure 4) or by setting J1 pins to VCC or GND. When HDC signal is Low, the data to/from the EVB is directed as a command, allowing WRITE-REG and READ-REG to/from the DCB1M internal registers.

2.2 Hardware features

- Noise robust DC powerline Communication
- UART, SPI, DMX, RDM, and I²C host interfaces
- Selectable powerline bitrate between 225Kbps to 1.4Mbit/s
- 251 selectable operating frequencies (5MHz to 30MHz, 100kHz spacing)
- 10V to 36V operation using a switching power supply
- Indication LEDs
- Small size EVB

2.3 EVB Connectors

2.3.1 J1 – Host Interface Connector

Table 1 – J1 Host interface connector

Pin Name	Direction	PU	Pin #	Pin Name	Direction	PU	Pin #
Reserved			1	Reserved			2
NRESET	I	PU	3	Reserved			4
INH	O		5	TXON	O		6
CODE_SEL0/EN_TX /INTERF/FREQ_SEL_0	IO		7	CODE_SEL1 /BUS_BUSY /FREQ_SEL_1	IO		8
IF_SEL0	I		9	IF_SEL1	I		10
INT/RTR/FREQ_SEL_2	IO		11	SCK /NLOOPBACK	I	PU	12
NSLEEP	I	PU	13	HDC	I	PU	14
HDO	O		15	HDI	I	PU	16
VCC (3.3V) output	P		17	GND	P		18
GND	P		19	VBAT (powerline) * Requires R6 = 0Ω	P		20

All input and output signals are compatible with 3.3V CMOS logic.

2.3.2 J2 – DC Power Line and test points

Table 2 J2 – DC Power Line and test points

Name	Pin #
TXO test-pin	1
TXON test-pin	2
RXI test-pin	3
3.3V output from the power supply	4
GND	5
VBAT DC powerline input	6

VBAT input connects the EVB to the DC powerline for communication and power supply.

Power supply requirements: 10V to 36V, minimum 150mA.

2.3.3 Display LEDs

- TX LED - Indicates transmission.
- RX LED - Data output, indicates reception.
- ON LED - Indicates 3.3V power on.

2.4 Mechanical Data

The mechanical dimension is depicted in Figure 3.

2.4.1 Top Layer

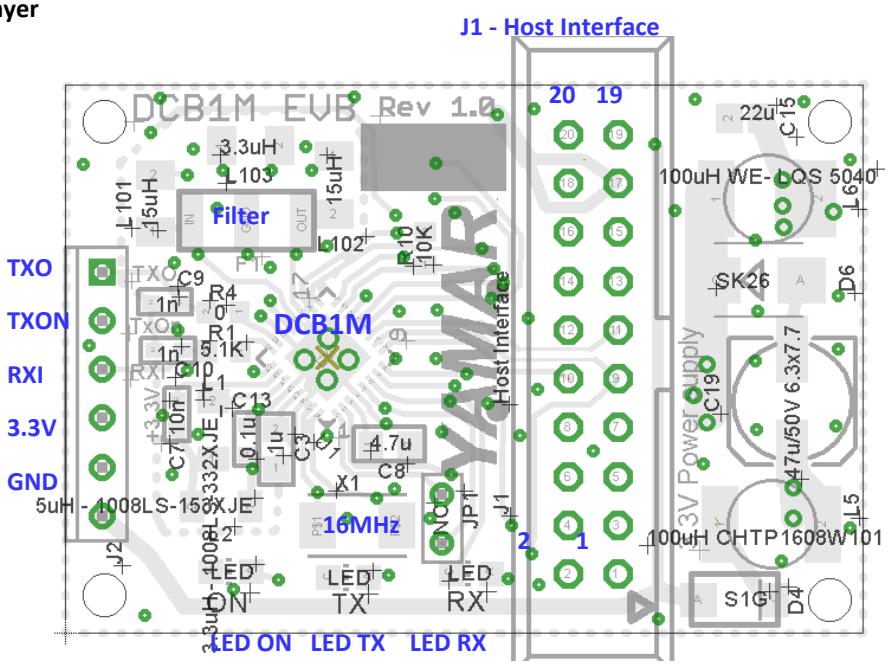

Figure 3 - EVB Top layer

2.4.2 Bottom Layer

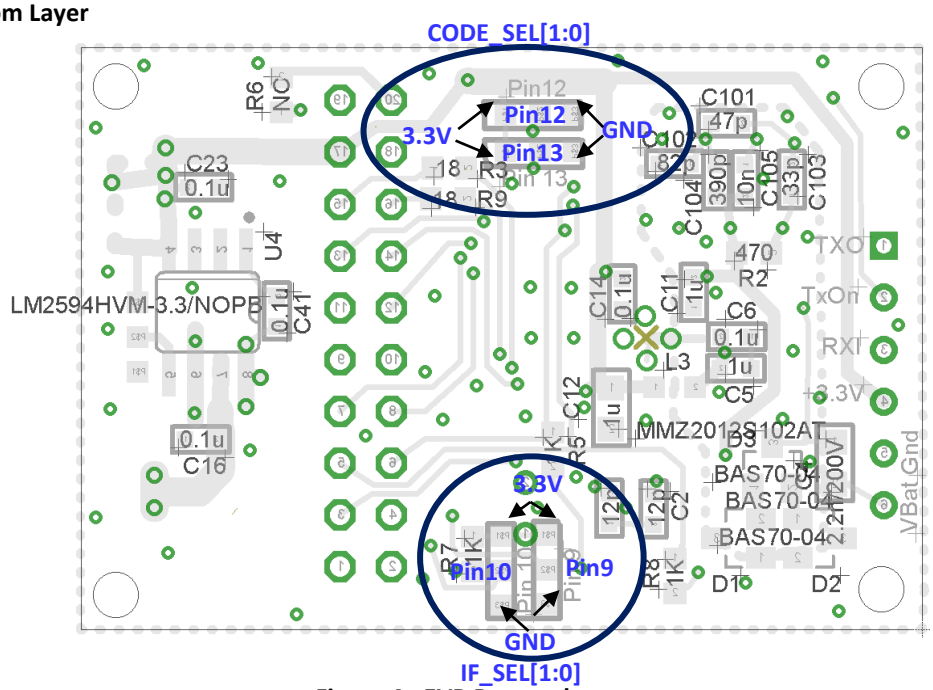

Figure 4 - EVB Bottom layer

3. EVB Operation

3.1 Configuration

DCB1M operation mode and its settings are configured at Power-up, Reset, and when ECU writes into its internal register (command mode, using the HDC pin). Refer to the DCB1M datasheet for further configuration information.

3.2 Interfacing to DCB1M EVB

The DCB1M EVB is designed to interface directly to UART, SPI, DMX512, RDM and I²C ECU.

The Host Interface connector J1 has all the signals required for the EVB proper operation. The PCB bottom has two 100K resistors connected to the DCB1M pin 9 and Pin 10 to determine the UART interface upon power-up when the corresponding pins on the connector are left open.

When using an external power supply instead/or in parallel to the EVB's power supply, it is recommended to add an inductor of at least 22uH in serial to the external power supply to avoid strong attenuation due to the power supply's internal filtering capacitors.

Figure 5 demonstrates an example of a UART interface using HDO, HDI, and HDC signals.

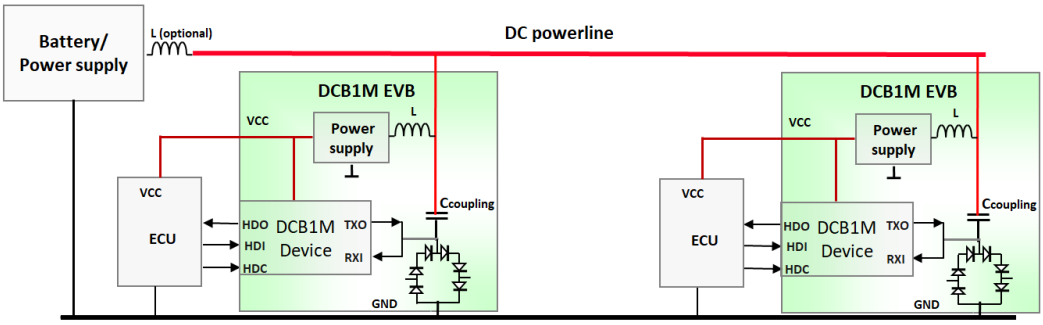

Figure 5 - The DCB1M EVB Interface with UART Host and DC Powerline.

Figure 6 demonstrates an example of an SPI interface using HDO, HDI, HDC, SCK, and INT signals.

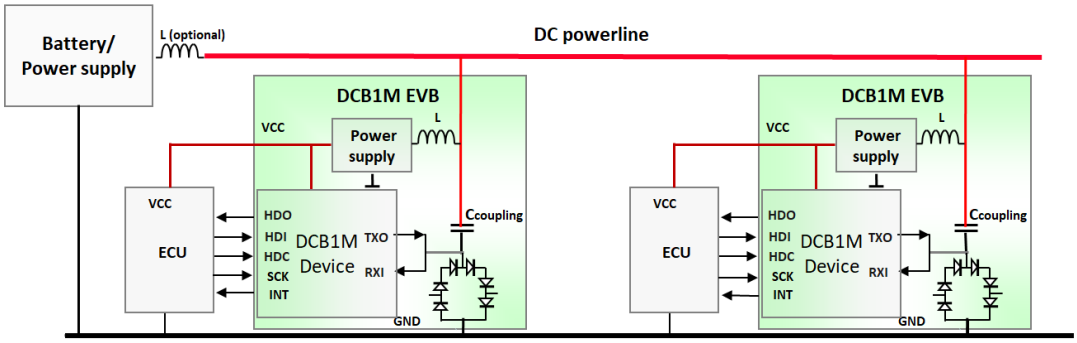

Figure 6 - The DCB1M EVB Interface with SPI Host and DC Powerline.

Figure 7 demonstrates an example of an I²C interface using HDO, SCK, and INT signals.

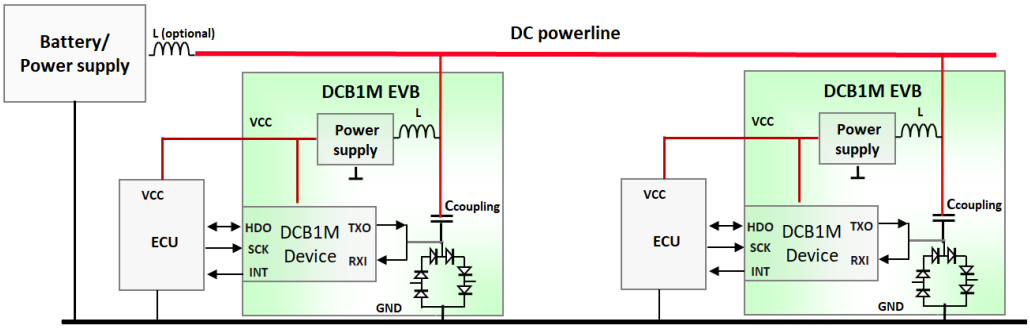

Figure 7 - The DCB1M EVB Interface with I²C Host and DC Powerline.

3.3 Interface DCB1M EVB directly with DMX/RDM controller

The DCB1M EVB interfaces directly to DMX512/RDM controller.

The Host Interface connector J1 has all the signals required for the EVB operation. The operating frequency is determined by 3 pins. The initial conditions of FREQ_SEL[0:1] are set upon power-up according to the corresponding J1 pins or by resistors on the PCB bottom layer. Two 100K resistors connected to the device pins 12 and 13. FREQ_SEL[2] pin is floated and has to be interfaced directly from the DMX512/RDM controller.

When using an external power supply in parallel to the EVB's power supply, it is recommended to add an inductor of at least 22uH in serial to the external power supply to avoid strong attenuation due to the power supply's internal filtering capacitors.

Figure 5 demonstrates an example of a UART interface using HDO, HDI, and HDC signals.

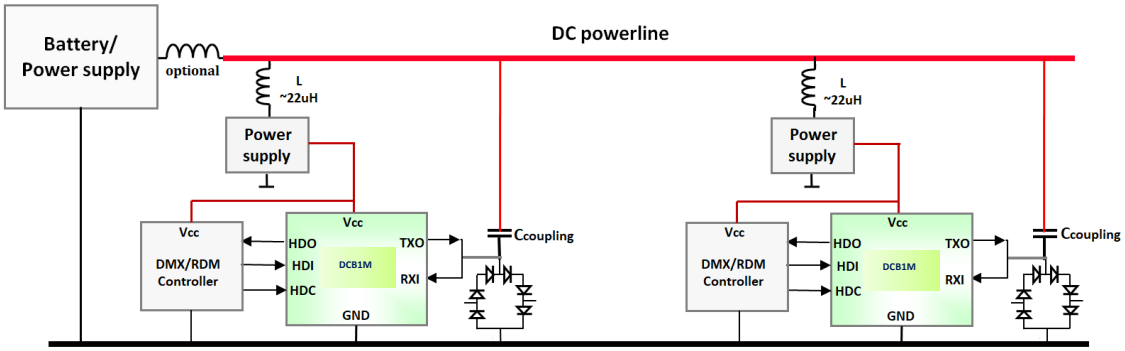

Figure 8 - DCB1M EVB Interface with DMX Controller and DC Powerline.

3.4 Interface DCB1M EVB to an existing DMX/RDM module

When interfacing to an existing DMX/RDM module that has already a built-in RS485 transceiver, an additional RS485 transceiver is required to translate the signals to Tx and Rx 3.3V logic.

Figure 9 depicts a typical DCB1M to RS485 transceiver interface connection.

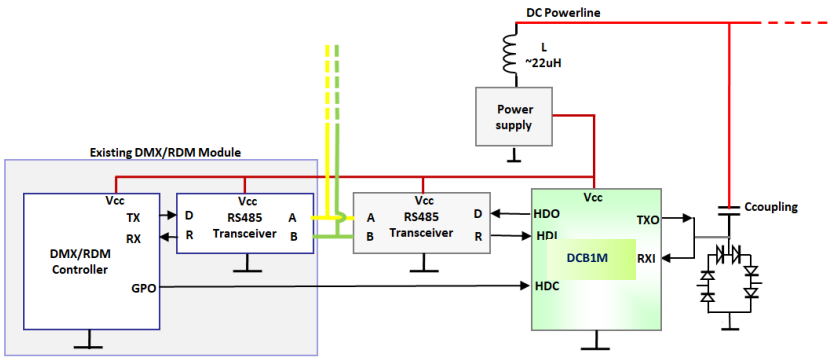

Figure 9 – Typical DCB1M to RS485 transceiver interface

* Yamar's EVB-Tester has an on-board RS485 transceiver for back-to-back DMX cable interface (see https://yamar.com/product/dc-bus-evb-tester/).

3.5 DC-BUS EVB Test Environment

The DC-BUS test environment contains an EVB Tester board controlling the tested EVB to its operating parameters. When operating as a transmitter it generates test messages transmitted over the powerline or via DC Powerline Attenuator that emulates the DC powerline. A second EVB operating as a receiver transfer the received data to a second EVB Tester that analyzes the received data or transfers it via its USB interface (when connected) to a PC for further analysis and display of the results.

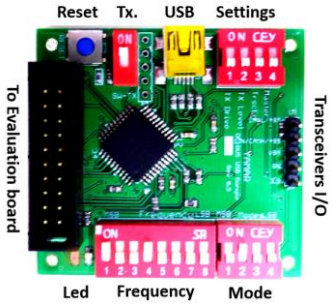

Figure 10 - EVB Tester

I. PC to PC communication via the powerline using the USB interface built in the EVB tester

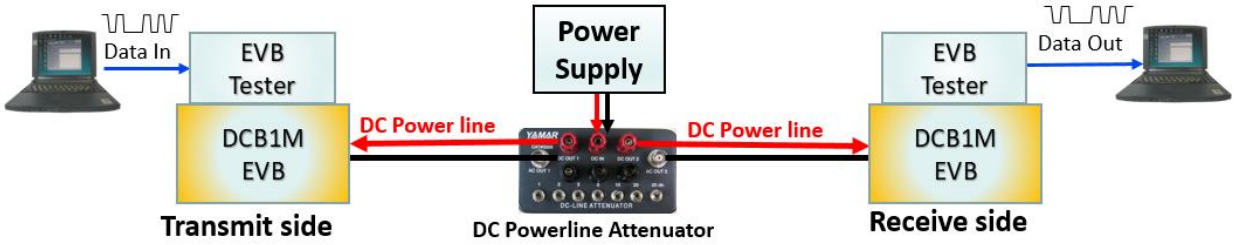

Figure 11 - PC to PC testing

II. TX test messages transmission from the EVB tester to a PC with a test program via the powerline.

Figure 12 - EVB Tester to PC testing

III. TX test messages transmission from EVB Tester to Rx EVB Tester that analyzes the received test messages and indicates the results with a LED.

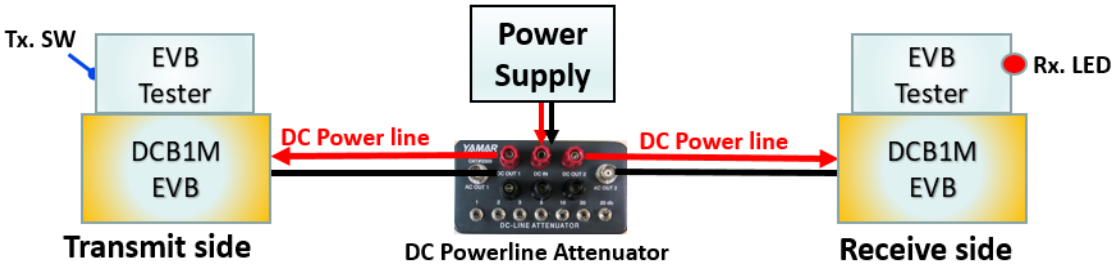

Figure 13 - EVB Tester to EVB Tester testing

3.5.1 DC Powerline Attenuator

The DC-powerline Attenuator is used for testing communication performance over the powerline in the lab. The attenuator allows adding attenuation (0 to 61dB) to the AC modulated signal over the battery powerlines (DC-Lines) keeping the DC voltage level unchanged.

Figure 14 - DC Powerline attenuator

3.6 EVB Quick setup

- ✓ Connect the communication signals via J1 to the host, according to the selected host interface (IF_SEL[1:0] pins must be set correspondingly).
- ✓ Connect the EVBs to the DC powerline.
- ✓ Configure the DCB1M if required using the HDC pin.
- ✓ Transmit and receive data to and from DCB1M EVBs connected to the DC powerline.

4. EVB DCB1M schematic

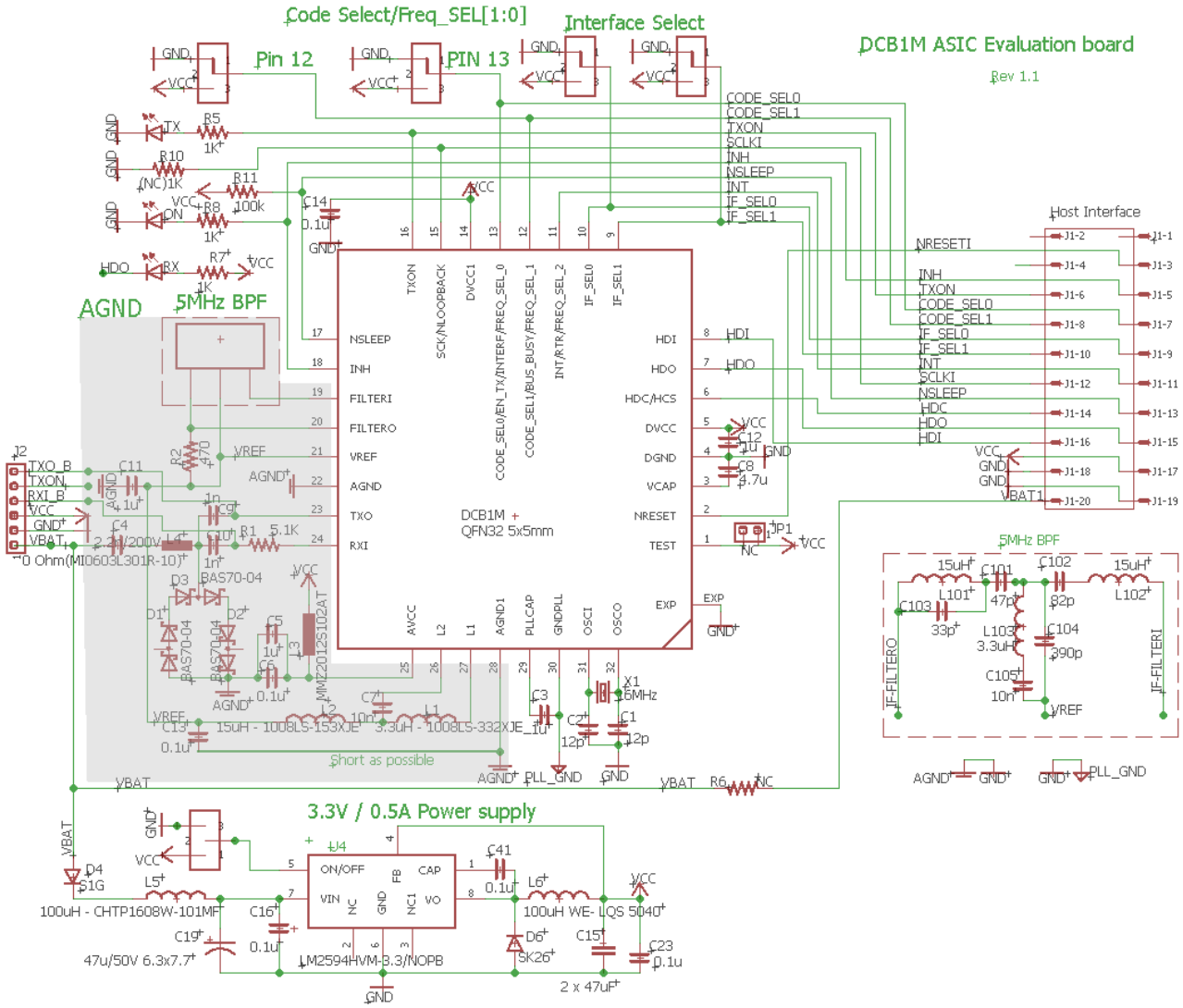

Figure 15 - DCB1M EVB circuitry

Revision History

Rev.	Date	Description
0.2	30-7-19	Initial version
0.3	2-9-2019	Update figures
0.4	15-11-2020	Update Figure 13 to Rev 1.1.
0.5	14-01-2021	Editing.
0.6	17-04-2023	Add DMX/RDM interface information