Features

- ESD/Surge protection for one line with uni-direction
- Provide transient protection for each line to
  IEC 61000-4-2 (ESD) ±30kV (air / contact)
  IEC 61000-4-4 (EFT) 80A (5/50ns)
  IEC 61000-4-5 (Lightning) 45A (8/20μs)
- For operating voltage of **28V and below**
- **1.6mm x 1.0mm DFN package** saves board space
- Protect one I/O line or one power line
- Fast turn-on and low clamping voltage
- Solid-state silicon-avalanche and active circuit triggering technology
- ***Green part***

Applications

- USB Power Delivery
- Power supply protection
- Cellular handsets and accessories
- Panel modules
- Portable devices
- Touch panels
- Notebooks and handhelds
- Peripherals

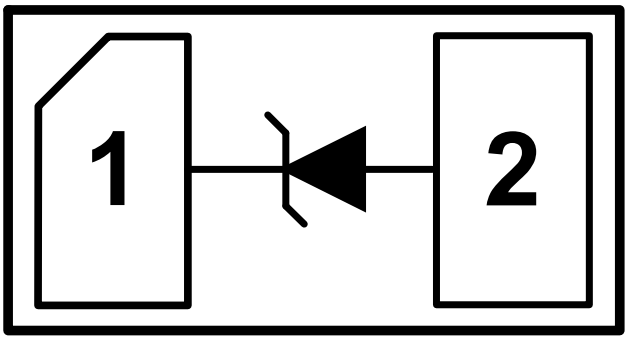
Description

AZ4528-01F is a design which includes a unidirectional surge rated clamping cell to protect one power line, or one control line, or one low speed data line in an electronic system. The AZ4528-01F has been specifically designed to protect sensitive components which are connected to power and control lines from over-voltage damage caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), Lightning, and Cable Discharge Event (CDE).

AZ4528-01F is a unique design which includes proprietary clamping cell in a single package. During transient conditions, the proprietary clamping cell prevents over-voltage on the power line or control/data lines, protecting any downstream components.

AZ4528-01F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

Circuit Diagram / Pin Configuration



DFN1610P2E (Bottom View)

Specifications

Absolute Maximum Ratings (T_A= 25°C, unless otherwise specified)			
Parameter	**Symbol**	**Rating**	**Unit**
Peak Pulse Current (t_p =8/20μs)	I_{PP} (Note 1)	45	A
Operating Voltage (pin-1 to pin-2)	V_{DC}	30.8	V
ESD per IEC 61000-4-2 (Air)	V_{ESD-1}	±30	kV
ESD per IEC 61000-4-2 (Contact)	V_{ESD-2}	±30	kV
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	°C
Operating Temperature	T_{OP}	-55 to +125	°C
Storage Temperature	T_{STO}	-55 to +150	°C

Electrical Characteristics						
Parameter	**Symbol**	**Condition**	**Min**	**Typ**	**Max**	**Unit**
Reverse Stand-Off Voltage	V_{RWM}	Pin-1 to pin-2, T = 25 °C.			28	V
Reverse Leakage Current	I_{Leak}	V_{RWM} = 28V, T = 25 °C, pin-1 to pin-2.			0.1	μA
Reverse Breakdown Voltage	V_{BV}	I_{BV} = 1mA, T = 25 °C, pin-1 to pin-2.	31.4		34.7	V
Forward Voltage	V_F	I_F = 15mA, T = 25 °C, pin-2 to pin-1.	0.5		1	V
Surge Clamping Voltage (Note 1)	$V_{CL-surge}$	I_{PP} = 5A, t_p = 8/20μs, T = 25 °C, pin-1 to pin-2.		35		V
		I_{PP} = 45A, t_p = 8/20μs, T = 25 °C, pin-1 to pin-2.		49		V
ESD Clamping Voltage (Note 2)	V_{CL-ESD}	IEC 61000-4-2 +8kV (I_{TLP} = 16A), T = 25 °C, contact mode, pin-1 to pin-2.		34.5		V
ESD Dynamic Turn-on Resistance	$R_{dynamic}$	IEC 61000-4-2 0~+8kV, T = 25 °C, contact mode, pin-1 to pin-2.		0.1		Ω
Channel Input Capacitance	C_{IN}	V_R = 0V, f = 1MHz, T = 25 °C, pin-1 to pin-2.		225	300	pF

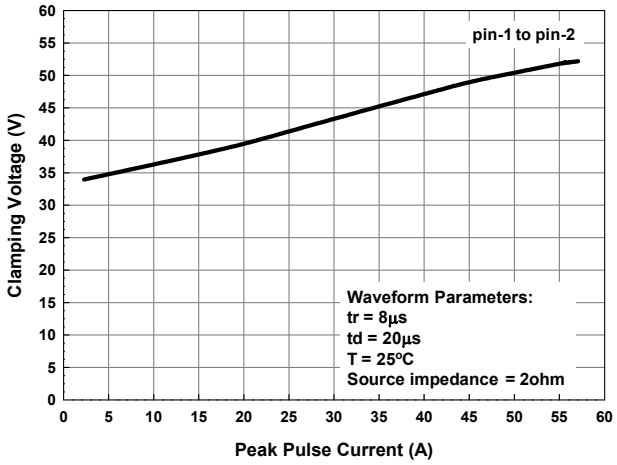
Note 1: The Peak Pulse Current and Peak Pulse Power measured conditions: t_p = 8/20μs, 2Ω source impedance.

Note 2: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.

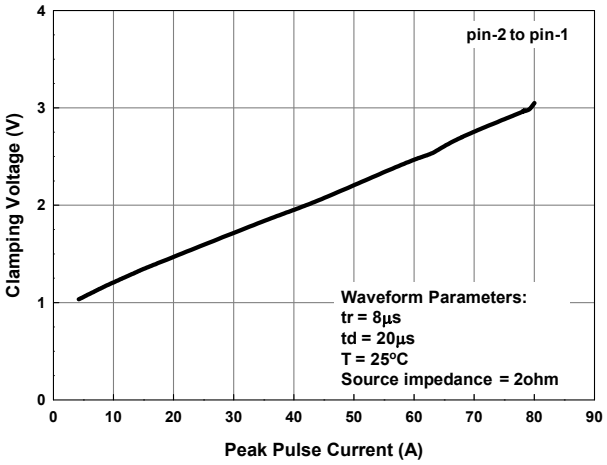
TLP conditions: Z_0= 50Ω, t_p= 100ns, t_r= 1ns.

Typical Characteristics

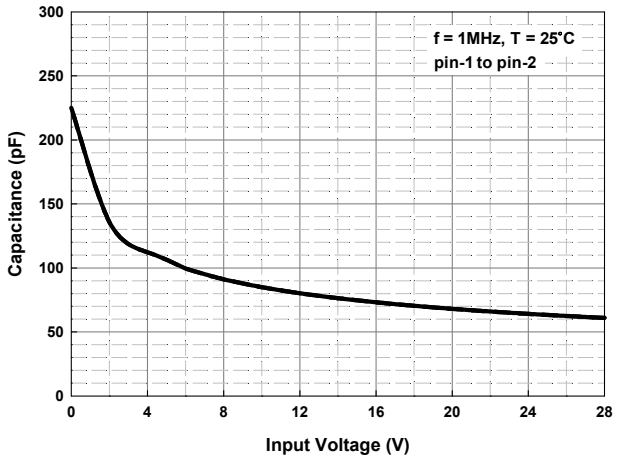
Reverse Clamping Voltage vs. Peak Pulse Current



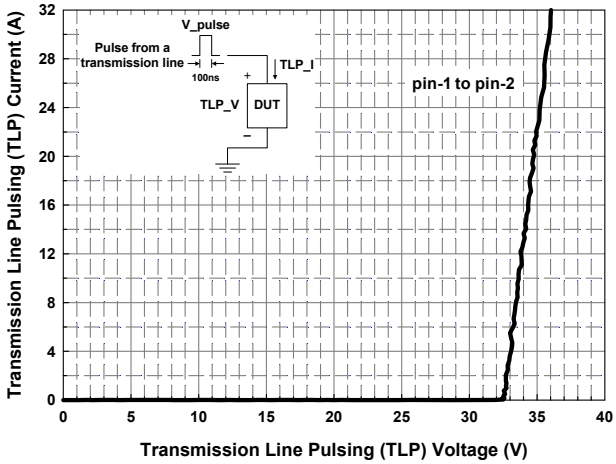
Forward Clamping Voltage vs. Peak Pulse Current



Typical Variation of C_{IN} vs. V_{IN}



Transmission Line Pulsing (TLP) Measurement



Applications Information

The AZ4528-01F is designed to protect one line against system ESD / EFT / Lightning pulses by clamping it to an acceptable reference.

The usage of the AZ4528-01F is shown in Fig. 1. Protected lines, such as data lines, control lines, or power lines, are connected to pin 1. The pin 2 should be connected to a ground plane on the board. In order to minimize parasitic inductance in the board traces, all path lengths connected to the pins of AZ4528-01F should be kept as short as possible.

In order to obtain enough suppression of ESD induced transient, a good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ4528-01F.
- Place the AZ4528-01F near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

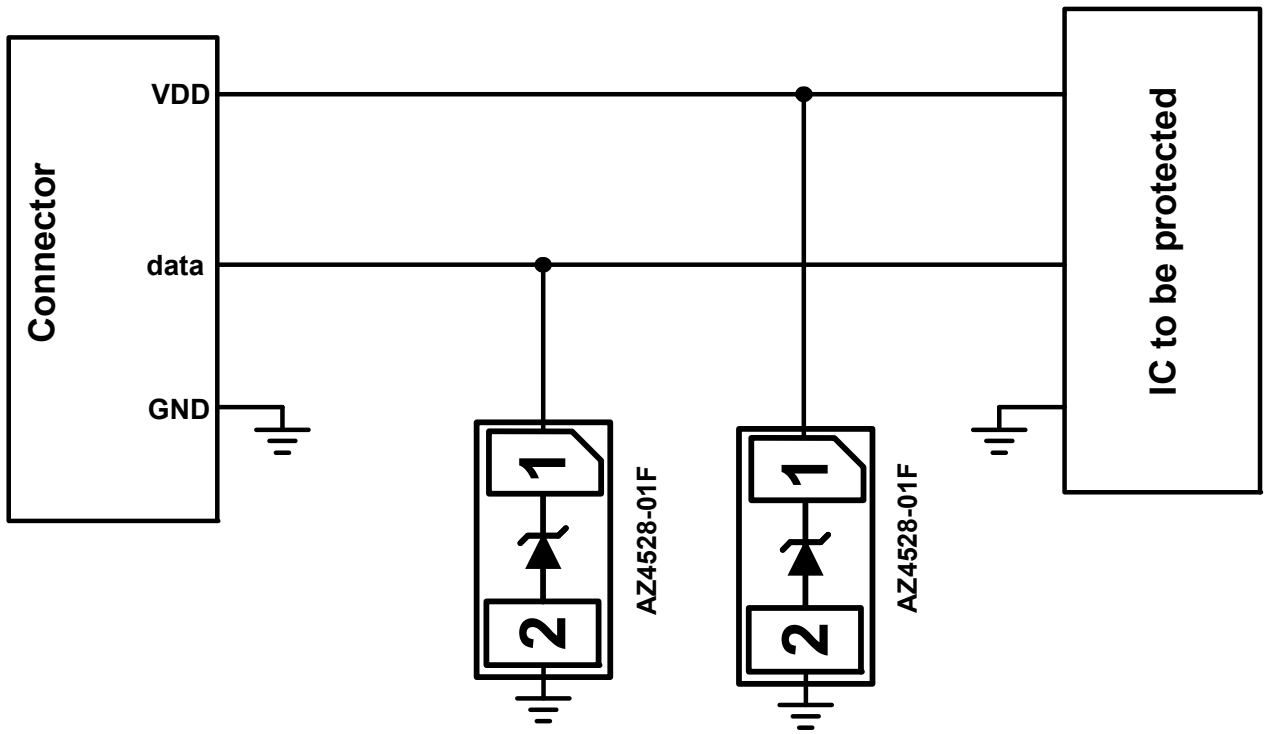


Fig. 1

Fig. 2 shows another simplified example of using AZ4528-01F to protect the control lines, low speed data lines, and power lines from ESD transient stress.

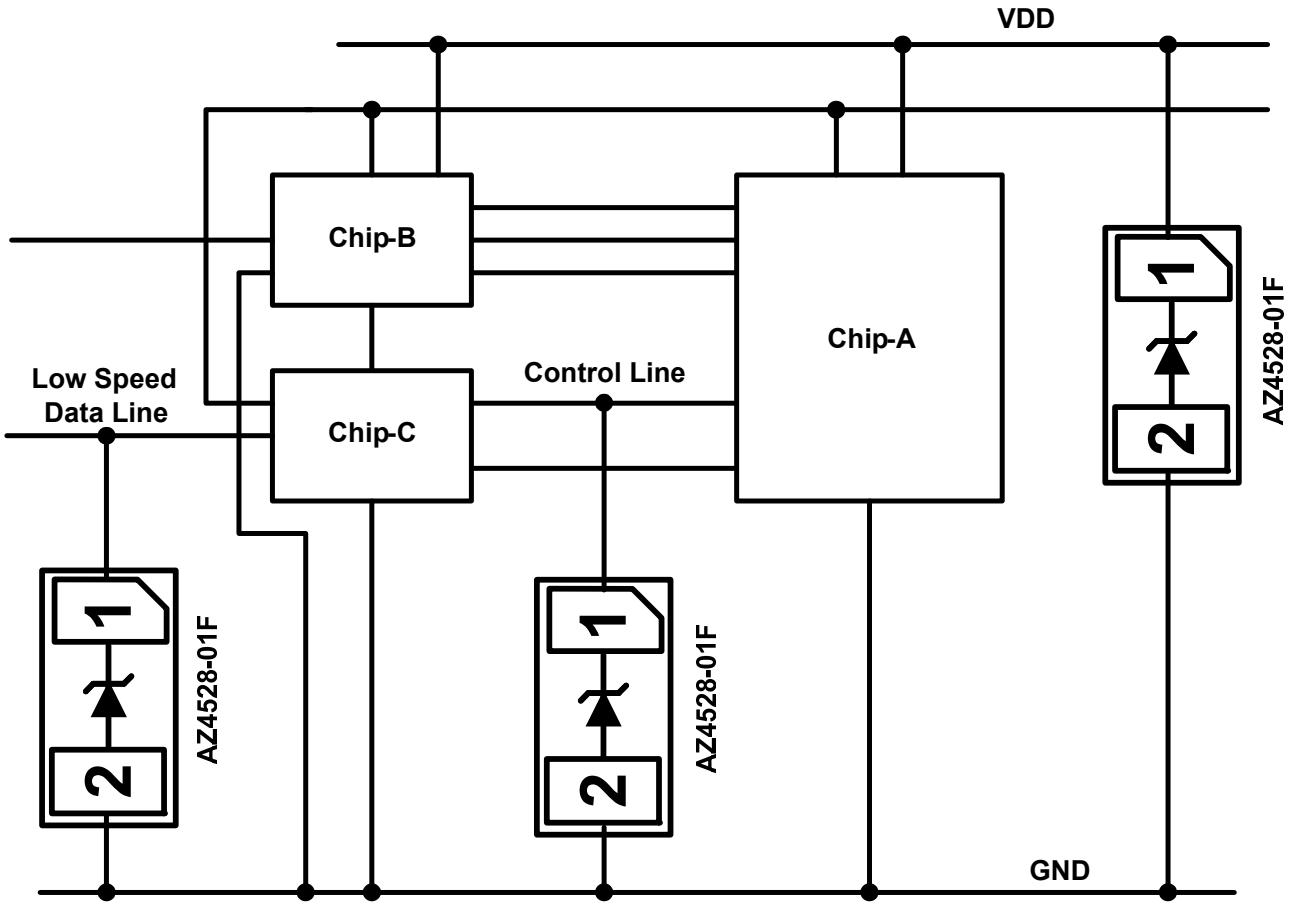
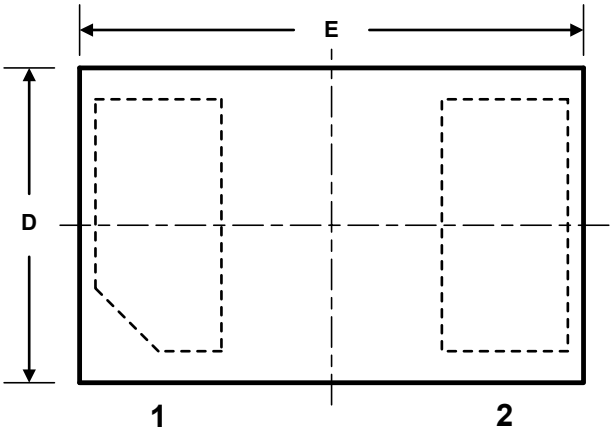


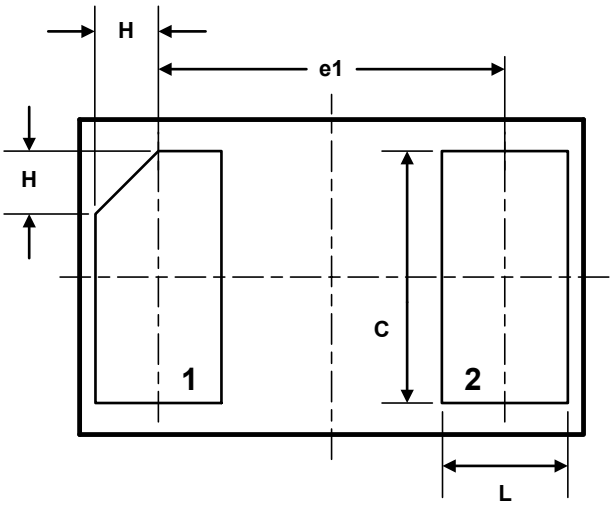
Fig. 2

Mechanical Details

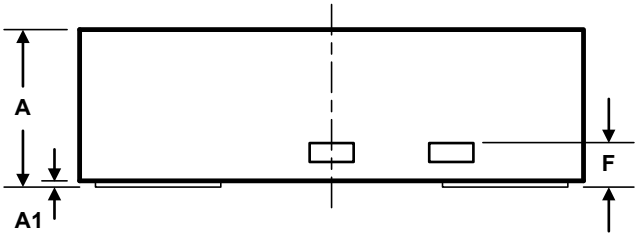
DFN1610P2E
Package Diagrams



Top View



Bottom View

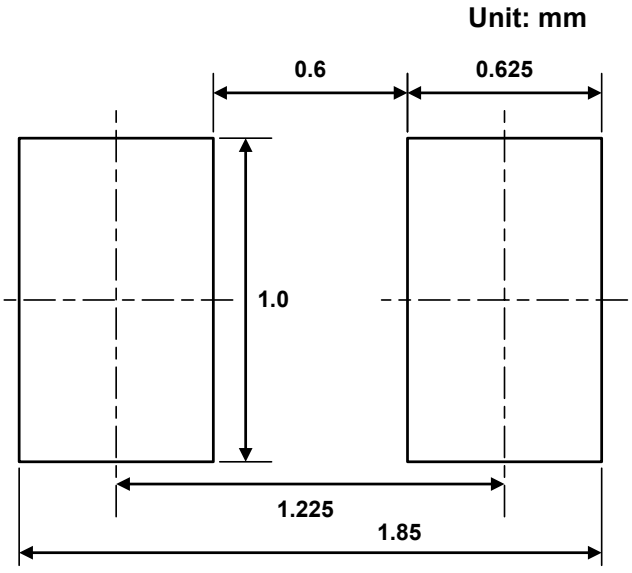


Side View

Package Dimensions

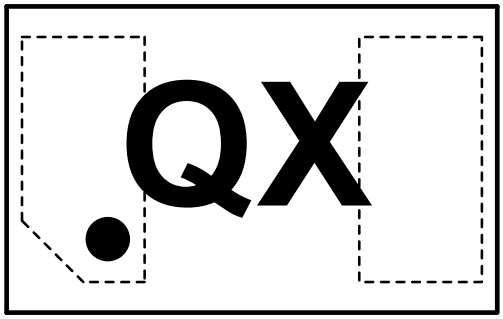
SYMBOL	Millimeters		
	Min.	Typ.	Max.
D	0.95	1.00	1.05
E	1.55	1.60	1.65
C	0.75	0.80	0.85
A	0.45	0.50	0.55
A1	-	0.02	0.05
e1	1.10 BSC		
F	0.10	0.15	0.20
H	0.15	0.20	0.25
L	0.35	0.40	0.45

Land Layout



Notes:
This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

Marking Code



Q = Device Code
X = Date Code

Part Number	Marking Code
AZ4528-01F.R7G (Green Part)	QX

Note. Green means Pb-free, RoHS, and Halogen free compliant.

Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ4528-01F.R7G	Green	T/R	7 inch	3,000/reel	4 reels = 12,000/box	6 boxes = 72,000/carton

Revision History

Revision	Modification Description
Revision 2022/03/18	Preliminary Release.
Revision 2022/05/19	Formal Release.