Features

- ESD Protect for 2 high-speed I/O channels
- Provide ESD protection for each channel to
  IEC 61000-4-2 (ESD) ±30kV (air), ±30kV (contact)
  IEC 61000-4-4 (EFT) 80A (5/50ns)
  IEC 61000-4-5 (Lightning) 12A (8/20μs)
- For low operating voltage applications: 3.3V maximum
- Low capacitance : 2.8pF typical
- Fast turn-on and Low clamping voltage
- Array of surge rated diodes with internal equivalent TVS diode
- Small package saves board space
- Solid-state silicon-avalanche and active circuit triggering technology
- ROHS part available
- Green part available

Applications

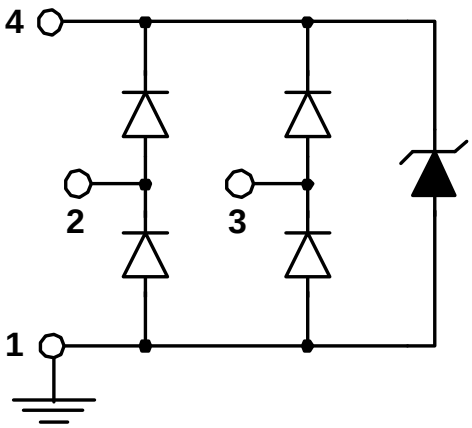
- **Fingerprint**
- Data and I/O lines protection
- Handheld electronics
- Analog input lines protection
- Video lines protection
- LAN applications
- 3.3V operating systems

Description

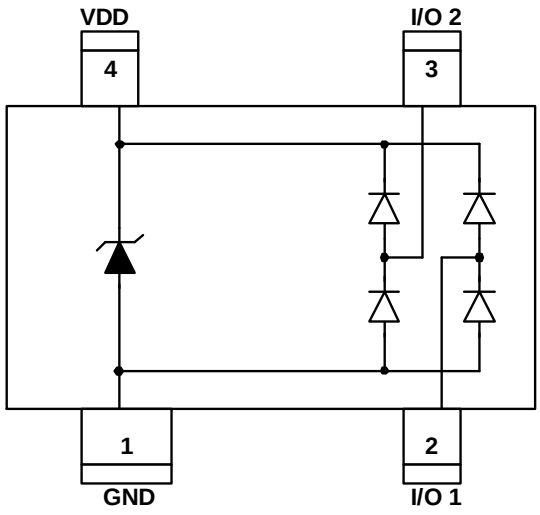
AZ1013-02N is a high performance design which includes surge rated diode arrays to protect high speed data interfaces. The AZ1013-02N has been specifically designed to protect sensitive components, which are connected to data and transmission lines, from over-voltage caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), and Lightning.

AZ1013-02N is a unique design which includes surge rated, low capacitance steering diodes and a unique design of clamping cell which is an equivalent TVS diode in a single package. During transient conditions, the steering diodes direct the transient to either the power supply line or to the ground line. The internal unique design of clamping cell prevents over-voltage on the power line, protecting any downstream components. AZ1013-02N may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (± 15kV air, ±8kV contact discharge).

Circuit Diagram



Pin Configuration



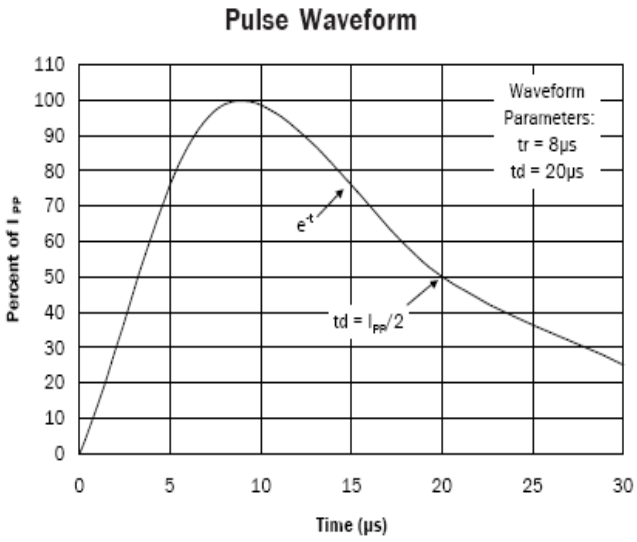
JEDEC SOT143-4L (Top View)

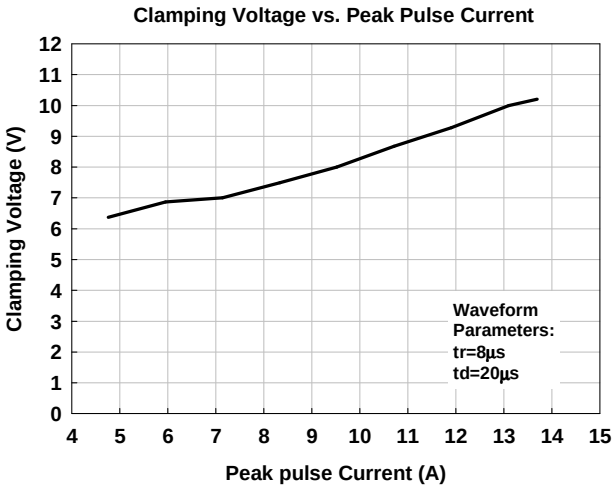
SPECIFICATIONS

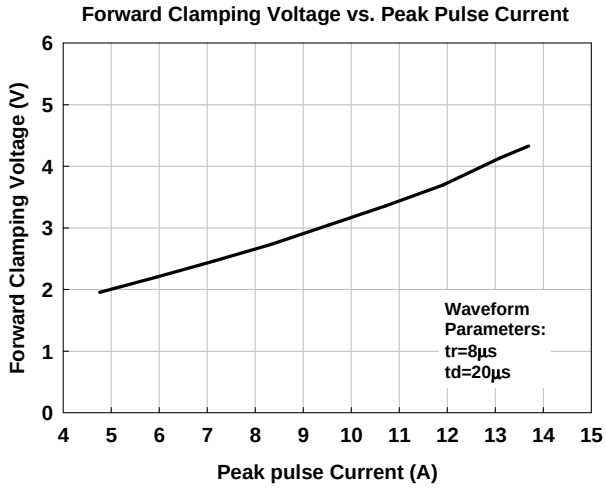
ABSOLUTE MAXIMUM RATINGS			
PARAMETER	**PARAMETER**	**RATING**	**UNITS**
Peak Pulse Current (tp =8/20μs)	I_{PP}	12	**A**
Operating Supply Voltage (VDD-GND)	V_{DC}	3.8	**V**
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	±30 ±30	**kV**
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	**°C**
Operating Temperature	T_{OP}	-55 to +125	**°C**
Storage Temperature	T_{STO}	-55 to +150	**°C**
DC Voltage at any I/O pin	V_{IO}	(GND – 0.5) to (VDD + 0.5)	**V**

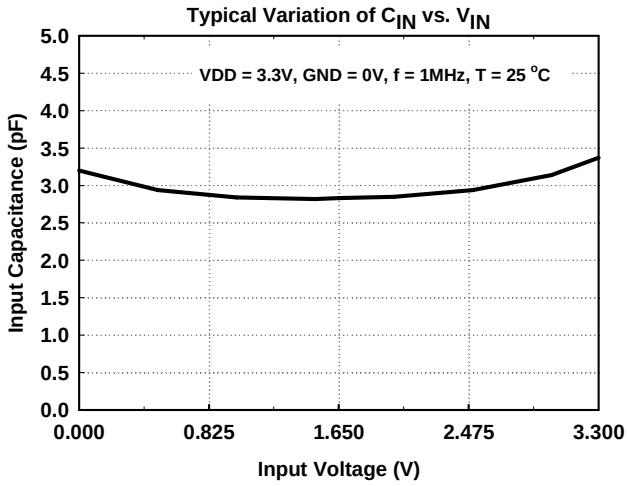
ELECTRICAL CHARACTERISTICS						
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Reverse Stand-Off Voltage	V_{RWM}	Pin 4 to pin 1, T=25 °C			3.3	**V**
Reverse Leakage Current	I_{Leak}	V_{RWM}=3.3V, T=25 °C, Pin 4 to pin 1			5	**μA**
Channel Leakage Current	I_{CH_Leak}	$V_{Pin\ 4}$ = 3.3V, $V_{Pin\ 1}$ = 0V, T=25 °C			1	**μA**
Reverse Breakdown Voltage	V_{BV}	I_{BV} = 1mA, T=25 °C Pin 4 to Pin 1	4.5		6.5	**V**
Forward Voltage	V_F	I_F = 15mA, T=25 °C Pin1 to Pin 4	0.6		1	**V**
Surge Clamping Voltage	V_{surge_CL}	I_{PP}=5A, tp=8/20μs, T=25 °C Any Channel pin to Ground		6.5	7.5	**V**
ESD Clamping Voltage-1	V_{ESD_CL1}	IEC 61000-4-2 +6kV, T=25 °C, Contact mode, Any Channel pin to Ground		9		**V**
ESD Clamping Voltage-2	V_{ESD_CL2}	IEC 61000-4-2 +6kV, T=25 °C, Contact mode, pin-4 to pin-1		6.5		**V**
Channel Input Capacitance	C_{IN}	V_{pin4} = 3.3V, V_{pin1} = 0V, **V_{IN} = 1.65V**, f = 1MHz, T=25 °C, Any Channel pin to Ground		2.8	3.5	**pF**
Channel to Channel Input Capacitance	C_{CROSS}	V_{pin4} = 3.3V, V_{pin1} = 0V, **V_{IN} = 1.65V**, f = 1MHz, T=25 °C , Between Channel pins		0.45	0.5	**pF**
Variation of Channel Input Capacitance	$\triangle C_{IN}$	V_{pin4} = 3.3V, V_{pin1} = 0V, **V_{IN} = 1.65V**, f = 1MHz, T=25 °C , Channel_x pin to Ground - Channel_y pin to Ground		0.05	0.1	**pF**

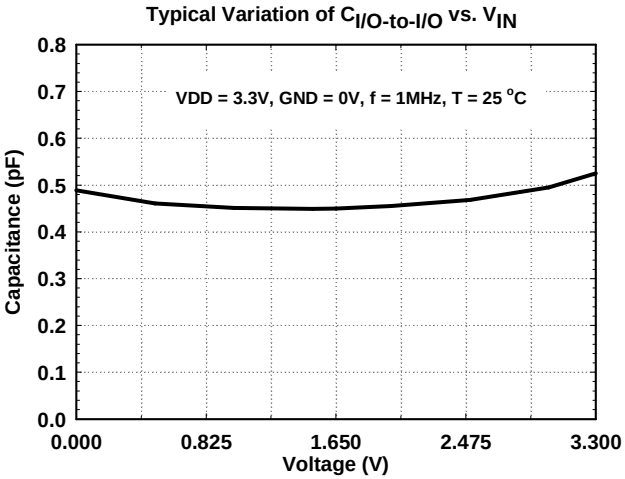
Typical Characteristics

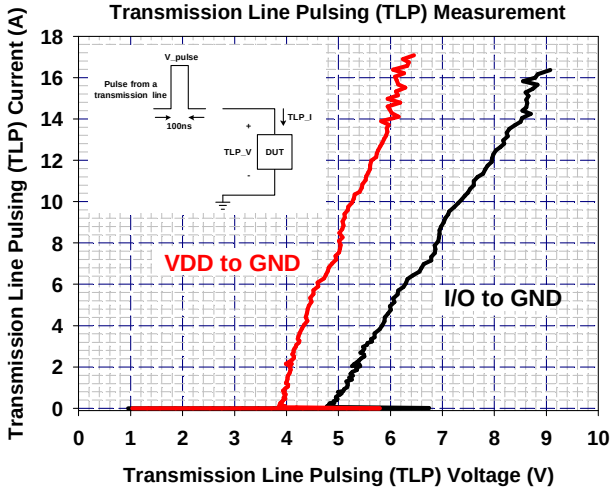












Applications Information

A. Design Considerations

The ESD protection scheme for system I/O connector is shown in the Fig. 1. In Fig. 1, the diodes D1 and D2 are general used to protect data line from ESD stress pulse. If the power-rail ESD clamping circuit is not placed between VDD and GND rails, the positive pulse ESD current (I_{ESD1}) will pass through the ESD current path1. Thus, the ESD clamping voltage V_{CL} of data line can be described as follow:

V_{CL} = Fwd voltage drop of D1 + supply voltage of VDD rail + $L_1 \times d(I_{ESD1})/dt + L_2 \times d(I_{ESD1})/dt$

Where L_1 is the parasitic inductance of data line, and L_2 is the parasitic inductance of VDD rail.

An ESD current pulse can rise from zero to its peak value in a very short time. As an example, a level 4 contact discharge per the IEC61000-4-2 standard results in a current pulse that rises from zero to 30A in 1ns. Here $d(I_{ESD1})/dt$ can be approximated by $\Delta I_{ESD1}/\Delta t$, or 30/(1x10-9). So just 10nH of total parasitic inductance (L_1 and L_2 combined) will lead to over 300V increment in V_{CL}! Besides, the ESD pulse current which is directed into the VDD rail may potentially damage any components that are attached to that rail. Moreover, it is common for the forward voltage drop of discrete diodes to exceed the damage threshold of the protected IC. This is due to the relatively small junction area of typical discrete components. Of course, the discrete diode is also possible to be destroyed due to its power dissipation capability is exceeded.

The AZ1013-02N has an integrated power-rail ESD clamped circuit between VDD and GND rails. It can successfully overcome previous disadvantages. During an ESD event, the positive ESD pulse current (I_{ESD2}) will be directed through the integrated power-rail ESD clamped circuit to GND rail (ESD current path2). The clamping voltage V_{CL} on the data line is small and protected IC will not be damaged because power-rail ESD clamped circuit offer a low impedance path to discharge ESD pulse current.

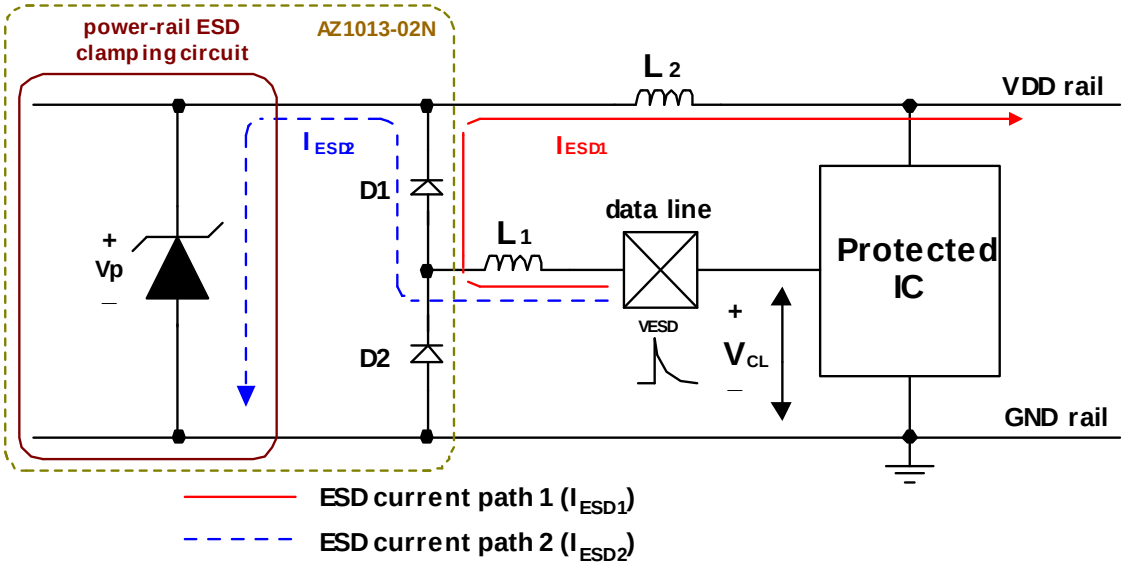


Fig. 1 Application of positive ESD pulse between data line and GND rail.

B. Device Connection

The AZ1013-02N is designed to protect two data lines and power rails from transient over-voltage (such as ESD stress pulse). The device connection of AZ1013-02N is shown in the Fig. 2. In Fig. 2, the two protected data lines are connected to the ESD protection pins (pin2, pin3) of AZ1013-02N. The ground pin (pin1) of AZ1013-02N is a negative reference pin. This pin should be directly connected to the GND rail of PCB (Printed Circuit Board). To get minimum parasitic inductance, the path length should keep as short as possible. In addition, the power pin (pin 4) of AZ1013-02N is a positive reference pin. **This pin should directly connect to the VDD rail of PCB**. When pin 4 of AZ1013-02N is connected to the VDD rail, the leakage current of ESD protection pin of AZ1013-02N becomes very small. Because the pin 4 of AZ1013-02N is directly connected to VDD rail, the VDD rail also can be protected by the power-rail ESD clamped circuit (not shown) of AZ1013-02N to make sure system is able to operate properly when ESD event happens.

Once the power pin (pin 4) of AZ1013-02N dose not be tied the VDD potential of the protected system, e.g. be floated, the leakage current of ESD protection pin of AZ1013-02N becomes large. **Therefore, the power pin (pin 4) of AZ1013-02N is not allowed to be floated when the protected system is operating.**

AZ1013-02N can provide protection for 2 I/O signal lines simultaneously. If the number of I/O signal lines is less than 2, the unused I/O pins can be simply left as NC pins.

In some cases, systems are not allowed to be reset or restart after the ESD stress directly applying at the I/O-port connector. Under this situation, in order to enhance the sustainable ESD Level, a 0.1μF chip capacitor can be added between the VDD and GND rails. The place of this chip capacitor should be as close as possible to the AZ1013-02N.

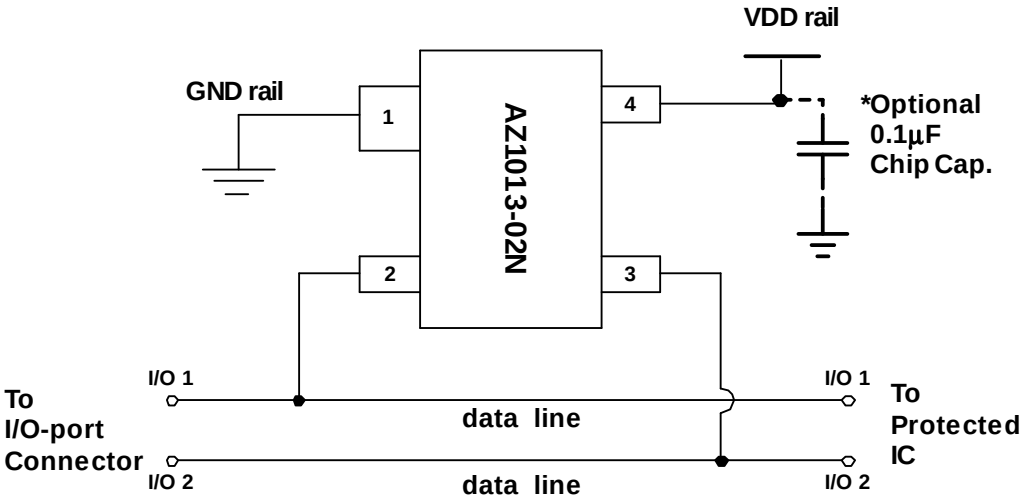


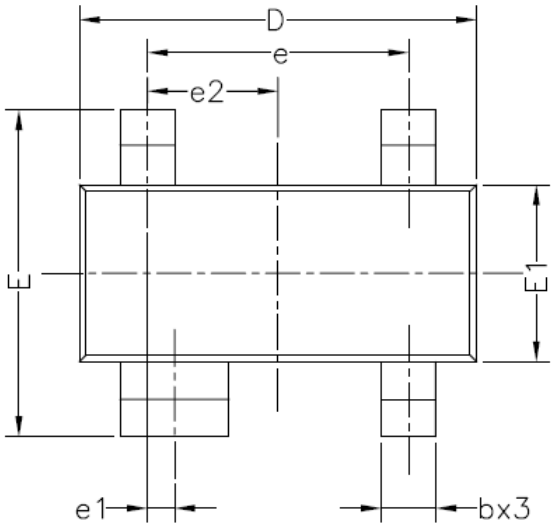
Fig. 2 Data lines and power rails connection of AZ1013-02N.

Mechanical Details

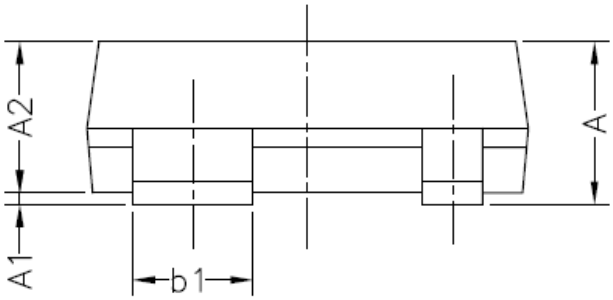
SOT143-4L

PACKAGE DIAGRAMS

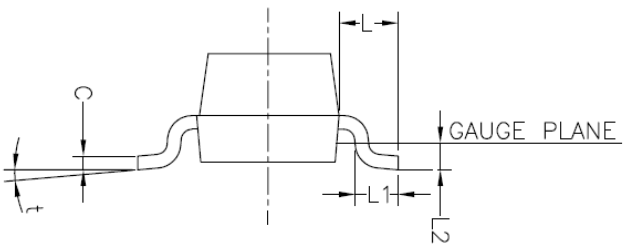
TOP VIEW



SIDE VIEW



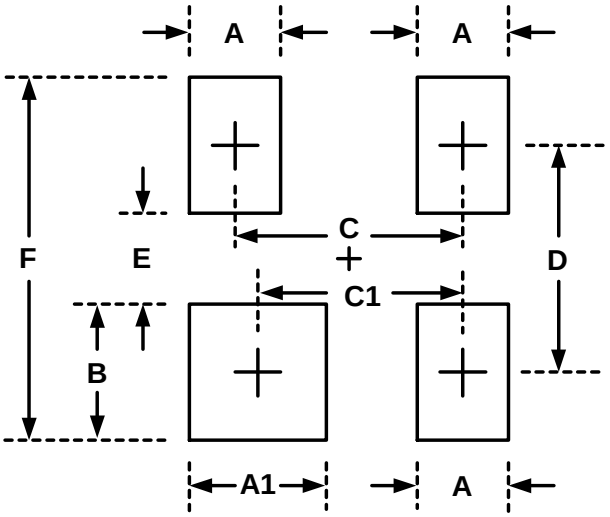
END VIEW



PACKAGE DIMENSIONS

Symbol	Millimeters		Inches	
	MIN.	MAX.	MIN.	MAX.
A	0.95	1.17	0.037	0.046
A1	0.05	0.1	0.002	0.004
A2	0.9	1.1	0.035	0.043
b	0.35	0.5	0.014	0.020
b1	0.76	0.89	0.030	0.035
C	0.09	0.18	0.004	0.007
D	2.8	3.04	0.110	0.120
E1	1.2	1.4	0.047	0.055
E	2.25	2.55	0.089	0.100
e1	0.20 BSC		0.0078 BSC	
e2	0.96 BSC		0.0377 BSC	
e	1.8	2.02	0.071	0.080
L	0.55 REF.		0.0216 BSC	
L1	0.3	0.6	0.012	0.024
L2	0.25 REF		0.0098 BSC	
t	0~9°		0~9°	

LAND LAYOUT

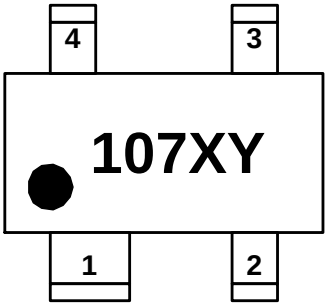


Dimensions		
Index	**Millimeter**	**Inches**
A	1.00	0.039
A1	1.40	0.055
B	1.40	0.055
C	1.92	0.076
C1	1.72	0.068
D	2.20	0.087
E	0.80	0.031
F	3.60	0.141

Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

MARKING CODE



107 = Device Code
X = Date Code
Y = Control Code

Part Number	Marking Code
AZ1013-02N (ROHS part)	107XY
AZ1013-02N **(Green part)**	**116XY**

Ordering Information

PN#	Material	Type	Reel size	MOQ/interal box	MOQ/carton
AZ1013-02N.R7G	Green	T/R	7 inch	4 reel= 12,000/box	6 box =72,000/carton

Revision History

Revision	Modification Description
Revision 2008/05/30	Preliminary Release.
Revision 2009/02/04	Formal Version Release.
Revision 2009/03/04	Update the PACKAGE DIMENSIONS.
Revision 2011/06/18	1. Update the Company Logo. 2. Add the Ordering Information.