

Product Specification

DESCRIPTION

The GLF4028 is an integrated power multiplexer switch with dual independent power switches connected to a single output pin to enable seamless transition between two input sources.

The GLF4028 provides a manual selection mode by the combination of the logic input pins of EN and SEL. The EN input pin is used along with the select (SEL) input pin to select VIN1 only, select VIN2 only, or turn both switches off.

The GLF4028 features an ultra-efficient I_QSmart^{TM} technology that offers quiescent current (I_Q) and shutdown current (I_{SD}) in the industry. Low R_{ON} reduces conduction losses while low I_Q and I_{SD} solutions help designers to reduce parasitic leakage current, improve system efficiency, and increase battery lifetime.

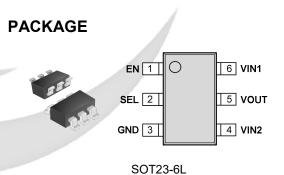
The GLF4028 blocks any cross-conduction current between two input power sources. When the switch is disabled, the GLF4028 prevents the reverse current to the input source from the output at any higher VOUT than VIN condition.

FEATURES

- Two-Input and Single-Output Power Multiplexer Switch
- Supply Voltage Range: 2.5 V to 5.5 V
- R_{ON}: 97 mΩ Typ. at 5.5 V_{IN1} or V_{IN2}
 105 mΩ Typ. at 4.5 V_{IN1} or V_{IN2}
- 2 A Continuous Output Current Capability Per Channel
- Ultra-Low Supply Current at Operation $I_Q: \ 3 \ \mu A \ Typ \ at \ 5.5 \ V_{IN}$
- Ultra-Low Stand-by Current I_{SD} : 5 nA Typ at 5.5 V_{IN}
- Smart Control Pins
 I_{EN} and I_{SEL} : 3 nA Typ at V_{EN} or V_{SEL} > V_{IH}
 R_{EN} and R_{SEL} : 500 kΩ Typ
- No Cross Conduction Between Two Inputs
- Reverse Current Blocking when Disabled
- Operating Temperature Range: -40 °C to 85 °C
- HBM: 6 kV, CDM: 2 kV

APPLICATIONS

- Smart Devices
- Smart Home Electronics

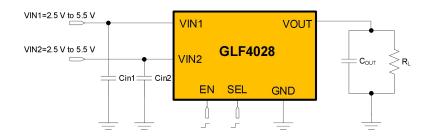


DEVICE ORDERING INFORMATION

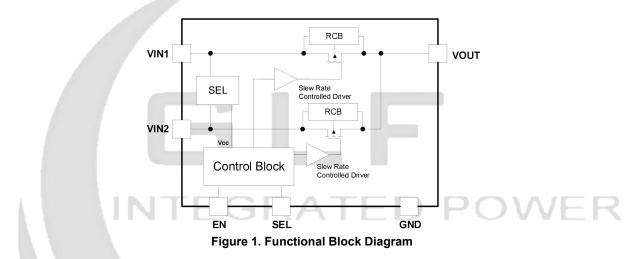
| Part Number | Part Number Top Mark | | Output Current, IOUT | Ultra-low I_Q at 5.5 V_{IN} | | |
|--------------|----------------------|-------|----------------------|---------------------------------|--|--|
| GLF4028-T2G7 | EP | 97 mΩ | 2 A | 3 μΑ | | |



APPLICATION DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

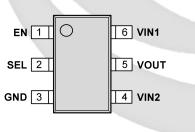


Figure 2. SOT23-6L

PIN DEFINITION

| | Pin # | Name | Description | | | | | |
|--|----------------|------|---|--|--|--|--|--|
| | 1 | EN | Enable to control the switch. Do not leave the EN pin floating. | | | | | |
| | 2 | SEL | Input Source Selection. Do not leave the SEL pin floating. | | | | | |
| | 3GND4VIN25VOUT | | Ground | | | | | |
| | | | Switch Input 2 | | | | | |
| | | | Switch Output | | | | | |
| | 6 | VIN1 | Switch Input 1 | | | | | |



ABSOLUTE MAXIMUM RATINGS

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions; extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Pa | arameter | Min. | Max. | Unit | |
|------------------------|--|-----------------------------------|------|------|------|--|
| VIN1, VIN2 VOUT, EN | Each Pin Voltage Range to GND | Each Pin Voltage Range to GND | | | | |
| IOUT | Maximum Continuous Switch Current | Maximum Continuous Switch Current | | | | |
| PD | Power Dissipation at T _A = 25°C | | 1.0 | W | | |
| T _{STG} | Storage Junction Temperature | -65 | 150 | °C | | |
| TA | Operating Temperature Range | Operating Temperature Range | | | | |
| θ _{JC} | Thermal Resistance, Junction to Case | 2 | | 90 | °C/W | |
| θյΑ | Thermal Resistance, Junction to Ambient | | | 180 | °C/W | |
| ESD | Electrostatic Discharge Canability | Human Body Model, JESD22-A114 | 6 | | kV | |
| ESD | Electrostatic Discharge Capability | Charged Device Model, JESD22-C101 | 2 | | κv | |

Notes: 1. The thermal resistance depends on the PCB layout and heat dissipation.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min. | Max. | Unit |
|------------|-------------------------------|------|------|------|
| VIN1, VIN2 | Supply Voltage | 2.5 | 5.5 | V |
| TA | Ambient Operating Temperature | -40 | +85 | °C |



ELECTRICAL CHARACTERISTICS

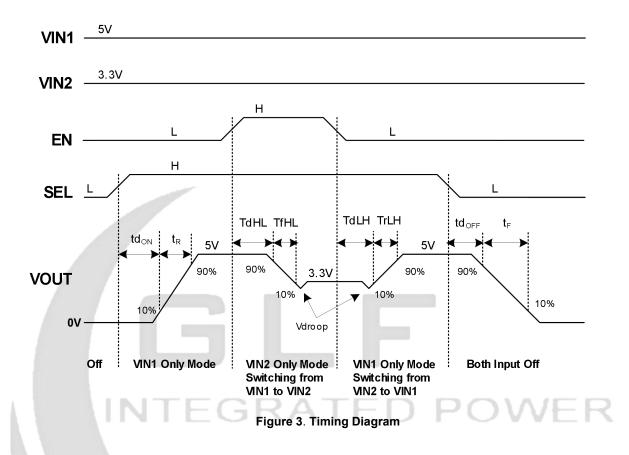
 V_{IN1} = V_{IN2} = 2.5 V to 5.5 V and T_A = 25°C. Unless otherwise noted

| Symbol | Parameter | Conditions | | Min. | Тур | Max | Unit |
|---------------------------------|-----------------------------------|---|--|------|-----|-----|------|
| Basic Oper | ation | | | | | | |
| la1, la2 | Quiescent Current | $ \begin{array}{ c c c c c c c c c c c c c c c c c c c$ | | 3 | 4.5 | μΑ | |
| | | As above, $T_A = 85^{\circ}C^{(1)}$ | | | 4 | | |
| | | V _{IN1,2} = 5.5 V, V _{OUT} = GND, EN = SI | EL = 0 V | | 5 | 20 | |
| $I_{SD1,} I_{SD2}$ | Shutdown Current | $V_{IN1,2}$ = 5.5 V, V_{OUT} = GND, EN = S T_A =85 °C ⁽¹⁾ | $V_{IN1,2} = 5.5 \text{ V}, V_{OUT} = \text{GND}, \text{EN} = \text{SEL} = 0 \text{ V},$ T _A =85 °C ⁽¹⁾ | | | | nA |
| | | | T _A = 25 °C | | 97 | 107 | |
| Ron | | V_{IN1} or V_{IN2} = 5.5 V, I_{OUT} = 500 mA | T _A = 85 °C ⁽¹⁾ | | 115 | | - |
| | | | T _A = 25 °C | | 105 | 118 | |
| | On-Resistance | V_{IN1} or V_{IN2} = 4.5 V, I_{OUT} = 500 mA T_A = 85 °C (| | | 125 | | mΩ |
| | | V _{IN1} or V _{IN2} = 3.3 V, I _{OUT} = 300 mA | | | 120 | 135 | |
| | | V_{IN1} or V_{IN2} = 2.5 V, I_{OUT} = 100 mA | | | 145 | 162 | |
| V _{IH} | EN, SEL Input Logic High Voltage | | | 1.2 | | | V |
| VIL | EN, SEL Input Logic Low Voltage | | | | | 0.4 | V |
| $I_{\text{EN}}, I_{\text{SEL}}$ | EN, SEL Current | V_{EN} or $V_{SEL} > V_{IH}$, Enabled | | | 3 | 20 | nA |
| Ren, Rsel | EN, SEL Pulldown Resistance (1) | V_{EN} or $V_{SEL} < V_{IL}$, Disabled | PO | S | 500 | R | kΩ |
| I _{RVS} | Reverse Current ⁽¹⁾ | $V_{IN1} = V_{IN2} = 0 V, V_{OUT} = 5.5 V, EN = S$ | EL=0 V | | 2.5 | | μA |
| Switching (| Characteristics ⁽²⁾ | | | | | | |
| t _{dON} | Turn-On Delay | | | | 250 | | |
| t _R | VOUT Rise Time |] | - | | 340 | | |
| TdHL | High-low Delay ⁽¹⁾ | | | | 3 | | μs |
| TfHL | High-low Fall Time ⁽¹⁾ | | | | 6 | | |
| Vdroop | Voltage Droop ⁽¹⁾ | V _{IN1} = 5 V, V _{IN2} = 3.3 RL=150 Ω, C _{OUT} =1.0 | | | 120 | | mV |
| TdLH | Low-high Delay ⁽¹⁾ | | P" | | 7 | | |
| TrLH | Low-high Rise Time (1) | | | | 4 | | |
| tdoff | Turn-Off Delay ⁽¹⁾ | | | | 13 | | μs |
| t _F | VOUT Fall Time ⁽¹⁾ | | Ī | | 350 | | |

Notes: 1. By design; characterized, not production tested. 2. $t_{ON} = t_{dON} + t_R$, $t_{OFF} = t_{dOFF} + t_F$



TIMING DIAGRAM AND TRUTH TABLE



| SEL | EN | Function | VOUT |
|-----|----|-----------------------|--------|
| 0 | 0 | Both switches are off | High-Z |
| 1 | 0 | Only VIN1 is selected | VIN1 |
| 1 | 1 | Only VIN2 is selected | VIN2 |

Table 1. Truth Table of Input Source Selection

TYPICAL PERFORMANCE CHARACTERISTICS

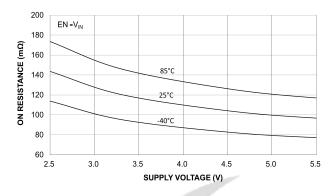
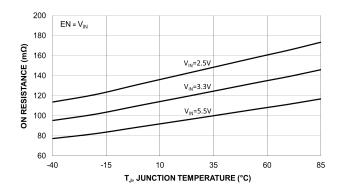
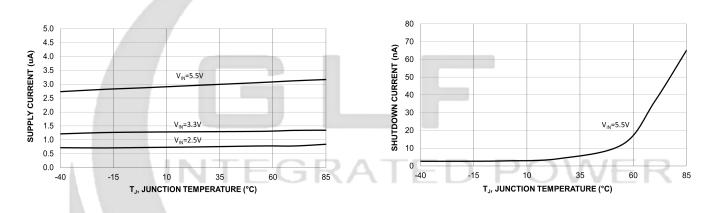
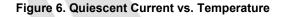


Figure 4. On-Resistance vs. Supply Voltage









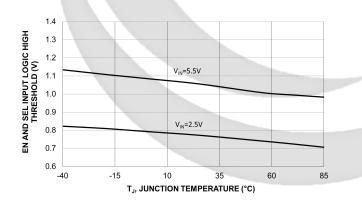


Figure 8. EN and SEL Input Logic High Threshold vs. Temperature

Figure 7. Shutdown Current vs. Temperature

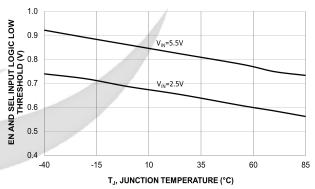


Figure 9. EN and SEL Input Logic Low Threshold vs. Temperature

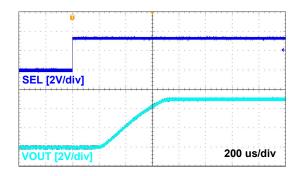


Figure 10. Turn-On Response V_{IN1}=5 V, C_{IN}=0.1 \ \mu\text{F}, C_{OUT}=1.0 \ \mu\text{F}, R_L=150 \ \Omega

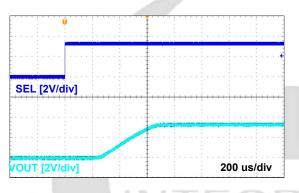
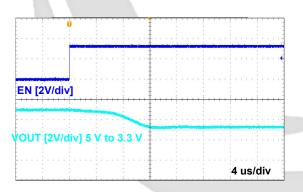


Figure 12. Turn-On Response V_{IN1}=3.3 V, C_{IN}=0.1 μF, C_{OUT}=1.0 μF, R_L=150 Ω





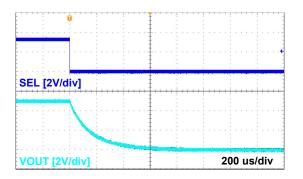


Figure 11. Turn-Off Response V_{IN1}=5 V, C_{IN}=0.1 \ \mu\text{F}, C_{OUT}=1.0 \ \mu\text{F}, R_L=150 \ \Omega

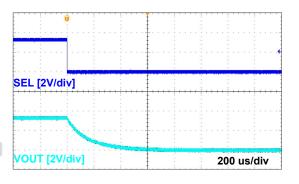


Figure 13. Turn-Off Response V_{IN1}=3.3 V, C_{IN}=0.1 μF, C_{OUT}=1.0 μF, R_L=150 Ω

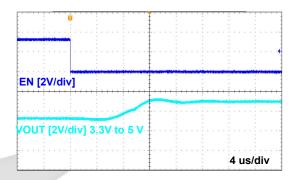


Figure 15. V_{OUT} Switchover from 3.3 V to 5 V V_{IN1}=5 V, V_{IN2}=3.3 V C_{IN}= C_{OUT}=1.0 μ F, R_L=150 Ω

| | | | 20 |) ms/div |
|------|---|-----------|----|----------|
| | VIN1 [1V/div] VIN2 [1V/div] Iout [50mA/div] | | | |
| | +++++++++++++++++++++++++++++++++++++++ | +++++ | | |
| | [] | | | |
| | VOUT [1V/div] | | | |
| | Ī | | | |

Figure 16. Reverse Current Blocking When Disabled $V_{IN1} = V_{IN2} = 0 V$, $V_{OUT} = 0 V$ to 4.5 V, $C_{IN} = C_{OUT} = 1.0 \mu F$, EN=SEL=0 V

APPLICATION INFORMATION

The GLF4028 is a fully integrated 2 A Power Mux with a fixed slew rate control to limit the inrush current during device turn on. The GLF4028 also has a wide voltage operating range from 2.5 V to 5.5 V. In the off state, the GLF4028 consumes very low leakage current to avoid unwanted power drain from limited input power supplies.

Input Source Selection

By changing the state of the SEL and EN pins, the GLF4028 offers a manual input selection mode. In each mode, the VOUT connects to one input source.

Input Capacitor

A capacitor is recommended to be placed close to the V_{IN} pin to reduce the voltage drop on the input power rail caused by transient inrush current at start-up. A higher input capacitor value can be used to further attenuate the input voltage drop.

Output Capacitor

An output capacitor is recommended to minimize voltage undershoot on the output pin during the transition when the switch is turned off. Undershoot can be caused by parasitic inductance from board traces or intentional load inductances. If load inductances do exist, use of an output capacitor can improve output voltage stability and system reliability. The C_{OUT} capacitor should be placed close to the VOUT and GND pins.

Reverse Current Blocking

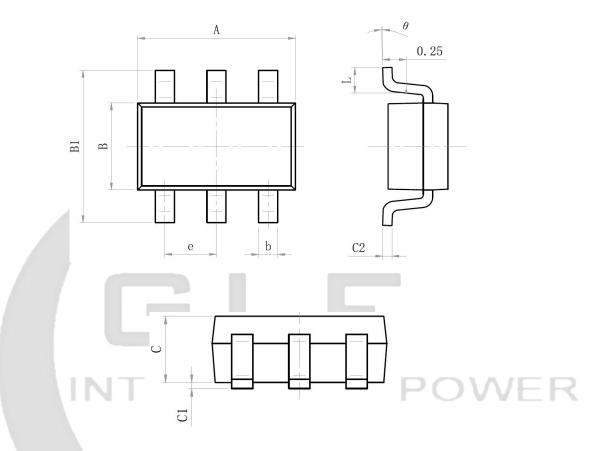
The GLF4028 also prevents the reverse current from the output voltage when both switches are turned off at EN = SEL = 0 V.

Board Layout

All traces should be as short as possible to minimize parasitic inductance effect. Wide traces for VIN, VOUT, and GND will help reduce signal degradation and parasitic effects during dynamic operations as well as improve the thermal performance at high load current.



PACKAGE OUTLINE

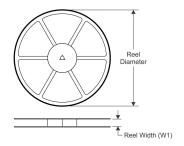


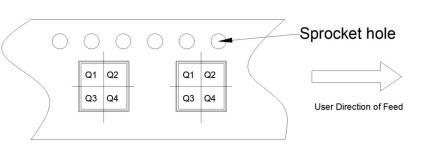
| Size Mark | Min(mm) | Max(mm) | Size Mark | Min(mm) | Max(mm) |
|--------------|---------|----------|--------------|---------|---------|
| А | 2.82 | 3.02 | С | 1.05 | 1.15 |
| е | 0.9 | 95 (BSC) | C1 | 0.03 | 0.15 |
| b | 0.28 | 0.45 | C2 | 0.12 | 0.23 |
| В | 1.50 | 1.70 | L | 0.35 | 0.55 |
| B1 | 2.60 | 3.00 | θ | 0° | 8° |



TAPE AND REEL INFORMATION

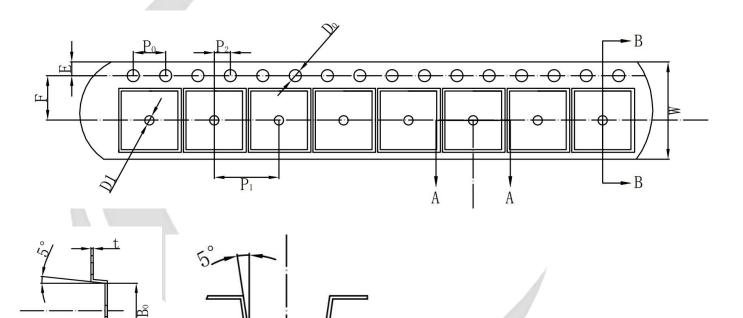
REEL DIMENSIONS





QUADRANT ASSIGNMENTS PIN 1 ORIENTATION TAPE

TAPE DIMENSIONS



| | | | | | | | - | - | | | |
|--------------|---------|------|------|-----------------------|------------------|------|------|------|----|---|------|
| Device | Package | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 | A0 | В0 | К0 | P1 | w | Pin1 |
| GLF4028-T2G7 | SOT23-6 | 6 | 3000 | 178 | 9 | 3.25 | 3.30 | 1.38 | 4 | 8 | Q3 |

Ao

Remark:

- A0: Dimension designed to accommodate the component width
- B0: Dimension designed to accommodate the component length
- C0: Dimension designed to accommodate the component thickness
- W: Overall width of the carrier tape

Ko

P1: Pitch between successive cavity centers



SPECIFICATION DEFINITIONS

| Document Type | Meaning | Product Status | | | |
|------------------------------|---|----------------|--|--|--|
| Target Specification | | | | | |
| Preliminary Specification | This is a draft version of a product specification. The specification is still under internal review and subject to change. GLF reserves the right to change the specification at any time without warning or notification. A preliminary specification in no way guarantees future production of the device in question. | Qualification | | | |
| Product Specification | This document represents the anticipated production performance characteristics of the device. | Production | | | |

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