YAMAR
EVB Manual

SIG102 Evaluation Board Manual

1. Overview

The SIG102 evaluation board (EVB) allows the operation of a sensors/actuators network of multiple SIG102 devices (EVBs) over the DC power line. The SIG102 eight I/O analog and digital pins are interfaced via the J2 I/O connector. One SIG102 operates as a master controls multiple SIG102 EVBs slaves over DC powerline using the UART/LIN protocol.
Figure 1 presents the EVB. This manual describes how to use and interface with the EVB. The SIG102 data sheet is a reference to this document.

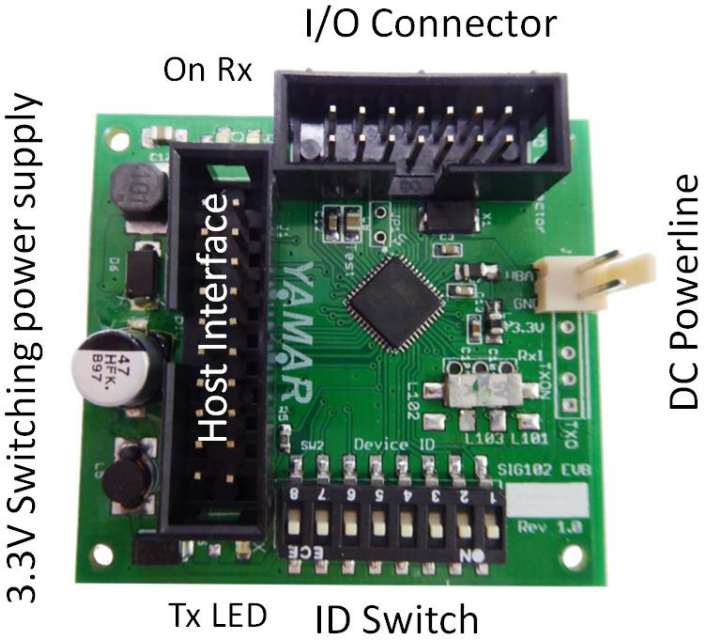

Figure 1 - SIG102 EVB

2. SIG102 EVB Description

2.1 Block Diagram Description

The SIG102 operates as an independent 8 I/O pins controller over the powerline. Read and Write commands to its eight I/O pins are executed when the command Id matches the EVB set Id. The EVB is also a physical communication layer of the UART/LIN protocol over DC powerlines at data rates of up to 115.2kbit/s. As so, the SIG102 may also be used as a new physical layer to the LIN protocol. The EVB can be connected directly to a UART/LIN controller (ECU) to operate as the network master through its TX and RX pins connected to HDI and HDO pins in the J1 Host connector. The EVB block diagram is depicted in Figure 2.

The EVB contains all the required hardware for device operation such as the device Id switch, J1 host connector (when operating as a master), J2 interface connector with the eight I/O pins, a line protection network, filter, 16MHz crystal, and a 3.3V switching power supply.

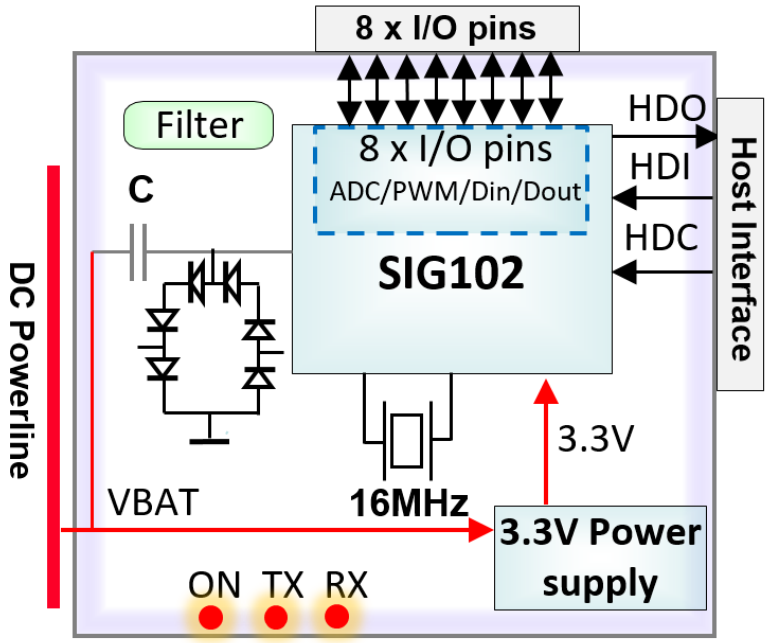

Figure 2 - SIG102 EVB Blocks

The received data signal from the DC powerline passes through a protection network into the SIG102 device. The SIG102 decodes the data and output it on the HDO pin of the Host interface connector. When the received message contains a command to the EVB set device Id, the SIG102 executes the command to/from its I/O pins.

At the transmitter side, each data from the ECU transferred to the SIG102 on the HDI pin. The SIG102 processes each data byte and modulate it on the selected carrier frequency on the TXO pin that drives the DC powerline via the protection network and coupling capacitor.

The built-in switching power supply provides the 3.3V voltage required for the SIG102 operation. The power supply operates in a wide input voltage range between 10V and 36V. The EVB current consumption is in the range of 30mA depending on the supply input voltage (powerline voltage).

The SIG102 internal registers, as described in the SIG102 datasheet determine the EVB operation conditions such as carrier frequency, bit rate, etc. When HDC signal low the data is directed as a command, allowing WRITE-REG and READ-REG to/from the SIG102 internal registers (see SIG102 datasheet).

2.2 Hardware features

- Noise robust DC powerline Communication
- Eight I/O pins, each configured as PWM output, ADC input, Digital Input, and Output
- UART/LIN host interfaces
- Selectable UART/LIN bitrate between 9.6Kbps to 115.2kbit/s
- 251 selectable operating frequencies (5MHz to 30MHz, 100kHz spacing)
- 10V to 36V operation using switching power supply
- Indication LEDs
- Small size EVB

2.3 EVB Connectors

2.3.1 J1 – Host Interface Connector

Table 1 – J1 Host interface connector

Pin Name	Direction	PU	Pin #	Pin Name	Direction	PU	Pin #
Reserved			1	Reserved			2
NRESET	I	PU	3	Reserved			4
INH	O		5	TXON	O		6
FREQ_SEL_0	I		7	FREQ_SEL_1	I		8
NAUTO_SLEEP	I		9	N_AUTO_FREQ_CHANGE	I		10
Reserved	O		11	NLOOPBACK	I	PU	12
NSLEEP	I	PU	13	HDC	I	PU	14
HDO	O		15	HDI	I	PU	16
VCC (3.3V) output	P		17	GND	P		18
GND	P		19	VBAT (powerline) * Requires R6 = 0 Ohm.	P		20

All input and output signals are compatible with 3.3V CMOS logic.

2.3.2 J2 – DC Power Line and test points

Table 2 J2 – DC Power Line and test points

Name	Pin #
TXO test-pin	1
TXON test-pin	2
RXI test-pin	3
3.3V output from the power supply	4
GND	5
VBAT DC powerline input (Max. 36V)	6

VBAT input connects the EVB to the DC powerline for communication and power supply.

Power supply requirements: 10V to 36V, minimum 150mA.

2.3.3 J3 – I/O Connector

Table 3 - J3 I/O Connector

Pin Name	Direction	PU	Pin #	Pin Name	Direction	PU	Pin #
Reserved	I/O		1	Reserved	I/O		2
IO-0	I/O		3	IO-1	I/O		4
IO-2	I/O		5	IO-3	I/O		6
IO-4	I/O		7	IO-5	I/O		8
IO-6	I/O		9	IO-7	I/O		10
VCC (3.3V) output	P		11	GND	P		12
GND	P		13	(*) VBat	P		14

All input and output signals are compatible with 3.3V CMOS logic.

2.3.4 Display LEDs

- TX LED - Indicates transmission.
- RX LED - Data output, indicates reception.
- ON LED - Indicates 3.3V power on.

2.4 Mechanical Data

The mechanical dimension is depicted in Figure 3.

2.4.1 Top Layer

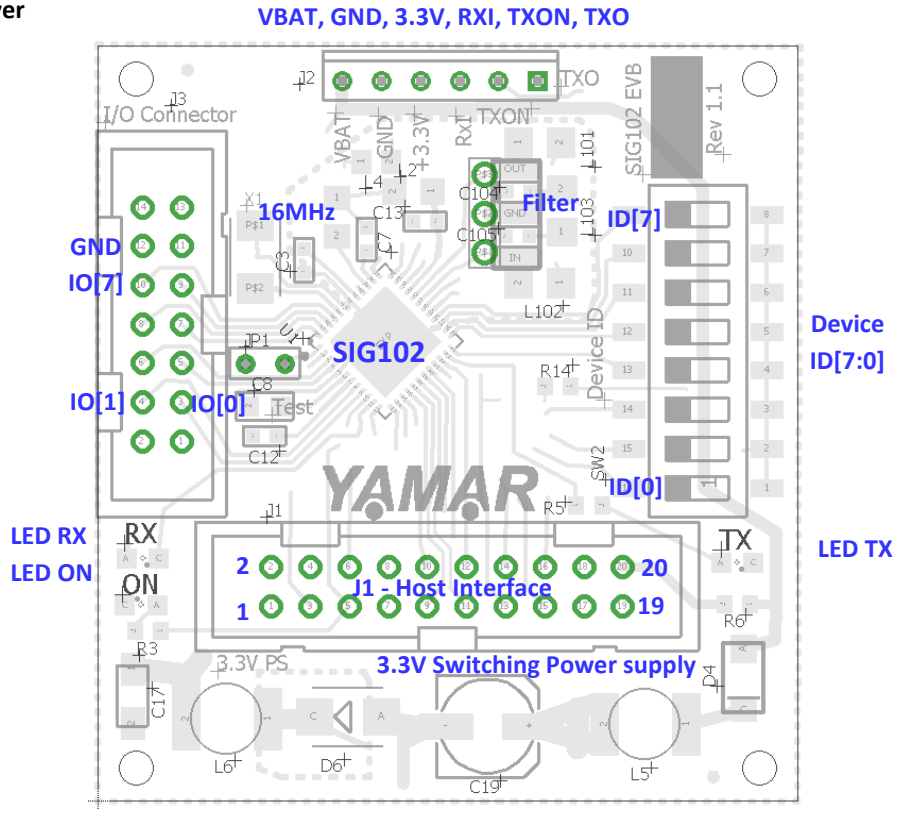

Figure 3 - EVB Top layer

2.4.2 Bottom Layer

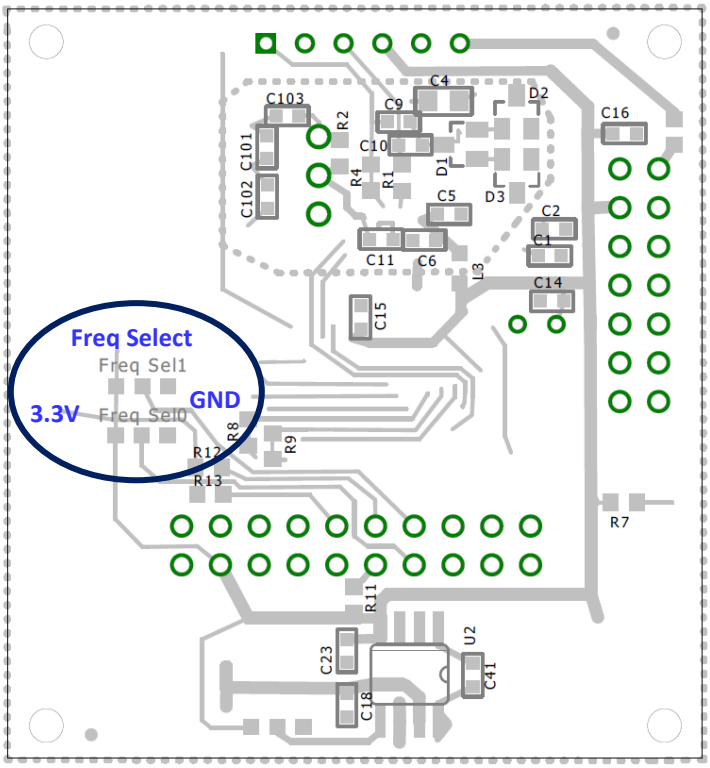

Figure 4 - EVB Bottom layer

3. EVB Operation

3.1 Configuration

The SIG102 mode of operation and its settings are configured at power-up, reset, and when Host writes into its internal register (command mode, using the HDC pin). See SIG102 datasheet for further configuration information.

3.2 Interfacing to SIG102 EVB

The SIG102 EVB is designed to interface directly to any UART/LIN controller or through a LIN transceiver.

The Host Interface connector J1 has all the signals required for the EVB proper operation. Three signals are essential; HDI, HDO, and GND (Data In, Data Out, and Ground). When designing the SIG102 for an operation other than the default setting (frequency, Sleep, I/O pins, etc.), the HDC pin has to be connected to any output pin of the UART/LIN controller for setting the SIG102 to the desired operation. Refer to SIG102 datasheet.

When using an external power supply instead/or in parallel to the EVB's power supply, it is recommended to add an inductor of at least 22uH in serial to the external power supply to avoid strong attenuation due to the power supply internal filtering capacitors.

3.3 Interfacing to UART/LIN Controller

The SIG102 interfaces directly to any uC UART/LIN I/O pins (3.3V logic) for UART/LIN communication protocol. In such a case the four pins as described in Table 4 should be used.

Table 4 – UART/LIN interface pins

SIG102	Controller	Description
HDI	**TX**	Data Input from the host controller.
HDC	**GPO**	Data/Command select input. When pulled down, the SIG102 enters command mode, enabling access to SIG102 internal registers.
HDO	**RX**	Data output to the host controller.
NLOOPBACK	**GPO**	Enable loopback of HDI to HDO pin. - When interfacing a UART port, the controller may disable/enable the loopback option. - When interfacing a LIN transceiver, loopback is disabled by keeping the pin floated (internal PU). - When interfacing a LIN controller, tie pin to GND. HDI loops back to HDO.

Figure 5 depicts a typical SIG102 to Controller UART/LIN interface connection.

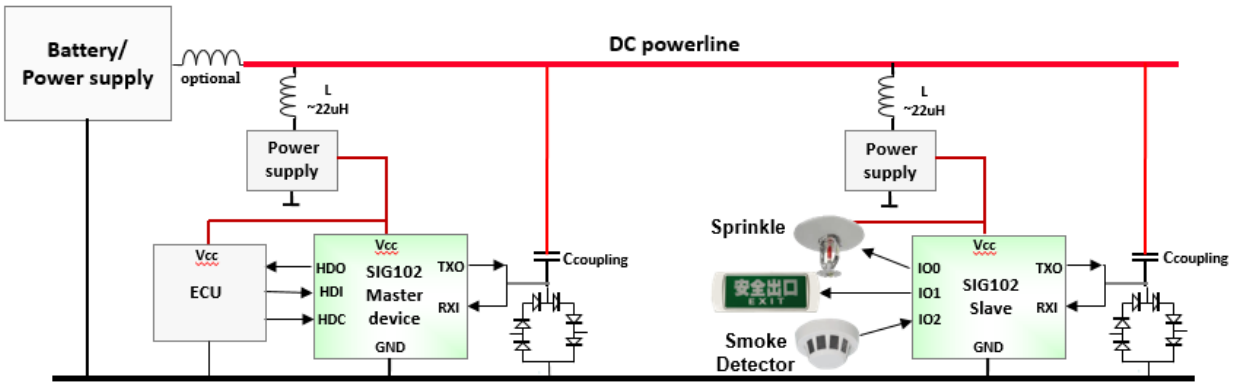

Figure 5 - Typical SIG102 to UART/LIN Controller interface

3.4 Interfacing to existing LIN module

When interfacing to a LIN module that has already a built-in LIN transceiver, an additional LIN transceiver is required to translate the signals to TX and RX 3.3V logic. The loopback between HDI and HDO pins has to be disabled. Keep NLOOPBACK pin floated. Figure 6 depicts a typical SIG102 to LIN transceiver interface connection.

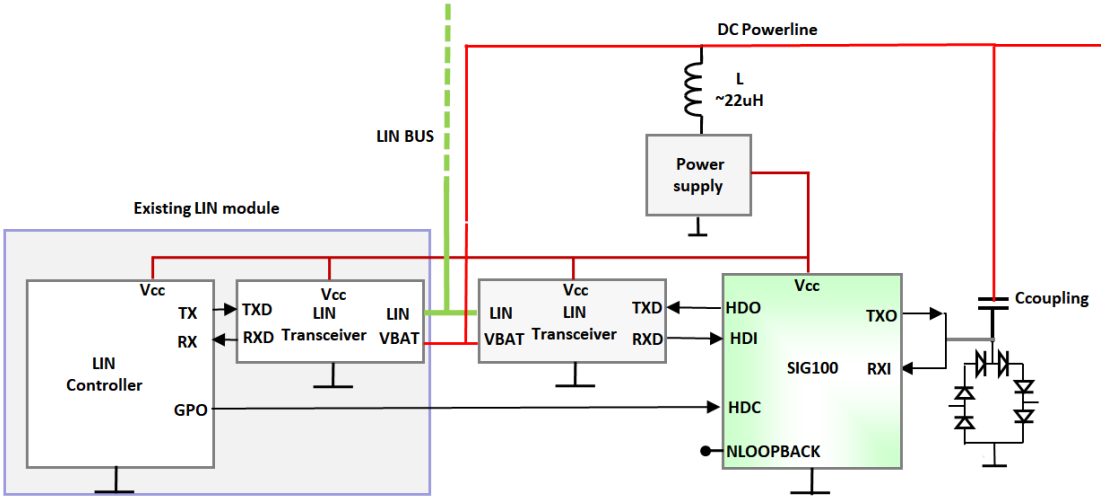

Figure 6 - Typical SIG102 to LIN transceiver interface

3.5 SIG102 EVB Test Environment

The SIG102 test environment contains EVB-Tester-board that sets the tested SIG102 EVB to its operating parameters. When operating as a transmitter it generates test messages transmitted over the powerline or via DC Powerline.

The PC Test program allows control of the eight I/O pins and activates the I/O pins of remote SIG102 EVBs.

A DC Powerline Attenuator can emulate the DC powerline with variable signal attenuation levels.

A second EVB operating as a receiver transfer the received data to a second EVB Tester that analyzes the received data or transfers it via its USB interface (when connected) to a PC for further analysis and display of the results.

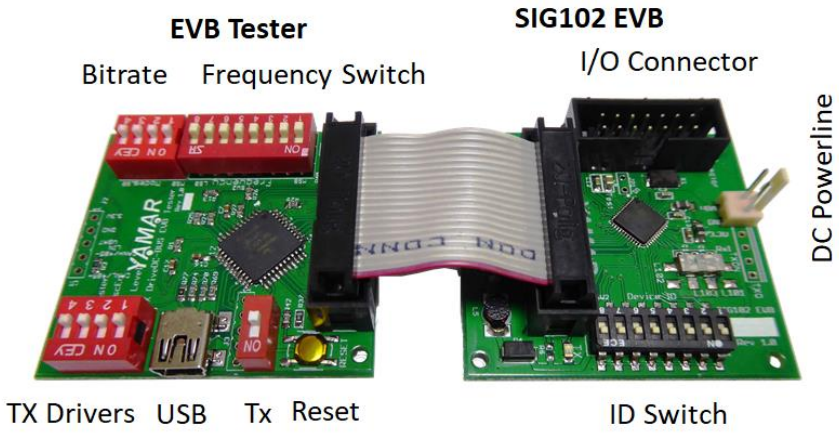

Figure 7 – EVB Tester and SIG102 EVB

I. PC to PC communication via the powerline using the USB interface built in the EVB tester.

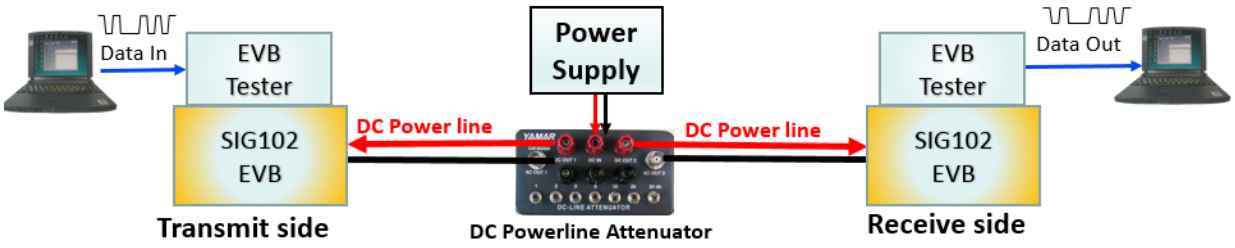

Figure 8 - PC to PC testing

II. TX test messages transmission from the EVB tester to a PC with a test program via the powerline.

Figure 9 - EVB Tester to PC testing

III. TX test messages transmission from EVB Tester to Rx EVB Tester that analyzes the received test messages and indicates the results with a LED.

Figure 10 - EVB Tester to EVB Tester

IV. TX powerline IOs control command from PC to remote SIG102 EVB.

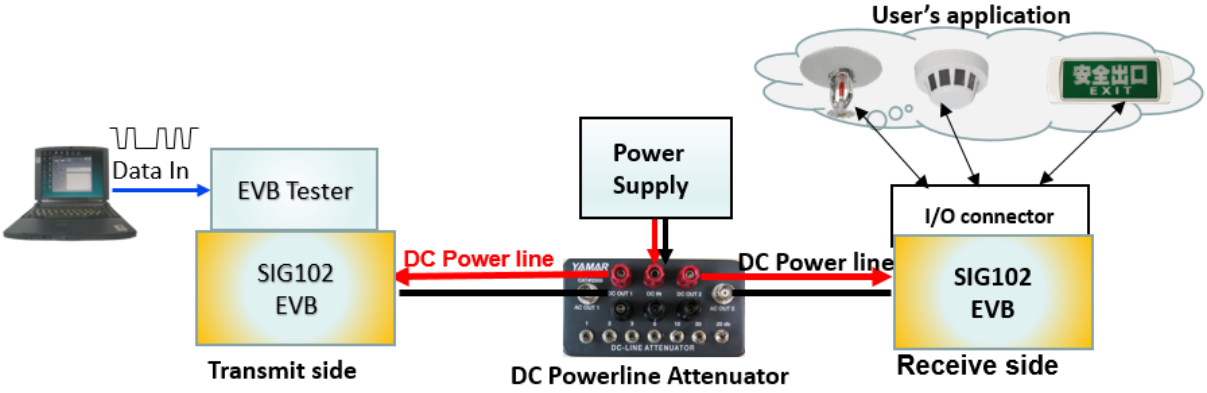

Figure 11 – PC to SIG102 EVBs IOs control

3.5.1 DC Powerline Attenuator

The DC-Powerline Attenuator is used for testing communication performance over the DC powerline in the lab. The attenuator allows adding attenuation (0 to 61dB) to the AC modulated signal over the DC power lines keeping the DC voltage level unchanged.

Figure 12 - DC Powerline attenuator

3.6 EVB Quick setup

- ✓ Connect the communication signals via J1 to the UART/LIN host.
- ✓ Connect I/O pins to the desired sensors and actuator signals via J2.
- ✓ Connect the EVBs to the DC powerline.
- ✓ Configure the SIG102 if required using the HDC pin.
- ✓ Transmit and receive data to and from SIG102 EVBs connected to the DC powerline.

4. EVB SIG102 schematic

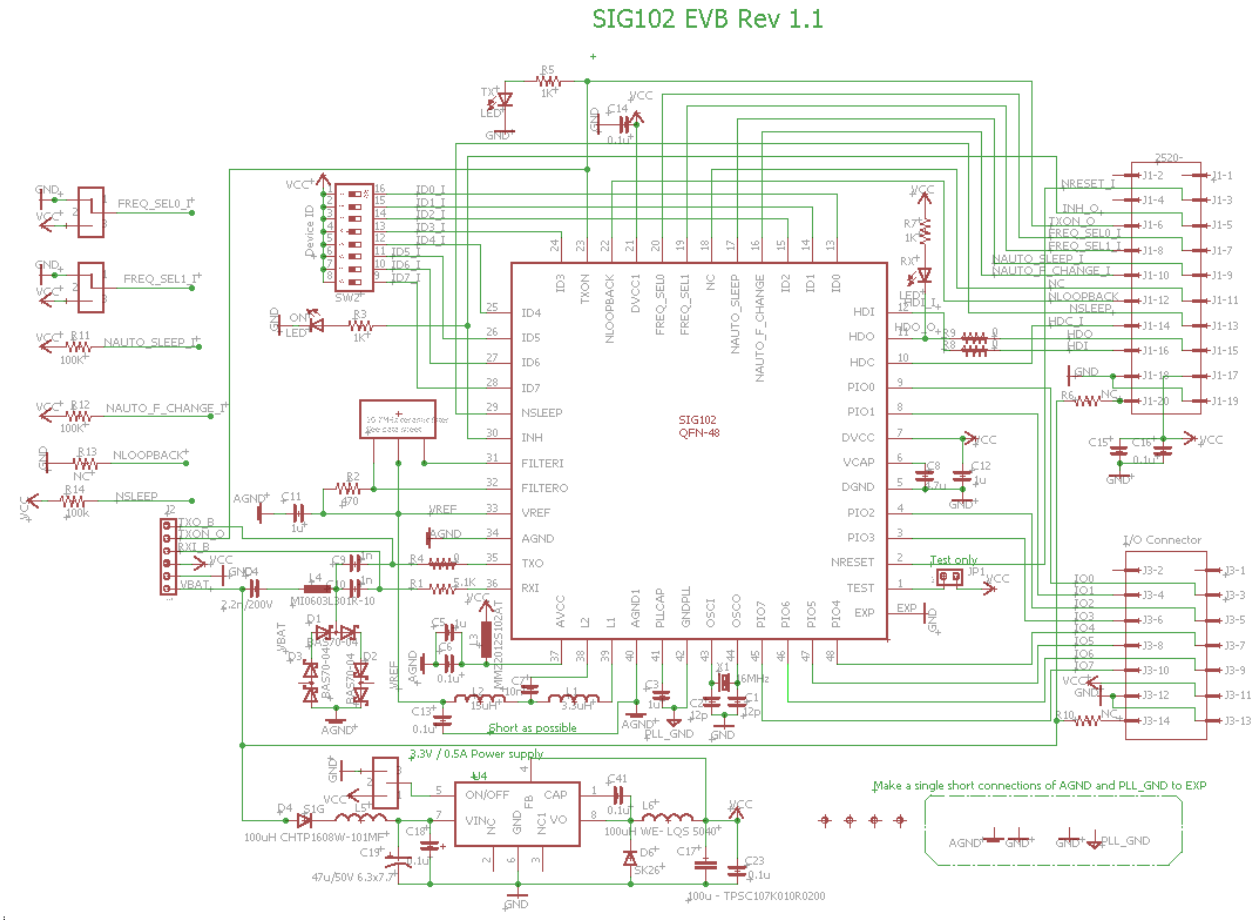

Figure 13 - SIG102 EVB circuitry

Revision History

Rev.	Date	Description
0.2	30/07/19	Initial version
0.3	09/09/19	Update schematics and text
0.4	25/11/19	Update Figures 1 and 10.
0.5	26/08/20	Editing.
0.6	15/11/20	Update Figure 13, C17 value to 2 x 47uF.
0.7	13/01/21	Editing.
0.8	15/10/21	Update Figures 3, 4, and 13.