Revision in SQJ402EP Datasheet from Rev. C to Rev. D

For further information, please contact your regional Vishay office.

CONTACT INFORMATION

Americas

Vishay Siliconix
2565 Junction Ave
-
San Jose CA United States 95134
Phone: 4089705799
Fax: 4089705799
business-americas@vishay.com

Europe

Vishay Electronic GmbH
Dr.-Felix-Zandman-Platz 1
-
Selb Germany 95100
Phone: 49-9287-71 0
Fax: 49-9287-70435
business-europe@vishay.com

Asia

Vishay Intertechnology Asia Pte. Ltd
37A Tampines Street 92 #07-01
-
Singapore Singapore 528886
Phone: 65 6788 6668
Fax: 65 6788 0988
business-asia@vishay.com

Description of Change: As part of Vishay Siliconix commitment to Quality, we would like to extend to you a courtesy advisory notification of a datasheet revision for SQJ402EP (Doc #67997 Rev D attached). There is no change to the materials or processes used in the manufacture of this part.

The changes per this Advisory reflect updates as
follows:

Typo correction on pages 1, 2, and 4 of datasheet.

Page1: Removed superscript “d” from Feature “AEC-Q101 Qualified”; superscript “b” from “Maximum Power Dissipation”; and note “d. Parametric verification ongoing”. Page2: Renamed superscript “e, f” to “d, e”; notes “e, f” to “d, e”; and notes “g, h, i” to a, b, c”. Page4: Corrected Tj labels of On Resistance vs Gate-to-Source Voltage chart that got swapped.

This advisory is for information only and there is no need for a response.

Reason for Change: Datasheet Revision

Expected Influence on Quality/Reliability/Performance: None

Part Numbers/Series/Families Affected: SQJ402EP-T1_BE3, SQJ402EP-T1_GE3, SQJ402EP-T2_BE3, SQJ402EP-T2_GE3,

Vishay Brand(S): Vishay Siliconix

Time Schedule:
Start Shipment Date: Mon Oct 2, 2023

Sample Availability: This is a datasheet revision only. There is no change to the materials or processes used in the manufacture of this part.

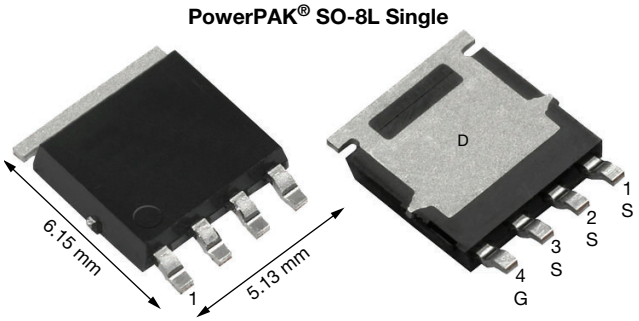
Product Identification: SQJ402EP-T1_BE3, SQJ402EP-T1_GE3, SQJ402EP-T2_BE3, SQJ402EP-T2_GE3

Qualification Data: N/A

Issued By: Vishay Siliconix, business-americas@vishay.com

Automotive N-Channel 100 V (D-S) 175 °C MOSFET

PowerPAK® SO-8L Single



Top View Bottom View

FEATURES

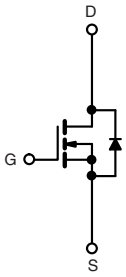
- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

AUTOMOTIVE GRADE

Pb-free

RoHS COMPLIANT

HALOGEN FREE



N-Channel MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	100
$R_{DS(on)}$ (Ω) at V_{GS} = 10 V	0.0110
$R_{DS(on)}$ (Ω) at V_{GS} = 4.5 V	0.0140
I_D (A)	32
Configuration	Single

ORDERING INFORMATION	
Package	PowerPAK SO-8L
Lead (Pb)-free and halogen-free	SQJ402EP (for detailed order number please see www.vishay.com/doc?79771)

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	100	V
Gate-source voltage		V_{GS}	± 20	
Continuous drain current [a]	T_C = 25 °C	I_D	32	A
	T_C = 125 °C		32	
Continuous source current (diode conduction) [a]		I_S	32	
Pulsed drain current [b]		I_{DM}	75	
Single pulse avalanche current	L = 0.1 mH	I_{AS}	31	
Single pulse avalanche energy		E_{AS}	48	mJ
Maximum power dissipation	T_C = 25 °C	P_D	83	W
	T_C = 125 °C		27	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) [d, e]			260	

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient	PCB mount [c]	R_{thJA}	65	°C/W
Junction-to-case (drain)		R_{thJC}	1.8	

Notes

a. Package limited
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %
c. When mounted on 1" square PCB (FR-4 material)
d. See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components

SPECIFICATIONS (T_C = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA		100	-	-	V
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		1.5	2.0	2.5	
Gate-source leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	V_{GS} = 0 V	V_{DS} = 100 V	-	-	1	µA
		V_{GS} = 0 V	V_{DS} = 100 V, T_J = 125 °C	-	-	50	
		V_{GS} = 0 V	V_{DS} = 100 V, T_J = 175 °C	-	-	150	
On-state drain current [a]	$I_{D(on)}$	V_{GS} = 10 V	V_{DS} ≥ 5 V	30	-	-	A
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 10.7 A	-	0.0090	0.0110	Ω
		V_{GS} = 10 V	I_D = 10.7 A, T_J = 125 °C	-	-	0.0170	
		V_{GS} = 10 V	I_D = 10.7 A, T_J = 175 °C	-	-	0.0210	
		V_{GS} = 4.5 V	I_D = 9.5 A	-	0.0115	0.0140	
Forward transconductance [b]	g_{fs}	V_{DS} = 15 V, I_D = 10.7 A		-	54	-	S
Dynamic [b]							
Input capacitance	C_{iss}	V_{GS} = 0 V	V_{DS} = 25 V, f = 1 MHz	-	1829	2286	pF
Output capacitance	C_{oss}			-	722	903	
Reverse transfer capacitance	C_{rss}			-	62	78	
Total gate charge [c]	Q_g	V_{GS} = 10 V	V_{DS} = 50 V, I_D = 10 A	-	34	51	nC
Gate-source charge [c]	Q_{gs}			-	6	-	
Gate-drain charge [c]	Q_{gd}			-	13	-	
Gate resistance	R_g	f = 1 MHz		0.65	1.39	2	Ω
Turn-on delay time [c]	$t_{d(on)}$	V_{DD} = 50 V, R_L = 5 Ω I_D ≅ 10 A, V_{GEN} = 10 V, R_g = 1 Ω		-	10	15	ns
Rise time [c]	t_r			-	10	15	
Turn-off delay time [c]	$t_{d(off)}$			-	27	40	
Fall time [c]	t_f			-	7	11	
Source-Drain Diode Ratings and Characteristics [b]							
Pulsed current [a]	I_{SM}			-	-	75	A
Forward voltage	V_{SD}	I_F = 7 A, V_{GS} = 0 V		-	0.77	1.2	V

Notes

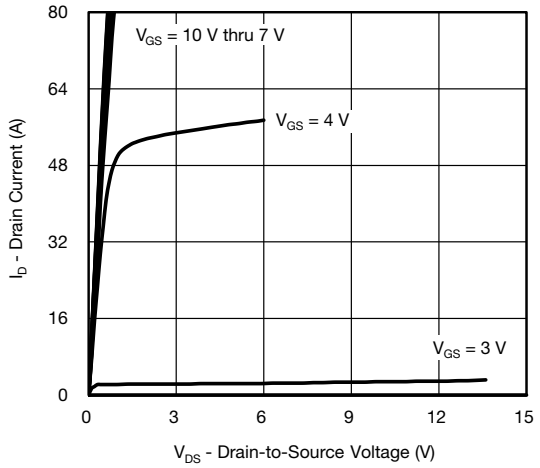
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %

b. Guaranteed by design, not subject to production testing

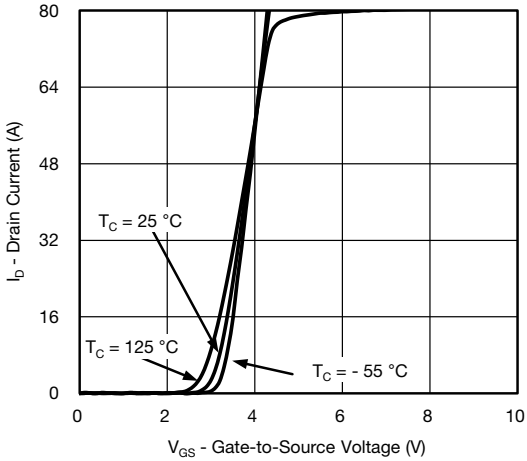
c. Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

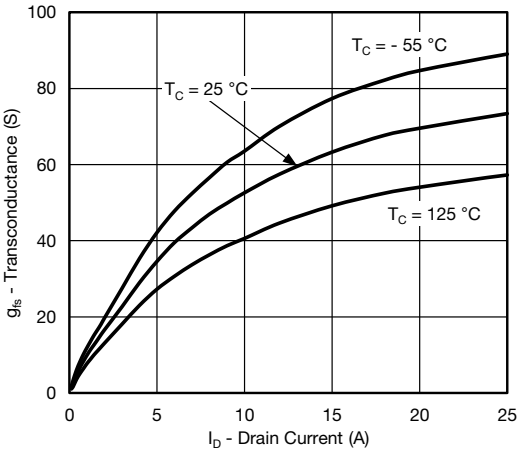
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



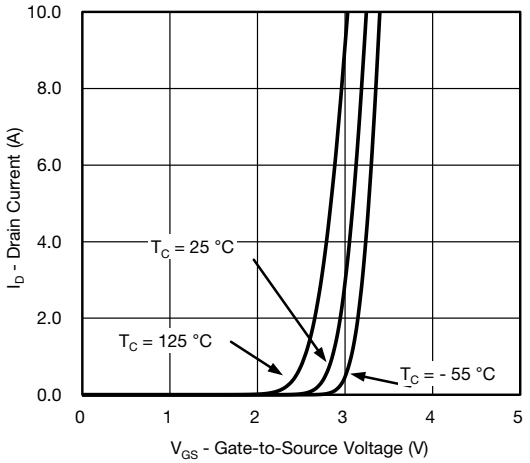
Output Characteristics



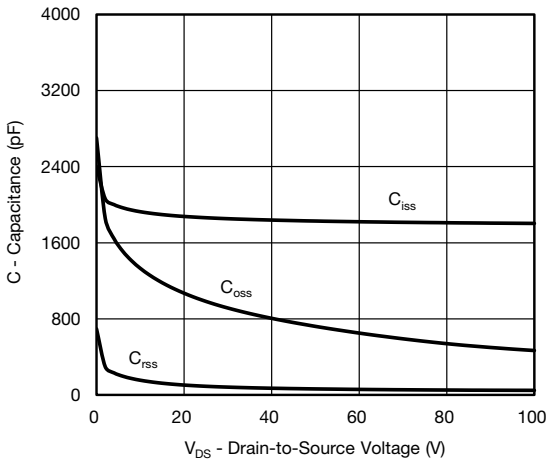
Transfer Characteristics



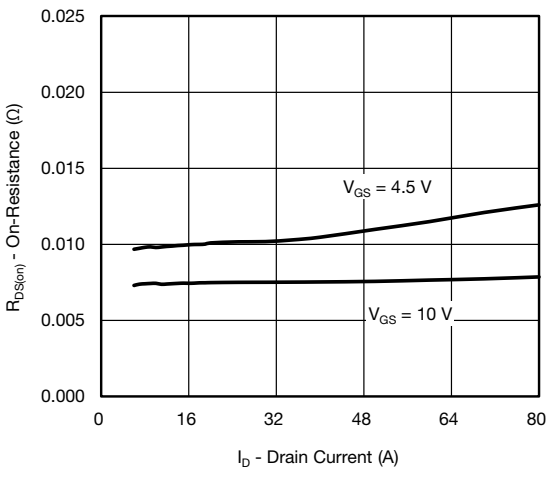
Transconductance



Transfer Characteristics

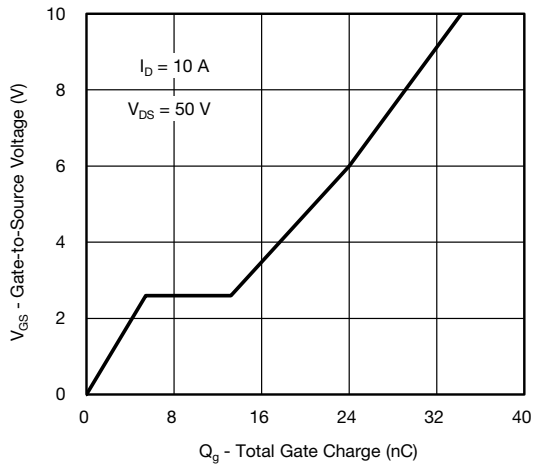


Capacitance

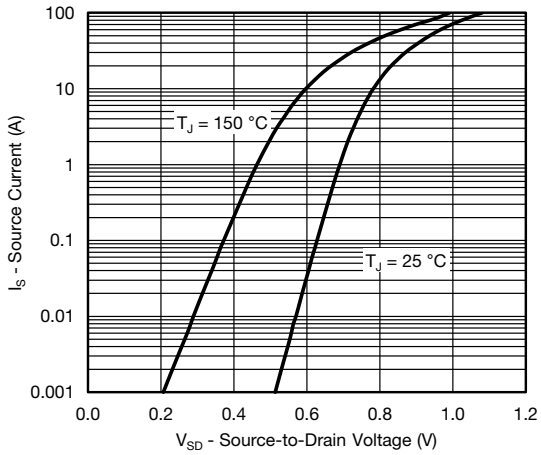


On-Resistance vs. Drain Current

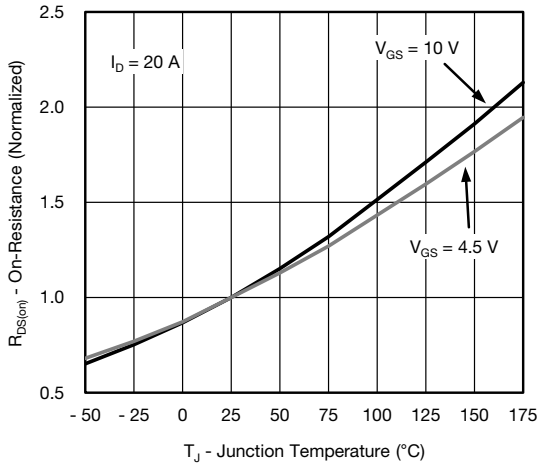
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



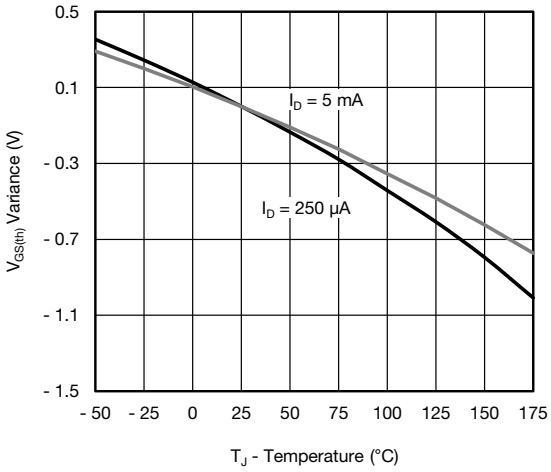
Gate Charge



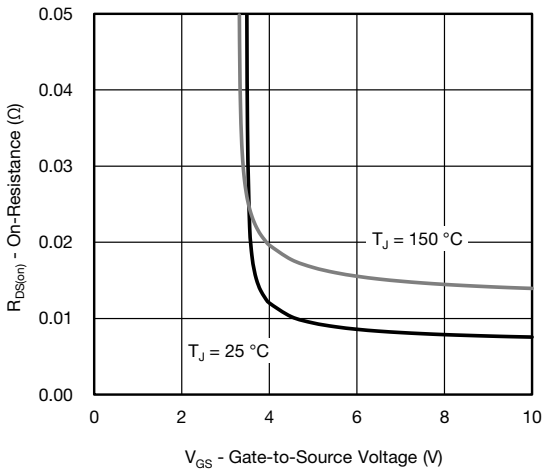
Source Drain Diode Forward Voltage



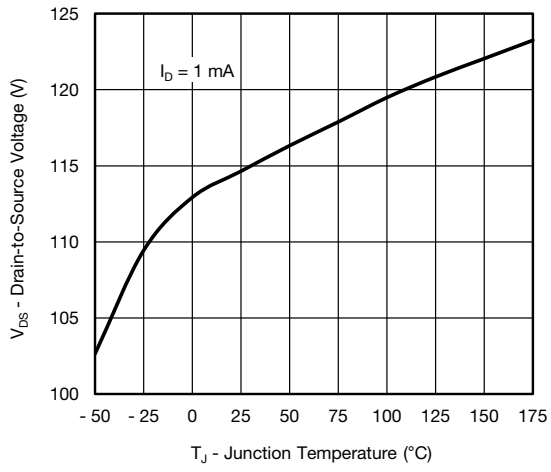
On-Resistance vs. Junction Temperature



Threshold Voltage

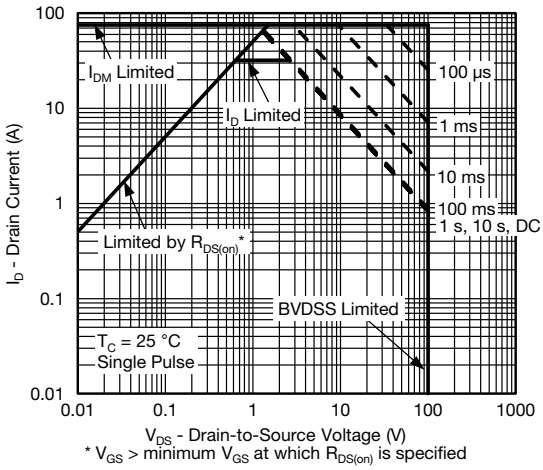


On-Resistance vs. Gate-to-Source Voltage

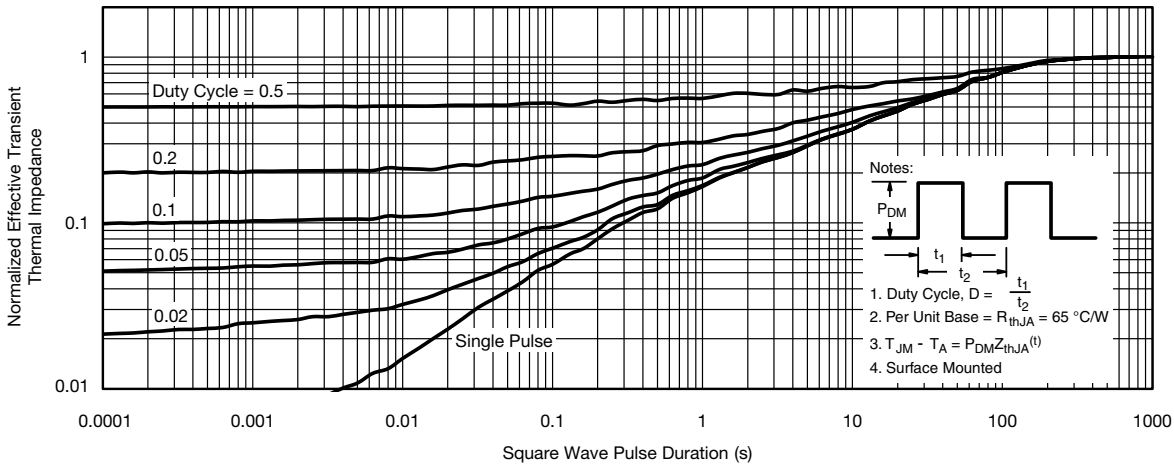


Drain Source Breakdown vs. Junction Temperature

THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)

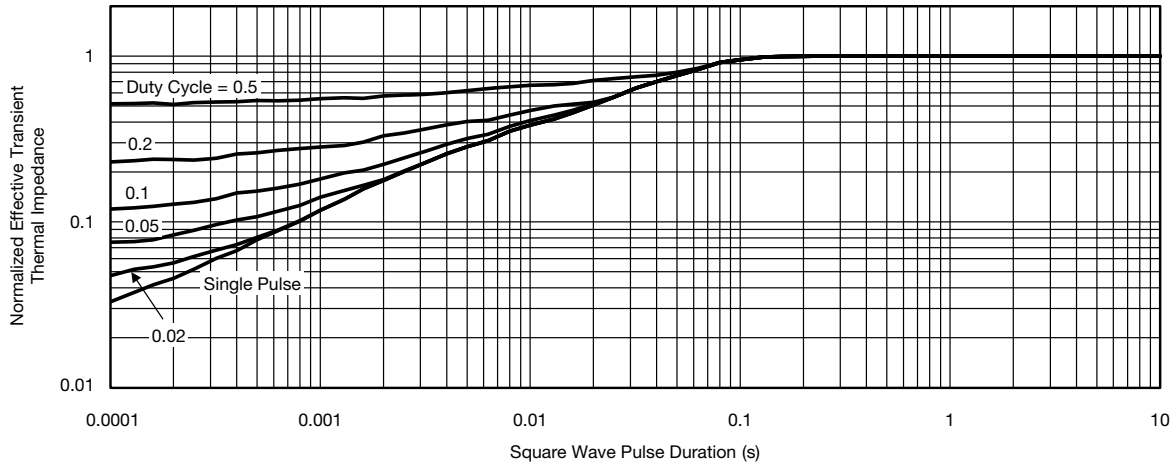


Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient

THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

Note

- The characteristics shown in the two graphs
  - Normalized transient thermal impedance junction-to-ambient (25 °C)
  - Normalized transient thermal impedance junction-to-case (25 °C)

  are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?67997.