USBULC6-2N4

Ultralow capacitance ESD protection for high speed interface

Features

- 2-line TVS diodes
- Ultralow capacitance 0.6 pF typ.
- 1.0 x 0.8 mm package
- 0.4 mm pitch
- Lead-free package

Benefits

- Flow-through layout
- Easy to implement
- Low profile: 0.55mm height max
- Very low PCB space: only 0.8 mm²

Complies with following standards

- IEC 61000-4-2 level 4:
  - 15 kV (air discharge)
  - 8 kV (contact discharge)

Applications

Where transient over-voltage protection in ESD sensitive equipment is required, such as:

- Computers
- Printers
- Communication systems
- Cellular phone handsets and accessories
- Video equipment

Description

The USBULC6-2N4 is a monolithic application specific discrete device dedicated to ESD protection of high speed data buses.

The device is available in the µQFN-4L package.

µQFN-4L

Figure 1. Configuration (top view)

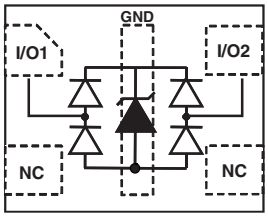
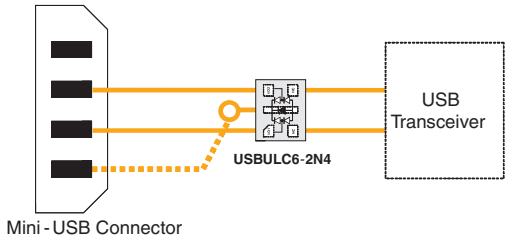


Figure 2. Application diagram



1 Characteristics

Table 1. Absolute maximum ratings T_{amb} = 25 °C

Symbol	Parameter	Value	Unit
V_{PP}	ESD discharge IEC 61000-4-2, level 4 Contact discharge Air discharge	 12 15	kV
I_{pp}	Peak pulse current (8/20 µs)	4	A
P_{pp}	Peak pulse power dissipation (8/20 µs)	50	W
T_j	Operating temperature range	-40 to + 150	°C
T_{stg}	Storage temperature range	-65 to +150	°C
T_L	Maximum lead temperature for soldering during 10 s	260	°C

Table 2. Electrical characteristics T_{amb} = 25 °C, otherwise specified

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	LV diode breakdown voltage	I_R = 1 mA	6			V
I_{RM}	LV diode leakage current	V_{RM} = 3 V			100	nA
C	LV diode input capacitance	V_R = 0 V, F= 240 MHz to 3 GHz Any I/O pin to ground		0.6	0.75	pF
V_{CL}	LV diode clamping voltage	I_{PP} = 1 A, t_p = 8/20 µs Any I/O pin to ground			10	V

Figure 3. Junction capacitance versus frequency (V_R = 0 V, typical values)

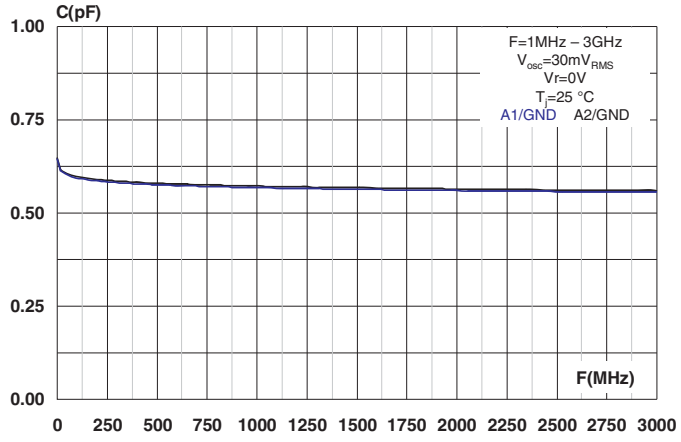


Figure 4. Variation of leakage current versus junction temperature (typical values)

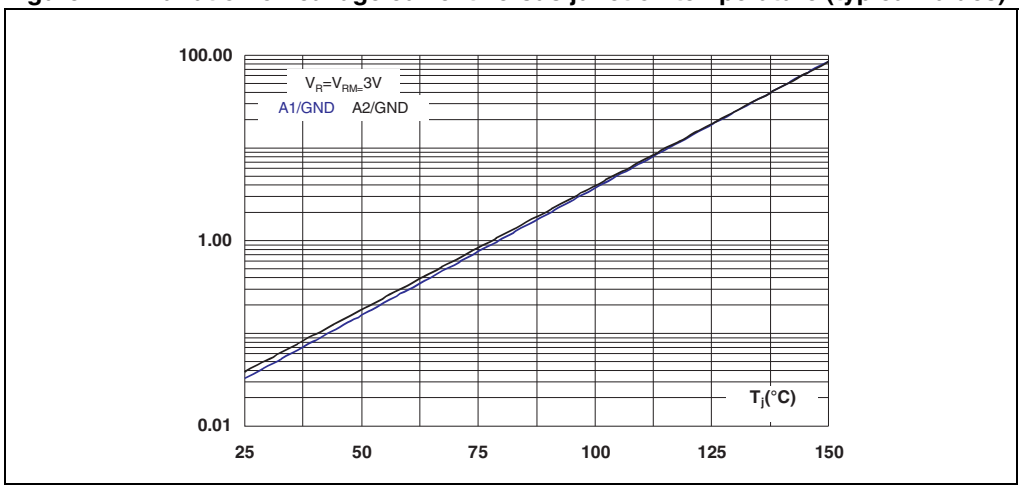


Figure 5. Attenuation measurement

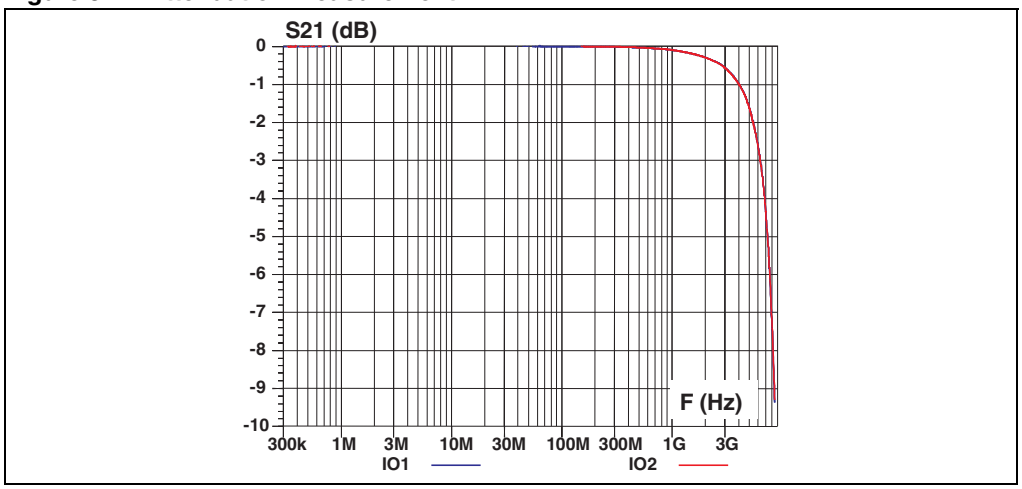


Figure 6. Eye diagram PCB only 400 mV amplitude, F = 480 Mbps

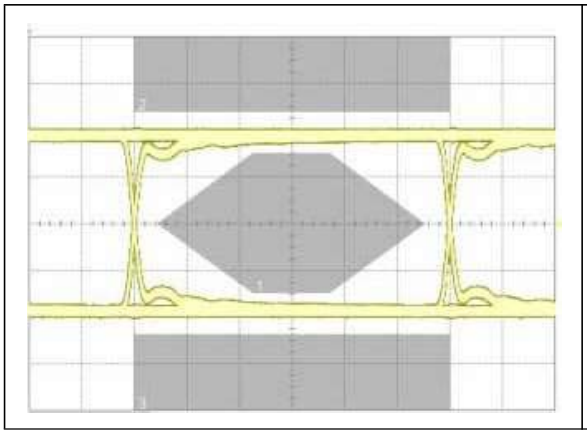


Figure 7. Eye diagram PCB + USBULC6-2N4 400 mV amplitude, F = 480 Mbps

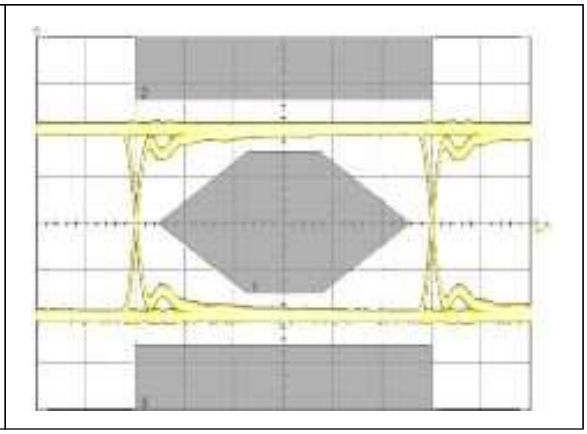


Figure 8. ESD response to IEC 61000-4-2 (+8 kV contact discharge) on one output $V_{(OUT)}$ and one input $V_{(IN)}$

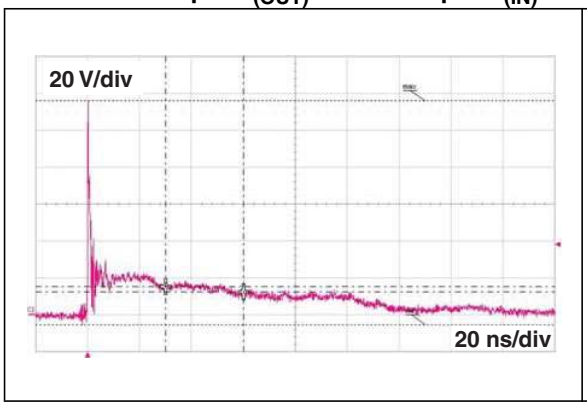
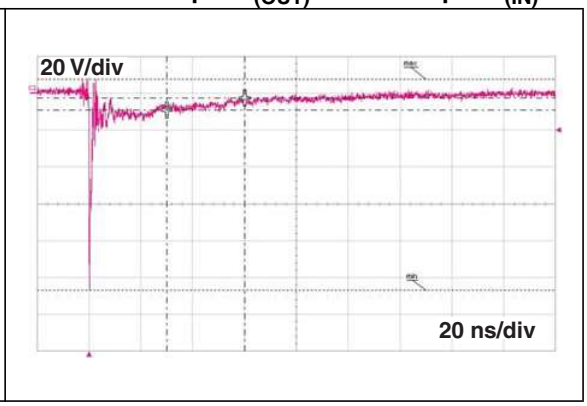
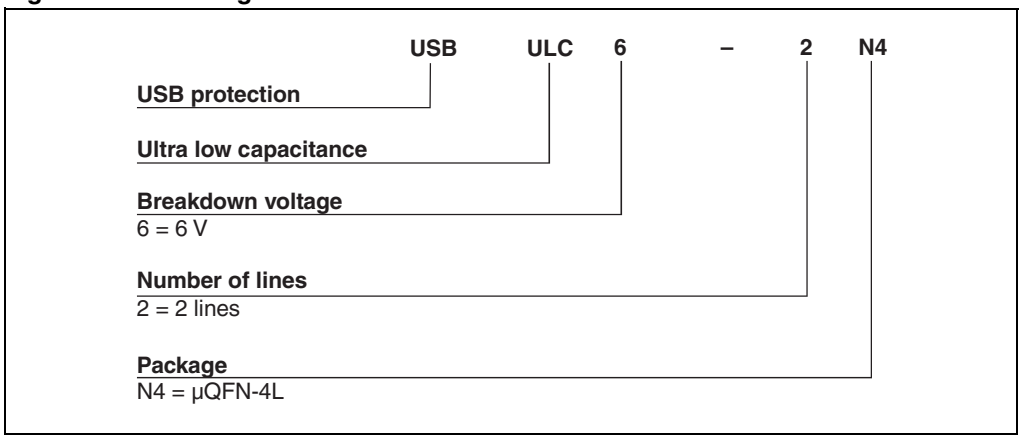


Figure 9. ESD response to IEC 61000-4-2 (-8 kV contact discharge) on one output $V_{(OUT)}$ and one input $V_{(IN)}$



2 Ordering information scheme

Figure 10. Ordering information scheme

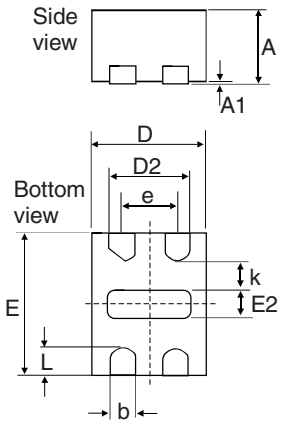


3 Package information

- Epoxy meets UL94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 3. µQFN-4L dimensions



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.45	0.50	0.55	0.018	0.020	0.022
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.15	0.20	0.25	0.006	0.008	0.010
D	0.75	0.80	0.85	0.030	0.031	0.033
D2	0.55	0.6	0.65	0.022	0.024	0.026
e	0.35	0.40	0.45	0.014	0.016	0.018
E	0.95	1.00	1.05	0.037	0.039	0.041
E2	0.15	0.20	0.25	0.006	0.008	0.010
k	0.17	0.20	0.23	0.007	0.008	0.009
L	0.15	0.20	0.25	0.006	0.008	0.010

Figure 11. Footprint recommendations (dimensions in mm)

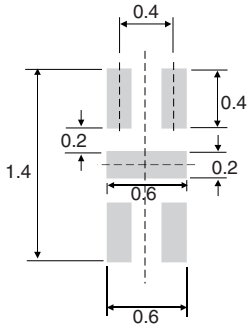
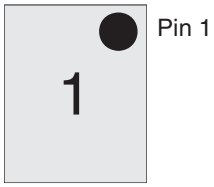
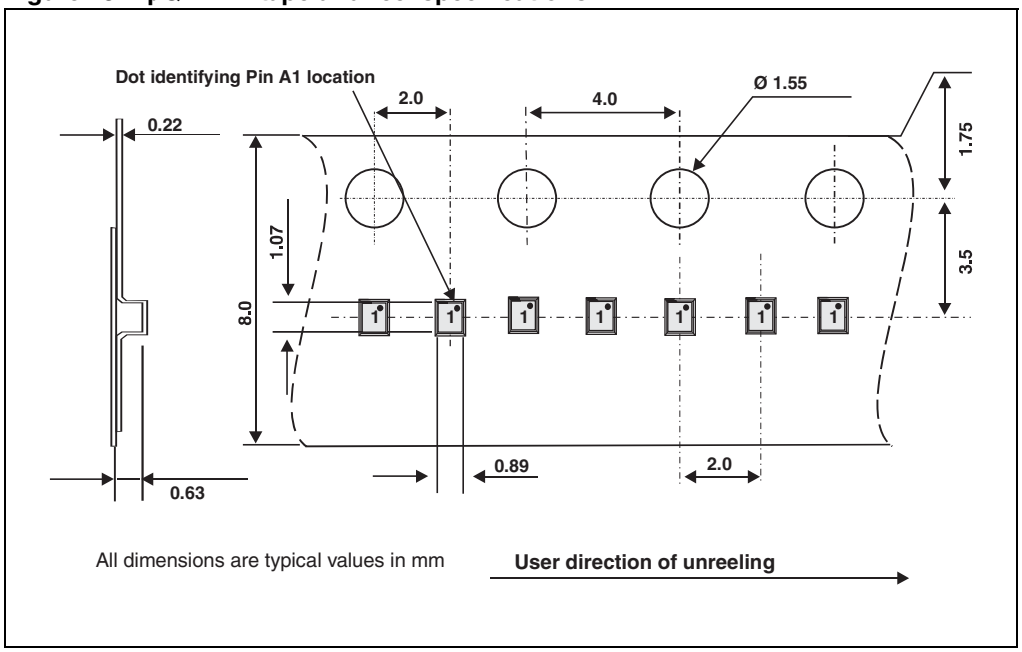


Figure 12. Marking



Note: Product marking may be rotated by 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

Figure 13. µQFN-4L tape and reel specifications

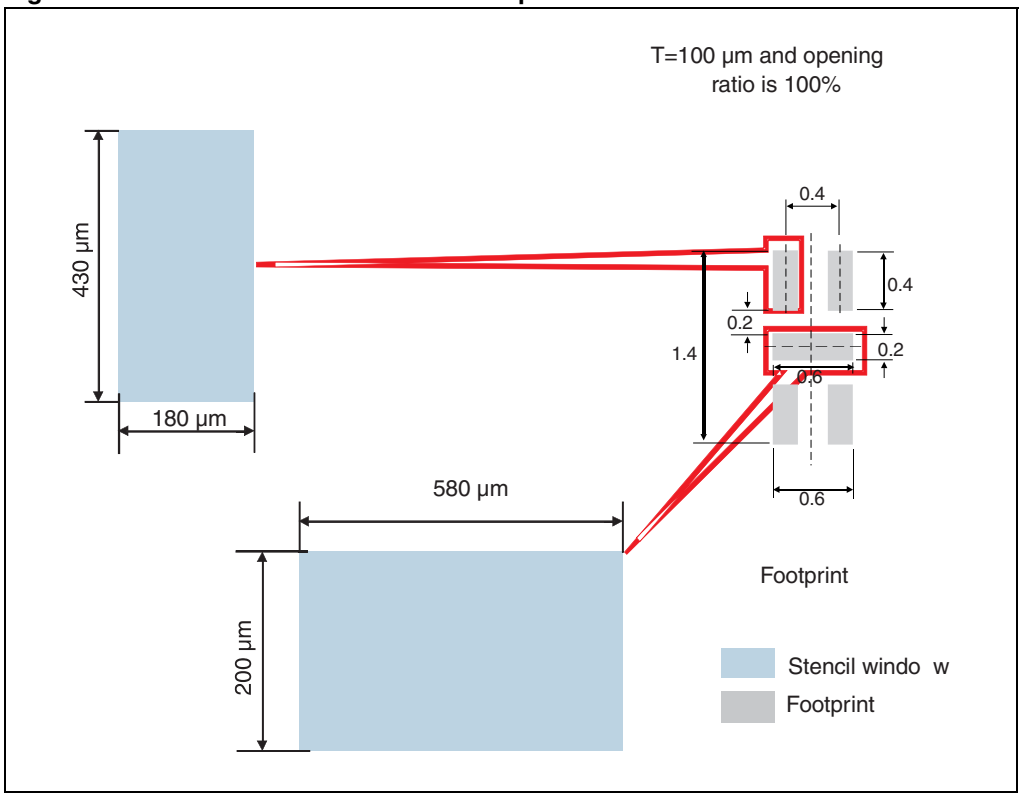


4 Recommendation on PCB assembly

4.1 Stencil opening design

1. Reference design
   a) Stencil opening thickness: 100 µm
   b) Stencil opening for central exposed pad: Opening to footprint ratio is 50%.
   c) Stencil opening for leads: Opening to footprint ratio is 90%.

Figure 14. Recommended stencil window position



4.2 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Solder paste with fine particles: powder particle size is 20-45 µm.

4.3 Placement

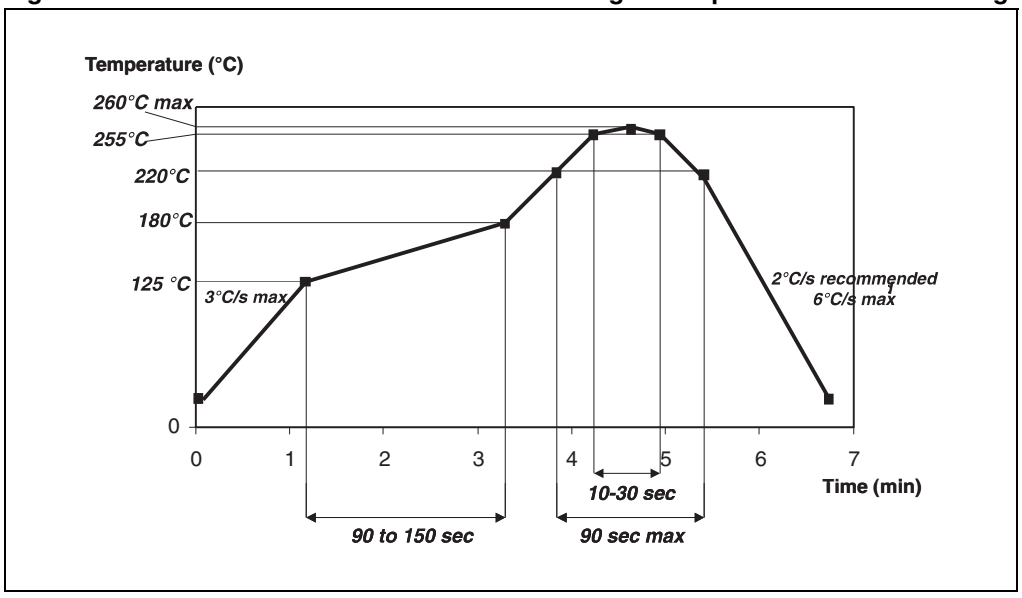
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

4.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

4.5 Reflow profile

Figure 15. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

5 Ordering information

Table 4. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
USBULC6-2N4	1(1)	µQFN	1.17 mg	10000	Tape and reel (7”)

1. The marking can be rotated by 90° to differentiate assembly location

6 Revision history

Table 5. Document revision history

Date	Revision	Changes
14-Sep-2011	1	Initial release.

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