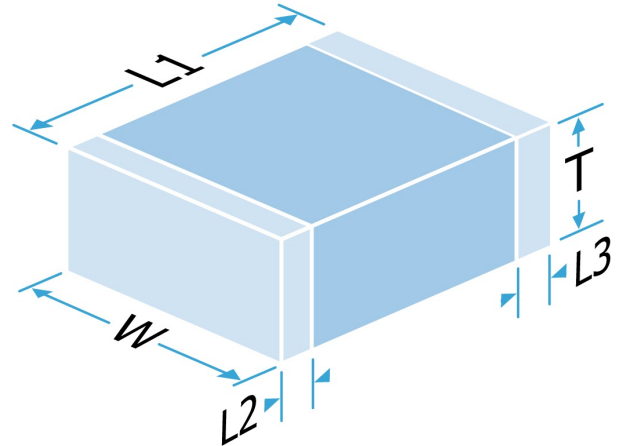


Part Number: 0805N102J101NT

Description: 0805 100Vdc 1.0nF ±5% C0G/NP0 (1B) - Contains Lead

A range of C0G/NP0 MLC capacitors to suit a variety of applications. Available in a wide selection of chip sizes, working voltages and termination options, including FlexiCap™, the world's first commercially available flexible termination.

Suffix code PXX or PX mandates the use of precious metal electrode (PME) materials. This may incur additional costs.



Mechanical Specification

Size Code	0805
Length (L1) in mm (")	2.0 ± 0.20 (0.079 ± 0.008)
Width (W) in mm (")	1.25 ± 0.20 (0.049 ± 0.008)
Thickness (T) in mm (")	1.37 Max (0.054 Max)
Minimum Termination Band (L2,L3) in mm (")	0.25 (0.010)
Maximum Termination Band (L2,L3) in mm (")	0.75 (0.030)
Termination Material	Nickel Barrier, Sn Plated Solder (RoHS compliant)
Solderability	Per MIL-STD-202, Method 208
Packaging	Tape and Reel, 3000 per reel
Conformal Coating	

General Electrical Specification

Rated Voltage	100Vdc
Nominal Capacitance Value	1.0nF
Capacitance Tolerance	±5%
Tangent of Loss Angle (Tan δ)	≤0.0015
Capacitance and Tan δ Test Conditions	1.0Vrms @ 1MHz
Voltage Proof	250Vdc
(Voltage applied for 5 secs max. @ 50mA max. charge current)	
Min Insulation Resistance (IR)	100.00GOhm @ 100Vdc
Dielectric Classification	C0G/NP0 (1B) - Contains Lead
Rated Temperature Range	-55°C / +125°C
Maximum Capacitance Change over Temperature Range	No DC Voltage 0±30ppm/°C Rated DC Voltage -
Climatic Category (IEC)	-
Ageing Characteristic	Zero

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Data is correct to the best of our knowledge, errors and omissions excepted.

Date: Tuesday, October 03, 2023

20231003 181313314UTC

Multilayer Ceramic Chip Capacitor

Part Number: 0805N102J101NT

Description: 0805 100Vdc 1.0nF ±5% C0G/NP0 (1B) - Contains Lead

Environmental

RoHS Compliant to 2011/65/EC as amended by 2015/863/EU
REACH Compliant
California Proposition 65

Non Compliant
Contains 1 to 8% w/w Lead Titanium Oxide (PbTiO₃, CAS 12060-00-3)
No exposure risk

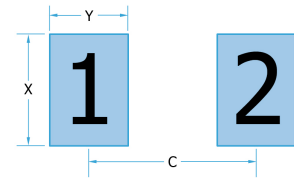
Board Layout

Knowles' conventional 2-terminal chip capacitors can generally be mounted using pad designs in accordance with international specification IPC-7351, Generic Requirements for Surface Mount Design and Land Pattern Standards, but there are some other factors that have been shown to reduce mechanical stress, such as reducing the pad width to less than the chip width. In addition, the position of the chip on the board should be considered.

Some high voltage parts may require modifications to the board layout and/or the addition of a conformal coating to prevent flashover. Refer to application note AN0043 for further information.

IPC-7351 pad design

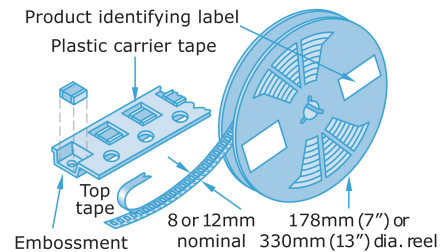
	0805	
C	1.80mm	0.071"
Y	1.15mm	0.045"
X	1.45mm	0.057"



Packaging

Tape packaging information for tape-and-reel parts:

Tape and reel packing of surface mounting chip capacitors for automatic placement are in accordance with IEC60286-3.



Soldering

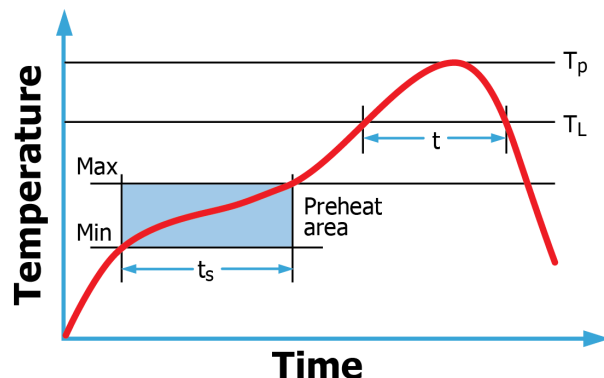
Reflow solder in accordance with IPC-A-610. Recommended reflow profile as laid down in IPC/JEDEC J-STD-020.

Wave soldering is also possible, but care must be taken for case sizes 1210 and larger and component thickness >1.0mm. Trials are encouraged.

Hand soldering is not recommended and can lead to component damage through thermal shock.

PdAg terminations are primarily intended for conductive epoxy attachment - they may be suitable for soldering but trials are recommended.

Application notes with mounting and handling guidance are available on request.



Compex

DLI

Johanson MFG

Novacap

Syfer

Voltronics

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Date: Tuesday, October 03, 2023

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