ATP I-Temp NVMe pSLC PCIe Gen3 M.2 2280 SSD (HW PLP) N750Pi

Datasheet

Version 1.0

PLP P/N
AF40GSAJA-8BAIP
AF80GSAJA-8BAIP
AF160GSAJA-8BBIP
AF320GSAJA-8BBIP

ATP I-Temp pSLC NVMe M.2 2280 SSD

Product Specification

- Capacities:
  - 40GB, 80GB, 160GB, 320GB
- Form Factors:
  - M.2 2280-D2-M
- Thickness:
  - Up to 3.5mm
- Weight:
  - <10 grams
- PCIe Gen3 x4 performance
  - Sequential Read: Up to 3,150 MB/s
  - Sequential Write: Up to 2,670 MB/s:
- Read and Write IOPS (QD32)
  - Random 4K Reads: Up to 147,789 IOPS
  - Random 4K Writes: Up to 114,227 IOPS
- LDPC (Low Density Parity Check) ECC algorithm
- End-to-End Data Path Protection
- Compliant with PCI Express Specification Rev.3.1a
- Compliant with PCIe M.2 Specification V1.1
- Compliant with NVMe Express Specification Rev.1.3b
- Support
  - SMART command set support
  - TRIM command
  - Global wear-leveling
  - Thermal throttling mechanism
- Power
  - 3.3V Input Power
- Temperature
  - Operating: -40°C to 85°C
  - Non-Operating: -40°C to 85°C
- Reliability
  - MTBF (Mean Time Between Failure): 2,000,000 hours
  - Shock (Non-operating): Half Sine 1,500G /0.5ms
  - Vibration (Non-operating): Sine 16.4G /10~2000Hz
  - Data Retention (@30°C): 5 Years (with 10% P/E cycle); 1 year (with 100% P/E cycle)
- Endurance (TBW in Sequential Write)
  - 40GB: 2,000 TB
  - 80GB: 4,000 TB
  - 160GB: 8,000 TB
  - 320GB: 16,000 TB
- Certifications and Declarations
  - CE
  - FCC
  - BSMI
  - -UKCA
- Product Ecological Compliance
  - RoHS
  - REACH

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Revision History

Date	Version	Changes compared to previous issue
Dec. 6th, 2021	1.0	- First release

1.0 Product Specification

1.1 Product Image

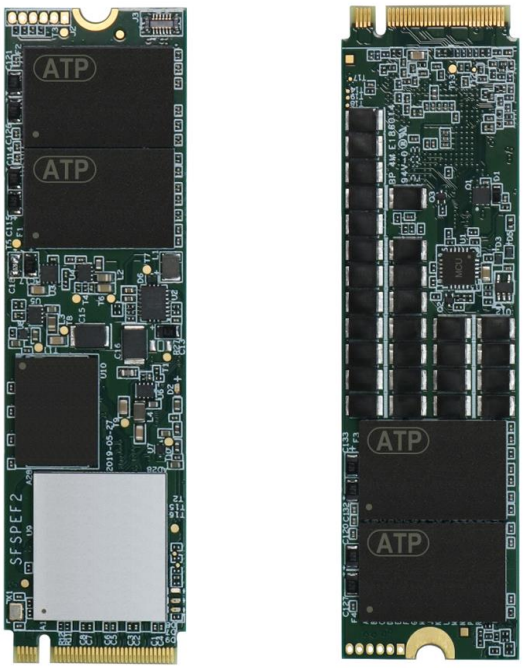


Figure 1-1: ATP Product Image (For Reference, PLP model)

1.2 Capacity

2 Table 1-2: Capacity Settings

Capacity	LBA
40GB	78,161,328
80GB	156,301,488
160GB	312,581,808
320GB	625,142,448

Note:

1. Sector size is 512 bytes
2. LBA counts are based on IDEMA (LBA1-03) standard

1.3 Environment Specifications

Table 1-3-1: Environment Specification

Type		Standard
Temperature	Operating	-40˚C to 85˚C
	Non-Operating	-40˚C to 85˚C
Relative Humidity	Operating	8% to 95%, noncondensing
	Non-Operating	8% to 93%, noncondensing
Altitude	Operating	80,000 feet Max.
	Non-Operating	80,000 feet Max.
Vibration	Non-Operating	Sine 16.4G, 10~2000Hz
Shock	Non-Operating	Half sine 1500G/0.5ms

Note: The environment temperature specification is based on ATP internal reliability test condition under +85˚C /-40˚C of sustaining burn-in temperature.

1.4 Reliability

Table1-4: Reliability

Type	Value
MTBF (@ 25˚C) [1]	>2,000,000 hours
Data Retention (@ 30˚C)[2]	5 years (with 10% P/E cycle); 1 year (with 100% P/E cycle)

Notes:

1. The Mean Time between Failures (MTBF) is calculated using a prediction methodology, Telcordia SR-332, which based on reliability data of the individual components in drive. It assumes nominal voltage, with all other parameters within specified range.
2. Data retention value may vary across different temperature range and is experimental result to be used for reference.

1.5 Electrical Characteristics

Table 1-5-1: Supply Power

Parameter	Symbol	Min	Typ.	Max	Unit	Remark
Supply voltage	V_{CC}	3.15	3.3	3.45	V	

Table 1-5-2: Power Consumption Measurement

40GB

Parameter	Symbol	Min	Typ.	Max	Unit	Remark
Sustained write power	P_W	-	2.4	2.9	W	RMS value
Sustained read power	P_R	-	2.7	3.1	W	RMS value
Idle power	P_S	-	0.8	0.9	W	RMS value

80GB

Parameter	Symbol	Min	Typ.	Max	Unit	Remark
Sustained write power	P_W	-	2.8	4.2	W	RMS value
Sustained read power	P_R	-	2.8	4.7	W	RMS value
Idle power	P_S	-	0.8	1.7	W	RMS value

160GB

Parameter	Symbol	Min	Typ.	Max	Unit	Remark
Sustained write power	P_W	-	3.1	5.2	W	RMS value
Sustained read power	P_R	-	3.3	4.6	W	RMS value
Idle power	P_S	-	0.8	1.7	W	RMS value

320GB

Parameter	Symbol	Min	Typ.	Max	Unit	Remark
Sustained write power	P_W	-	3.2	6.8	W	RMS value
Sustained read power	P_R	-	2.9	4.8	W	RMS value
Idle power	P_S	-	0.8	1.7	W	RMS value

Notes:

1. All power measured is under room temperature and using PCIe interface.
2. Sequential power measured under 100% read mode or 100% write mode with 1023KB data transfers.

1.6 IOPS

Table 1-6: IOPS (QD32) (Up to)

Capacity	4K Random Read IOPS (QD32)	4K Random Write IOPS (QD32)
40GB	108,288	107,776
80GB	147,789	111,770
160GB	147,558	114,227
320GB	142,797	110,182

Notes:

1. IOPS may vary by application/system usage
2. IOPS is calculated by dividing capacity by (4K QD32 testing result)/4x1024
3. The testing is assumed under clean state and done in room temperature

1.7 Maximum Read/Write Performance

Table 1-7: Performance (Up to)

Type	Capacity	Sequential Read	Sequential Write
Crystal Disk Mark	40GB	1,825 MB/s	570 MB/s
	80GB	3,145 MB/s	1,155 MB/s
	160GB	3,150 MB/s	2,340 MB/s
	320GB	3,145 MB/s	2,670 MB/s

Notes:

1. Performance may vary by application/system usage
2. Performance is measured by CrystalDiskMark in room temperature. The testing drive is assumed under clean state.

1.8 Write/Erase Endurance[1]

Table 1-8: TBW

Capacity	Random write[2]	Sequential write[3]
40GB	800 TB	2,000 TB
80GB	1600 TB	4,000 TB
160GB	3200 TB	8,000 TB
320GB	6400 TB	16,000 TB

1. Endurance can be predicted based on the usage conditions applied to the device, the internal NAND component cycles, the write amplification factor, and the wear leveling efficiency of the drive. TBW may vary depending on application, please contact ATP for TCO evaluation if specific usage type applies.
2. The random endurance calculation is based on JESD219A Enterprise workload.
3. The sequential write endurance calculation is based on pure sequential write at 128K transfer size to run in 4K alignment test pattern

2.0 Product Overview

2.1 Block Diagram

ATP SSD consists of below functional blocks. The advanced architecture is optimized to provide highest data reliability and transfer performance.

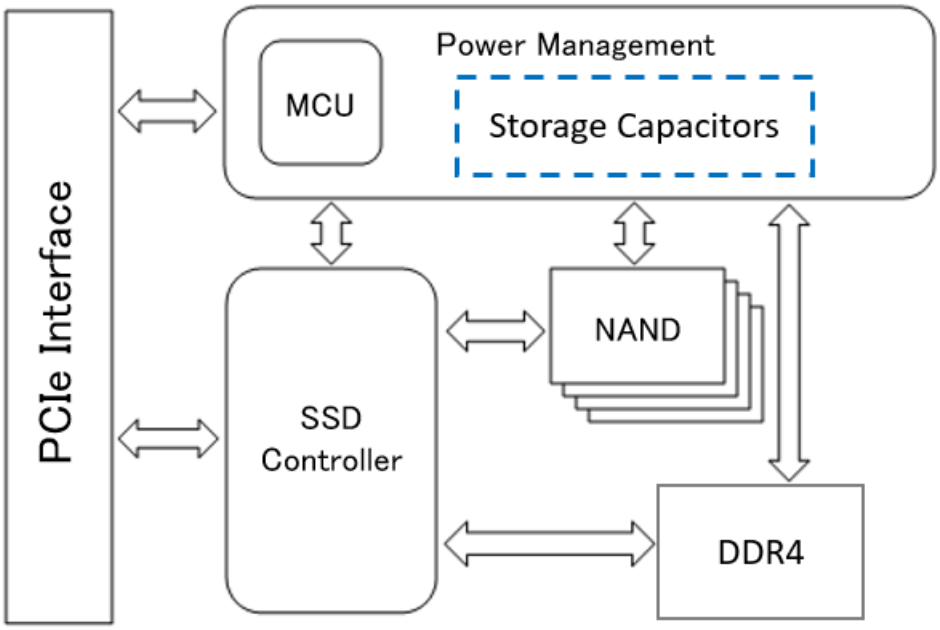


Figure 2-1: Block diagram for ATP NVMe SSD (PLP)

2.2 Power Protector --- Data Integrity Under Power-cycling

The unstable power conditions of most applications such as transportation, networking/ telecommunications and embedded systems run the risk of data loss and drive corruption during a sudden power failure.

A hardware design power protection is the ideal configuration for holding up power, ensuring a sufficient amount of reserve power during power abnormalities and minimizing the consequences of host re-designs for adding new features. During a sudden power failure, the abnormality is identified by a power loss detection circuit and activates the power protection mechanism. The device then draws power from power protection reservoir, where the reserve power is stored. The reserve power gives enough time for the flash device to conclude the last writing command without losing any data.

2.3 Auto-Refresh Technology --Data Integrity Protection

Over time the error bits accumulate to the threshold in the flash memory cell and eventually become uncorrectable despite the use of an ECC engine. In the traditional handling method, the data is moved to a different location in the flash memory; despite the corrupted data is beyond repaired before the transition.

The situation is worse in frequent read applications, such as navigation systems or OS boot-up devices. The map or operating system is preloaded into the storage media and there may be one time write and following by read operation only. Read disturbance is the result of electrical interference from multiple read operations in surrounding cells. After NAND flash accumulates 100,000 read cycles, uncorrectable ECC errors may occur in the affected pages which results in data failure in the same block.

To prevent data corruption, ATP memory product monitors the error bit levels in each read operation. When it reaches the preset threshold value, Auto-Refresh is activated by programming the data into another block before the data is corrupted. After the re-programming operation is completed, the controller reads the data and compares the data/parity to ensure data integrity.

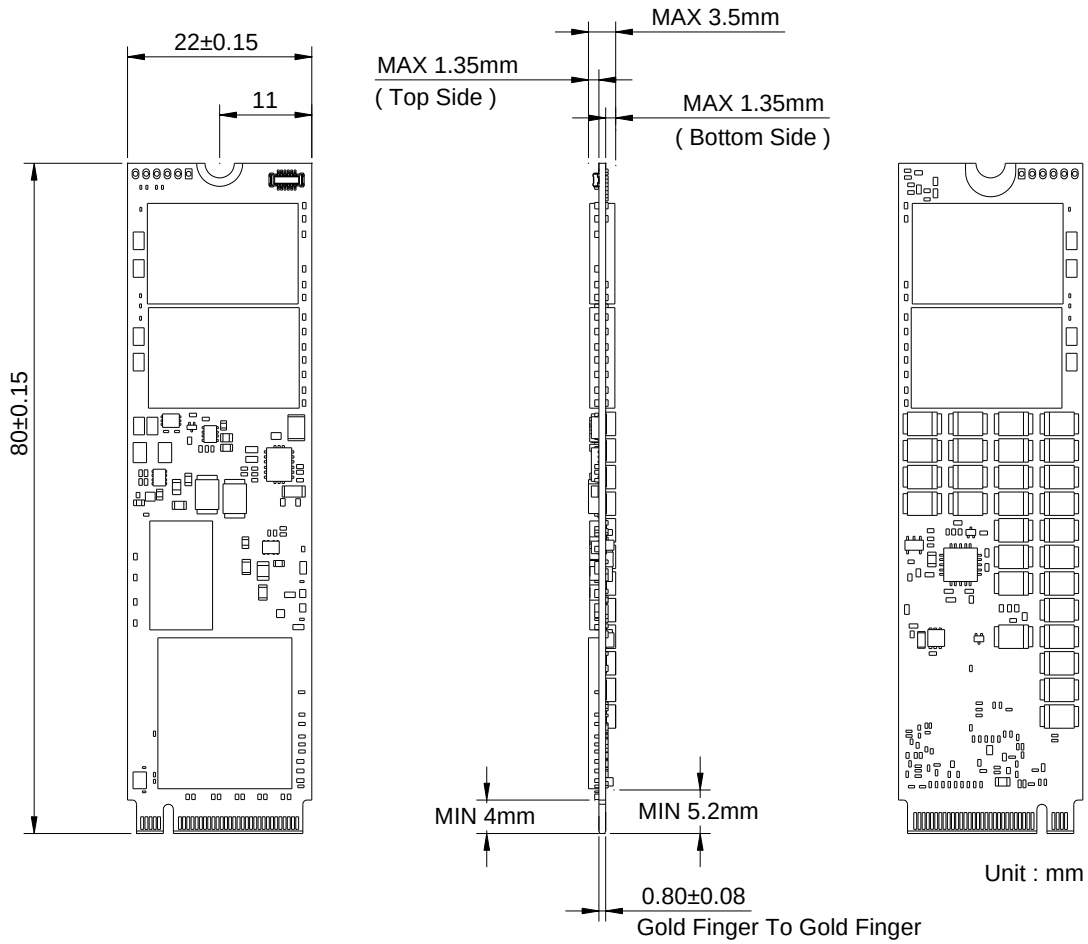
Owing to different user experiences, please contact ATP for Auto-Refresh in real applications.

3.0 Mechanical Dimension & NVMe SSD Pin Assignment

3.1 Mechanical Form Factor (Units in mm)

Table 3.1: Mechanical Dimension

Type		Value
M.2 2280-D2-M	Length	80 mm +/- 0.15
	Width	22 mm +/- 0.15
	Thickness	3.5mm (MAX)

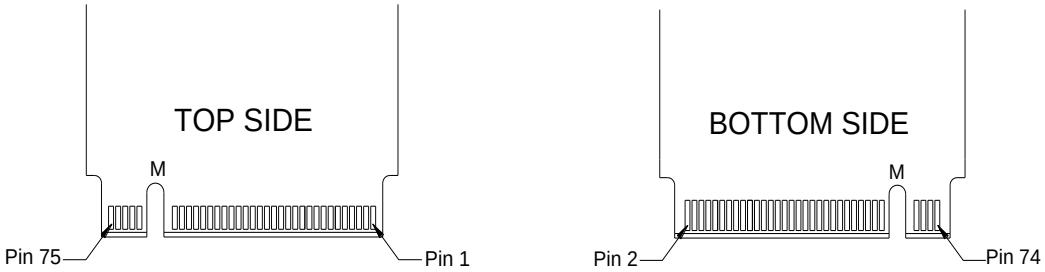


PLP model drawing

3.2 Pin Location

The following figure shows the pin location of the M.2 Embedded SSD, the golden finger is with both signal and power segments.

Figure 3-2



3.3 Pin Assignment

Pin assignment in show in Table 3-1 below.

Table 3-1

Pin No.	Function	Description	Pin No.	Function	Description
1	GND	Ground	2	3.3V	3.3 V Source
3	GND	Ground	4	3.3V	3.3 V Source
5	PETn3	PCIe 3 Transmit(-)	6	N/C	No Connect
7	PETp3	PCIe 3Transmit(+)	8	N/C	No Connect
9	GND	Ground	10	LED1# (O)	LED
11	PERn3	PCIe 3 Receive(-)	12	3.3V	3.3 V Source
13	PERp3	PCIe 3 Receive(+)	14	3.3V	3.3 V Source
15	GND	Ground	16	3.3V	3.3 V Source
17	PETn2	PCIe 2 Transmit(-)	18	3.3V	3.3 V Source
19	PETp2	PCIe 2Transmit(+)	20	N/C	No Connect
21	GND	Ground	22	N/C	No Connect
23	PERn2	PCIe 2 Receive(-)	24	N/C	No Connect
25	PERp2	PCIe 2 Receive(+)	26	N/C	No Connect
27	GND	Ground	28	N/C	Force ROM
29	PETn1	PCIe 1 Transmit(-)	30	N/C	No Connect
31	PETp1	PCIe 1Transmit(+)	32	N/C	No Connect
33	GND	Ground	34	N/C	No Connect

Pin No.	Function	Description	Pin No.	Function	Description
35	PERn1	PCIe 1 Receive(-)	36	N/C	No Connect
37	PERp1	PCIe 1 Receive(+)	38	N/C	No Connect
39	GND	Ground	40	SMB_CLK(I/O)	No Connect
41	PETn0	PCIe 0 Transmit(-)	42	SMB_DATA(I/O)	No Connect
43	PETp0	PCIe 0 Transmit(+)	44	ALERT# (O)	Reserved No Connect
45	GND	Ground	46	N/C	No Connect
47	PERn0	PCIe 0 Receive(-)	48	N/C	No Connect
49	PERp0	PCIe 0 Receive(+)	50	PERST# (I) 3.3V	PCIe Reset
51	GND	Ground	52	CLKREQ# (I/O) (0/3.3V)	Clock Request
53	REFCLKn	REFCLKn	54	PEWAKE# (I/O) (0/3.3V)	Reserved No Connect
55	REFCLKp	REFCLKp	56	Reserved for MFG_DATA	UART_RX
57	GND	Ground	58	Reserved for MFG_CLOCK	UART_TX
Module Key			Module Key		
67	N/C	No Connect	68	SUSCLK(32kHz) (I) (0/3.3V)	No Connect
69	NC-PCIe	Reserved No Connect	70	3.3V	3.3V Source
71	GND	Ground	72	3.3V	3.3V Source
73	GND	Ground	74	3.3V	3.3V Source
75	GND	Ground			

4.0 Command Set

4.1 Administrative Command Set

ATP NVMe SSD supports the following Administrative Command Sets:

Table 4-1

Opcode	Optional/Mandatory	Command
00h	M	Delete I/O Submission Queue
01h	M	Create I/O Submission Queue
02h	M	Get Log Page
04h	M	Delete I/O Completion Queue
05h	M	Create I/O Completion Queue
06h	M	Identify
08h	M	Abort
09h	M	Set Feature
0Ah	M	Get Feature
0Ch	M	Asynchronous Event Request
10h	O	Firmware Commit
11h	O	Firmware Image Download
14h	O	Device Self-test
NVM Command Set Specific		
80h	O	Format NVM
81h	O	Security Send
82h	O	Security Receive
84h	O	Sanitize

4.2. NVM Command Sets

ATP NVMe SSD supports the following NVM Command Sets:

Opcode	Optional/Mandatory	Command
00h	M	Flush
01h	M	Write
02h	M	Read
04h	O	Write Uncorrectable
05h	O	Compare
08h	O	Write Zeros
09h	O	Dataset Management

4.3. Get Log Page

ATP NVMe SSD supports the following Get Log Page:

Table 4-3

Opcode	Optional/Mandatory	Command
01h	M	Error Information
02h	M	SMART/Health Information
03h	M	Firmware Slot Information
05h	O	Command Effects Log
06h	O	Device Self-test
07h	O	Telemetry Host-Initiated
08h	O	Telemetry Controller-Initiated

4.4. Get/Set Feature

ATP NVMe SSD supports the following Get/Set Feature:

Table 4-4

Opcode	Optional/Mandatory	Command
01h	M	Arbitration
02h	M	Power Management
03h	O	LBA Range Type
04h	M	Temperature Threshold
05h	M	Error Recovery
06h	O	Volatile Write Cache
07h	M	Number of Queues
08h	M	Interrupt Coalescing
09h	M	Interrupt Vector Configuration
0Ah	M	Write Atomicity Normal
0Bh	M	Asynchronous Event Configuration
0Ch	O	Autonomous Power State Transition
0Eh	O	Timestamp
10h	O	Host Controlled Thermal Management
NVM Command Set Specific		
80h	O	Software Progress Marker

4.5. SMART Information

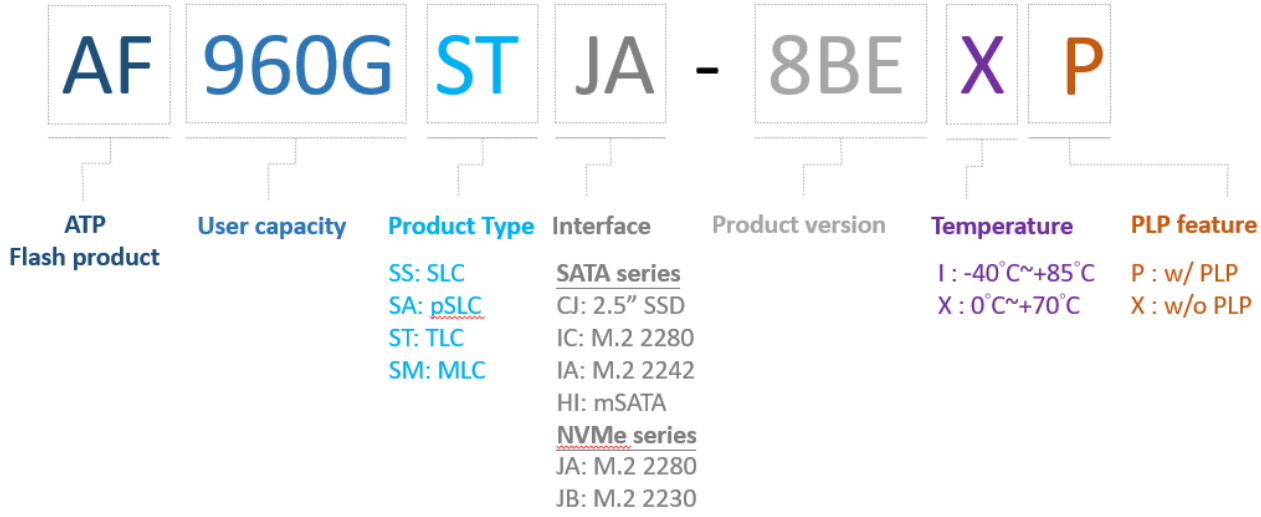
ATP NVMe SSD supports S.M.A.R.T. Attributes.

Table 4-5

ID	Byte Address	Bytes	Attribute Name
1	0	1	Critical Warning
2	1~2	2	Composite Temperature
3	3	1	Available Spare
4	4	1	Available Spare Threshold
5	5	1	Percentage Used
6	32~47	16	Data Units Read
7	48~63	16	Data Units Written
8	64~79	16	Host Read Commands
9	80~95	16	Host Write Commands
10	96~111	16	Controller Busy Time
11	112~127	16	Power Cycles
12	128~143	16	Power On Hours
13	144~159	16	Unsafe Shutdowns
14	160~175	16	Media and Data Integrity Errors
15	176~191	16	Number of Error Information Log Entries
16	192~195	4	Warning Composite Temperature Time
17	196~199	4	Critical Composite Temperature Time
18	200~201	2	Device Temperature
19	202~203	2	Normalized ASIC Temperature
20	216~219	4	Thermal Management Temperature 1 Transition Count
21	220~223	4	Thermal Management Temperature 2 Transition Count
22	224~227	4	Total Time For Thermal Management Temperature 1
23	228~231	4	Total Time For Thermal Management Temperature 2

5.0 Part Number Decoder

Standard Part Number



(Only for reference)

OEM Part Number

(Only for reference)

6.0 Certification and Declarations

Certification	Mark	Description
CE compliant		The CE marking (also known as CE mark) is a mandatory conformance mark on many products placed on the single market in the European Economic Area (EEA). The CE marking certifies that a product has met EU consumer safety, health or environmental requirements. CE stands for Conformité Européenne, "European conformity" in French.
FCC		FCC Part 15 Class B was used for Evolution of United States (US) Emission Standards for Commercial Electronic Products, The United States (US) covers all types of unintentional radiators under Subparts A and B (Sections 15.1 through 15.199) of FCC 47 CFR Part 15, usually called just FCC Part 15
BSMI compliant		BSMI logo signifies the product is compliant with Taiwan EMC standard for CNS13438.
UKCA		The UKCA (UK Conformity Assessed) marking is a new UK product mark for the products that conforms to the CE marking and sold in Great Britain, which is effective from 1st of January 2021.
RoHS	-	Compliant with the Restriction of Hazardous Substances (RoHS) Directive (2011/65/EU)
REACH	-	Compliant with REACH (Registration, Evaluation, Authorization and Restriction of Chemicals which is an EU Regulation that came into force on 1 June 2007

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