AOZ5007

High-Current, High-Performance DrMOS Power Module

General Description

The AOZ5007 is a high efficiency synchronous buck power stage module consisting of two asymmetrical MOSFETs and an integrated driver. The MOSFETs are individually optimized for operation in the synchronous buck configuration. The high side MOSFET has low capacitance and gate charge for fast switching with low duty cycle operation. The low side MOSFET has ultra low $R_{DS(ON)}$ to minimize conduction losses.

The AOZ5007 is available with two PWM options. AOZ5007QI is intended for use with TTL compatible PWM inputs. AOZ5007QI-01 has lower thresholds on the PWM signal and can operate with 3 V inputs. All other parameters are identical for the two versions. Both versions are tri-state compatible that allows both power MOSFETs to be turned off.

A number of features are provided making the AOZ5007 a highly versatile power module. The boot supply diode is integrated in the driver. The low side MOSFET can be driven into diode emulation mode to provide asynchronous operation when required. The pinout is optimized for low inductance routing of the converter keeping the parasitics and their effects to the minimum.

Features

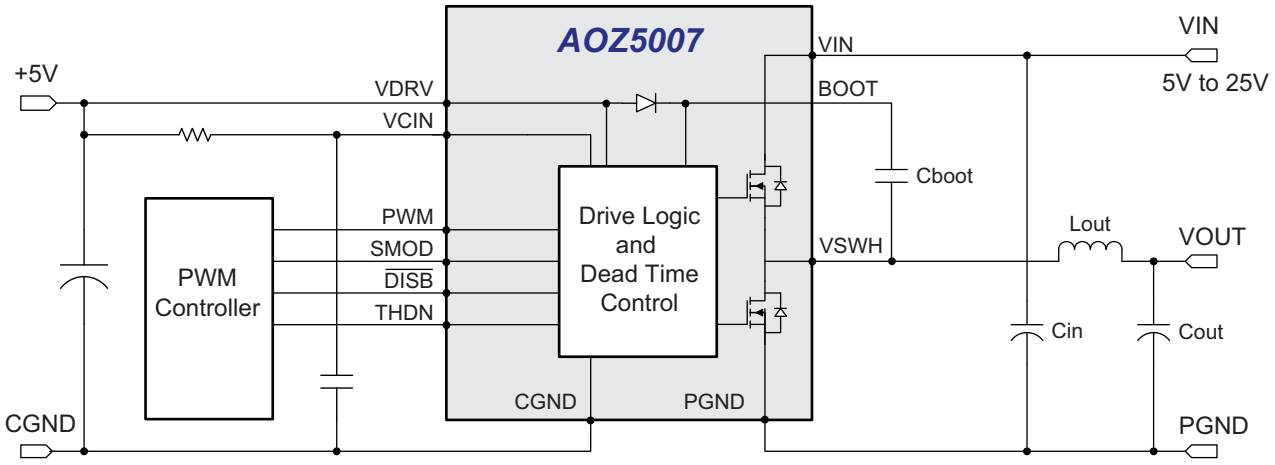
- Fully complies with Intel DrMOS Rev 4.0 specifications
- 4.5 V to 25 V input voltage range
- 4.5 V to 5.5 V driver supply range
- Up to 50 A output current
- Up to 1.5 MHz PWM operation
- Tri state PWM input
- Undervoltage protection
- Integrated boot supply diode
- Diode Emulation mode of operation
- Thermal shutdown alarm with flag
- Small 6x6 QFN-40L package

Applications

- Servers
- Notebook computers
- VRMs for motherboards
- Point of load DC/DC converters
- Memory and graphic cards
- Video gaming consoles

Green Product

Typical Application Circuit

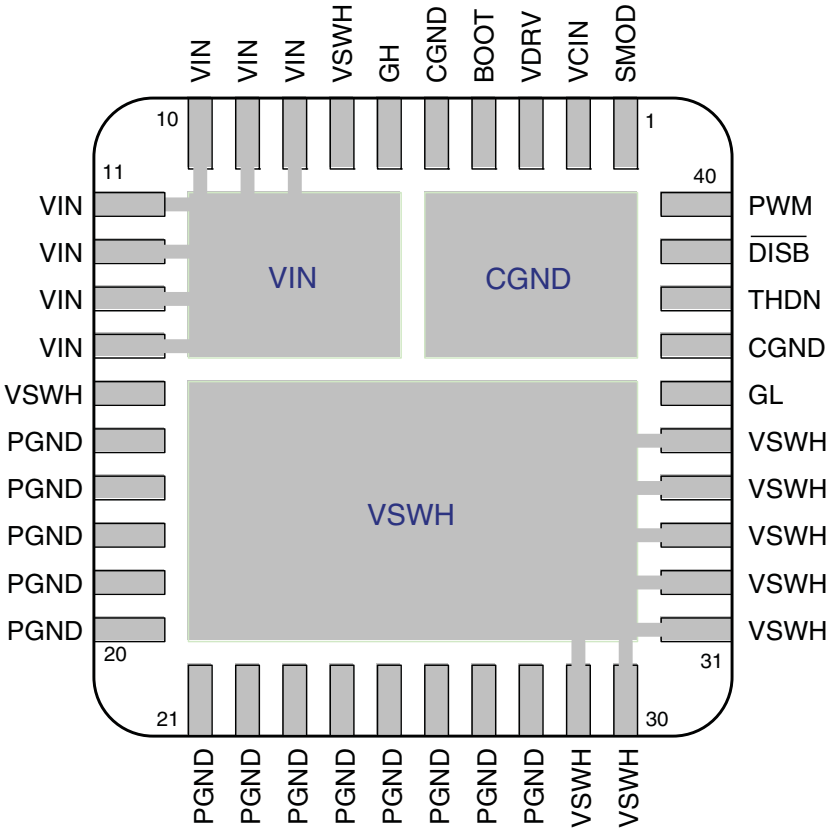


Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ5007QI	-40 °C to +85 °C	6x6 QFN-40L	Green Product
AOZ5007QI-01			

AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.
Please visit www.aosmd.com/web/quality/rohs_compliant.jsp for additional information.

Pin Configuration

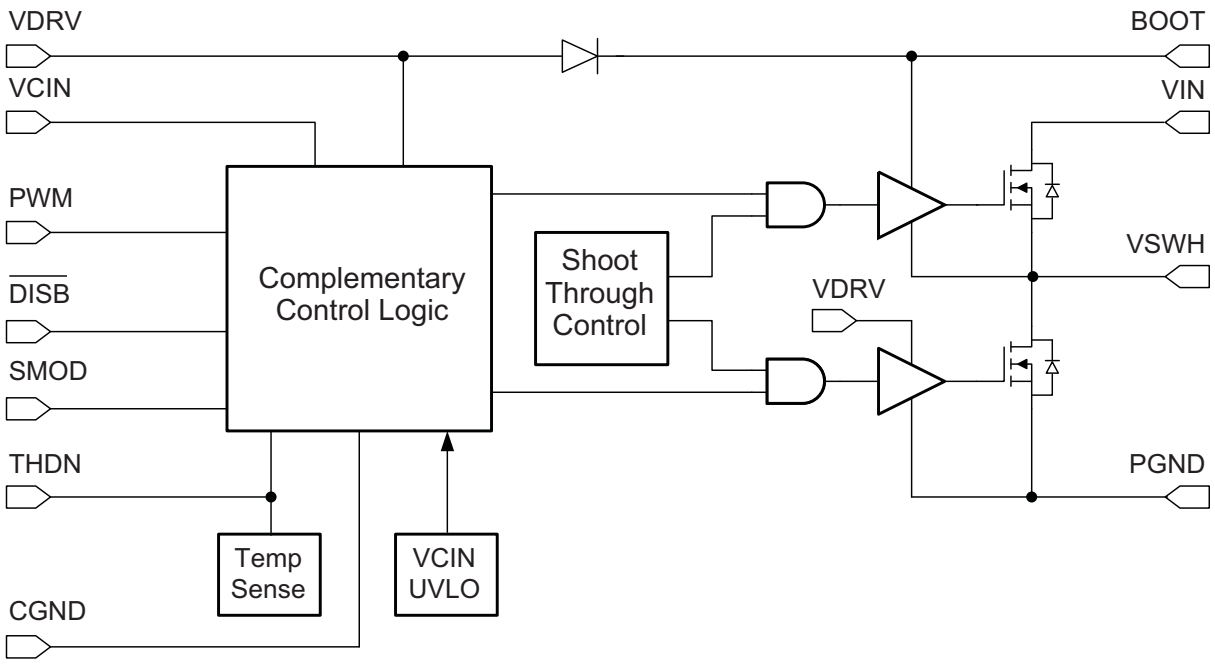


6x6 QFN-40
(Top View)

Pin Description

Pin Number	Pin Name	Pin Function
1	SMOD	Skip Mode input. When the pin is held active low, Diode Emulation or Skip Mode is enabled for the LS FET.
2	VCIN	Control supply input. Nominal 5 V. Can be derived from the gate drive supply VDRV with an RC filter for noise bypass.
3	VDRV	Gate drive supply input. Nominal 5 V.
4	BOOT	Gate drive supply for the HS FET. Nominal 5 V. The bootstrap diode is internal to the module. Connect a 0.1 μF or higher ceramic capacitor between VSWH node at pin 7.
5, 37	CGND	Control or analog ground for return of control signals and bypass capacitors. Attached to exposed pad in the driver section.
6	GH	Gate of the HS FET. Used for module testing during production. No user connections.
7	VSWH	Switching or the phase node for bootstrap capacitor connection.
8 to 14	VIN	Power input to the switching MOSFETs. Attached to the HS FET drain tab.
15	VSWH	Switching or the phase node pin. Not for power connections.
16 to 28	PGND	Power ground. Internally connected to control GND of pin 37.
29 to 35	VSWH	Switching or phase node connected to source of high side MOSFET and drain of the low side MOSFET. Electrically attached to the LS FET drain tab.
36	GL	Gate of the LS FET. Used for module testing during production. No user connections.
38	THDN	Open drain output of the thermal shutdown circuit. Active low.
39	$\overline{\text{DISB}}$	Disable pin for the controller. Both gates are held active low when $\overline{\text{DISB}}$ is grounded.
40	PWM	Pulse Width Modulated Tri State input from external controller.

Functional Block Diagram



Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
Supply Voltage (VIN)	-0.3 V to 30 V
Switch Node Voltage (VSWH)	-0.3 V to 30 V
Bootstrap Voltage (VBOOT)	-0.3 V to 30 V
VBOOT Voltage Transient (1)	40 V
Supply and Gate Drive Voltages: {VCIN, VDRV, (VBOOT – VSWH), THDN(3)}	-0.3 V to 7 V
Control Inputs (PWM, SMOD, $\overline{DISB}$)	-0.3 V to VCIN+0.3 V
Storage Temperature (T_S)	-40 °C to +150 °C
Junction Temperature (T_J)	-40 °C to +150 °C
ESD Rating(2)	2 kV

Notes:

1. Peak voltages can be applied for 100 nS per switching cycle.
2. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1.5 kΩ in series with 100 pF.
3 JEDEC Class II pulse conditions and failure criterion used. Level B exceptions are using a negative pulse limited to -0.5 V on THDN.

Recommended Operating Conditions

The device is not guaranteed to operate beyond the Maximum Recommended Operating Conditions.

Parameter	Rating
Supply Voltage (VIN)	4.5 V to 25 V
Supply and Gate Drive Voltages {VCIN, VDRV, (VBOOT – VSWH)}	4.5 V to 5.5 V
Control Inputs (PWM, SMOD, $\overline{DISB}$)	0 V to VCIN – 0.3 V
Operating Frequency	200 kHz to 1.5 MHz

Electrical Characteristics(4)

T_A = 25°C, V_{IN} = 12V, VDRV = VCIN = 5 V unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VIN	Operating Voltage		4.5		25	V
VCIN		VDRV Tied to VCIN	4.5		5.5	V
$R_{\theta JC}$(5)	Thermal Resistance	PCB Temp = 100 °C		3		°C / W
$R_{\theta JA}$ (5)		AOS Evaluation Board		10		°C / W
INPUT SUPPLY AND UVLO						
V_{CINON}	Undervoltage Lockout	V_{CIN} Rising		3.5	3.9	V
$V_{CINHYST}$				550		mV
I_{VCIN}	Control Circuit Bias Current	$\overline{DISB}$ = 0, VCIN = 5 V		50	75	µA
		$\overline{DISB}$ = High, V_{PWM} = Open		350	500	µA
		$\overline{DISB}$ = High, V_{PWM} = 0 V		650		µA
I_{VDRV}	Drive Circuit Operating Current	$\overline{DISB}$ = High, V_{PWM} = 300 kHz @ 50%		25		mA
		$\overline{DISB}$ = High, V_{PWM} = 1 MHz @ 50%		60		mA
PWM INPUT (AOZ5007QI)						
V_{PWMH}	PWM Input High Threshold	V_{PWM} Rising, VCIN = 5 V	3.6	3.9	4.1	V
V_{PWML}	PWM Input Low Threshold	V_{PWM} Falling, VCIN = 5 V	0.8	1.0	1.2	V
I_{PWM}	PWM Pin Input Current	Source or Sink, V_{PWM} = 0 V to 5 V		±250		µA
V_{TRIH}	PWM Input Tri State Threshold	V_{PWM} Rising, VCIN = 5 V	1.0	1.3	1.6	V
V_{TRIL}		V_{PWM} Falling, VCIN = 5 V	3.4	3.7	4.0	V
V_{TRRH}	Tri State Threshold Hysteresis	V_{PWM} Rising, VCIN = 5 V		280		mV
V_{TRFH}		V_{PWM} Falling, VCIN = 5 V		170		mV

Electrical Characteristics[4] (Continued)

T_A = 25°C, V_{IN} = 12V, VDRV = VCIN = 5 V unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
PWM INPUT (AOZ5007QI-01)						
V_{PWMH}	PWM Input High Threshold	V_{PWM} Rising, VCIN = 5 V	1.8	2.0	2.2	V
V_{PWML}	PWM Input Low Threshold	V_{PWM} Falling, VCIN = 5 V	0.8	1.0	1.2	V
I_{PWM}	PWM Pin Input Current	Source or Sink, V_{PWM} = 0 V to 3V		±10		µA
V_{TRIH}	PWM Input Tri State Threshold	V_{PWM} Rising, VCIN = 5 V	1.0	1.3	1.6	V
V_{TRIL}		V_{PWM} Falling, VCIN = 5 V	1.5	1.75	2.0	V
V_{TRRH}	Tri State Threshold Hysteresis	V_{PWM} Rising, VCIN = 5 V		300		mV
V_{TRFH}		V_{PWM} Falling, VCIN = 5 V		300		mV
DISB INPUT						
V_{DISBON}	Outputs Enable Threshold	VCIN = 5 V	2.0			V
$V_{DISBOFF}$	Outputs Disable Threshold	VCIN = 5 V			0.8	V
I_{DISB}	$\overline{DISB}$ pin input current	Source or Sink		±10		µA
SMOD INPUT						
V_{SMODH}	SMOD Enable Threshold	VCIN = 5 V	2.0			V
V_{SMODL}	SMOD Disable Threshold	VCIN = 5 V			0.8	V
I_{SMOD}	SMOD Pin Input Current	Source or Sink		±10		µA
GATE DRIVER TIMINGS						
t_{PDLU}	PWM to HS Gate	PWM H → L, GH H → L		20		ns
t_{PDLL}	PWM to LS Gate	PWM L → H, GL H → L		35		ns
t_{PDHU}	LS to HS Gate Deadtime	GL H → L, GH L → H		16		ns
t_{PDHL}	HS to LS Gate Deadtime	GH H → L, GL L → H		17		ns
t_{TSSHD}	Tri State Shutdown Delay			170		ns
t_{PTS}	Tri State Propagation Delay			35		ns
THERMAL SHUTDOWN[6]						
T_{JTHDN}	Shutdown Threshold			150		°C
T_{JHYST}	Hysteresis			15		°C
V_{THDNL}	THDN Pin Output Low	5 kΩ pull up resistor to VCIN		0.06		V
R_{THDNL}	THDN Pull Down Resistance			60		Ω

Notes:

4. All voltages are specified with respect to the corresponding GND pin
5. Characterisation value. Not tested in production.
6. Temperature sensed on the driver pad.

Typical Performance Characteristics

Unless otherwise noted, VIN = 12 V, VDRV = VCIN = 5 V, F_{sw} = 500 kHz, L_{out} = 470 nH, V_{out} = 1.0 V, Module Loss measured on AOS evaluation board at T_A = 25 °C. Module loss includes power MOSFET loss plus drive circuit loss.

Fig 1. Module Loss vs. Load Current

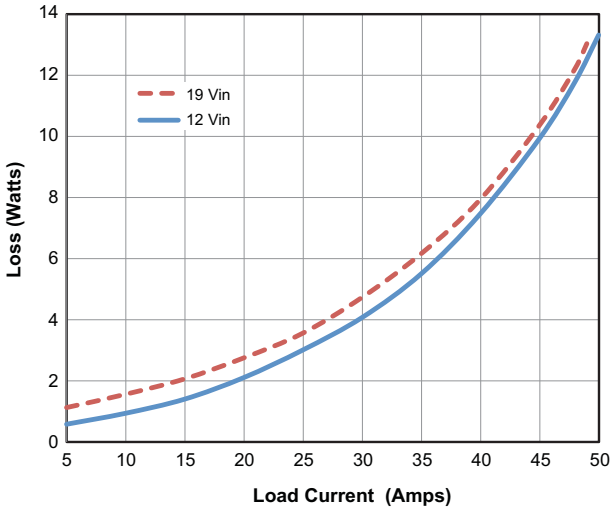


Fig 2. Output Current vs. Temperature

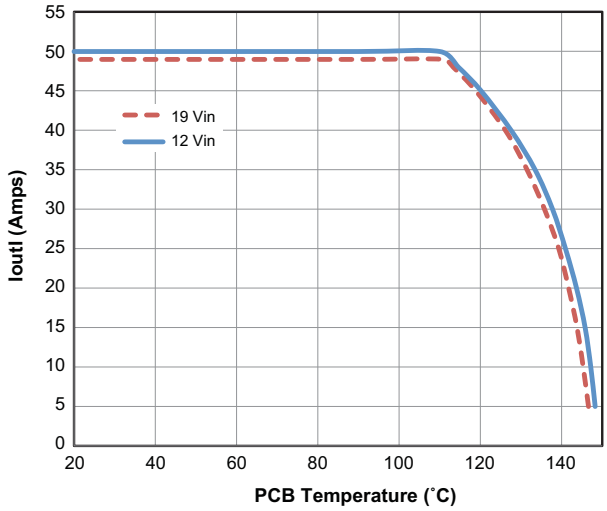


Fig 3. Normalised Module Loss vs. Output Voltage

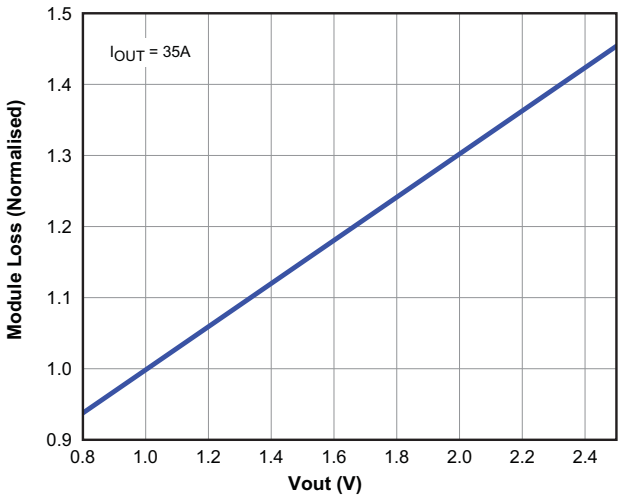
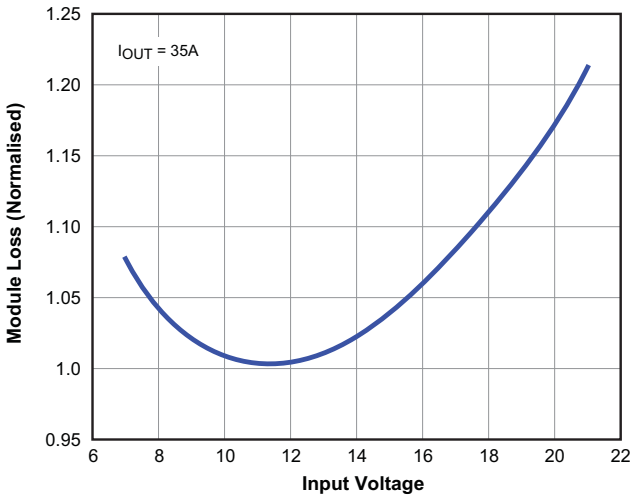


Fig 4. Normalised Module Loss vs. Input Voltage



Typical Performance Characteristics (Continued)

Fig 5. Normalised Module Loss vs. Drive Voltage

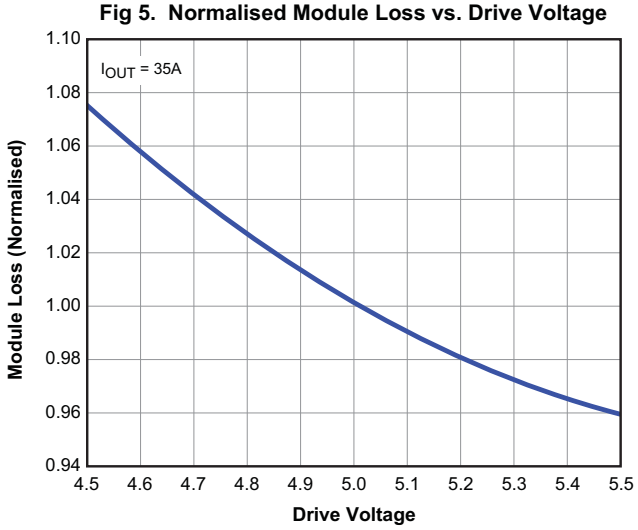


Fig 6. IDrv vs. Drive Voltage

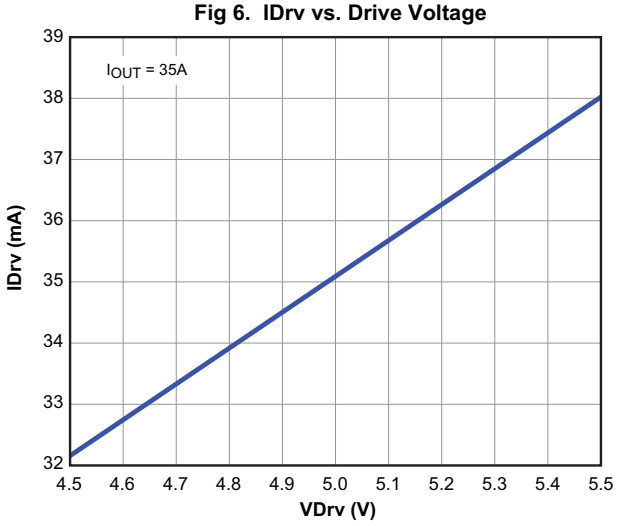


Fig 7. IDrv vs. Frequency

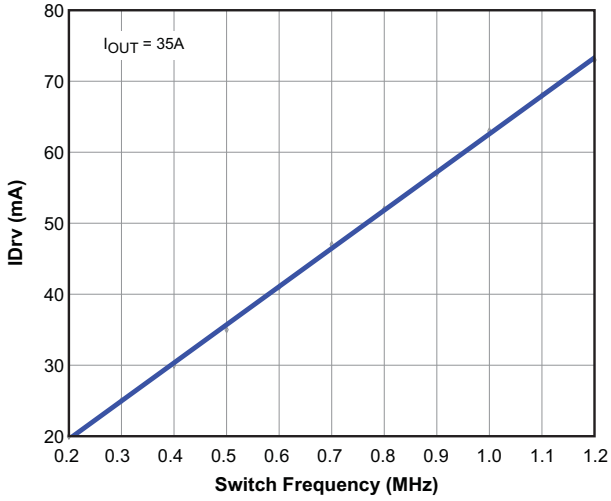


Fig 8. Normalised Module Loss vs. Switch Frequency

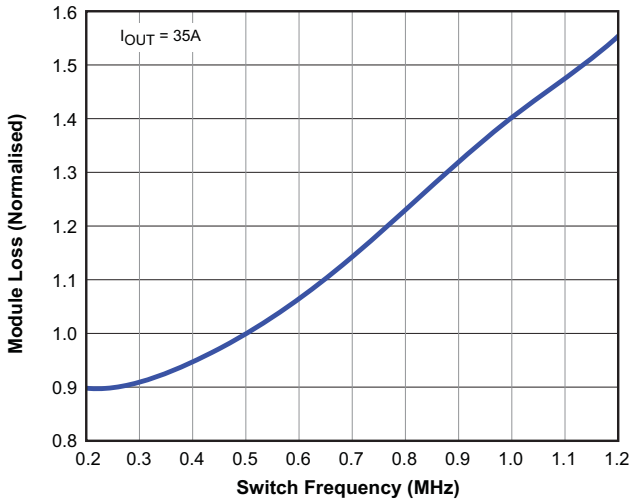


Fig 9. I_{DRV} + I_{VCIN} vs. Temperature

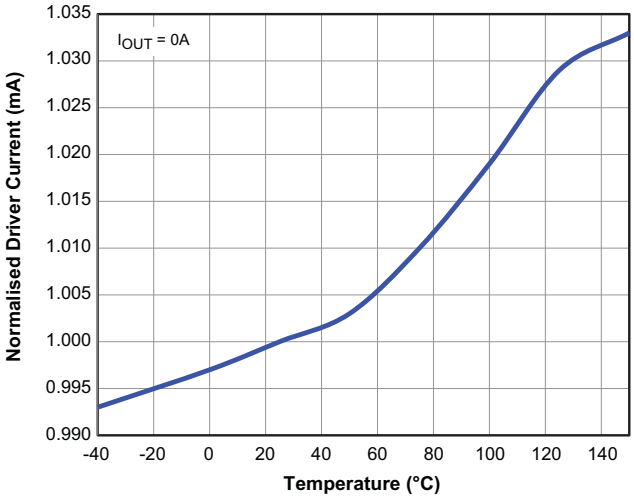
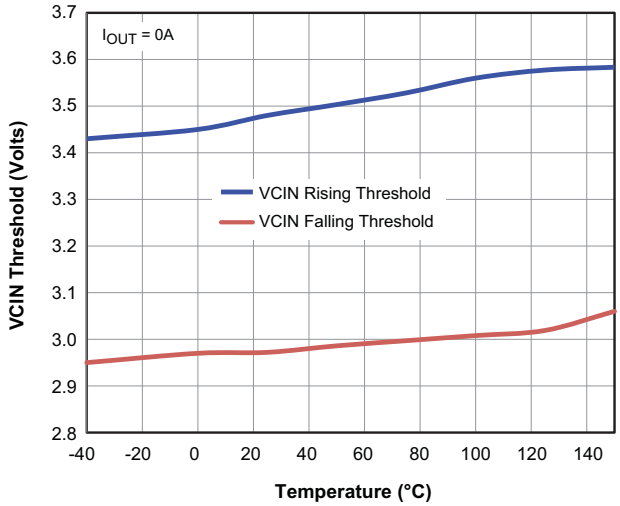


Fig 10. VDRV UVLO Threshold vs. Temperature



Typical Performance Characteristics (Continued)

Fig 11. PWM Input Threshold vs. Temperature

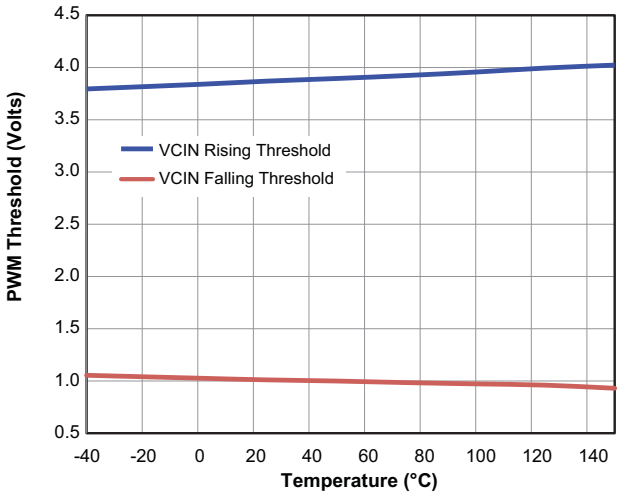


Fig 12. PWM Input Tristate Threshold vs. Temperature

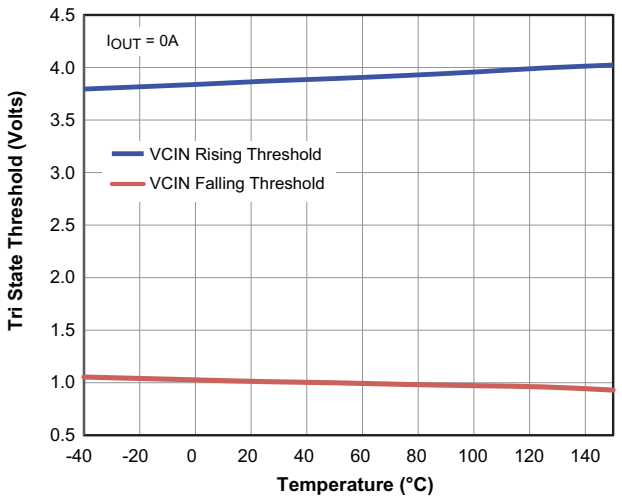


Fig 13. PWM Input Tri State Hold Off Time vs. Temperature

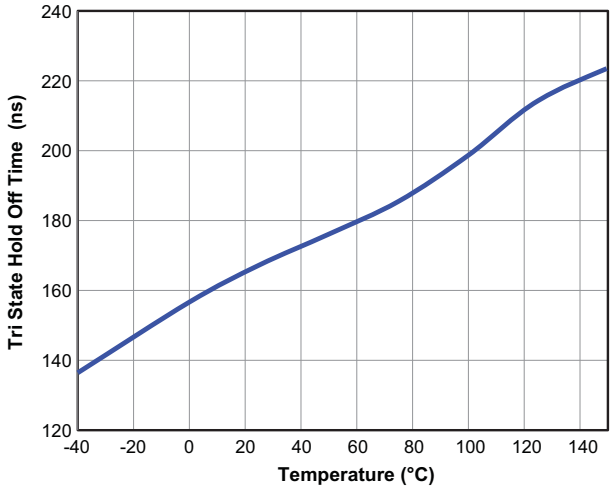


Fig 14. $\overline{DISB}$ Input Threshold vs. Temperature

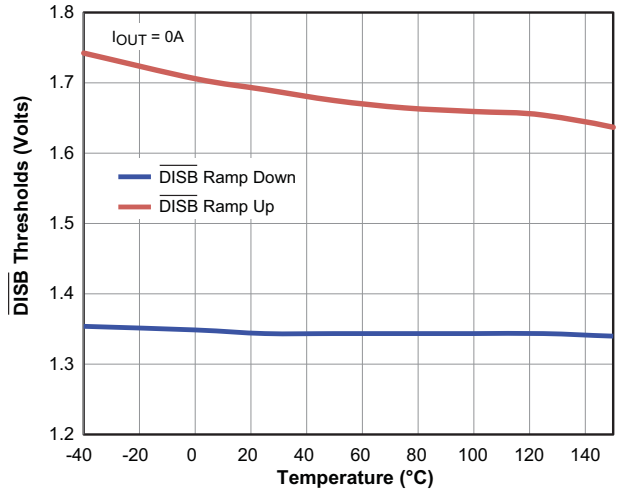
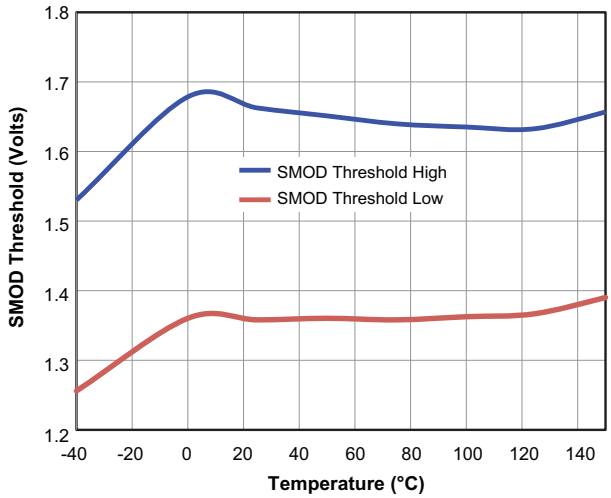


Fig 15. SMOD Input Threshold vs. Temperature



Timing Diagram

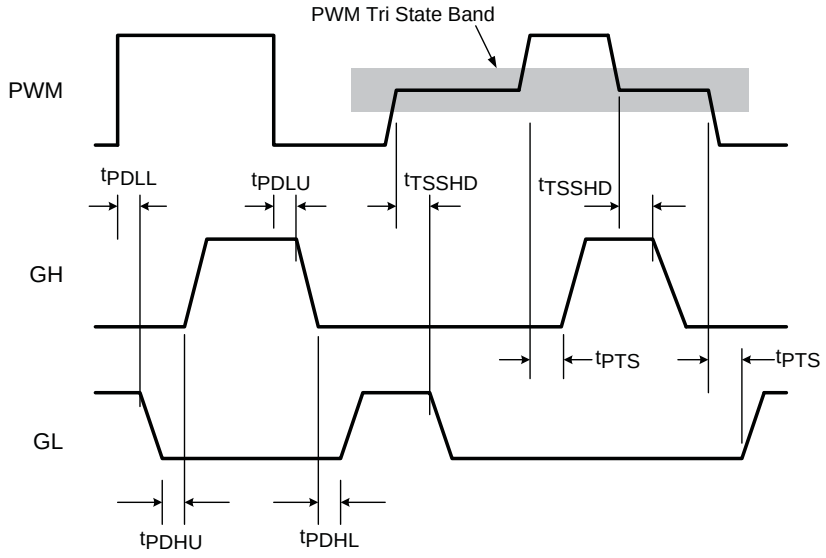


Figure 16. Timing Diagram

Application Information

AOZ5007QI and AOZ5007QI-01 are fully integrated power modules designed to work over an input voltage range of 4.5 V to 25 V with 5 V supplies for gate drive and internal control circuits. A number of features are provided making the AOZ5007QI a highly versatile power module. High side and low side power MOSFETs are combined in one package with the pin outs optimized for power routing with minimum parasitic inductances. The MOSFETs are individually tailored for efficient operation as either high side or low side switches in a low duty cycle synchronous buck converter. A high current driver is also included in the package which minimizes the gate drive loop and results in extremely fast switching. The modules are fully compatible with Intel DrMOS specification Rev 4.0 in form fit and function.

Powering the Module and the Gate Drives

An external supply VDRV of 5 V is required for driving the MOSFETs. The MOSFETs are designed with low gate thresholds so that lower drive voltage can be used to reduce the switching and drive losses without compromising the conduction losses. The control logic supply VCIN can be derived from the gate drive supply VDRV through an RC filter to bypass the switching noise. See Figure 17 for recommended gate drive supply connections. The gate driver is capable of supplying several amperes of peak current into the LS FET to achieve extremely fast switching. A ceramic bypass capacitor of 1 μF or higher is recommended from VDRV to CGND.

The boost supply for driving the high side MOSFET is generated by connecting a small capacitor between BOOT pin and the switching node VSWH. It is recommended that this capacitor Cboot be connected as close as possible to the device across pins 4 and 7. Boost diode is integrated into the package. Rboot is an optional resistor used by designers to slow down the turn on speed of the high side MOSFET. The value is a compromise between the need to keep both the switching time and VSWH node spikes as low as possible and is typically 1 Ω to 5 Ω.

Undervoltage Lockout and Enable

VCIN is monitored for UVLO conditions and both outputs are actively held low unless adequate gate supply is available. The undervoltage lockout is set at 3.5 V with a 550 mV hysteresis. Since the PWM control signals are provided typically from an external controller or a digital processor extra care must be taken during start up. The AOZ5007QI must be powered up and enabled before the PWM input is applied. It should be ensured that PWM signal goes through a proper soft start sequence to minimise inrush current in the converter during start up. Powering the module with a full duty cycle PWM signal already applied may lead to a number of undesirable consequences as explained below.

Outputs can also be turned off through the $\overline{\text{DISB}}$ pin. When this input is grounded the drivers are disabled and held active low. The module is in standby mode with low quiescent current of less than 75 μA.

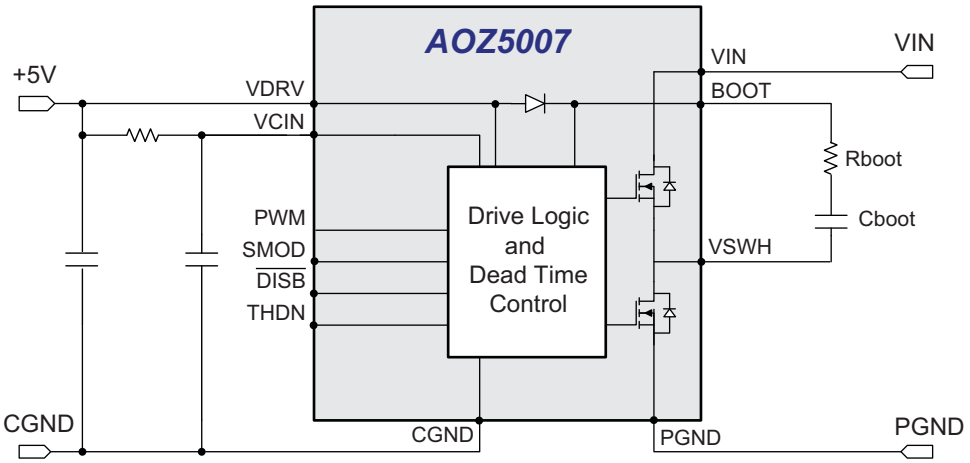


Figure 17. Applying VDRV and Generating BOOT Supply

IMPORTANT: If the $\overline{\text{DISB}}$ is used it is necessary to ensure proper coordination with soft start and enable features of the external PWM controller in the system. Every time AOZ5007QI is disabled through $\overline{\text{DISB}}$ there will be no output and the external controller may enter into open loop and put out a PWM signal with maximum duty ratio possible. If the AOZ5007QI is re-enabled by taking $\overline{\text{DISB}}$ high, there will be extremely large inrush currents while the output voltage builds up again which may drive the system into current limit. There might be undesirable consequences such as inductor saturation, overloading of the input or even a catastrophic failure of the device. It is recommended that the PWM controller be disabled when AOZ5007QI is disabled or non operational because of UVLO. The PWM controller should always be enabled with a soft start to minimise stresses on the converter.

In general it should be noted that AOZ5007QI is a combination of two MOSFETs with an unintelligent driver, all of which are optimized for switching at the highest efficiency. Other than UVLO and thermal protection, it does not have any monitoring or protection functions built in. The PWM controller should be designed in to perform these functions under all possible operating and transient conditions.

Input Voltage VIN

AOZ5007QI is rated to operate over a wide input range of 4.5 V to 25 V. As with any other synchronous buck converter, large pulse currents at high frequency and extremely high di/dt rates will be drawn by the module during normal operation. It is strongly recommended to bypass the input supply very close to package leads with X7R or X5R quality ceramic capacitors.

The high side MOSFET in AOZ5007QI is optimized for fast switching with low duty ratios. It has ultra low gate charges which have been achieved as a trade off with higher $R_{DS(ON)}$ value. When the module is operated at low VIN the duty ratio will be higher and conduction losses in the HS FET will also be correspondingly higher. This will be compensated to some extent by reduced switching losses. The total power loss in the module may appear to be low even though in reality the HS MOSFET losses may be disproportionately high. Since the two MOSFETs have their own exposed pads and PCB copper areas for heat dissipation, the HS FET may be much hotter than the LS FET. It is recommended that worst case junction temperature be measured and ensured to be within safe limits when the module is operated with high duty ratios.

PWM Input

AOZ5007QI is offered in two versions which can be interfaced with PWM logic compatible with either 5 V (TTL) or 3V (CMOS). Refer to Figure 16 for the timing and propagation delays between the PWM input and the gate drives. The PWM is also a tri state compatible input. When the input is high impedance or unconnected both the gate drives will be off and the gates are held active low. The PWM Threshold Table (Table 1) lists the thresholds for high and low level transitions as well as tri state operation. As shown in Figure 16, there is a hold off delay between the time PWM signal enters the tri state window and the corresponding gate drive is pulled low.

This delay is typically 170 ns and intended to prevent spurious triggering of the tri state mode which may be caused either by noise induced glitches in the PWM waveform or slow rise and fall times.

Table 1. PWM Input and Tri State Thresholds

Thresholds →	V_{PWMH}	V_{PWML}	V_{TRIH}	V_{TRIL}
AOZ5007QI	3.9V	1.0 V	1.3V	3.7V
AOZ5007QI-01	2V	1V	1.3V	1.75 V

Note: See Figure 16 for propagation delays and tri state window.

Diode Mode Emulation of Low Side MOSFET (SMOD)

AOZ5007QI can be operated in the diode emulation or skip mode using the SMOD pin. This is useful if the converter has to operate in asynchronous mode during start up, light load or under pre bias conditions. If SMOD is taken high, the controller will use the PWM signal as reference and generate both the high and low side complementary gate drive outputs with the minimal delays necessary to avoid cross conduction. When the pin is taken low the HS FET drive is not affected but diode emulation mode is activated for the LS FET. See Table 2 for a comprehensive view of all logic inputs and corresponding drive conditions.

Table 2. Control Logic Truth Table

$\overline{DISB}$	SMOD	PWM	GH	GL
L	X	X	L	L
H	L	H	H	L
H	L	L	L	See Note
H	H	Tri State	L	L
H	H	H	H	L
H	H	L	L	H

Note: Diode emulation mode is activated when SMOD pin is held low.

Gate Drives

AOZ5007QI has an internal high current high speed driver that generates the floating gate drive for the HS FET and a complementary drive for the LS FET. Propagation delays between transitions of the PWM waveform and corresponding gate drives are kept to the minimum. An internal shoot through protection scheme ensures that neither MOSFET turns on while the other one is still conducting, thereby preventing shoot through condition of the input current. When the PWM signal makes a transition from H → L or L → H, the corresponding gate drive GH or GL begins to turn off. The adaptive timing circuit monitors the falling edge of the gate voltage and when the level goes below 1V, the complementary gate driver is turned on. The dead time between the two switches is minimized, at the same time preventing cross conduction across the input bus. The adaptive circuit also monitors the switching node VSWH and ensures that transition from one MOSFET to another always takes place without cross conduction, even under transient and abnormal conditions of operation.

The gate pins GH and GL are brought out on pins 6 and 36 respectively. However these connections are not made directly to MOSFET gate pads and their voltage measurement may not reflect the actual gate voltage applied inside the package. The gate connections are primarily for functional tests during manufacturing and no connections should be made to them in the application.

Thermal Shutdown

The module temperature is internally sensed and an alarm is asserted if it exceeds 150 °C. The alarm is reset when the temperature cools down to 135 °C. The THDN is an open drain pin that is pulled to CGND to indicate an over temperature condition. It may be pulled up to VCIN through a resistor for monitoring purposes.

PCB Layout Guidelines

AOZ5007 is a high current module rated for operation up to 1.5 MHz. This requires extremely fast switching speeds to keep the switching losses and device temperatures within limits. Having a robust gate driver integrated in the package helps to minimise the driver-to-MOSFET gate pad connections without involving the parasitics of the package or PCB traces. While excellent switching speeds are achieved, correspondingly high levels of dv/dt and di/dt will be observed throughout the power train which requires careful attention to PCB layout to minimise voltage spikes and other transients. As with any synchronous buck converter layout the critical requirement is to minimise the area of the primary switching current loop, formed by the HS FET, LS FET and the input bypass capacitor C_{in}. The PCB design is somewhat simplified because of the optimized pin out in AOZ5007QI. The bulk of VIN and PGND pins are located adjacent to each other and the input bypass capacitors should be placed as close as possible to these pins. The area of the secondary switching loop, formed by LS FET, output inductor and output capacitor C_{out} is the next critical parameter. The ground plane should be extended and the negative pins of C_{out} should be returned to it, again as close as possible to the device pins.

The AOZ5007QI is extremely efficient. MOSFETs in the package are directly attached to individual exposed pads to simplify thermal management. Both VIN and VSWH pads should be attached to large areas of PCB copper. Thermal reliefs should be avoided to ensure proper heat

dissipation to the board. An inner power plane layer dedicated to VIN, typically the 12 V system input, is desirable and vias should be provided near the device to connect the VIN copper pour to the power plane. Though ground does not form a part of any device tabs, significant amount of heat is dissipated though multiple PGND pins. A large copper pour connected to PGND pins and further to the system ground plane through vias will further improve thermal management of the system.

Figure 18 illustrates the various copper pours and bypass capacitor locations.

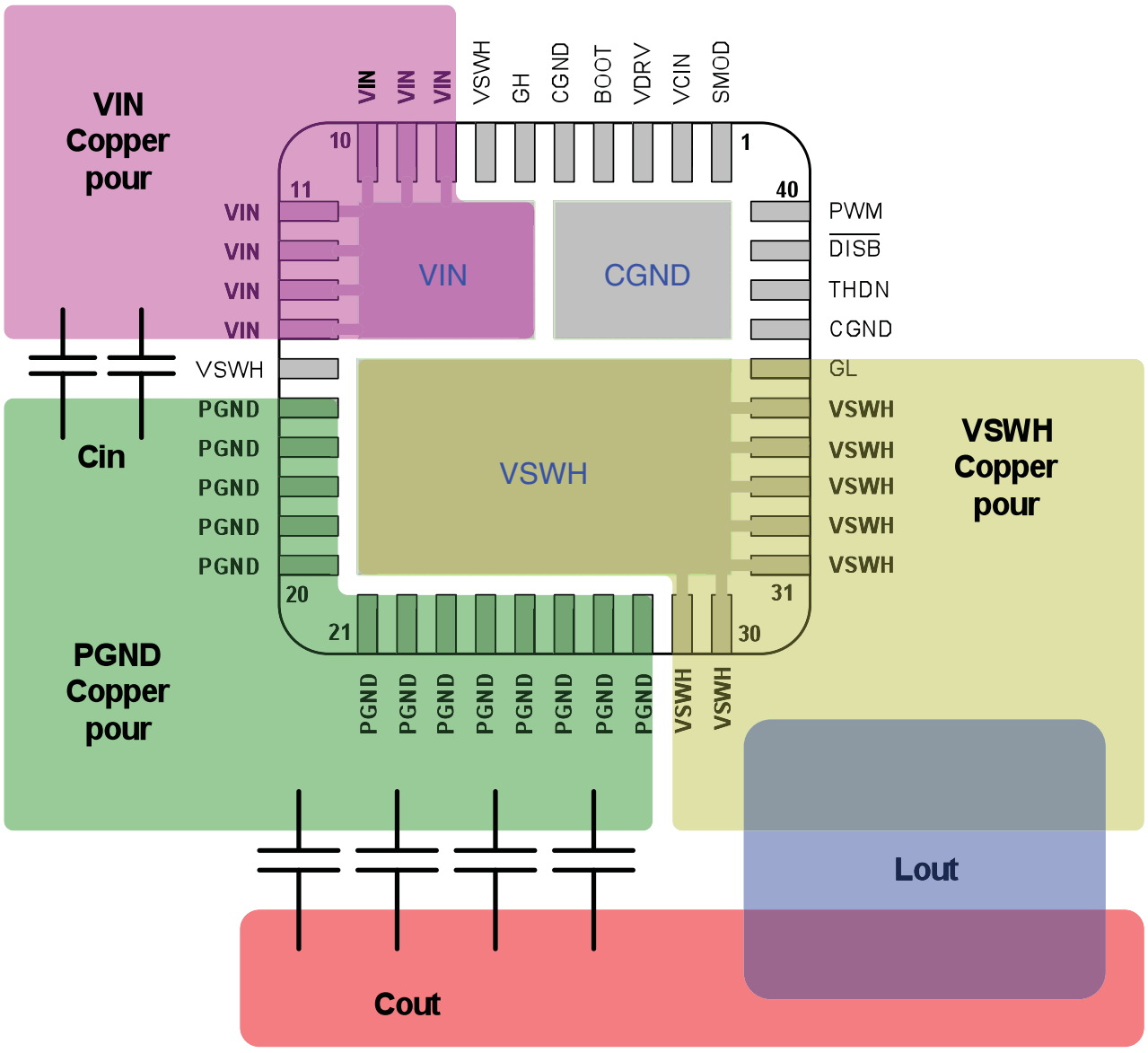
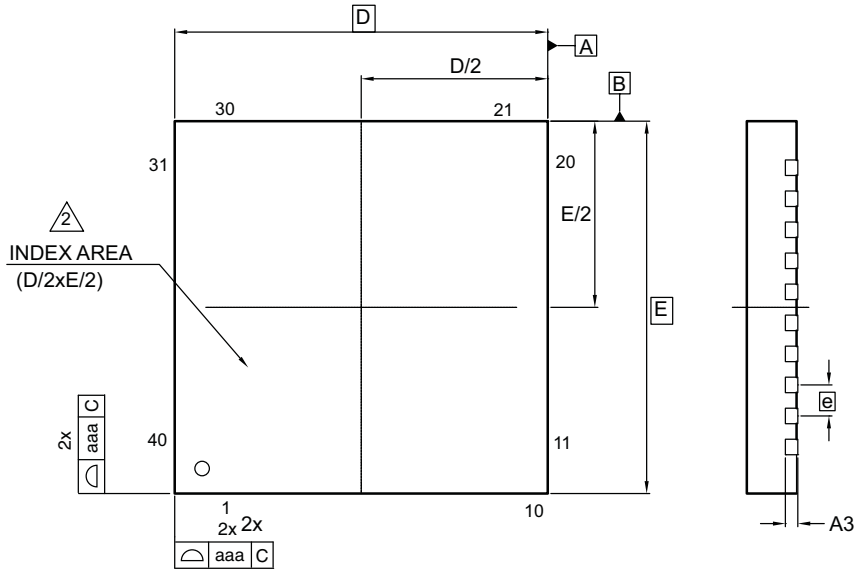
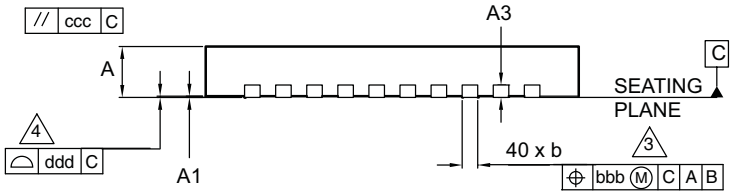


Figure 18. PCB Layout Illustration for Minimizing Current Loops

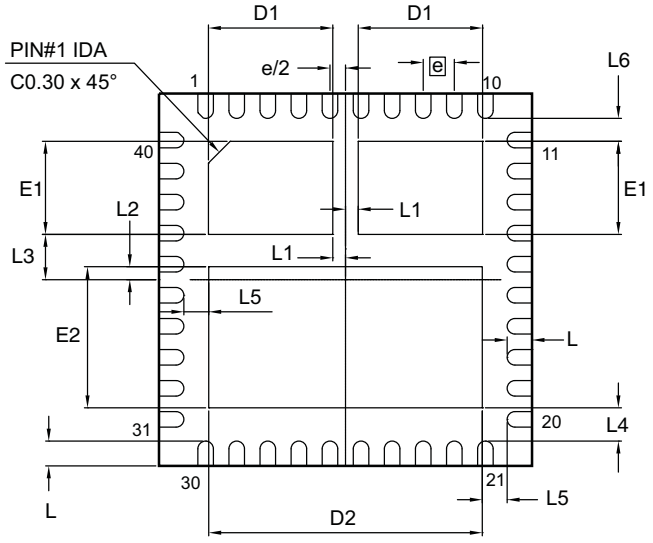
Package Dimensions, 6x6 QFN-40 EP3_S



TOP VIEW



SIDE VIEW

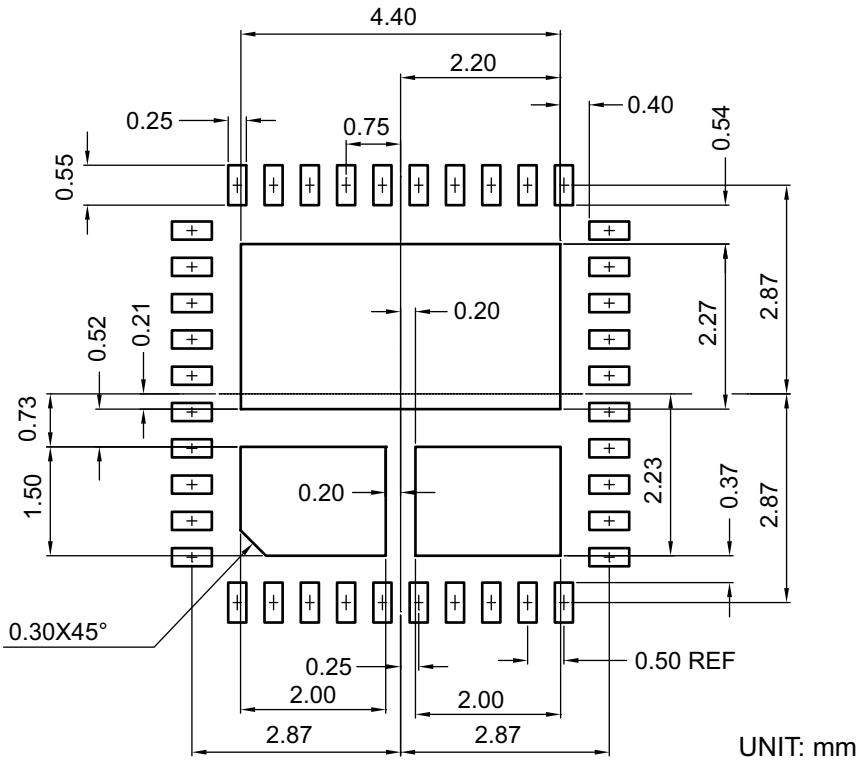


BOTTOM VIEW

Notes:

1. All dimensions are in millimeters.
2. The location of the terminal #1 identifier and terminal numbering convention conforms to JEDEC publication 95 SPP-002.
3. Dimension b applies to metallized terminal and is measured between 0.20mm and 0.35mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measured in that radius area.
4. Coplanarity applies to the terminals and all other bottom surface metalization.

Package Dimensions, 6x6 QFN-40 EP3_S (Continued)



RECOMMENDED LAND PATTERN

Dimensions in millimeters

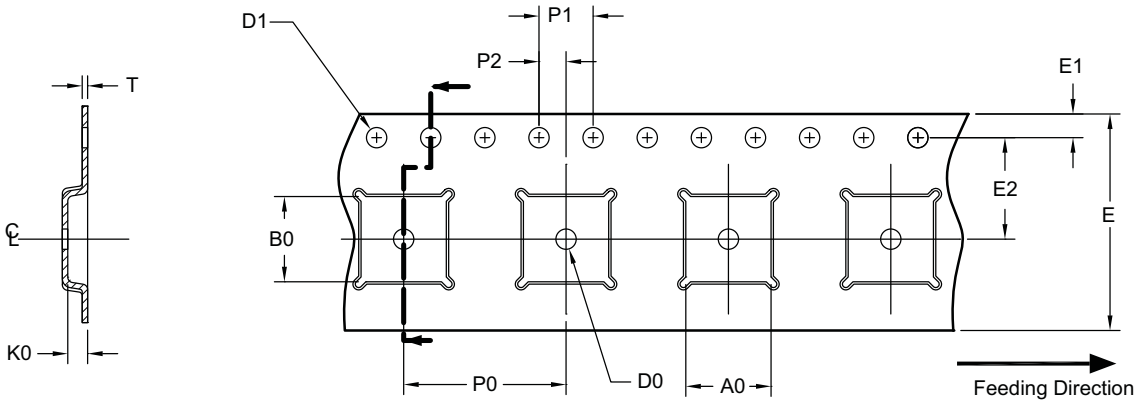
Symbols	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.20	0.25	0.35
D		6.00 BSC	
D1	1.90	2.00	2.10
D2	4.30	4.40	4.50
E		6.00 BSC	
E1	1.40	1.50	1.60
E2	2.17	2.27	2.37
e		0.50 BSC	
L	0.30	0.40	0.50
L1	0.15	0.20	0.25
L2	0.15	0.21	0.26
L3	0.63	0.73	0.83
L4	0.44	0.54	0.64
L5	0.30	0.40	0.50
L6	0.27	0.37	0.47
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.08	

Dimensions in inches

Symbols	Min.	Typ.	Max.
A	0.028	0.030	0.031
A1	0.000	0.001	0.002
A3		0.008 REF	
b	0.008	0.010	0.014
D		0.236 BSC	
D1	0.075	0.079	0.083
D2	0.169	0.173	0.177
E		0.236 BSC	
E1	0.055	0.059	0.063
E2	0.085	0.089	0.093
e		0.020 BSC	
L	0.012	0.016	0.020
L1	0.006	0.008	0.010
L2	0.006	0.008	0.010
L3	0.024	0.028	0.032
L4	0.017	0.021	0.025
L5	0.012	0.016	0.020
L6	0.011	0.015	0.019
aaa		0.006	
bbb		0.004	
ccc		0.004	
ddd		0.003	

Tape and Reel Dimensions, 6x6 QFN

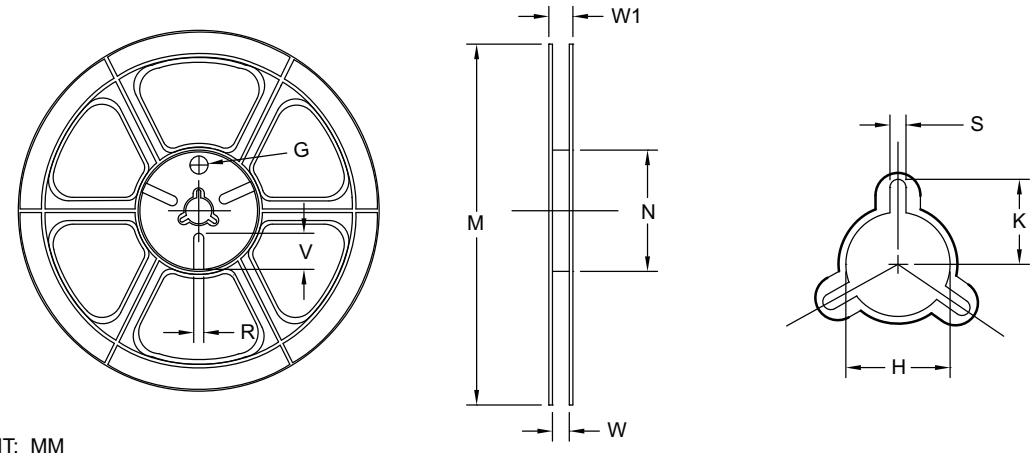
Carrier Tape



UNIT: MM

Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
QFN6x6 (16mm)	6.30 ±0.20	6.30 ±0.20	1.10 ±0.20	1.50 MIN.	1.50 +0.1 -0.0	16.0 ±0.3	1.75 ±0.10	7.5 ±0.1	12.00 ±0.20	4.00 ±0.20	2.00 ±0.10	0.30 ±0.05

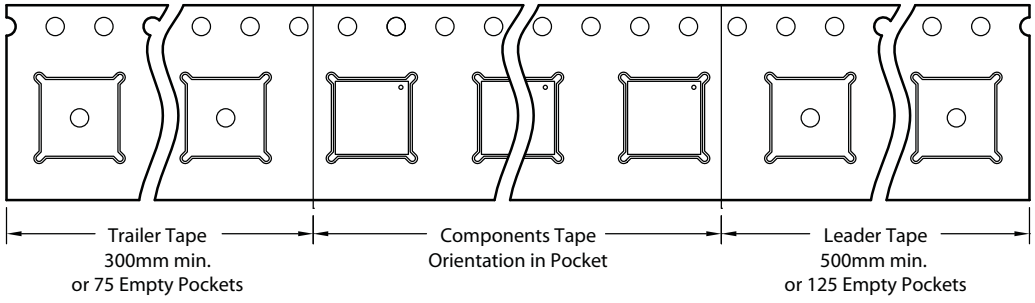
Reel



UNIT: MM

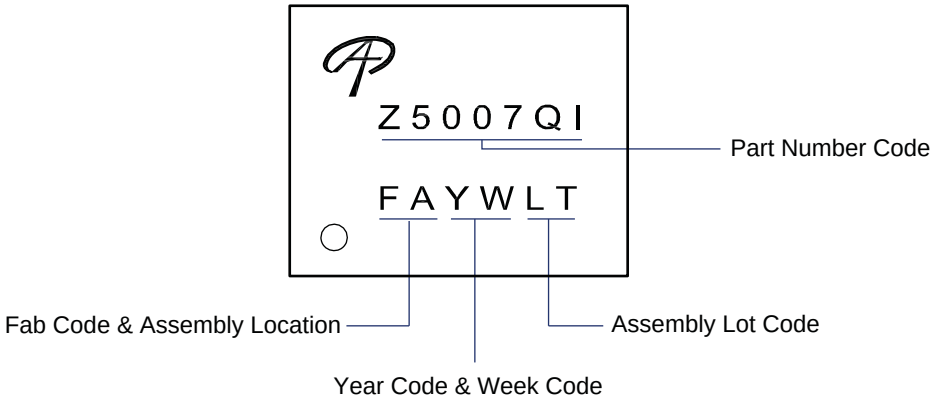
Tape Size	Reel Size	M	N	W	W1	H	K	S	G	R	V
16mm	Ø330	Ø330 Max.	Ø100 Min.	16.4 +2.0 -0.0	22.4 Max.	Ø13.0 +0.5 -0.2	10.1 Min.	1.5 Min.	---	---	---

Leader/Trailer and Orientation

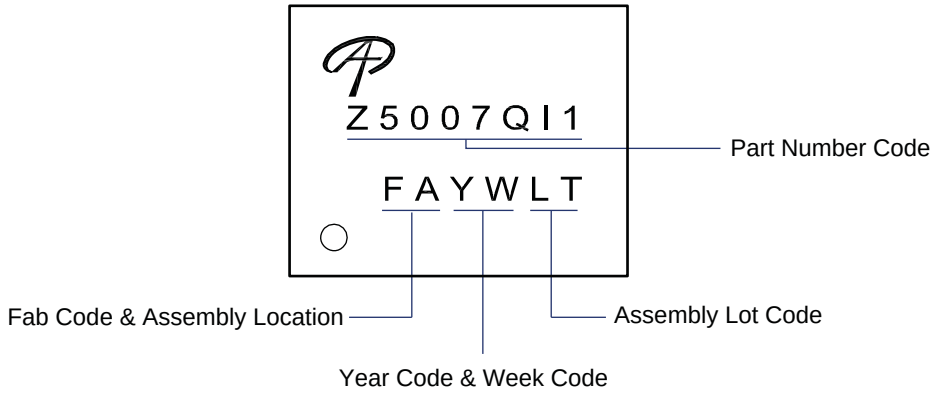


Part Marking

AOZ5007QI
(6.0 x 6.0 QFN)



AOZ5007QI-01
(6.0 x 6.0 QFN)



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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.