PRODUCT / PROCESS CHANGE INFORMATION

1. PCI basic data	
1.1 Company	STMicroelectronics International N.V
1.2 PCI No.	MDG/23/14199
1.3 Title of PCI	ASE Kaohsiung (Taiwan) - qualification of a second source substrate supplier (SCC - Shennan Circuit Company) for BGA package, size from BGA5x5 to BGA18x18, for listed products
1.4 Product Category	STM32Fxx, STM32Hxx, STM32Lxx, STM32MPxx, STM32Uxx, & STM32Wxx in BGA package
1.5 Issue date	2023-08-20

2. PCI Team	
2.1 Contact supplier	
2.1.1 Name	ROBERTSON HEATHER
2.1.2 Phone	+1 8475853058
2.1.3 Email	heather.robertson@st.com
2.2 Change responsibility	
2.2.1 Product Manager	Ricardo Antonio DE SA EARP
2.1.2 Marketing Manager	Veronique BARLATIER
2.1.3 Quality Manager	Pascal NARCHE

3. Change		
3.1 Category	3.2 Type of change	3.3 Manufacturing Location
Materials	Any change on substrate (part number, supplier, plant, design or composition of any layer, etc..)	ASE Kaohsiung (Taiwan)

4. Description of change		
	Old	New
4.1 Description	First source Supplier, either ASEMTL-SH or TCI or Kinsus or Nanya is used over the different impacted products.	First source remains either ASEMTL-SH or TCI or Kinsus or Nanya depending on the product. Second source supplier SCC for all impacted products.
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	NO CHANGE - Same Form, Fit, Function 1. Same substrate design for all package sizes, - Same Bonding diagram for each package - Same Package Outline Assembly (POA) 2. Same substrate Materials stack-up, 3. Same substrate Material thickness, 4. Same bill of material (BOM)	

5. Reason / motivation for change	
5.1 Motivation	Qualified new supplier to support customer demand
5.2 Customer Benefit	SERVICE IMPROVEMENT

6. Marking of parts / traceability of change	
6.1 Description	Traceability ensure by ST internal tools

7. Timing / schedule	
7.1 Date of qualification results	2023-07-13
7.2 Intended start of delivery	2023-09-06
7.3 Qualification sample available?	Not Applicable

8. Qualification / Validation			
8.1 Description	14199 MDG-GPM-RER2316 V1-PCI14199_ASEKH 2nd src SCC substrate for BGA5x5 to 18x18 for listed products - RER report.pdf		
8.2 Qualification report and qualification results	Available (see attachment)	**Issue Date**	2023-08-20

9. Attachments (additional documentations)
14199 Public product.pdf 14199 MDG-GPM-RER2316 V1-PCI14199_ASEKH 2nd src SCC substrate for BGA5x5 to 18x18 for listed products - RER report.pdf 14199 PCN14199 Additional information.pdf

10. Affected parts		
10. 1 Current		**10.2 New (if applicable)**
10.1.1 Customer Part No	**10.1.2 Supplier Part No**	**10.1.2 Supplier Part No**
	STM32F207ICH6	
	STM32F207IEH6	
	STM32F207IGH6	
	STM32F207IGH7	
	STM32F217IGH6	
	STM32F407IEH6	
	STM32F407IGH6	
	STM32F407IGH6TR	
	STM32F407IGH7	
	STM32F417IEH6	
	STM32F417IGH6	
	STM32F427IGH6	
	STM32F427IGH7	
	STM32F427IIH6	
	STM32F427IIH6TR	
	STM32F427IIH7	
	STM32F429IEH6	
	STM32F429IGH6	
	STM32F429IIH6	
	STM32F429IIH6TR	
	STM32F437IGH6	
	STM32F437IIH6	
	STM32F437IIH6TR	
	STM32F439IIH6	
	STM32G491REI6	
	STM32G4A1REI6	
	STM32H723ZGI6	
	STM32H725AEI6	
	STM32H725AGI6	
	STM32H725IGK6	
	STM32H730ABI6Q	
	STM32H730IBK6Q	
	STM32H735IGK6	
	STM32H743XIH6	
	STM32H745XGH6	
	STM32H745XIH6	
	STM32H747XIH6	
	STM32H750XBH6	
	STM32H753XIH6	

	STM32H755XIH3	
	STM32H755XIH6	
	STM32H757XIH6	
	STM32L072RBI6	
	STM32L072RZI6	
	STM32L151VCH6	
	STM32L151VCH6TR	
	STM32L152VCH6	
	STM32L162VCH6	
	STM32L431RBI6	
	STM32L431RCI6	
	STM32L431VCI6	
	STM32L433RBI6	
	STM32L433RCI3	
	STM32L433RCI6	
	STM32L433VCI3	
	STM32L433VCI6	
	STM32L443RCI3	
	STM32L443RCI6	
	STM32L443VCI6	
	STM32L451VCI6	
	STM32L451VEI6	
	STM32L452VCI6	
	STM32L452VEI6	
	STM32L462VEI6	
	STM32L471QEI6	
	STM32L471QGI6	
	STM32L476QEI6	
	STM32L476QGI3	
	STM32L476QGI6	
	STM32L476QGI6TR	
	STM32L486QGI6	
	STM32L486QGI6TR	
	STM32L496QEI6	
	STM32L496QGI3	
	STM32L496QGI6	
	STM32L496QGI6P	
	STM32L4A6QGI6	
	STM32L4A6QGI6P	
	STM32L4P5AGI6	
	STM32L4P5AGI6P	
	STM32L4Q5AGI6	
	STM32L4R5QGI6	
	STM32L4R5QII6	
	STM32L4S5QII6	
	STM32MP151AAA3	
	STM32MP151CAA3	
	STM32MP151CAA3T	
	STM32MP151FAA1	
	STM32MP153AAA3	
	STM32MP153CAA3	

	STM32MP157AAA3	
	STM32MP157AAA3T	
	STM32MP157CAA3	
	STM32MP157FAA1	
	STM32U585AII6	
	STM32U585AII6Q	
	STM32U585QII3	
	STM32U5A9NJH6Q	
	STM32WB55VCQ6	
	STM32WB55VCQ7	
	STM32WB55VEQ6	
	STM32WB55VEQ7	
	STM32WB55VGQ6	
	STM32WL55JCI6	
	STM32WL55JCI7	
	STM32WLE4JCI6	
	STM32WLE5J8I6	
	STM32WLE5JBI6	
	STM32WLE5JCI6	

Reliability Evaluation Report

MDG-GPM-RER2316

PCI14199

ASE Kaohsiung (Taiwan) - Second source SCC substrate for BGA5x5 to BGA18x18 for listed products

General Information	
Commercial Product	QE32L072RZI6 QE32H733ZGI6 QC32L4P5AGI6 QE32MP157CAA3 QE32U5A9NJH6Q
Product Line	447X66, 483X66,471X66,500X66,481X66
Die revision	Cut 2.1 Cut 1.1 Cut 1.1 Cut 2.1 Cut 2.0
Package	UFBGA 5X5X0.6 64L P 0.5 mm UFBGA 7x7x0.6 144L P0.5mm UFBGA 7x7x0.6 169L P 0.5 mm LFBGA18x18 448L P.8 B.4 TFBGA 13x13x1.2 216L P 0.8 mm
Silicon Technology	CMOSF9S, TN090CE, CMOS040, TN040CE, CMOSM40MI
Division	MDG-GPM

Traceability	
Diffusion Plant	Rousset 8, TSMC Fab14, Crolles 300
Assembly Plant	ASE Kaohsiung - TAIWAN

Reliability Assessment	
Pass	x
Fail	

Release	Date	Author	Function
1.0	July 11th, 2023	Céline NAVARRO	GPM BE Q&R

DOCUMENT ACTORS:

Name	Function	Location	Date
Berengere ROUTIER-SCAPPUCCI	GPM BE Q&R Manager	ROUSSET	July 12th, 2023
Pascal NARCHE	Subgroup Quality Manager	ROUSSET	July 13th, 2023

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RELIABILITY EVALUATION OVERVIEW

- **OBJECTIVE**

The aim of this report is to present the reliability evaluation performed for the qualification 2nd second source substrate supplier (SCC - Shennan Circuit Company) for BGA5x5 to BGA18x18.

PCI 14199 changes are described here below:

	Current condition Substrate supplier	New condition Substrate supplier
Assembly site	ASE Kaohsiung (Taiwan)	
From BGA5x5 To BGA18x18	ASEMTL-SH TCI Kinsus Nanya	(1st and 2nd source) ASEMTL-SH and SCC TCI and SCC Kinsus and SCC Nanya and SCC

- **CONCLUSION**

All reliability tests have been completed with positive results for BGA5x5 to BGA18x18. Neither functional nor parametric rejects were detected at final electrical testing.
Note: THB trial on BGA 18x18 (die 500) is for monitoring and will be completed in August 2023.

Package oriented tests have not put in evidence any criticality. Physical analysis performed on samples submitted to tests has not put in evidence any issue. ESD CDM are in accordance with ST spec.

According to good reliability tests results in line with validated product mission profile and reliability strategy, the qualification is granted for second source substrate supplier (SCC - Shennan Circuit Company) for BGA5x5 to BGA18x18 in ASE Kaohsiung.

Refer to Section 3.0 for reliability test results.

TABLE OF CONTENT

1. RELIABILITY STRATEGY

Reliability trials performed as part of this reliability evaluation are in agreement with ST 0061692 specification, in full compliancy with the JESD-47 international standard.

For details on test conditions, generic data used and specifications references, refer to test results summary in section 3.

2. PRODUCT OR TEST VEHICLE CHARACTERISTICS

2.1. Generalities

.

Package line	Partial rawline code	Number of lots
UFBGA 5x5 64L	E12I*447QEXZ	1
UFBGA 7x7 144L	E1L4*483QEXZ	1
UFBGA 7x7 169L	20OQ*471QCXZ	1
LFBGA 18x18 448L	E1GU*500QEXZ	1
TFBGA 13X13 216L	E2RM*481QEXB	1

2.2. Traceability

2.2.1. Wafer Fab Information

Main die 483XXXZ

Wafer Fab Information	
FAB	
Wafer fab name / location	Crolles 300
Wafer diameter (inches)	12
Wafer thickness (µm)	775 ± 25
Silicon process technology	CMOS040
Number of masks	51
Die finishing front side (passivation) materials	PSG + NITRIDE
Die finishing back side Materials	RAW SILICON
Die area (Stepping die size)	15.668775 mm² (3753, 4175)
Die pad size	**Geometry**: Rectangular; **Open(X,Y)**: 54.9,54.4 µm
Sawing street width (X,Y) (µm)	80,80
Metal levels/Materials/Thicknesses	

Wire bond pad metal	Composition	Thickness
1	Cu	0.13 µm
2	Cu	0.14 µm
3	Cu	0.14 µm
4	Cu	0.14 µm
5	Cu	0.14 µm
6	Cu	0.85 µm
7	Cu	0.85 µm
8	Ta/TaN/AlCu	1.525 µm

Main die - S447XXXZ

Wafer Fab Information	
FAB	
Wafer fab name / location	ST SAS Rousset / Rousset 8
Wafer diameter (inches)	8
Wafer thickness (µm)	375
Silicon process technology	CMOSF9S
Number of masks	37
Die finishing front side (passivation) materials	USG + NitUV (HFP USG+UV Nitride)
Die finishing back side Materials	RAW SILICON - BACK GRINDING
Die area (Stepping die size)	10.962397 mm² (3329, 3293)
Die pad size	**Geometry**: Rectangular; **Open(X,Y)**: 53,108 µm
Sawing street width (X,Y) (µm)	80,80
Metal levels/Materials/Thicknesses	

Wire bond pad metal	Composition	Thickness
1	TaN/Ta/Cu	0.28 µm
2	Ti/AlCu/TxTN	0.31 µm
3	Ti/AlCu/TxTN	0.31 µm
4	Ti/AlCu/TxTN	0.31 µm
5	Ti/AlCu/TxTN	1.2 µm

Main die - R471XXXZ

Wafer Fab Information	
FAB	
Wafer fab name / location	TSMC Taiwan / TSMC Fab14 DIFF
Wafer diameter (inches)	12
Wafer thickness (µm)	775
Silicon process technology	TN090CE
Number of masks	46
Die finishing front side (passivation) materials	USG + NITRIDE
Die finishing back side Materials	RAW SILICON
Die area (Stepping die size)	20.12679744 mm² (4476.8, 4495.8)
Die pad size	**Geometry**: Rectangular; **Open(X,Y)**: 123,59 µm
Sawing street width (X,Y) (µm)	80,80

Metal levels/Materials/Thicknesses

Wire bond pad metal	Composition	Thickness
1	TaN/Ta/CuSeed/Cu	0.24 µm
2	TaN/Ta/CuSeed/Cu	0.31 µm
3	TaN/Ta/CuSeed/Cu	0.31 µm
4	TaN/Ta/CuSeed/Cu	0.31 µm
5	TaN/Ta/CuSeed/Cu	0.31 µm
6	TaN/Ta/CuSeed/Cu	0.85 µm
7	AlCu	1.45 µm

Main die - R500XXXZ

Wafer Fab Information	
FAB	
Wafer fab name / location	Crolles 300
Wafer diameter (inches)	12
Wafer thickness (µm)	775
Silicon process technology	CMOS040
Number of masks	39
Die finishing front side (passivation) materials	PSG + NITRIDE
Die finishing back side Materials	RAW SILICON
Die area (Stepping die size)	26.2236 mm² (5200, 5043)
Die pad size	**Geometry**: Rectangular; **Open(X,Y)**: 41.4,90 µm
Sawing street width (X,Y) (µm)	72,72
Metal levels/Materials/Thicknesses	

Wire bond pad metal	Composition	Thickness
1	Cu	0.13 µm
2	Cu	0.14 µm
3	Cu	0.14 µm
4	Cu	0.14 µm
5	Cu	0.14 µm
6	Cu	0.9 µm
7	Cu	0.9 µm
8	Ta/TaN/AlCu	1.45 µm

Main die - R481XXXB

Wafer Fab Information	
FAB	
Wafer fab name / location	TSMC Taiwan / TSMC Fab14
Wafer diameter (inches)	12
Wafer thickness (µm)	775
Silicon process technology	TN040CE
Number of masks	54
Die finishing front side (passivation) materials	Oxide + Nitride
Die finishing back side Materials	RAW SILICON
Die area (Stepping die size)	29.66201 mm² (5398, 5495)
Die pad size	**Geometry** / **Open(X,Y)** Rectangular / 54.9,54.9 µm Rectangular / 54.9,55.38 µm
Sawing street width (X,Y) (µm)	80,196.8
Metal levels/Materials/Thicknesses	**Wire bond pad metal** / **Composition** / **Thickness** 1 / Cu / 0.125 µm 2 / Cu / 0.145 µm 3 / Cu / 0.145 µm 4 / Cu / 0.145 µm 5 / Cu / 0.145 µm 6 / Cu / 0.85 µm 7 / Cu / 3.5 µm 8 / Al / 1.5 µm

2.2.2. Assembly Information

Assembly Information	
Package 1: UFBGA 5X5X0.6 64L P 0.5 MM	**Die 447**
Assembly plant name / location	ASE TAIWAN / SC ASE - TAIWAN
Pitch (mm)	0.5
Die thickness after back-grinding (µm)	75±12
Die sawing method	Mechanical sawing
Bill of Material elements	
Substrate material/supplier/reference	UFBGA 5x5 64L P0.5 ASE A25619
Type(glue/film)/ die attach material/ supplier	ABLESTICK ATB-125
Balls metallurgy/diameter (BGA)	200 DIAM SN96.5 AG3.5%
Wire bonding material/diameter	Gold 0.8 mils
Molding compound material/supplier/reference	Resin KYOCERA G1250AAS ULA
Package Moisture Sensitivity Level (JEDEC J-STD020D)	3
Package 2: UFBGA 7x7 144L P 0.5 MM	**Die 483**
Assembly plant name / location	ASE TAIWAN / SC ASE - TAIWAN
Pitch (mm)	0.5
Die thickness after back-grinding (µm)	75±10
Die sawing method	Laser groove + mechanical sawing
Bill of Material elements	
Substrate material/supplier/reference	UFBGA 7x7 144L 483 ASE A26879
Type(glue/film)/ die attach material/ supplier	ABLESTICK ATB-125
Balls metallurgy/diameter (BGA)	SOLDER BALLS WITH 200 DIAM SN96.5 AG3.5%
Wire bonding material/diameter	gold 0.8 mils
Molding compound material/supplier/reference	Resin KYOCERA G1250AAS ULA
Package Moisture Sensitivity Level (JEDEC J-STD020D)	3
Package 3: UFBGA 7X7 169L P 0.5 MM	**Die 471**
Assembly plant name / location	ASE TAIWAN / SC ASE - TAIWAN
Pitch (mm)	0.5
Die thickness after back-grinding (µm)	75±10
Die sawing method	Laser groove + mechanical sawing
Bill of Material elements	
Substrate material/supplier/reference	UFBGA 7x7 169L P0.5 LEGACY ASE A26829
Type(glue/film)/ die attach material/ supplier	ABLESTICK ATB-125
Balls metallurgy/diameter (BGA)	SOLDER BALLS WITH 200 DIAM SN96.5 AG3.5%
Wire bonding material/diameter	CuPd 0.8 mils
Molding compound material/supplier/reference	Resin KYOCERA G1250AAS ULA
Package Moisture Sensitivity Level (JEDEC J-STD020D)	3

Package 4: LFBGA18x18 448L 0.8 MM PITCH	Die 500
Assembly plant name / location	SC AMKOR ATK4 - KOREA
Pitch (mm)	0.8
Die thickness after back-grinding (µm)	102±10
Die sawing method	Laser groove + mechanical sawing
Bill of Material elements	
Substrate material/supplier/reference	LFBGA 18x18 448L P0.8 ASE A28411
Type(glue/film)/ die attach material/ supplier	ABLESTICK ATB-125
Balls metallurgy/diameter (BGA)	SOLDER BALLS WITH 400 DIAM SACN305
Wire bonding material/diameter	gold 0.7 mils
Molding compound material/supplier/reference	Resin KYOCERA G1250AAS ULA
Package Moisture Sensitivity Level (JEDEC J-STD020D)	3
Package 5: TFBGA 13X13X1.2 216L 0.8 MM PITCH	**Die 481**
Assembly plant name / location	SC AMKOR ATK4 - KOREA
Pitch (mm)	0.8
Die thickness after back-grinding (µm)	100±15
Die sawing method	Laser groove + mechanical sawing
Bill of Material elements	
Substrate material/supplier/reference	TFBGA 13X13 216L SID A29154-A ASEKH
Type(glue/film)/ die attach material/ supplier	ABLESTICK ATB-125
Balls metallurgy/diameter (BGA)	Solder balls SACN305 0.4 mm DIA
Wire bonding material/diameter	GOLD 0.8mils
Molding compound material/supplier/reference	Resin KYOCERA G1250AAS ULA
Package Moisture Sensitivity Level (JEDEC J-STD020D)	3

2.2.3.Reliability testing information

Reliability Testing Information	
Reliability laboratory name / location	Grenoble Rel Lab, Rousset MDG Rel Lab, Shenzhen BE Lab

Note: ST is ISO 9001 certified. This induces certification of all internal and subcontractor labs. ST certification document can be downloaded under the following link: http://www.st.com/content/st_com/en/support/quality-and-reliability/certifications.html

3. TEST RESULTS SUMMARY

3.1. Lot information

Lot #	Diffusion Lot / Wafer ID	Die Revision (Cut)	Assy Lot / Trace Code	Raw Line	Package	Note
Lot 1	VG219565	Cut 2.1	AA236001	E12I*447QEXZ	UFBGA 5X5X0.6 64L 0.5 MM PITCH	1 Reliability lot including CDM +CA
Lot 2	VQ202356	Cut 2.1	AA235004	E1L4*483QEXZ	UFBGA 7x7x0.60 144L 0.5 MM PITCH	1 Reliability lot including CDM +CA
Lot 3	9R205599	Cut 2.1	AA235006	20OQ*471QCXZ	UFBGA 7X7X0.6 169L 0.5 MM PITCH	1 Reliability lot including CDM +CA
Lot4	VQ212622	Cut 2.1	AA235023	E1GU*500QEXZ	LFBGA18X18 448L 0.8 MM PITCH	1 Reliability lot including CDM +CA
Lot5	9R119304	Cut 2.1	AA238011	E2RM*481QEXB	TFBGA 13X13X1.2 216L 0.8 MM PITCH	1 Reliability lot including CDM +CA

3.2. Test plan and results summary

ACCELERATED ENVIRONMENT STRESS TESTS

Test code	Stress method	Stress Conditions	Lots Qty	S.S.	Total	Results/Lot Fail/S.S.	Comments:(N/A =Not Applicable)
PC	JSTD 020 JESD 22-A113 7191395	24h bake@125°C, MSL3 (192h/30°C/60%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	5	308	1540	Lot 1: 0/308 Lot 2: 0/308 Lot 3: 0/308 Lot 4: 0/308 Lot 5: 0/308	NA
HTSL	JESD22-A103	Ta= 150°C Duration= 1000hrs ☑ After PC	5	77	385	Lot 1: 0/77 Lot 2: 0/77 Lot 3: 0/77 Lot 4: 0/77 Lot 5: 0/77	NA
TC	JESD22-A104	Ta= -50 to 150°C Cyc= 1000 ☑ After PC	5	77	385	Lot 1: 0/77 Lot 2: 0/77 Lot 3: 0/77 Lot 4: 0/77 Lot 5: 0/77	NA
THB	JESD22-A101	Ta= 85%HR/85°C/VDD max Duration= 1000hrs ☑ After PC	5	77	385	Lot 1: 0/77 Lot 2: 0/77 Lot 3: 0/77 Lot 4: Aug'23* Lot 5: 0/77	(*) THB die 500 is for monitoring
UHAST	JESD22-A118	Ta= 130°C/85%RH Duration= 96hrs ☑ After PC	5	77	385	Lot 1: 0/77 Lot 2: 0/77 Lot 3: 0/77 Lot 4: 0/77 Lot 5: 0/77	NA

ELECTRICAL VERIFICATION TESTS

Test code	Stress method	Stress Conditions	Lots Qty	S.S.	Total	Results/Lot Fail/S.S.	Comments:(N/A =Not Applicable)
ESD CDM	JEDEC JS-002	Voltage=500V for die 447 500V for die 483 250V for die 471 250V for die 500 500V for die 481	5	3	15	Lot 1: 0/3 Lot 2: 0/3 Lot 3: 0/3 Lot 4: 0/3 Lot 5: 0/3	NA

PACKAGE ASSEMBLY INTEGRITY TESTS

Test code	Stress method	Stress Conditions	Lots Qty	S.S.	Total	Results/Lot Fail/S.S.	Comments:(N/A =Not Applicable)
CA	Construction analysis including solderability, physical dimensions, wire pull & ball shear	JESD 22B102 JESD B100/ B108 ST internal specifications	6	50	300	Lot 1: 0/50 Lot 2: 0/50 Lot 3: 0/50 Lot 4: 0/50 Lot 5: 0/50	SHZ_CA_22_00449 SHZ_CA_22_00471 SHZ_CA_22_00472 SHZ_CA_22_00056 SHZ_CA_22_00034

Note: Test method revision reference is the one active at the date of reliability trial execution.

4. APPLICABLE AND REFERENCE DOCUMENTS

Reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
SOP2.4.4	Record Management Procedure
SOP2.6.2	Internal Change Management
SOP2.6.7	Finished Good Maturity Management
SOP2.6.9	Package & Process Maturity Management in BE
SOP2.6.11	Program Management for Product Development
SOP2.6.17	Management of Manufacturing Transfers
SOP2.6.19	Front-End Technology Platform Development and Qualification
DMS 0061692	Reliability Tests and Criteria for Product Qualification
JEDEC JS-002	Electrostatic discharge (ESD) sensitivity testing charge device model (CDM)
JESD 22-A103	High Temperature Storage Life
J-STD-020	Moisture/reflow sensitivity classification for non-hermetic solid state surface mount devices
JESD22-A113	Preconditioning of non-hermetic surface mount devices prior to reliability testing
JESD22-A118	Unbiased Highly Accelerated temperature & humidity Stress Test
JESD22-A104	Temperature cycling
JESD22-A101	Temperature Humidity Bias
JESD 22B102	Solderability test
JESD B100/ B108	Physical dimension

5. GLOSSARY

ESD - CDM	Electrostatic Discharge - Charged device model
CA	Construction analysis
HTSL	Storage Life High temperature storage life
PC	Preconditioning
TC	Temperature Cycling
THB	Temperature Humidity Bias
UHAST	Unbiased HAST (Highly Accelerated Stress Test)
DMS	ST Advanced Documentation Controlled system/ Documentation Management System

6. REVISION HISTORY

Release	Date	Description
1.0	July 11th , 2023	Initial release

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Reliability Evaluation Report

MDG-GPM-RER2316

PCI14199

ASE Kaohsiung (Taiwan) - Second source SCC substrate for BGA5x5 to BGA18x18 for listed products

General Information	
Commercial Product	QE32L072RZI6 QE32H733ZGI6 QC32L4P5AGI6 QE32MP157CAA3 QE32U5A9NJH6Q
Product Line	447X66, 483X66,471X66,500X66,481X66
Die revision	Cut 2.1 Cut 1.1 Cut 1.1 Cut 2.1 Cut 2.0
Package	UFBGA 5X5X0.6 64L P 0.5 mm UFBGA 7x7x0.6 144L P0.5mm UFBGA 7x7x0.6 169L P 0.5 mm LFBGA18x18 448L P.8 B.4 TFBGA 13x13x1.2 216L P 0.8 mm
Silicon Technology	CMOSF9S, TN090CE, CMOS040, TN040CE, CMOSM40MI
Division	MDG-GPM

Traceability	
Diffusion Plant	Rousset 8, TSMC Fab14, Crolles 300
Assembly Plant	ASE Kaohsiung - TAIWAN

Reliability Assessment	
Pass	x
Fail	

Release	Date	Author	Function
1.0	July 11th, 2023	Céline NAVARRO	GPM BE Q&R

DOCUMENT ACTORS:

Name	Function	Location	Date
Berengere ROUTIER-SCAPPUCCI	GPM BE Q&R Manager	ROUSSET	July 12th, 2023
Pascal NARCHE	Subgroup Quality Manager	ROUSSET	July 13th, 2023

This report is a summary of the reliability trials performed in good faith by STMicroelectronics. This report does not imply for STMicroelectronics expressly or implicitly any contractual obligations other than as set forth in STMicroelectronics General Terms and Conditions of Sale.

RELIABILITY EVALUATION OVERVIEW

- **OBJECTIVE**

The aim of this report is to present the reliability evaluation performed for the qualification 2nd second source substrate supplier (SCC - Shennan Circuit Company) for BGA5x5 to BGA18x18.

PCI 14199 changes are described here below:

	Current condition Substrate supplier	New condition Substrate supplier
Assembly site	ASE Kaohsiung (Taiwan)	
From BGA5x5 To BGA18x18	ASEMTL-SH TCI Kinsus Nanya	(1st and 2nd source) ASEMTL-SH and SCC TCI and SCC Kinsus and SCC Nanya and SCC

- **CONCLUSION**

All reliability tests have been completed with positive results for BGA5x5 to BGA18x18. Neither functional nor parametric rejects were detected at final electrical testing.
Note: THB trial on BGA 18x18 (die 500) is for monitoring and will be completed in August 2023.

Package oriented tests have not put in evidence any criticality. Physical analysis performed on samples submitted to tests has not put in evidence any issue. ESD CDM are in accordance with ST spec.

According to good reliability tests results in line with validated product mission profile and reliability strategy, the qualification is granted for second source substrate supplier (SCC - Shennan Circuit Company) for BGA5x5 to BGA18x18 in ASE Kaohsiung.

Refer to Section 3.0 for reliability test results.

TABLE OF CONTENT

1. RELIABILITY STRATEGY

Reliability trials performed as part of this reliability evaluation are in agreement with ST 0061692 specification, in full compliancy with the JESD-47 international standard.

For details on test conditions, generic data used and specifications references, refer to test results summary in section 3.

2. PRODUCT OR TEST VEHICLE CHARACTERISTICS

2.1. Generalities

.

Package line	Partial rawline code	Number of lots
UFBGA 5x5 64L	E12I*447QEXZ	1
UFBGA 7x7 144L	E1L4*483QEXZ	1
UFBGA 7x7 169L	20OQ*471QCXZ	1
LFBGA 18x18 448L	E1GU*500QEXZ	1
TFBGA 13X13 216L	E2RM*481QEXB	1

2.2. Traceability

2.2.1. Wafer Fab Information

Main die 483XXXZ

Wafer Fab Information	
FAB	
Wafer fab name / location	Crolles 300
Wafer diameter (inches)	12
Wafer thickness (µm)	775 ± 25
Silicon process technology	CMOS040
Number of masks	51
Die finishing front side (passivation) materials	PSG + NITRIDE
Die finishing back side Materials	RAW SILICON
Die area (Stepping die size)	15.668775 mm² (3753, 4175)
Die pad size	**Geometry**: Rectangular; **Open(X,Y)**: 54.9,54.4 µm
Sawing street width (X,Y) (µm)	80,80
Metal levels/Materials/Thicknesses	

Wire bond pad metal	Composition	Thickness
1	Cu	0.13 µm
2	Cu	0.14 µm
3	Cu	0.14 µm
4	Cu	0.14 µm
5	Cu	0.14 µm
6	Cu	0.85 µm
7	Cu	0.85 µm
8	Ta/TaN/AlCu	1.525 µm

Main die - S447XXXZ

Wafer Fab Information	
FAB	
Wafer fab name / location	ST SAS Rousset / Rousset 8
Wafer diameter (inches)	8
Wafer thickness (µm)	375
Silicon process technology	CMOSF9S
Number of masks	37
Die finishing front side (passivation) materials	USG + NitUV (HFP USG+UV Nitride)
Die finishing back side Materials	RAW SILICON - BACK GRINDING
Die area (Stepping die size)	10.962397 mm² (3329, 3293)
Die pad size	**Geometry**: Rectangular; **Open(X,Y)**: 53,108 µm
Sawing street width (X,Y) (µm)	80,80
Metal levels/Materials/Thicknesses	

Wire bond pad metal	Composition	Thickness
1	TaN/Ta/Cu	0.28 µm
2	Ti/AlCu/TxTN	0.31 µm
3	Ti/AlCu/TxTN	0.31 µm
4	Ti/AlCu/TxTN	0.31 µm
5	Ti/AlCu/TxTN	1.2 µm

Main die - R471XXXZ

Wafer Fab Information	
FAB	
Wafer fab name / location	TSMC Taiwan / TSMC Fab14 DIFF
Wafer diameter (inches)	12
Wafer thickness (µm)	775
Silicon process technology	TN090CE
Number of masks	46
Die finishing front side (passivation) materials	USG + NITRIDE
Die finishing back side Materials	RAW SILICON
Die area (Stepping die size)	20.12679744 mm² (4476.8, 4495.8)
Die pad size	**Geometry**: Rectangular; **Open(X,Y)**: 123,59 µm
Sawing street width (X,Y) (µm)	80,80

Metal levels/Materials/Thicknesses

Wire bond pad metal	Composition	Thickness
1	TaN/Ta/CuSeed/Cu	0.24 µm
2	TaN/Ta/CuSeed/Cu	0.31 µm
3	TaN/Ta/CuSeed/Cu	0.31 µm
4	TaN/Ta/CuSeed/Cu	0.31 µm
5	TaN/Ta/CuSeed/Cu	0.31 µm
6	TaN/Ta/CuSeed/Cu	0.85 µm
7	AlCu	1.45 µm

Main die - R500XXXZ

Wafer Fab Information	
FAB	
Wafer fab name / location	Crolles 300
Wafer diameter (inches)	12
Wafer thickness (µm)	775
Silicon process technology	CMOS040
Number of masks	39
Die finishing front side (passivation) materials	PSG + NITRIDE
Die finishing back side Materials	RAW SILICON
Die area (Stepping die size)	26.2236 mm² (5200, 5043)
Die pad size	**Geometry**: Rectangular; **Open(X,Y)**: 41.4,90 µm
Sawing street width (X,Y) (µm)	72,72
Metal levels/Materials/Thicknesses	

Wire bond pad metal	Composition	Thickness
1	Cu	0.13 µm
2	Cu	0.14 µm
3	Cu	0.14 µm
4	Cu	0.14 µm
5	Cu	0.14 µm
6	Cu	0.9 µm
7	Cu	0.9 µm
8	Ta/TaN/AlCu	1.45 µm

Main die - R481XXXB

Wafer Fab Information	
FAB	
Wafer fab name / location	TSMC Taiwan / TSMC Fab14
Wafer diameter (inches)	12
Wafer thickness (µm)	775
Silicon process technology	TN040CE
Number of masks	54
Die finishing front side (passivation) materials	Oxide + Nitride
Die finishing back side Materials	RAW SILICON
Die area (Stepping die size)	29.66201 mm² (5398, 5495)
Die pad size	**Geometry** / **Open(X,Y)** Rectangular / 54.9,54.9 µm Rectangular / 54.9,55.38 µm
Sawing street width (X,Y) (µm)	80,196.8
Metal levels/Materials/Thicknesses	**Wire bond pad metal** / **Composition** / **Thickness** 1 / Cu / 0.125 µm 2 / Cu / 0.145 µm 3 / Cu / 0.145 µm 4 / Cu / 0.145 µm 5 / Cu / 0.145 µm 6 / Cu / 0.85 µm 7 / Cu / 3.5 µm 8 / Al / 1.5 µm

2.2.2. Assembly Information

Assembly Information	
Package 1: UFBGA 5X5X0.6 64L P 0.5 MM	**Die 447**
Assembly plant name / location	ASE TAIWAN / SC ASE - TAIWAN
Pitch (mm)	0.5
Die thickness after back-grinding (µm)	75±12
Die sawing method	Mechanical sawing
Bill of Material elements	
Substrate material/supplier/reference	UFBGA 5x5 64L P0.5 ASE A25619
Type(glue/film)/ die attach material/ supplier	ABLESTICK ATB-125
Balls metallurgy/diameter (BGA)	200 DIAM SN96.5 AG3.5%
Wire bonding material/diameter	Gold 0.8 mils
Molding compound material/supplier/reference	Resin KYOCERA G1250AAS ULA
Package Moisture Sensitivity Level (JEDEC J-STD020D)	3
Package 2: UFBGA 7x7 144L P 0.5 MM	**Die 483**
Assembly plant name / location	ASE TAIWAN / SC ASE - TAIWAN
Pitch (mm)	0.5
Die thickness after back-grinding (µm)	75±10
Die sawing method	Laser groove + mechanical sawing
Bill of Material elements	
Substrate material/supplier/reference	UFBGA 7x7 144L 483 ASE A26879
Type(glue/film)/ die attach material/ supplier	ABLESTICK ATB-125
Balls metallurgy/diameter (BGA)	SOLDER BALLS WITH 200 DIAM SN96.5 AG3.5%
Wire bonding material/diameter	gold 0.8 mils
Molding compound material/supplier/reference	Resin KYOCERA G1250AAS ULA
Package Moisture Sensitivity Level (JEDEC J-STD020D)	3
Package 3: UFBGA 7X7 169L P 0.5 MM	**Die 471**
Assembly plant name / location	ASE TAIWAN / SC ASE - TAIWAN
Pitch (mm)	0.5
Die thickness after back-grinding (µm)	75±10
Die sawing method	Laser groove + mechanical sawing
Bill of Material elements	
Substrate material/supplier/reference	UFBGA 7x7 169L P0.5 LEGACY ASE A26829
Type(glue/film)/ die attach material/ supplier	ABLESTICK ATB-125
Balls metallurgy/diameter (BGA)	SOLDER BALLS WITH 200 DIAM SN96.5 AG3.5%
Wire bonding material/diameter	CuPd 0.8 mils
Molding compound material/supplier/reference	Resin KYOCERA G1250AAS ULA
Package Moisture Sensitivity Level (JEDEC J-STD020D)	3

Package 4: LFBGA18x18 448L 0.8 MM PITCH	Die 500
Assembly plant name / location	SC AMKOR ATK4 - KOREA
Pitch (mm)	0.8
Die thickness after back-grinding (µm)	102±10
Die sawing method	Laser groove + mechanical sawing
Bill of Material elements	
Substrate material/supplier/reference	LFBGA 18x18 448L P0.8 ASE A28411
Type(glue/film)/ die attach material/ supplier	ABLESTICK ATB-125
Balls metallurgy/diameter (BGA)	SOLDER BALLS WITH 400 DIAM SACN305
Wire bonding material/diameter	gold 0.7 mils
Molding compound material/supplier/reference	Resin KYOCERA G1250AAS ULA
Package Moisture Sensitivity Level (JEDEC J-STD020D)	3
Package 5: TFBGA 13X13X1.2 216L 0.8 MM PITCH	**Die 481**
Assembly plant name / location	SC AMKOR ATK4 - KOREA
Pitch (mm)	0.8
Die thickness after back-grinding (µm)	100±15
Die sawing method	Laser groove + mechanical sawing
Bill of Material elements	
Substrate material/supplier/reference	TFBGA 13X13 216L SID A29154-A ASEKH
Type(glue/film)/ die attach material/ supplier	ABLESTICK ATB-125
Balls metallurgy/diameter (BGA)	Solder balls SACN305 0.4 mm DIA
Wire bonding material/diameter	GOLD 0.8mils
Molding compound material/supplier/reference	Resin KYOCERA G1250AAS ULA
Package Moisture Sensitivity Level (JEDEC J-STD020D)	3

2.2.3.Reliability testing information

Reliability Testing Information	
Reliability laboratory name / location	Grenoble Rel Lab, Rousset MDG Rel Lab, Shenzhen BE Lab

Note: ST is ISO 9001 certified. This induces certification of all internal and subcontractor labs. ST certification document can be downloaded under the following link: http://www.st.com/content/st_com/en/support/quality-and-reliability/certifications.html

3. TEST RESULTS SUMMARY

3.1. Lot information

Lot #	Diffusion Lot / Wafer ID	Die Revision (Cut)	Assy Lot / Trace Code	Raw Line	Package	Note
Lot 1	VG219565	Cut 2.1	AA236001	E12I*447QEXZ	UFBGA 5X5X0.6 64L 0.5 MM PITCH	1 Reliability lot including CDM +CA
Lot 2	VQ202356	Cut 2.1	AA235004	E1L4*483QEXZ	UFBGA 7x7x0.60 144L 0.5 MM PITCH	1 Reliability lot including CDM +CA
Lot 3	9R205599	Cut 2.1	AA235006	20OQ*471QCXZ	UFBGA 7X7X0.6 169L 0.5 MM PITCH	1 Reliability lot including CDM +CA
Lot4	VQ212622	Cut 2.1	AA235023	E1GU*500QEXZ	LFBGA18X18 448L 0.8 MM PITCH	1 Reliability lot including CDM +CA
Lot5	9R119304	Cut 2.1	AA238011	E2RM*481QEXB	TFBGA 13X13X1.2 216L 0.8 MM PITCH	1 Reliability lot including CDM +CA

3.2. Test plan and results summary

ACCELERATED ENVIRONMENT STRESS TESTS

Test code	Stress method	Stress Conditions	Lots Qty	S.S.	Total	Results/Lot Fail/S.S.	Comments:(N/A =Not Applicable)
PC	JSTD 020 JESD 22-A113 7191395	24h bake@125°C, MSL3 (192h/30°C/60%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	5	308	1540	Lot 1: 0/308 Lot 2: 0/308 Lot 3: 0/308 Lot 4: 0/308 Lot 5: 0/308	NA
HTSL	JESD22-A103	Ta= 150°C Duration= 1000hrs ☑ After PC	5	77	385	Lot 1: 0/77 Lot 2: 0/77 Lot 3: 0/77 Lot 4: 0/77 Lot 5: 0/77	NA
TC	JESD22-A104	Ta= -50 to 150°C Cyc= 1000 ☑ After PC	5	77	385	Lot 1: 0/77 Lot 2: 0/77 Lot 3: 0/77 Lot 4: 0/77 Lot 5: 0/77	NA
THB	JESD22-A101	Ta= 85%HR/85°C/VDD max Duration= 1000hrs ☑ After PC	5	77	385	Lot 1: 0/77 Lot 2: 0/77 Lot 3: 0/77 Lot 4: Aug'23* Lot 5: 0/77	(*) THB die 500 is for monitoring
UHAST	JESD22-A118	Ta= 130°C/85%RH Duration= 96hrs ☑ After PC	5	77	385	Lot 1: 0/77 Lot 2: 0/77 Lot 3: 0/77 Lot 4: 0/77 Lot 5: 0/77	NA

ELECTRICAL VERIFICATION TESTS

Test code	Stress method	Stress Conditions	Lots Qty	S.S.	Total	Results/Lot Fail/S.S.	Comments:(N/A =Not Applicable)
ESD CDM	JEDEC JS-002	Voltage=500V for die 447 500V for die 483 250V for die 471 250V for die 500 500V for die 481	5	3	15	Lot 1: 0/3 Lot 2: 0/3 Lot 3: 0/3 Lot 4: 0/3 Lot 5: 0/3	NA

PACKAGE ASSEMBLY INTEGRITY TESTS

Test code	Stress method	Stress Conditions	Lots Qty	S.S.	Total	Results/Lot Fail/S.S.	Comments:(N/A =Not Applicable)
CA	Construction analysis including solderability, physical dimensions, wire pull & ball shear	JESD 22B102 JESD B100/ B108 ST internal specifications	6	50	300	Lot 1: 0/50 Lot 2: 0/50 Lot 3: 0/50 Lot 4: 0/50 Lot 5: 0/50	SHZ_CA_22_00449 SHZ_CA_22_00471 SHZ_CA_22_00472 SHZ_CA_22_00056 SHZ_CA_22_00034

Note: Test method revision reference is the one active at the date of reliability trial execution.

4. APPLICABLE AND REFERENCE DOCUMENTS

Reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
SOP2.4.4	Record Management Procedure
SOP2.6.2	Internal Change Management
SOP2.6.7	Finished Good Maturity Management
SOP2.6.9	Package & Process Maturity Management in BE
SOP2.6.11	Program Management for Product Development
SOP2.6.17	Management of Manufacturing Transfers
SOP2.6.19	Front-End Technology Platform Development and Qualification
DMS 0061692	Reliability Tests and Criteria for Product Qualification
JEDEC JS-002	Electrostatic discharge (ESD) sensitivity testing charge device model (CDM)
JESD 22-A103	High Temperature Storage Life
J-STD-020	Moisture/reflow sensitivity classification for non-hermetic solid state surface mount devices
JESD22-A113	Preconditioning of non-hermetic surface mount devices prior to reliability testing
JESD22-A118	Unbiased Highly Accelerated temperature & humidity Stress Test
JESD22-A104	Temperature cycling
JESD22-A101	Temperature Humidity Bias
JESD 22B102	Solderability test
JESD B100/ B108	Physical dimension

5. GLOSSARY

ESD - CDM	Electrostatic Discharge - Charged device model
CA	Construction analysis
HTSL	Storage Life High temperature storage life
PC	Preconditioning
TC	Temperature Cycling
THB	Temperature Humidity Bias
UHAST	Unbiased HAST (Highly Accelerated Stress Test)
DMS	ST Advanced Documentation Controlled system/ Documentation Management System

6. REVISION HISTORY

Release	Date	Description
1.0	July 11th , 2023	Initial release

Public Products List

Publict Products are off the shelf products. They are not dedicated to specific customers, they are available through ST Sales team, or Distributors, and visible on ST.com

PCI Title : ASE Kaohsiung (Taiwan) - qualification of a second source substrate supplier (SCC - Shennan Circuit Company) for BGA package, size from BGA5x5 to BGA18x18, for listed products

PCI Reference : MDG/23/14199

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

STM32WB55VCQ6	STM32L471QGI6	STM32H755XIH3
STM32L433VCI3	STM32F439IIH7	STM32F427IIH6TR
STM32F407IEH7	STM32F217IGH6TR	STM32F207IFH6TR
STM32L452VCI6	STM32U575QGI6TR	STM32L072RBI6
STM32L4R5QGI6TR	STM32F407IGH6TR	STM32F407IEH6
STM32L431VCI7TR	STM32F207IGH7	STM32L486QGI6
STM32F217IEH6	STM32MP151DAA1	STM32F439IIH6
STM32WL54JCI6	STM32L4P5QEI6	STM32F207IEH6TR
STM32L476QGI3TR	STM32F429IIH6TR	STM32L443VCI6
STM32H750XBH6	STM32MP151CAA3T	STM32F427IIH6
STM32F207IEH6	STM32MP151AAA3T	STM32F207ICH6
STM32L431VCI6	STM32G474PEI6	STM32F207IGH6
STM32L072RBI6TR	STM32WL54JCI7	STM32U585QII6
STM32F427IIH7	STM32WB55VEQ6TR	STM32G491REI6
STM32F439IIH6TR	STM32L471QEI7	STM32F417IGH6TR
STM32G0B1RCI6N	STM32H755XIH6	STM32U585QII3Q
STM32L072RZI6	STM32L486QGI6TR	STM32L462VEI6
STM32F427IGH7	STM32WLE5JCI7	STM32F427IGH6
STM32L476QEI6	STM32F417IGH6	STM32U585QII3QTR
STM32G473PCI6	STM32L431RBI6TR	STM32L496QEI6
STM32U585AII3	STM32MP157FAA1	STM32L072RZI6DTR
STM32G473PEI6	STM32L476QGI6TR	STM32G491RCI6
STM32WB55VGQ6	STM32L151VCH6TR	STM32L443RCI3TR
STM32F417IEH6	STM32U575AGI6TR	STM32L431RBI6
STM32MP157AAA3	STM32G0B1REI6N	STM32F439IGH6
STM32MP157CAA3	STM32U585QII6Q	STM32H730IBK6Q
STM32L073RZI6	STM32L452VEI6TR	STM32G0B1VCI6
STM32L496QGI3	STM32F427IGH6TR	STM32L072RZI6D
STM32H743XIH6	STM32F407IGH7	STM32L4R5QII6P
STM32L431RCI6TR	STM32F407IEH6TR	STM32MP153AAA3
STM32F437IIH6TR	STM32L451VEI6	STM32L073RZI6TR
STM32U585AII6	STM32L433RBI6	STM32L4Q5AGI6P
STM32U599NIH6Q	STM32L4P5QGI6	STM32F207IFH6
STM32L4P5QGI6TR	STM32U575AGI6	STM32F429IIH6
STM32WLE5JCI6	STM32MP157DAA1	STM32U575AII6Q

Public Products List

STM32MP153DAA1	STM32U585QII6QTR	STM32F407IGH6
STM32F437IIH6	STM32L4P5QGI6S	STM32G0B1REI7N
STM32G0B1VBI6	STM32L471QGI6TR	STM32F429IEH6
STM32L433RCI6	STM32U575QII6	STM32H730ABI6Q
STM32L4A6QGI6	STM32L072RZI6TR	STM32L4R5QGI6STR
STM32L452VEI3	STM32F217IGH6	STM32WL55JCI6TR
STM32H753XIH6	STM32MP151FAA1	STM32WLE4JBI6
STM32MP157CAA3T	STM32L433RCI3	STM32L4P5AEI6
STM32G0B1RBI6N	STM32WB55VCQ7	STM32U575AII6
STM32MP153CAA3T	STM32L476QGI3	STM32L496QEI6TR
STM32L4R5QGI6	STM32F437IGH6	STM32MP151CAA3
STM32L496QGI6	STM32L496QGI6STR	STM32U575QII3
STM32L471QEI6	STM32F429IGH6	STM32H742XGH6
STM32F207IGH6TR	STM32H745XIH3	STM32L433VCI6
STM32MP151AAA3	STM32U585AII6QTR	STM32L462VEI6TR
STM32H745XIH3TR	STM32L4Q5QGI6	STM32U585QII6TR
STM32L476QGI6P	STM32L451VCI6	STM32H725IGK6
STM32G474PCI6	STM32L496QGI6S	STM32L443RCI6TR
STM32G474PEI6TR	STM32L431RCI6	STM32L4R5QGI6S
STM32H725IGK3TR	STM32U585AII6TR	STM32L433VCI6TR
STM32U575QGI3Q	STM32MP153FAA1	STM32MP153AAA3T
STM32H745XIH6TR	STM32L4R5QII6TR	STM32G0B1RCI6NTR
STM32U575QGI6Q	STM32MP153CAA3	STM32G473PBI6
STM32MP157AAA3T	STM32L4Q5AGI6	STM32L152VCH6
STM32G474PBI6	STM32G0B1VEI6	STM32L476QEI6TR
STM32U575AGI6Q	STM32U585QII3TR	STM32L471QEI3TR
STM32H735IGK3	STM32H725IGK3	STM32H725AEI6
STM32H743XGH6	STM32L433RCI6TR	STM32G484PEI6
STM32L476QGI6	STM32L443RCI6	STM32U585AII6Q
STM32L452VEI3TR	STM32H753XIH6TR	STM32H747XGH6
STM32WB55VGQ7	STM32L431RBI3	STM32U575QGI3TR
STM32H735IGK6	STM32L443RCI3	STM32G483PEI6
STM32U575QII6Q	STM32G4A1REI6	STM32L471QEI6TR
STM32L4S5QII6	STM32WLE5J8I6	STM32L152VCH6D
STM32L4P5AGI6	STM32L4S5QII3P	STM32L162VCH6
STM32U585QII3	STM32H733ZGI6	STM32L452VEI6
STM32L4P5AGI6P	STM32L4R5QII6	STM32U575QII6TR
STM32H747XIH6	STM32WLE4JCI6	STM32U575QII3TR
STM32WB55VEQ7	STM32H730ZBI6	STM32WL55JCI6
STM32H725AGI3TR	STM32L431VCI7	STM32L471QEI7TR
STM32H745XGH6	STM32WL55JCI7	STM32H735AGI6
STM32H745XIH6	STM32H725AGI6	STM32H725AGI3
STM32WLE5JCI6TR	STM32U599NJH6Q	STM32WB55VEQ6
STM32L431VCI3	STM32U5A9NJH6Q	STM32H742XIH6
STM32L162VCH6TR	STM32U575QGI3	STM32H723ZEI6
STM32H725IEK6	STM32H757XIH6	STM32U575QGI6
STM32L151VCH6	STM32G0B1VCI6TR	STM32L4P5QGI6STR
STM32WLE5JBI6	STM32WLE4J8I6	STM32L4A6QGI6P
STM32L496QGI6P	STM32WB55VGQ6TR	STM32H723ZGI6
STM32L431VCI3TR		

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