

XP10NA8R4IT

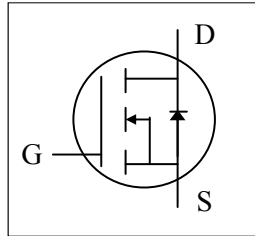
Halogen-Free Product

N-CHANNEL ENHANCEMENT MODE

POWER MOSFET



- ▼ 100% R_g & UIS Test
- ▼ Simple Drive Requirement
- ▼ Fast Switching Characteristic
- ▼ RoHS Compliant & Halogen-Free

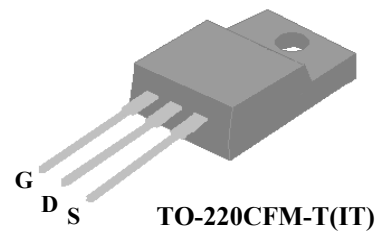


BV _{DSS}	100V
R _{DS(ON)}	8.4mΩ
I _D	44A

Description

XP10NA8R4 series are innovative design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The TO-220CFM package is widely preferred for all commercial-industrial through hole applications. The mold compound provides a high isolation voltage capability and low thermal resistance between the tab and the external heat-sink.



Absolute Maximum Ratings@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	100	V
V _{GS}	Gate-Source Voltage	+20	V
I _D @T _C =25°C	Drain Current, V _{GS} @ 10V	44	A
I _D @T _C =100°C	Drain Current, V _{GS} @ 10V	28	A
I _{DM}	Pulsed Drain Current ¹	180	A
P _D @T _C =25°C	Total Power Dissipation	32	W
P _D @T _A =25°C	Total Power Dissipation	1.92	W
E _{AS}	Single Pulse Avalanche Energy ³	125	mJ
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Value	Units
R _{thj-c}	Maximum Thermal Resistance, Junction-case	3.9	°C/W
R _{thj-a}	Maximum Thermal Resistance, Junction-ambient	65	°C/W

Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
B _V DSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	100	-	-	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =24A	-	-	8.4	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	2	-	4	V
g _{fs}	Forward Transconductance	V _{DS} =5V, I _D =24A	-	47	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =80V, V _{GS} =0V	-	-	25	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±20V, V _{DS} =0V	-	-	±0.1	uA
Q _g	Total Gate Charge ⁴	I _D =24A	-	42	67.2	nC
Q _{gs}	Gate-Source Charge ⁴	V _{DS} =50V	-	11	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge ⁴	V _{GS} =10V	-	16	-	nC
t _{d(on)}	Turn-on Delay Time ⁴	V _{DS} =50V	-	14	-	ns
t _r	Rise Time ⁴	I _D =24A	-	60	-	ns
t _{d(off)}	Turn-off Delay Time ⁴	R _G =7.5Ω	-	35	-	ns
t _f	Fall Time ⁴	V _{GS} =10V	-	70	-	ns
C _{iss}	Input Capacitance ⁴	V _{GS} =0V	-	2030	3248	pF
C _{oss}	Output Capacitance ⁴	V _{DS} =80V	-	300	-	pF
C _{rss}	Reverse Transfer Capacitance ⁴	f=1.0MHz	-	20	-	pF
R _g	Gate Resistance	f=1.0MHz	-	0.7	1.4	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{SD}	Forward On Voltage ²	I _S =24A, V _{GS} =0V	-	-	1.3	V
t _{rr}	Reverse Recovery Time ⁴	I _S =24A, V _{GS} =0V	-	50	-	ns
Q _{rr}	Reverse Recovery Charge ⁴	di/dt=100A/μs	-	70	-	nC

Notes:

- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse test
- 3.Starting T_j=25°C , V_{DD}=50V , L=0.1mH , R_G=25Ω , V_{GS}=10V
- 4.Guaranteed by design.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT, AUTOMOTIVE OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

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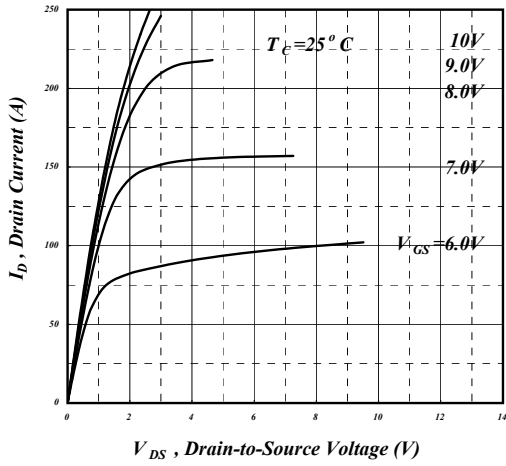


Fig 1. Typical Output Characteristics

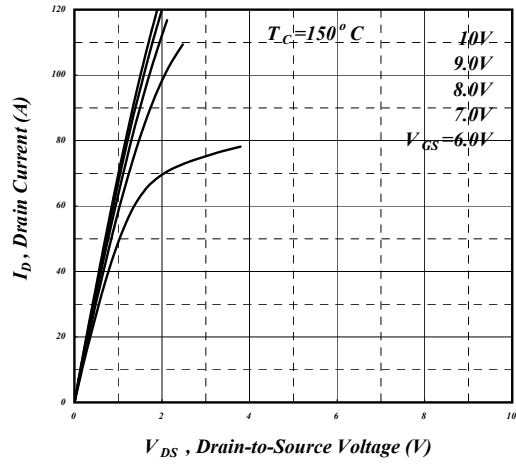


Fig 2. Typical Output Characteristics

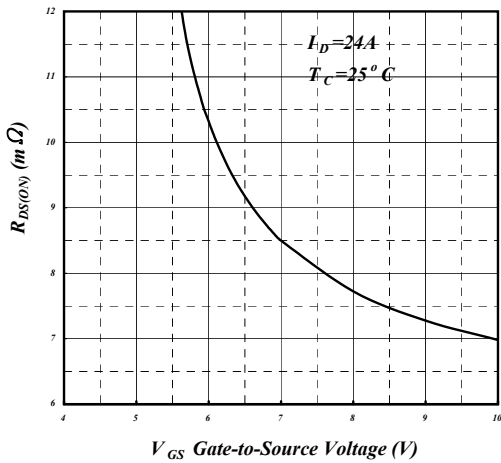


Fig 3. On-Resistance v.s. Gate Voltage

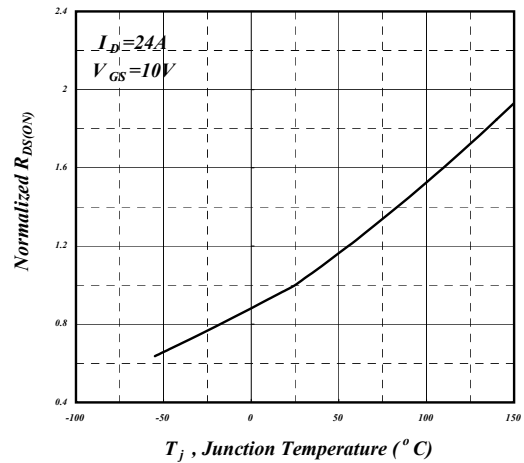


Fig 4. Normalized On-Resistance v.s. Junction Temperature

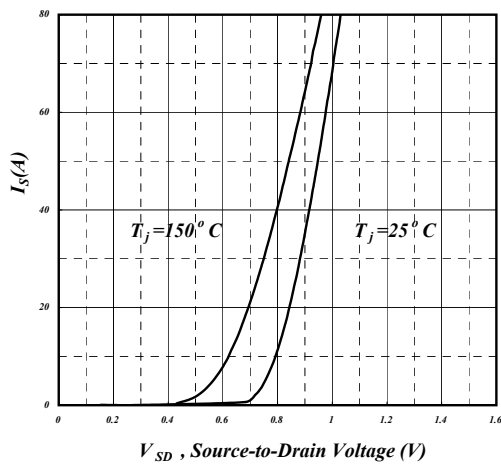


Fig 5. Forward Characteristic of Reverse Diode

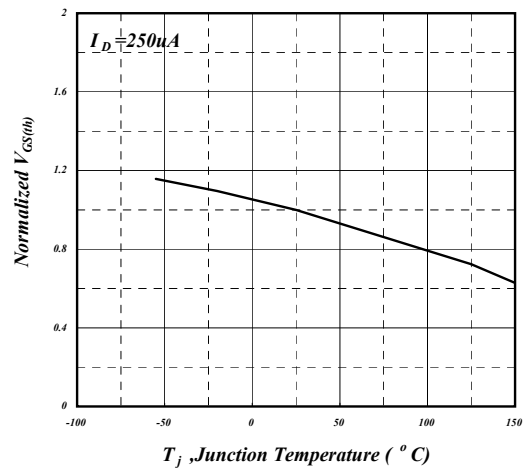


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

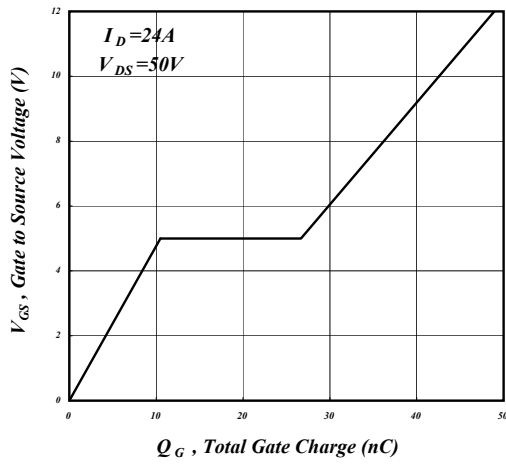


Fig 7. Gate Charge Characteristics

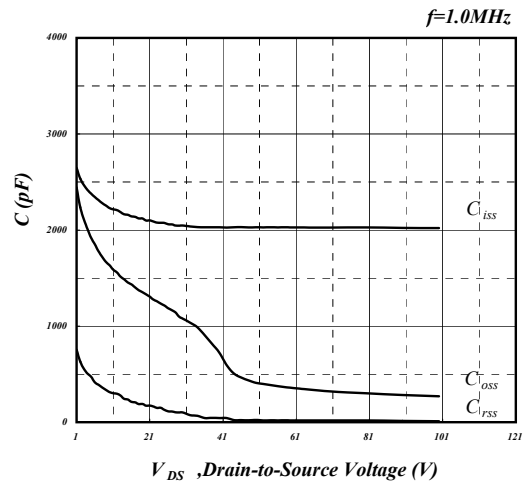


Fig 8. Typical Capacitance Characteristics

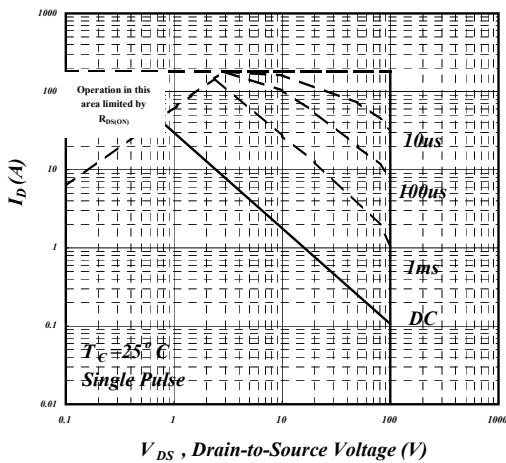


Fig 9. Maximum Safe Operating Area

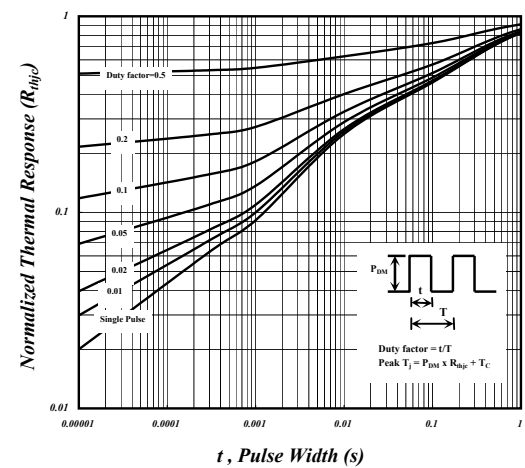


Fig 10. Effective Transient Thermal Impedance

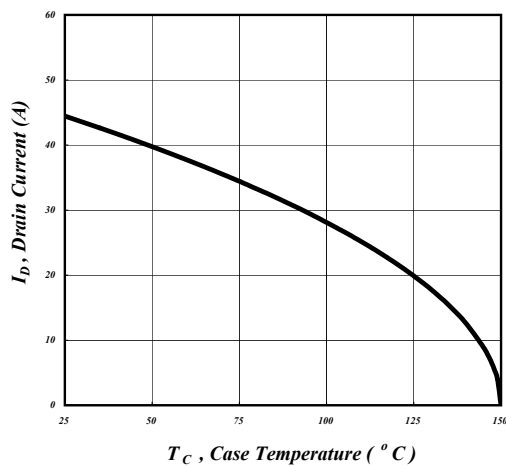


Fig 11. Drain Current v.s. Case Temperature

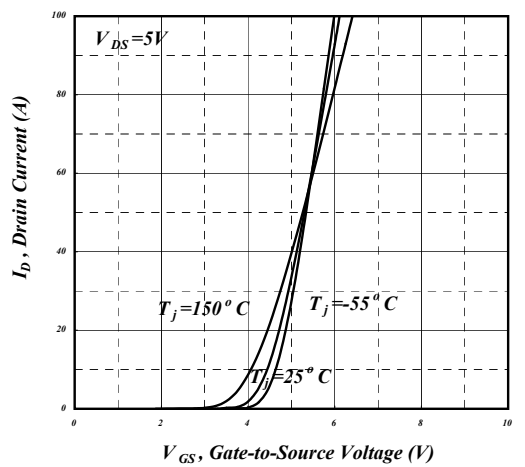


Fig 12. Transfer Characteristics

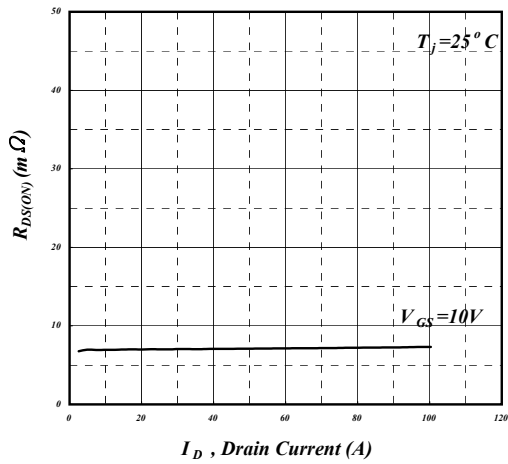


Fig 13. Typ. Drain-Source on State Resistance

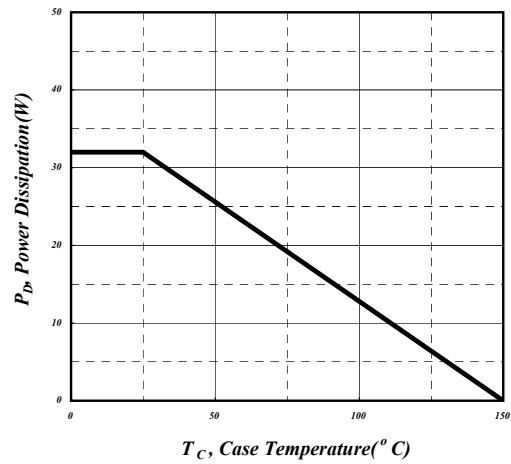


Fig 14. Total Power Dissipation

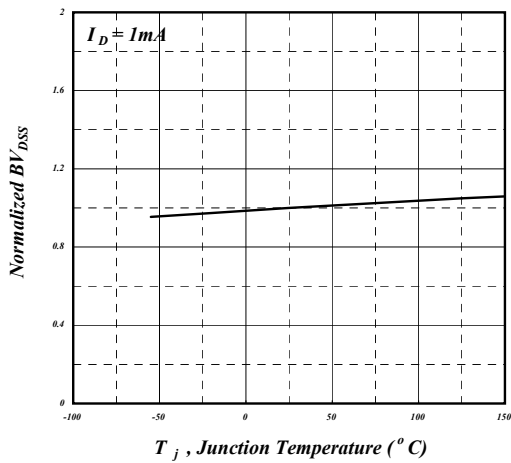


Fig 15. Normalized BV_{DSS} v.s. Junction Temperature

MARKING INFORMATION

