NI ELVIS III Specifications

2023-07-12

Contents

Hardware Specifications

The following specifications are typical for the range 10 °C to 35 °C unless otherwise noted.

Caution Observe all instructions and cautions in the user documentation. Using the product in a manner not specified can damage the product and compromise the built-in safety protection.

Attention Suivez toutes les instructions et respectez toutes les mises en garde de la documentation d'utilisation. L'utilisation du produit de toute autre façon que celle spécifiée risque de l'endommager et de compromettre la protection de sécurité intégrée.

Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- **Typical** specifications describe the performance met by a majority of models.
- **Nominal** specifications describe an attribute that is based on design, conformance testing, or supplemental testing.

Specifications are **Typical** unless otherwise noted.

Processor and FPGA

Type	Xilinx Z-7020

Speed	667 MHz
Cores	2

Operating System

Note For minimum software support information, visit ni.com/info and enter the Info Code swsupport.

Supported operating system	NI Linux Real-Time (32-bit)

Memory

Nonvolatile	1 GB
Volatile	
DDR3	512 MB
Clock frequency	533 MHz
Data bus width	16 bits

Note For information about the life span of the nonvolatile memory and about best practices for using nonvolatile memory, visit ni.com/info and enter the Info Code SSDBP.

USB Port

USB host port	USB 2.0 Hi-Speed, with standard A connector, 900 mA
USB device port	USB 2.0 Hi-Speed, with standard C connector

Network

Network interface	10Base-T, 100Base-TX, and 1000Base-T Ethernet
Compatibility	IEEE 802.3
Communication rates	10 Mbps, 100 Mbps, 1000 Mbps auto-negotiated
Maximum cabling distance	100 m/segment

Wireless

Radio mode	IEEE 802.11 a/b/g/n
Wireless mode	Off (default), client
Frequency band	2.4 GHz/5 GHz
Channel width	
2.4 GHz	20 MHz
5 GHz	20 MHz/40 MHz
Channels	

2.4 GHz	1 to 13
5 GHz	36 to 165
Antenna	
Number of antennas	1
Type	External dual-band RP-SMA male omnidirectional dipole
Gain	
2.4 GHz band	3.0 dBi, maximum
5 GHz band	4.0 dBi, maximum
Security	
Client mode	WPA, WPA2, WPA2-Enterprise
Access point mode	WPA2-Personal
Enterprise security EAP types (client mode only)	EAP-TLS, EAP-TTLS/MS-CHAPv2, PEAPv0/MS-CHAPv2

Power Requirements

Power supply voltage range	19 V ± 5%
Power consumption	
Maximum	76 W
Typical	20 W

Note NI recommends using the NI ELVIS III with the provided power supply (786817-01). Contact NI if a replacement is needed.

Control I/O

The following I/O is provided by the NI ELVIS III on the application board connector. Not all application boards will utilize or expose all of these resources.

Analog Input

Number of banks	2, capable of independent operation
Number of channels per bank	8 single-ended or 4 differential
ADC resolution	16 bits
Input range	±10 V, ±5 V, ±2 V, ±1 V
Maximum sampling rate (single channel)	1 MS/s
Large signal bandwidth (-3 dB)	>500 kHz

Table 2. Analog Input Accuracy

Measurement Conditions	Percent of Reading (Gain Error)	Percent of Range (Offset Error)
Typical (25 °C ± 5 °C)	0.064%	0.004%
Maximum (10 °C to 35 °C)	0.397%	0.054%

Recommended sampling rate (multi-channel)	≤500 kS/s aggregate
Multi-channel settling time	2 µs (±16 LSB for full scale step)
Input impedance	

Powered on	>1 GΩ
Powered off	>850 Ω
Overvoltage protection	
Powered on	±25 V, up to two AI lines
Powered off	±15 V, up to two AI lines

Analog Output

Number of channels	4, capable of independent operation
DAC Resolution	16 bits
Output range	±10 V
Maximum update rate	1.6 MS/s
Slew rate (100 pF load)	8.2 V/µs

Table 3. Analog Output Accuracy

Measurement Conditions	Percent of Reading (Gain Error)	Percent of Range (Offset Error)
Typical (25 °C ± 5 °C)	0.089%	0.029%
Maximum (10 °C to 35 °C)	0.430%	0.100%

Current drive	4 mA/channel maximum
Capacitive drive	3.3 nF
Output impedance	0.5 Ω

Protection	Short-circuit to ground
Power-on state	0 V

Digital I/O

Number of DIO channels	40
Direction control	Individually programmable as input or output
Logic level	5 V compatible LVTTL input; 3.3 V LVTTL output
Pull-up/down	40.2 kΩ pull-up to 3.3 V
Protection	±30 V
Input logic levels	
Input low voltage, V_{IL}	
Minimum	0 V
Maximum	0.8 V
Input high voltage, V_{IH}	
Minimum	2.0 V
Maximum	5.25 V
Output logic levels	
Output low voltage, V_{OL} sinking 4 mA	
Minimum	0 V
Maximum	0.4 V

Output high voltage, V_{OH} sourcing 4 mA	
Minimum	2.4 V
Maximum	3.465 V
Minimum output pulse width	20 ns
Maximum frequencies for secondary digital functions	
SPI	4 MHz
PWM	100 kHz
Quadrature encoder input	100 kHz
IC	400 kHz
UART lines	
Maximum baud rate	230,400 bps
Data bits	5, 6, 7, 8
Stop bits	1, 2
Parity	Odd, Even, Mark, Space
Flow control	XON/XOFF

Fixed User Power Supplies

Notice Exceeding the power limits may cause unpredictable device behavior.

+15 V power output	
Output voltage (no load)	+15 V ± 5%
Maximum current	500 mA
Ripple and noise (20 MHz bandwidth)	150 mV peak-to-peak maximum
Protection	Short-circuit to ground
-15 V power output	
Output voltage (no load)	-15 V ± 5%
Maximum current	-500 mA
Ripple and noise (20 MHz bandwidth)	150 mV peak-to-peak maximum
Protection	Short-circuit to ground
+5 V power output	
Output voltage (no load)	+5 V ± 5%
Maximum current	2 A
Ripple and noise (20 MHz bandwidth)	50 mV peak-to-peak maximum
Protection	Short-circuit to ground
+3.3 V power output	
Output voltage (no load)	+3.3 V ± 5%
Maximum current	310 mA
Ripple and noise (20 MHz bandwidth)	33 mV peak-to-peak maximum

Protection	Short-circuit to ground

USB Line

USB	USB 2.0 Hi-Speed, 900 mA

Instrumentation I/O

Oscilloscope

Number of channels	4
Maximum sampling rate (per channel)	
with repetitive sampling enabled	400 MS/s
without repetitive sampling enabled	100 MS/s
Resolution	14 bits
Bandwidth	50 MHz at -3 dB
Input impedance	1 MΩ ‖ 15 pF
Input coupling	AC, DC
AC coupling cut-off frequency	12 Hz at -3 dB
Overvoltage protection	±50 V
Accuracy	2% of input + 1% of full scale

Table 4. Input Range

Range	Full Scale	Offset	Offset Accuracy
High gain (≤200 mV/div)	2 V peak-to-peak	±1 V	±25 mV
Low gain (>200 mV/div)	50 V peak-to-peak	±25 V	±625 mV

Note Input voltages should not exceed 50 V DC or 30 V RMS.

Function and Arbitrary Waveform Generator

Number of channels	2
Maximum update rate (per channel)	100 MS/s
Resolution	14 bits
Slew rate	188 V/µs
Small signal bandwidth (-3 dB)	15 MHz with no load

Figure 3. Function Generator Maximum Amplitude vs Frequency

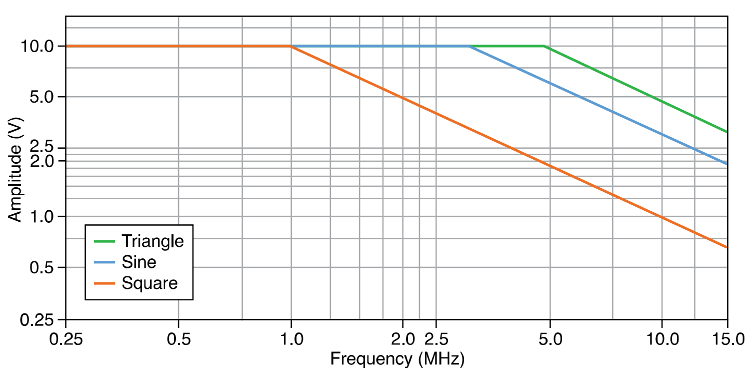


Table 5. Output Range

Gain Setting	AC Amplitude Range	DC Offset Range	Resolution	Amplitude Error	DC Offset Error	Total Output Range
High gain	±10 V	±10 V	1.25 mV/LSB	±0.5%	±50 mV	±10 V
Low gain	±2.5 V	±10 V	0.3 mV/LSB	±0.5%	±20 mV	±10 V

Output impedance	50 Ω
DC current drive	30 mA maximum
Overvoltage protection (per channel)	±10 V, short-circuit to ground
Power-on state	High Impedance

Trigger

Logic level	5 V compatible LVTTL input; 3.3 V LVTTL output
Pull down	1 MΩ
Input logic levels	
Input low voltage, V_{IL}	
Minimum	0 V
Maximum	0.8 V
Input high voltage, V_{IH}	
Minimum	2.0 V
Maximum	5.25 V
Output logic levels	

Output low voltage, V_{OL} sinking 4 mA	
Minimum	0 V
Maximum	0.4 V
Output high voltage, V_{OH} sourcing 4 mA	
Minimum	2.4 V
Maximum	3.465 V
Protection	Short-circuit to ground

Logic Analyzer/Pattern Generator

Number of channels	16
Maximum sampling rate (per channel)	100 MS/s
Logic level	5 V compatible LVTTL input; 3.3 V LVTTL output
Pull down	1 MΩ
Direction control	Individually programmable as Logic Analyzer or Pattern Generator
Input logic levels	
Input low voltage, V_{IL}	
Minimum	0 V
Maximum	0.8 V
Input high voltage, V_{IH}	

Minimum	2.0 V
Maximum	5.25 V
Output logic levels	
Output low voltage, V_{OL} sinking 4 mA	
Minimum	0 V
Maximum	0.4 V
Output high voltage, V_{OH} sourcing 4 mA	
Minimum	2.4 V
Maximum	3.465 V
Protection	Short-circuit to ground

Digital Multimeter (DMM)

Isolated functions	DC/AC voltage, DC/AC current, resistance, diode voltage, diode continuity
Non-isolated functions	Capacitance, inductance
Isolation level	Functional isolation
Resolution	4.5 digits
Input impedance	10 MΩ
Input coupling	DC/AC

Connectivity	Banana jacks
Voltage input protection	±60 V
Current input protection	2.5 A fuse, 5MF2.5-R
Measurements	
Voltage measurement	
DC ranges	50 mV DC, 500 mV DC, 5 V DC, 50 V DC
AC ranges	50 mV RMS, 500 mV RMS, 5 V RMS, 30 V RMS
Input frequency range (AC voltage)	40 Hz to 1 kHz
DC voltage measurement accuracy (50 mV DC)	0.2% of range
DC voltage measurement accuracy (500 mV DC, 5 V DC, 50 V DC)	0.1% of range
AC voltage measurement accuracy at 50 Hz and 60 Hz (50 mV RMS)	0.2% of range
AC voltage measurement accuracy at 50 Hz and 60 Hz (500 mV RMS, 5 V RMS, 30 V RMS)	0.1% of range
Current measurement	
DC ranges	2 A DC
AC ranges	2 A RMS
Shunt resistance	20 mΩ
Input frequency range (AC current)	40 Hz to 1 kHz

DC current measurement accuracy	0.1% of range
AC current measurement accuracy at 50 Hz and 60 Hz	0.1% of range
Resistance measurement	
Ranges	50 Ω, 500 Ω, 5 kΩ, 50 kΩ, 500 kΩ, 5 MΩ, 50 MΩ
Resistance measurement accuracy (500 Ω, 5 kΩ, 50 kΩ, 500 kΩ, 5 MΩ)	0.1% of range
Resistance measurement accuracy (50 Ω, 50 MΩ)	1% of range

IV Analyzer

2 wire impedance analyzer	
Current range	±30 mA
Voltage sweep range	±10 V
Excitation frequency	1 Hz to 15 MHz
2/3 wire current-voltage analyzer	
Supported devices	Diodes, NPN and PNP bipolar transistors
Base current range	±1 mA
Maximum collector current	±30 mA
Maximum collector voltage	±10 V

Table 6. Capacitance Measurement Range

Range	Effective Frequency	Effective Test Resistance
50 pF to 500 pF	10 kHz	100 kΩ
500 pF to 5 nF	1 kHz	10 kΩ
5 nF to 50 nF	1 kHz	10 kΩ
50 nF to 500 nF	1 kHz	1 kΩ
500 nF to 5 µF	1 kHz	1 kΩ
5 µF to 50 µF	1 kHz	100 Ω
50 µF to 500 µF	100 Hz	100 Ω

Capacitance measurement accuracy	1% of range

Table 7. Inductance Measurement Range

Range	Effective Frequency	Effective Test Resistance
10 µH to 100 µH	100 kHz	100 Ω
100 µH to 1 mH	10 kHz	100 Ω
1 mH to 10 mH	10 kHz	1 kΩ
10 mH to 100 mH	1 kHz	1 kΩ

Inductance measurement accuracy	1% of range

Variable Power Supplies

Notice Exceeding the power limits may cause unpredictable device behavior.

Positive variable power output	
Output voltage	+1 V to +15 V
Output current	+500 mA maximum

DC Voltage accuracy	±50 mV - $\|I_{out}\|$ × 0.25 mV/mA
Ripple and noise	20 mV_{pk-pk}
Voltage readback accuracy	±15 mV
Current readback accuracy	±5 mA
Negative variable power output	
Output voltage	-1 V to -15 V
Output current	-500 mA maximum
DC Voltage accuracy	±50 mV + $\|I_{out}\|$ × 0.25 mV/mA
Ripple and noise	55 mV_{pk-pk} + $\|V_{out}\|$ × 10 mV_{pk-pk}/V
Voltage readback accuracy	±15 mV
Current readback accuracy	±5 mA

Physical Characteristics

Weight	3.02 kg (6.66 lbs)

Figure 4. Top Dimensions

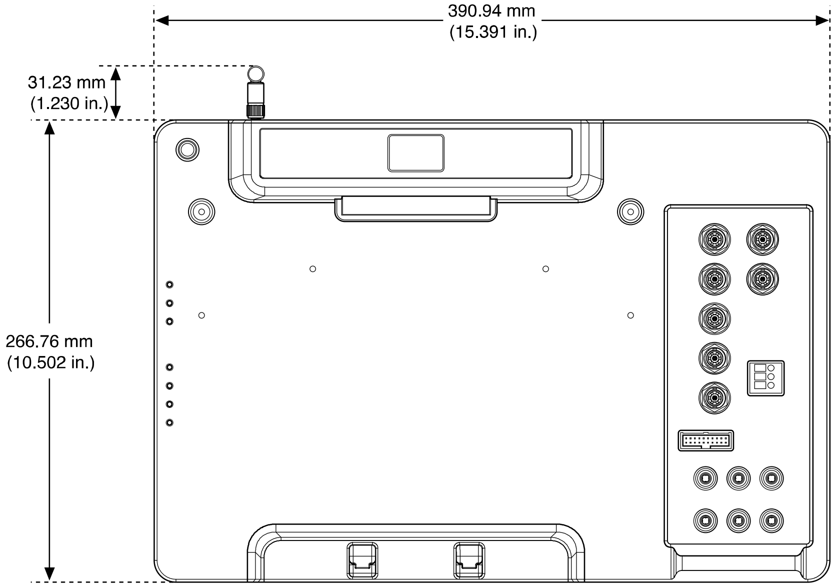


Figure 5. Side Dimensions

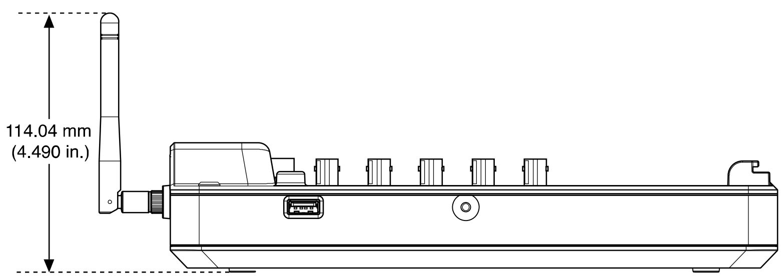
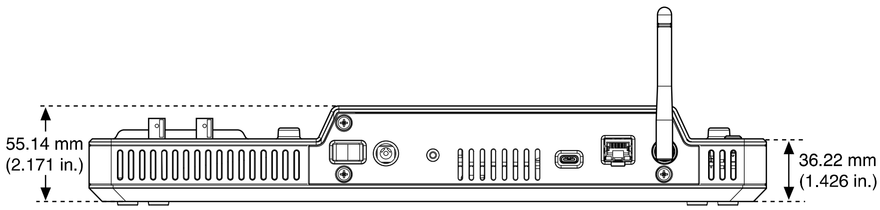


Figure 6. Rear Dimensions



Environmental Guidelines

Notice This model is intended for use in indoor applications only.

Environmental Characteristics

Temperature and Humidity

Temperature	
Operating	10 °C to 35 °C
Storage	-20 °C to 70 °C
Humidity	
Operating	10% RH to 90% RH, noncondensing
Storage	10% RH to 90% RH, noncondensing
Pollution Degree	2
Maximum altitude	5,000 m

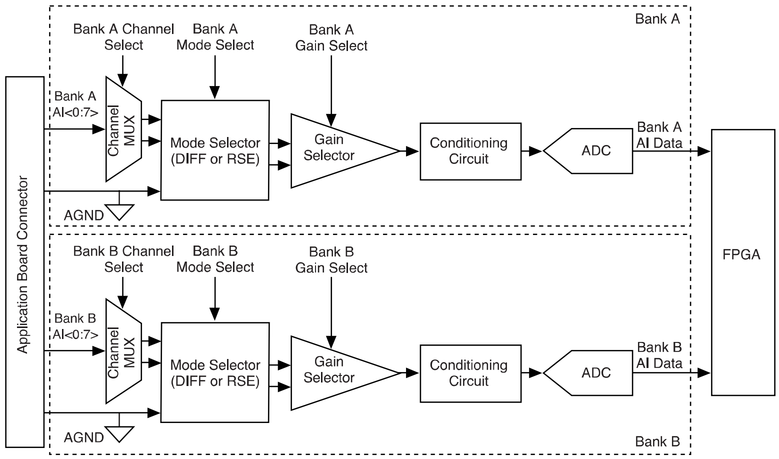
Environmental Standards

This product meets the requirements of the following environmental standards for electrical equipment.

- IEC 60068-2-1 Cold
- IEC 60068-2-2 Dry heat
- IEC 60068-2-78 Damp heat (steady state)

Note To verify marine approval certification for a product, refer to the product label or visit ni.com/certification and search for the certificate.

Analog Input Circuitry



The NI ELVIS III provides eight differential (or 16 single-ended) high-impedance analog input channels on the NI ELVIS III Prototyping Board. These inputs are divided into two identical banks (Bank A and Bank B) to enable simultaneous processing in the FPGA. Each of the banks consists of a channel multiplexer (MUX), mode selector, gain selector, conditioning circuit, and ADC. For applications that use multiple channels, each of the selected channels are scanned into the ADC using the MUX.

Channel Multiplexer

There is one channel multiplexer (MUX) in each of the analog input banks. Its function is to select the active channel(s) where the analog signal is channeled through the analog input circuitry and eventually to the ADC. The MUX in bank A will select the channels from Bank A/AI0 to A/AI7 while MUX in bank B will select the channels from Bank B/AI0 to B/AI7.

Mode Selector

The mode selector selects between differential or single-ended input modes. In differential mode, the analog input channel selected is referenced to its associated pair while in single-ended mode, the analog input channel selected is referenced to the analog ground (AGND). Refer to the Connecting Analog Input Signals section for more information.

Gain Selector

The gain selector enables the user to select the input range of ±10 V, ±5 V, ±2 V, and ±1 V for the analog input operation. It is important to select a suitable input range that is larger but close to the peak-to-peak amplitude of the analog signal to be measured. This ensures that the maximum resolution of the ADC is utilized for better readout accuracy. The NI ELVIS III can sample channels in any order of the input range at the maximum conversion rate or lower. Each channel in a scan list can be individually programmed with a different input range.

Conditioning Circuit

The conditioning circuit receives the analog signal from the gain selector stage and it shapes the analog signal using its internal circuitry so that the analog signal can be read by the ADC correctly.

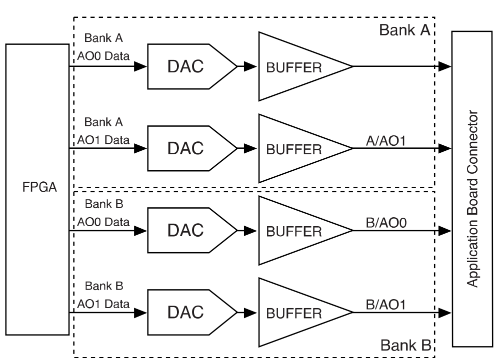
Analog-to-Digital Converter

The NI ELVIS III uses an analog-to-digital converter (ADC) to convert the AI signal into a 16-bit digital number.

FPGA

The FPGA processes the digital number which represents the analog signal read by analog input circuitry. The NI ELVIS III can perform both single and multiple analog to digital conversions for a fixed or infinite number of samples. The first-in-first-out buffer inside the FPGA can be implemented to hold the digital numbers during analog input acquisitions to ensure no data is lost.

Analog Output Circuitry



The NI ELVIS III provides four analog output channels on the NI ELVIS III Prototyping Board. These channels are controlled independently by the FPGA. Each analog output channel consists of a DAC and an output buffer.

FPGA

The FPGA converts the intended voltage level into digital codes which are then sent to the DAC for digital-to-analog conversion.

Digital-to-Analog Converter

Each analog output channel has a 16-bit digital-to-analog converter (DAC) to convert digital codes to analog voltages.

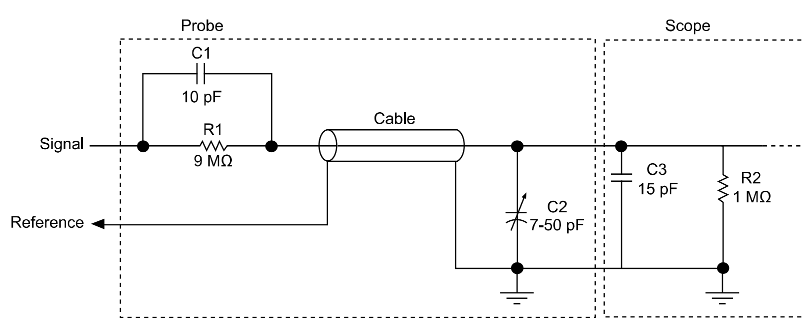
Output Buffer

The output buffer receives the analog voltage from the DAC and converts it to an output analog signal with a range of ±10 V.

Oscilloscope Probe and Probe Compensation

The NI ELVIS III oscilloscope is compatible with attenuating probes. These are useful for measuring high bandwidth signals because the series resistor isolates the cable capacitance of the probe and the input capacitance of the of the scope from the loading signal. Additionally the attenuating probe allows for measurement of higher voltages.

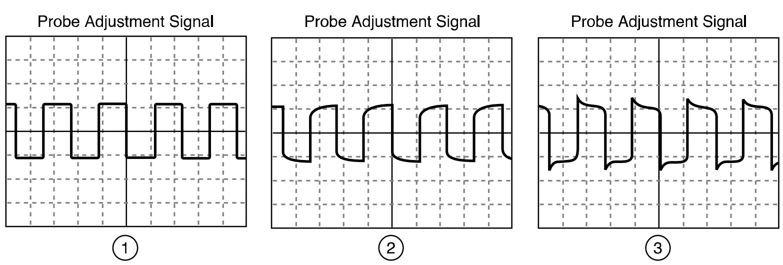
Figure 1. 10X Attenuating Probe and Oscilloscope Circuitry



Probe Compensation Adjustment

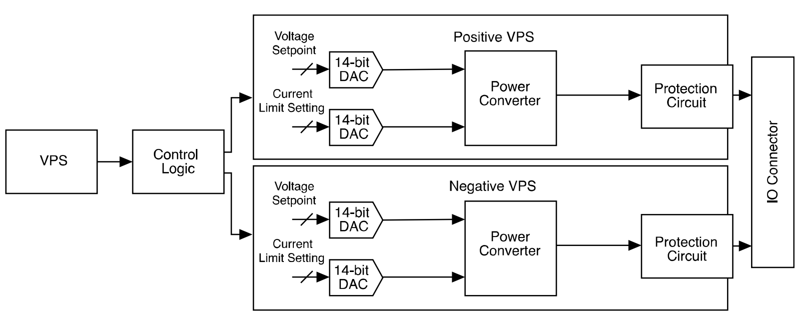
Before taking a measurement, make a compensation adjustment of the probe using the following steps:

1. Set the Function Generator as follows:
   - Frequency, 1 kHz
   - Amplitude, 1 V
   - Duty Cycle, 50%
   - Square Wave
2. Perform compensation of the 10X probe on a scope channel by measuring the function generator output.
3. Tune the capacitor on the probe and observe the waveform acquired by the scope.
   Stop when there is no undershoot or overshoot of the waveform. The following figure shows probe adjustment compensation scenarios:



1. Properly Compensated
2. Under Compensated
3. Over Compensated

Variable Power Supplies Circuitry



The NI ELVIS III provides a one positive and one negative variable power supply. The positive supply can provide adjustable output voltage from +1 V to +15 V and negative supply can provide -15 V to -1 V.

Digital-to-Analog Converter

The NI ELVIS III gets the set point from the Variable Power Supply SFP. A DAC is used to convert the digital set point to the control voltage.

Amplifier

The amplifier stage scales the control voltage of the DAC output to the correct adjust voltage, which is the input of the regulation loop.

Power Converter

The amplifier output, power converter, and its output construct the regulation loop that produces the required output voltage and keeps it stable.