Embedded Multi Chip Package
eMCP

e•MMC™5.1 HS400 + LPDDR4X

04EM08-M4EM627-06D00

Datasheet
v1.2

Kingston Digital Inc.

Contents

Section 1

Product Overview & Packaging

Product Features

- Embedded Multi-Media storage and LPDDR4X DRAM combined into a single Multi-Chip package
- Package: JEDEC 149 ball FBGA Type –8.0 mm x 9.5 mm x (Max 0.8mm)
- Operating temperature range: –25℃ to +85℃

Introduction

The eMCP device is a Multi-Chip Package Memory device which combines e•MMC™ (JESD84-B51) and Low Power DDR4X(JESD209-4C) Synchronous Dynamic RAM. The e•MMC™ part is an embedded flash memory storage solution with a MultiMediaCard interface (e•MMC™). The e•MMC™ controller directly manages NAND flash, including error conrol, wear-leveling, IOPS optimization and read sensing.

The device is suitable for use in data memory of mobile communication system to reduce not only PCB size but also power consumption. This device is available in 149-ball FBGA Type.

Table 1-1 Device Summary

Product Part number	NAND Density	DRAM Density	CH & CS DRAM	Package	Operating voltage
04EM08-M4EM627-06D00	04GB	8Gb	1CH, 1CS	FBGA 149	VCC=3.3V, VCCQ=1.8/3.3V VDD1 = 1.8V, VDD2= 1.1V, VDDQ = 0.6V

Device Block Diagram

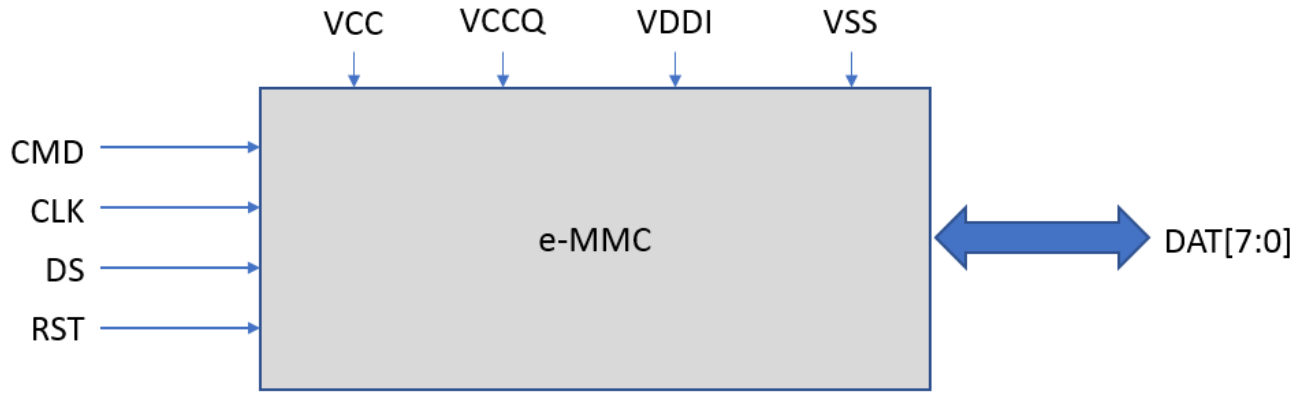
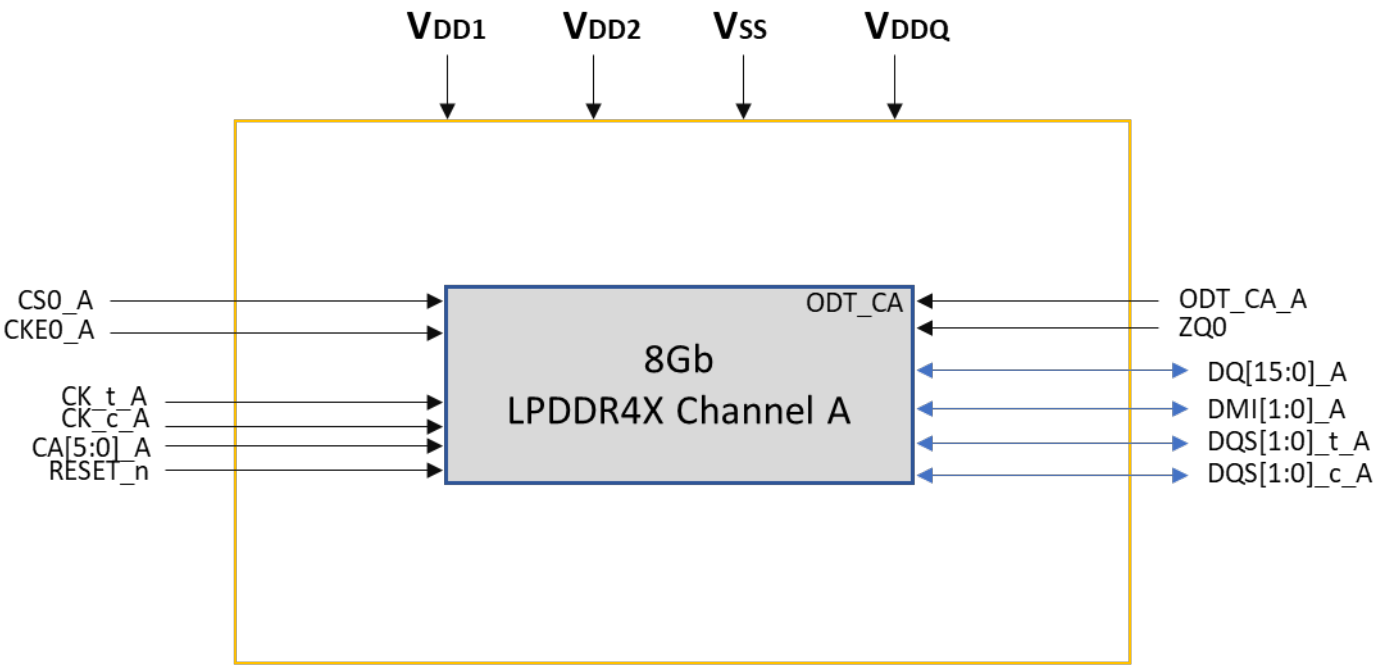


Figure 1-1 Device Block Diagram



Note: ODT_CA for rank 0 of each channel is wired to the respective ODT package ball. Any additional ranks are wired to VSS within the package. The ODT_CA pin is ignored by LPDDR4X devices. ODT_CA is fully controlled through MR11 and MR22. The ODT_CA pin must be connected to either VDD2 or VSS.

Figure 1-2 LPDDR4X Block Diagram

Operating Temperature Range

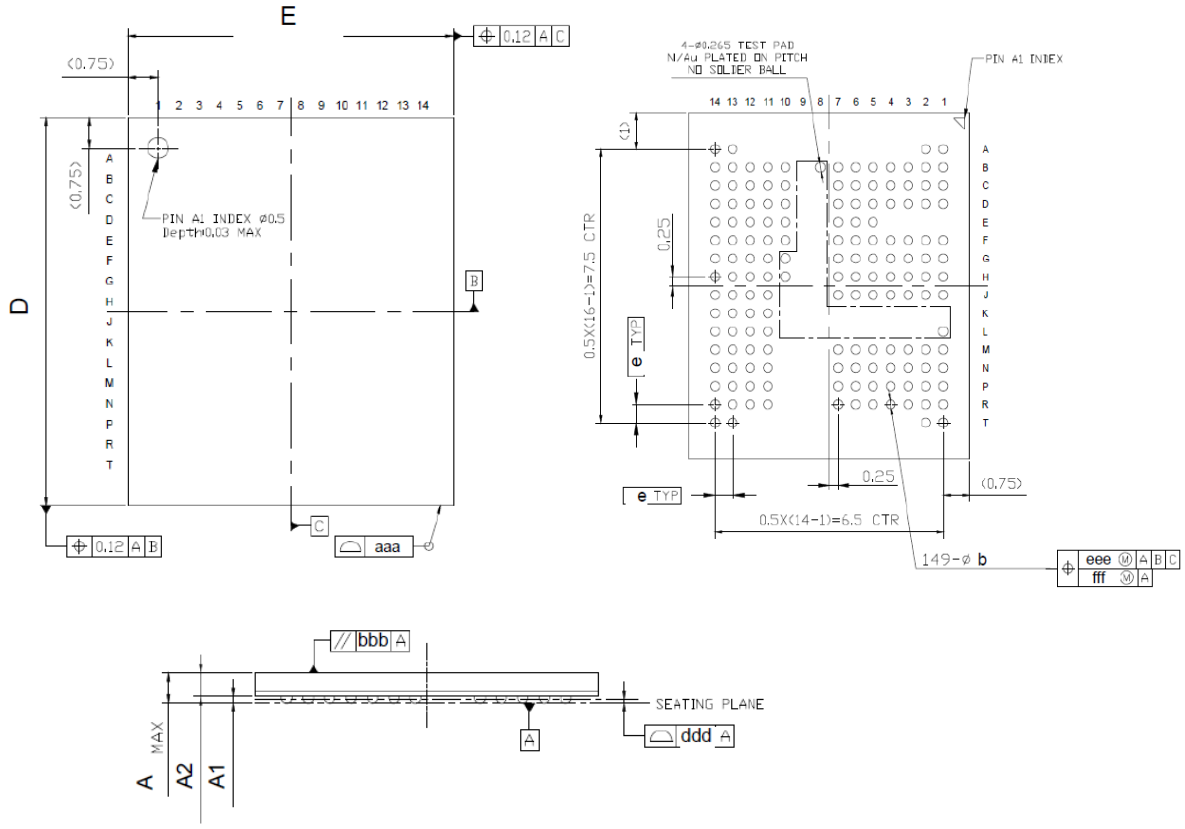
Table 1-2 Device Operating Temperature

Parameter	Rating	Unit	Note
Operating temperature	-25 ~ +85	℃	

Package Mechanical

8.0 x 9.5 x (Max 0.8mm)

Table 1-3 Device Package Dimensions



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	0.800	-	-	0.031
A1	0.130	0.160	0.190	0.005	0.006	0.007
A2	0.505	0.570	0.635	0.020	0.022	0.025
b	0.24	0.29	0.34	0.009	0.011	0.013
D	9.442	9.500	9.558	0.372	0.374	0.376
E	7.942	8.000	8.058	0.313	0.315	0.317
e	0.500			0.020		
JEDEC	MO-276 (REF.)					
aaa	0.058					
bbb	0.100					
ddd	0.080					
eee	0.120					
fff	0.050					

N	SE (mm)	SD (mm)	E1 (mm)	D1 (mm)
149	0.25	0.25	6.5	7.5

Ball Assignment (149 ball)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	DNU	DNU											DNU	DNU	A
B	DNU	NC	NC	NC	NC	NC	NC			VCCQ	VCCQ	VCC	NC	DNU	B
C	VSF1	VSF3	VSF5	VSF7	VSF9	VSSm	CMD			VSSm	DAT7	DAT6	VCC	VDDI	C
D	VSF2	VSF4	VSF6	VSF8	NC	VSSm	RST_n			DS	VSSm	VSSm	DAT1	DAT4	D
E					VDD2	VDD2	VDD2			VSSm	DAT2	DAT5	VCC	VCC	E
F	DQ10	VDD2	DQ8	DQ9	VSS	VSS	DQS1_t			CLK	VSSm	VSSm	DAT3	DAT0	F
G	DQ11	VDDQ	VDDQ	VSS	DQ12	VDDQ	DQS1_c				ODT(ca)	NC	VCCQ	VCCQ	G
H	DMI1	VSS	VDDQ	DQ14	VSS	DQ15	VDDQ				VSS	NC	VSS	CLK_t	H
J	DQ13	VSS	VSS	VSS	VDD2	VDD2	VDD2				VSS	CA0	VSS	CLK_c	J
K											CA1	VSS	CS1	CKE1	K
L											CA4	VSS	CS0	CKE0	L
M	DQ3	VSS	DMI0	VSS	DQ6	VSS	DQS0_c				CA3	VSS	VSS	RESET_n	M
N	DQ2	VSS	VSS	DQ5	VSS	DQ7	DQS0_t				CA2	VSS	CA5	ZQ1	N
P	DQ1	DQ0	VDDQ	VSS	DQ4	VSS	VDD2				VDD2	VDD2	VDD1	ZQ0	P
R	DNU	VDD1	VDD2	VDDQ	VDDQ	VDD2	VDD1				VDDQ	VDDQ	VDD1	DNU	R
T	DNU	DNU											DNU	DNU	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Follow JEDEC Standard Specification No.JESD209-4C

NOTE 1: 149 ball count, O.5 mm pitch, 14 x 16 rows.

NOTE 2: Top View, A1 in top left corner.

NOTE 3: The ODT_CA is ignored by LPDDR4X devices , ODT_CS/CA/CK function is fully controlled through MR11 and MR22. The ODT_CA pin shall connected to either VDD2 or VSS.

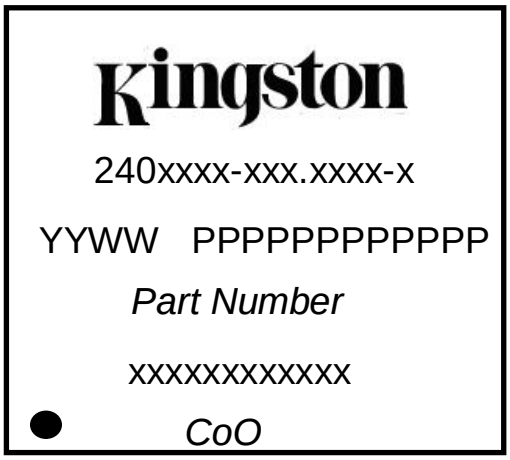
NOTE 4: DRAM die pad VSS and VSSQ signals are combined to VSS package balls.

NOTE 5: The flash ball-out supports eMMC 5.x

NOTE 6: Vendor specific function (VSF) - this terminal should not have any external electrical connections, but it may have an internal connection. The terminal may be routed to provide accessibility and may be used for general purpose vendor specific operations.

ASSIGNMENT (TOP VIEW)

Device Marking



Line 1: Kingston logo

Line 2: 240xxxx-xxx.xxxx-x: Internal control number

Line 3: YYWW: Date code (YY– Last 2 digital of year, WW- Work week)

PPPPPPPPPPP Internal control number (within 12 digits)

Line 4: Part Number: xxxxxx-xxxxxxx

Line 5: xxxxxxxxxxx: Internal control number (within 12 digits)

Line 6: Country of Origin (CoO): TAIWAN *or* CHINA

Section 2

Embedded Multi-Media Card (e•MMC 5.1)

Product Features

- Packaged managed NAND flash memory with *e*•MMC™ 5.1 interface
- Backward compatible with all prior *e*•MMC™ specification revisions
- Operating voltage range:
  - VCCQ = 1.8 V/3.3 V
  - VCC = 3.3 V
- Operating Temperature (T_{case}) - 25C to +85C
- Storage Temperature -40C to +85C
- Compliant with e•MMC™ 5.1 JEDEC Standard Number JESD84-B51

e•MMC™ Specific Feature Support

- High-speed *e*•MMC™ protocol
- Variable clock frequencies of 0-200MHz
- Ten-wire bus interface (clock, 1 bit command, 8 bit data bus) with an optional hardware reset
- Supports three different data bus widths: 1 bit(default), 4 bits, 8 bits
- Bus Modes:
  - Single data transfer rate: up to 52MB/s (using 8 parallel data lines at 52MHz)
  - Dual data rate mode (DDR-104) : up to 104MB/s @ 52MHz
  - High speed, single data rate mode (HS-200) : up to 200MB/s @ 200MHz
  - High speed, dual data rate mode (HS-400) : up to 400MB/s @ 200MHz
- Supports alternate boot operation mode to provide a simple boot sequence method
- Supports SLEEP/AWAKE (CMD5)
- Host initiated explicit sleep mode for power saving
- Enhanced write protection with permanent and partial write protection options
- Multiple user data partition with enhanced attribute for increased reliability
- Error free memory access
  - Cyclic Redundancy Code (CRC) for reliable command and data communication
  - Internal error correction code (ECC) for improved data storage integrity
  - Internal enhanced data management algorithm
  - Data protection for sudden power failure during program operations
- Security
  - Secure block erase commands
  - Enhanced write protection with permanent and partial protection options
- Power off notification
- Field firmware update (FFU)
- Production state awareness
- Device health report
- Enhanced strobe
- Cache flushing report
- Cache barrier
- Background operation control & High Priority Interrupt (HPI)
- RPMB throughput improvement

- Secure write protection
- Pre EOL information
- Optimal size

Product Description

Kingston's e•MMC™ products conform to the JEDEC e•MMC™ 5. standard. These devices are an ideal universal storage solution for many commercial and industrial applications. In a single integrated packaged device, e•MMC™ combines multi-level cell (MLC) NAND flash memory with an onboard e•MMC™ controller, providing an industry standard interface to the host system. The integrated e•MMC™ controller directly manages NAND flash media which relieves the host processor of these tasks, including flash media error control, wear-leveling, NAND flash management and performance optimization. Future revision to the JEDEC e•MMC™ standard will always maintain backward compatibility. The industry standard interface to the host processor ensures compatibility across future NAND flash generations as well, easing product sustainment throughout the product life cycle.

Device Performance

Table 2-1 below provides sequential read and write speeds for all capacities. Performance numbers can vary under different operating conditions. Values are given at HS400 bus mode.

Product	Typical value	
	Read Sequential (MB/s)	Write Sequential (MB/s)
04EM08-M4EM627-06D00	250	12
Note 1: Values given for an 8-bit bus width, running HS400 mode from KSI proprietary tool, V_{CC}=3.3V,V_{CCQ}=1.8V.		
Note 2: For performance number under other test conditions, please contact KSI representatives.		
Note 3: Performance numbers might be subject to changes without notice.		

Table 2-1 - Sequential Read / Write Performance

Power Consumption

Device current consumption for various device configurations is defined in the power class fields of the EXT_CSD register. Power consumption values are summarized in Table 2-2 below.

Product	Read(mA)		Write(mA)		Standby(mA)
	VCCQ(1.8V)	VCC(3.3V)	VCCQ(1.8V)	VCC(3.3V)	
04EM08-M4EM627-06D00	85.7	37.3	34.9	22.6	0.13
Note 1: Values given for an 8-bit bus width, a clock frequency of 200MHz DDR mode, V_{CC}= 3.3V±5%, V_{CCQ}=1.8V±5%					
Note 2: Standby current is measured at Vcc=3.3V±5% ,8-bit bus width without clock frequency.					
Note 3: Current numbers might be subject to changes without notice.					

Table 2-2 - Device Power Consumption

Device and Partition Capacity

The device NAND flash capacity is divided across two boot partitions (4096 KB each), a Replay Protected Memory Block (RPMB) partition (4096 KB), and the main user storage area. Four additional general purpose storage partitions can be created from the user partition. These partitions can be factory preconfigured or configured in-field by following the procedure outlined in section 6.2 of the JEDEC e•MMC™ specification JESD84-B51. A small portion of the NAND storage capacity is used for the storage of the onboard controller firmware and mapping tables. Additionally, several NAND blocks are held in reserve to boost performance and extend the life of the e•MMC™ device. Table2-3dentifies the specific capacity of each partition. This information is reported in the device EXT_CSD register. The contents of this register are also listed in the Appendix.

User density	Boot partition 1	Boot partition 2	RPMB
3,791,650,816 Bytes	2048 KB	2048 KB	512 KB

Table 2-3 - Partition Capacity

Table 2-4 - e•MMC™ Operating Voltage

Parameter	Symbol	Min	Nom	Max	Unit
Supply voltage (NAND)	V_{CC}	2.7	3.3	3.6	V
Supply voltage (I/O)	V_{CCQ} (1)	2.7	3.3	3.6	V
		1.7	1.8	1.95	V
Supply power-up for 3.3V	t_{PRUH}			35	ms
Supply power-up for 1.8V	t_{PRUL}			25	ms
Note 1：V_{CCQ} (I/O) 3.3 volt range is not supported while operating in HS200 & HS400 modes					

e•MMC™ Bus Modes

Kingston e•MMC™ devices support all bus modes defined in the JEDEC e•MMC™ 5.1 specification. These modes are summarized in Table 2-5 below.

Table 2-5 - e•MMC™ Bus Modes

Mode	Data Rate	IO Voltage	Bus Width	CLK Frequency	Maximum Data Bus Throughput
Legacy MMC	Single	3.3V / 1.8V	1, 4, 8	0 – 26 MHz	26 MB/s
High Speed SDR	Single	3.3V / 1.8V	4, 8	0 – 52 MHz	52 MB/s
High Speed DDR	Dual	3.3V / 1.8V	4, 8	0 – 52 MHz	104 MB/s
HS200	Single	1.8V	4, 8	0 – 200 MHz	200 MB/s
HS400	Dual	1.8V	8	0 – 200 MHz	400 MB/s

Signal Description

Table 2-6a - e•MMC™ Signals

Name	Type	Description
CLK	I	Clock: Each cycle of this signal directs a one bit transfer on the command and either a one bit (1x) or a two bits transfer (2x) on all the data lines. The frequency may vary between zero and the maximum clock frequency.
DAT[7:0]	I/O/PP	Data: These are bidirectional data channels. The DAT signals operate in push-pull mode. These bidirectional signals are driven by either the e•MMC™ device or the host controller. By default, after power up or reset, only DAT0 is used for data transfer. A wider data bus can be configured for data transfer, using either DAT0-DAT3 or DAT0-DAT7, by the e•MMC™ host controller. The e•MMC™ device includes internal pull-ups for data lines DAT1-DAT7. Immediately after entering the 4-bit mode, the device disconnects the internal pull ups of lines DAT1, DAT2, and DAT3. Correspondingly, immediately after entering to the 8-bit mode, the device disconnects the internal pull-ups of lines DAT1–DAT7.

Table 2-6b - e•MMC™ Signals (continued)

Name	Type	Description
CMD	I/O/PP/OD	Command: This signal is a bidirectional command channel used for device initialization and transfer of commands. The CMD signal has two operation modes: open-drain for initialization mode, and push-pull for fast command transfer. Commands are sent from the e•MMC™ host controller to the e•MMC™ device and responses are sent from the device to the host.
DS	O	This signal is generated by the device and used for output in HS400 mode. The frequency of this signal follows the frequency of CLK. For data output each cycle of this signal directs two bits transfer(2x) on the data - one bit for positive edge and the other bit for negative edge. For CRC status response output and CMD response output (enabled only HS400 enhanced strobe mode), the CRC status and CMD Response are latched on the positive edge only, and don't care on the negative edge.
RST_n	I	Hardware Reset: By default, hardware reset is disabled and must be enabled in the EXT_CSD register if used. Otherwise, it can be left un-connected.
RFU	-	Reserved for future use: These pins are not internally connected. Leave floating
NC	-	Not Connected: These pins are not internally connected. Signals can be routed through these balls to ease printed circuit board design. See Kingston's Design Guidelines for further details.
VSF	-	Vendor Specific Function: These pins are not internally connected
Vddi	-	Internal Voltage Node: Note that this is not a power supply input. This pin provides access to the output of an internal voltage regulator to allow for the connection of an external Creg capacitor. See Kingston's Design Guidelines for further details.
Vcc	S	Supply voltage for core
Vccq	S	Supply voltage for I/O
Vss	S	Supply ground for core
Vssq	S	Supply ground for I/O
Note: I=Input; O=Ouput; PP=Push-Pull; OD=Open_Drain; NC=Not Connected(or logical high); S=Power Supply		

Design Guidelines

Design guidelines are outlined in a separate document. Contact your KSI Representative for more information.

Card Identification Register (CID)

The Card Identification (CID) register is a 128-bit register that contains device identification information used during the *e*•MMC™ protocol device identification phase. Refer to JEDEC Standard Specification No.JESD84-B51 for details.

Field	Bits	Value
MID	[127:120]	0x70
reserved	[119:114]	0x00
CBX	[113:112]	0x01
OID	[111:104]	0x00
PNM	[103:56]	EE4NU8
PRV	[55:48]	0x06
PSN	[47:16]	Random
MDT	[15:8]	month, year
CRC	[7:1]	Follows JEDEC Standard
reserved	[0:0]	0x01

Card Specific Data Register [CSD]

The Card-Specific Data (CSD) register provides information on how to access the contents stored in *e*•MMC™. The CSD registers are used to define the error correction type, maximum data access time, data transfer speed, data format…etc. For details, refer to section 7.3 of the JEDEC Standard Specification No.JESD84-B51.

Field	Bits	Value
CSD_Structure	[127:126]	0x03 (V2.0)
SPEC_VER	[125:122]	0x04 (V4.0~4.2)
reserved	[121:120]	0x00
TAAC	[119:112]	0x4F (40ms)
NSAC	[111:104]	0x01
TRAN_SPEED	[103:96]	0x32 (26Mbit/s)
CCC	[95:84]	0x8F5
READ_BL_LEN	[83:80]	0x09 (512 Bytes)
READ_BL_PARTIAL	[79:79]	0x00
WRITE_BLK_MISALIGN	[78:78]	0x00
READ_BLK_MISALIGN	[77:77]	0x00
DSR_IMP	[76:76]	0x00
reserved	[75:74]	0x00
C_SIZE	[73:62]	0xFFF
VDD_R_CURR_MIN	[61:59]	0x07 (100mA)
VDD_R_CURR_MAX	[58:56]	0x07 (200mA)
VDD_W_CURR_MIN	[55:53]	0x07 (100mA)
VDD_W_CURR_MAX	[52:50]	0x07 (200mA)
C_SIZE_MULT	[49:47]	0x07 (512 Bytes)
ERASE_GRP_SIZE	[46:42]	0x1F
ERASE_GRP_MULT	[41:37]	0x1F
WP_GRP_SIZE	[36:32]	0x07
WP_GRP_ENABLE	[31:31]	0x01
DEFAULT_ECC	[30:29]	0x00

Field	Bits	Value
R2W_FACTOR	[28:26]	0x02
WRITE_BL_LEN	[25:22]	0x09 (512 Bytes)
WRITE_BL_PARTIAL	[21:21]	0x00
reserved	[20:17]	0x00
CONTENT_PROT_APP	[16:16]	0x00
FILE_FORMAT_GRP	[15:15]	0x00
COPY	[14:14]	0x00
PERM_WRITE_PROTECT	[13:13]	0x00
TMP_WRITE_PROTECT	[12:12]	0x00
FILE_FORMAT	[11:10]	0x00
ECC	[9:8]	0x00
CRC	[7:1]	Follow JEDEC Standard
reserved	[0:0]	0x01

Extended Card Specific Data Register [EXT_CSD]

The Extended CSD register defines the Device properties and selected modes. It is 512 bytes long. The most significant 320 bytes are the Properties segment, which defines the Device capabilities and cannot be modified by the host. The lower 192 bytes are the Modes segment, which defines the configuration the Device is working in. These modes can be changed by the host by means of the SWITCH command. For details, refer to section 7.4 of the JEDEC Standard Specification No.JESD84-B51.

Field	Byte	Value
Reserved	[511:506]	0
EXT_SECURITY_ERR	[505:505]	0x00
S_CMD_SET	[504:504]	0x01
HPI_FEATURES	[503:503]	0x01
BKOPS_SUPPORT	[502:502]	0x01
MAX_PACKED_READS	[501:501]	0x3C
MAX_PACKED_WRITES	[500:500]	0x3C
DATA_TAG_SUPPORT	[499:499]	0x01
TAG_UNIT_SIZE	[498:498]	0x03
TAG_RES_SIZE	[497:497]	0x00
CONTEXT_CAPABILITIES	[496:496]	0x05
LARGE_UNIT_SIZE_M1	[495:495]	0x03
EXT_SUPPORT	[494:494]	0x03
SUPPORTED_MODES	[493:493]	0x01
FFU_FEATURES	[492:492]	0x00
OPERATION_CODE_TIMEOUT	[491:491]	0x00
FFU_ARG	[490:487]	65535
BARRIER_SUPPORT	[486:486]	0x01
Reserved	[485:309]	0
CMDQ_SUPPORT	[308:308]	0x00
CMDQ_DEPTH	[307:307]	0x00
Reserved	[306:306]	0x00

Field	Byte	Value
NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED	[305:302]	0
VENDOR_PROPRIETARY_HEALTH_REPORT	[301:270]	0
DEVICE_LIFE_TIME_EST_TYP_B	[269:269]	0x01
DEVICE_LIFE_TIME_EST_TYP_A	[268:268]	0x01
PRE_EOL_INFO	[267:267]	0x01
OPTIMAL_READ_SIZE	[266:266]	0x01
OPTIMAL_WRITE_SIZE	[265:265]	0x04
OPTIMAL_TRIM_UNIT_SIZE	[264:264]	0x01
DEVICE_VERSION	[263:262]	0
FIRMWARE_VERSION	[261:254]	0x06
PWR_CL_DDR_200_360	[253:253]	0x00
CACHE_SIZE	[252:249]	512
GENERIC_CMD6_TIME	[248:248]	0x19
POWER_OFF_LONG_TIME	[247:247]	0xFF
BKOPS_STATUS	[246:246]	0x00
CORRECTLY_PRG_SECTORS_NUM	[245:242]	0
INI_TIMEOUT_AP	[241:241]	0x64
CACHE_FLUSH_POLICY	[240:240]	0x01
PWR_CL_DDR_52_360	[239:239]	0x00
PWR_CL_DDR_52_195	[238:238]	0x00
PWR_CL_200_195	[237:237]	0x00
PWR_CL_200_130	[236:236]	0x00
MIN_PERF_DDR_W_8_52	[235:235]	0x00
MIN_PERF_DDR_R_8_52	[234:234]	0x00
Reserved	[233:233]	0x00
TRIM_MULT	[232:232]	0x11
SEC_FEATURE_SUPPORT	[231:231]	0x55
SEC_ERASE_MULT	[230:230]	0x1E
SEC_TRIM_MULT	[229:229]	0x1E

Field	Byte	Value
BOOT_INFO	[228:228]	0x07
Reserved	[227:227]	0x00
BOOT_SIZE_MULT	[226:226]	0x10
ACC_SIZE	[225:225]	0x06
HC_ERASE_GRP_SIZE	[224:224]	0x01
ERASE_TIMEOUT_MULT	[223:223]	0x11
REL_WR_SEC_C	[222:222]	0x01
HC_WP_GRP_SIZE	[221:221]	0x08
S_C_VCC	[220:220]	0x08
S_C_VCCQ	[219:219]	0x08
PRODUCTION_STATE_AWARENESS_TIMEOUT	[218:218]	0x14
S_A_TIMEOUT	[217:217]	0x13
SLEEP_NOTIFICATION_TIME	[216:216]	0x0F
SEC_COUNT	[215:212]	7405568
SECURE_WP_INFO	[211:211]	0x01
MIN_PERF_W_8_52	[210:210]	0x08
MIN_PERF_R_8_52	[209:209]	0x08
MIN_PERF_W_8_26_4_52	[208:208]	0x08
MIN_PERF_R_8_26_4_52	[207:207]	0x08
MIN_PERF_W_4_26	[206:206]	0x08
MIN_PERF_R_4_26	[205:205]	0x08
Reserved	[204:204]	0x00
PWR_CL_26_360	[203:203]	0x00
PWR_CL_52_360	[202:202]	0x00
PWR_CL_26_195	[201:201]	0x00
PWR_CL_52_195	[200:200]	0x00
PARTITION_SWITCH_TIME	[199:199]	0x03
OUT_OF_INTERRUPT_TIME	[198:198]	0x04
DRIVER_STRENGTH	[197:197]	0x1F

Field	Byte	Value
DEVICE_TYPE	[196:196]	0x57
Reserved	[195:195]	0x00
CSD_STRUCTURE	[194:194]	0x02
Reserved	[193:193]	0x00
EXT_CSD_REV	[192:192]	0x08
CMD_SET	[191:191]	0x00
Reserved	[190:190]	0x00
CMD_SET_REV	[189:189]	0x00
Reserved	[188:188]	0x00
POWER_CLASS	[187:187]	0x00
Reserved	[186:186]	0x00
HS_TIMING	[185:185]	0x01
STROBE_SUPPORT	[184:184]	0x01
BUS_WIDTH	[183:183]	0x02
Reserved	[182:182]	0x00
ERASED_MEM_CONT	[181:181]	0x00
Reserved	[180:180]	0x00
PARTITION_CONFIG	[179:179]	0x00
BOOT_CONFIG_PROT	[178:178]	0x00
BOOT_BUS_CONDITIONS	[177:177]	0x00
Reserved	[176:176]	0x00
ERASE_GROUP_DEF	[175:175]	0x00
BOOT_WP_STATUS	[174:174]	0x00
BOOT_WP	[173:173]	0x00
Reserved	[172:172]	0x00
USER_WP	[171:171]	0x00
Reserved	[170:170]	0x00
FW_CONFIG	[169:169]	0x00
RPMB_SIZE_MULT	[168:168]	0x04

Field	Byte	Value
WR_REL_SET	[167:167]	0x00
WR_REL_PARAM	[166:166]	0x15
SANITIZE_START	[165:165]	0x00
BKOPS_START	[164:164]	0x00
BKOPS_EN	[163:163]	0x00
RST_n_FUNCTION	[162:162]	0x00
HPI_MGMT	[161:161]	0x00
PARTITIONING_SUPPORT	[160:160]	0x07
MAX_ENH_SIZE_MULT	[159:157]	452
PARTITIONS_ATTRIBUTE	[156:156]	0x00
PARTITION_SETTING_COMPLETED	[155:155]	0x00
GP_SIZE_MULT_4	[154:152]	0
GP_SIZE_MULT_3	[151:149]	0
GP_SIZE_MULT_2	[148:146]	0
GP_SIZE_MULT_1	[145:143]	0
ENH_SIZE_MULT	[142:140]	0
ENH_START_ADDR	[139:136]	0
Reserved	[135:135]	0x00
SEC_BAD_BLK_MGMNT	[134:134]	0x00
PRODUCTION_STATE_AWARENESS	[133:133]	0x00
TCASE_SUPPORT	[132:132]	0x00
PERIODIC_WAKEUP	[131:131]	0x00
PROGRAM _CID_CSD_DDR_SUPPORT	[130:130]	0x01
Reserved	[129:128]	0
VENDOR_SPECIFIC_FIELD	[127:67]	N/A
ERROR_CODE	[66:65]	0
ERROR_TYPE	[64:64]	0x00
NATIVE_SECTOR_SIZE	[63:63]	0x00
USE_NATIVE_SECTOR	[62:62]	0x00

Field	Byte	Value
DATA_SECTOR_SIZE	[61:61]	0x00
INI_TIMEOUT_EMU	[60:60]	0x00
CLASS_6_CTRL	[59:59]	0x00
DYNCAP_NEEDED	[58:58]	0x00
EXCEPTION_EVENTS_CTRL	[57:56]	0
EXCEPTION_EVENTS_STATUS	[55:54]	0
EXT_PARTITIONS_ATTRIBUTE	[53:52]	0
CONTEXT_CONF	[51:37]	0
PACKED_COMMAND_STATUS	[36:36]	0x00
PACKED_FAILURE_INDEX	[35:35]	0x00
POWER_OFF_NOTIFICATION	[34:34]	0x00
CACHE_CTRL	[33:33]	0x00
FLUSH_CACHE	[32:32]	0x00
BARRIER_CTRL	[31:31]	0x00
MODE_CONFIG	[30:30]	0x00
MODE_OPERATION_CODES	[29:29]	0x00
Reserved	[28:27]	0
FFU_STATUS	[26:26]	0x00
PRE_LOADING_DATA_SIZE	[25:22]	0
MAX_PRE_LOADING_DATA_SIZE	[21:18]	3670016
PRODUCT_STATE_AWARENESS_ENABLEMENT	[17:17]	0x01
SECURE_REMOVAL_TYPE	[16:16]	0x09
CMDQ_MODE_EN	[15:15]	0x00
Reserved	[14:0]	0

Section 3

Low Power Double Data Rate 4X

(LPDDR4X SDRAM)

8Gb(8Gbx1)SDP LPDDR4X SDRAM

Product Features

LPDDR4X

•Ultra-low voltage core and I/O power supplies
- VDD1 = 1.70–1.95V; 1.8V nominal
- VDD2 = 1.06–1.17V; 1.1V nominal
- VDDQ = 0.57–0.65V; 0.60V nominal

• Organization
- 64M words × 16 bits × 8 banks

• JEDEC LPDDR4X-compliant
•2KB page size (×16 bits)
- Row address: R0 to R15 (×16 bits)
- Column address: C0 to C9

• Frequency range
- 2133–10 MHz (data rate range: 4266–20 Mb/s/pin)

• 16n prefetch DDR architecture
• 8 internal banks per channel for concurrent operation
• Single-data-rate CMD/ADR entry
• Bidirectional/differential data strobe per byte lane
• Programmable READ and WRITE latencies (RL/WL)
• Programmable and on-the-fly burst lengths (BL =16/32)
• Directed per-bank refresh for concurrent bank operation and ease for command scheduling
• Up to 8.53 GB/s (×16 bits) per die
• On-chip temperature sensor to control self refresh rate
• Partial-array self refresh (PASR)
• Selectable output drive strength (DS)
• Clock-stop capability
• Operating temperature range
- TC = –25°C to +85°C

Product Description

The LPDDR4X part of device is fully compatible with the JEDEC Standard Specification No. JESD209-4-1. This datasheet describes the key and specific features of the LPDDR4X. Any additional information required to interface the device to a host system and all the practical methods for device detection and access can be found in the proper sections of the JEDEC Standard Specification.

LPDDR4X Interface

Pin Function and Descriptions

Table 3-1 – Pin Function and Descriptions

Name	Type	Description
CK_t_A CK_c_A	Input	**Clock:** CK_t and CK_c are differential clock inputs. All address, command and control input signals are sampled on positive edge of CK_t and the negative edge of CK_c. AC timings for CA parameters are referenced to clock.
CKE_A	Input	**Clock Enable:** CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is sampled at the rising edge of CK.
CS_A	Input	Chip Select: Considered part of the command code and is sampled on the rising edge of CK.
CA[5:0]_A	Input	**Command/Address Inputs**: Provide the command and address inputs according to the command truth table.
DQ[15:0]_A	I/O	Data Inputs/Output: Bidirectional data bus.
DQS[1:0]_t_A DQS[1:0]_c_A	I/O	**Data Strobe:** DQS_t and DQS_c are bi-directional differential output clock signals used to strobe data during a READ or WRITE. The data strobe is generated by the DRAM for a READ and is edge-aligned with data. The data strobe is generated by the SoC memory controller for a WRITE and is trained to precede data. Each byte of data has a data strobe signal pair.
DMI[1:0]_A	I/O	**Data mask/Data bus inversion:** DMI is a dual use bi-directional signal used to indicate data to be masked, and data which is inverted on the bus. For data bus inversion (DBI), the DMI signal is driven HIGH when the data on the data bus is inverted, or driven LOW when the data is in its normal state. DBI can be disabled via a mode register setting. For data mask, the DMI signal is used in combination with the data lines to indicate data to be masked in a MASK WRITE command (see the Data Mask (DM) and Data Bus Inversion (DBI) sections for details). The data mask function can be disabled via a mode register setting. Each byte of data has a DMI signal.
ZQ	I/O	**ZQ calibration reference:** Used to calibrate the output drive strength and the termination resistance. The ZQ pin shall be connected to VDDQ through a 240Ω ±1% resistor.
ODT_CA_A	Input	**CA ODT control:** CA ODT control: The ODT_CA pin is ignored by LPDDR4X devices. ODT_CA is fully controlled through MR11 and MR22. The ODT_CA pin shall be connected to VSS or VDD2.
VDDQ, VDD1, VDD2	Supply	**Power supplies:** Isolated on the die for improved noise immunity.
VSS, VSSQ	Supply	**Ground reference:** Power supply ground reference.
RESET_n	Input	**Reset:** When asserted LOW, the RESET pin resets all channels of the die.
DNU	-	**Do not use:** Do not connect.

Note:

1)"_A" indicate DRAM channel.

Simplified State Diagram

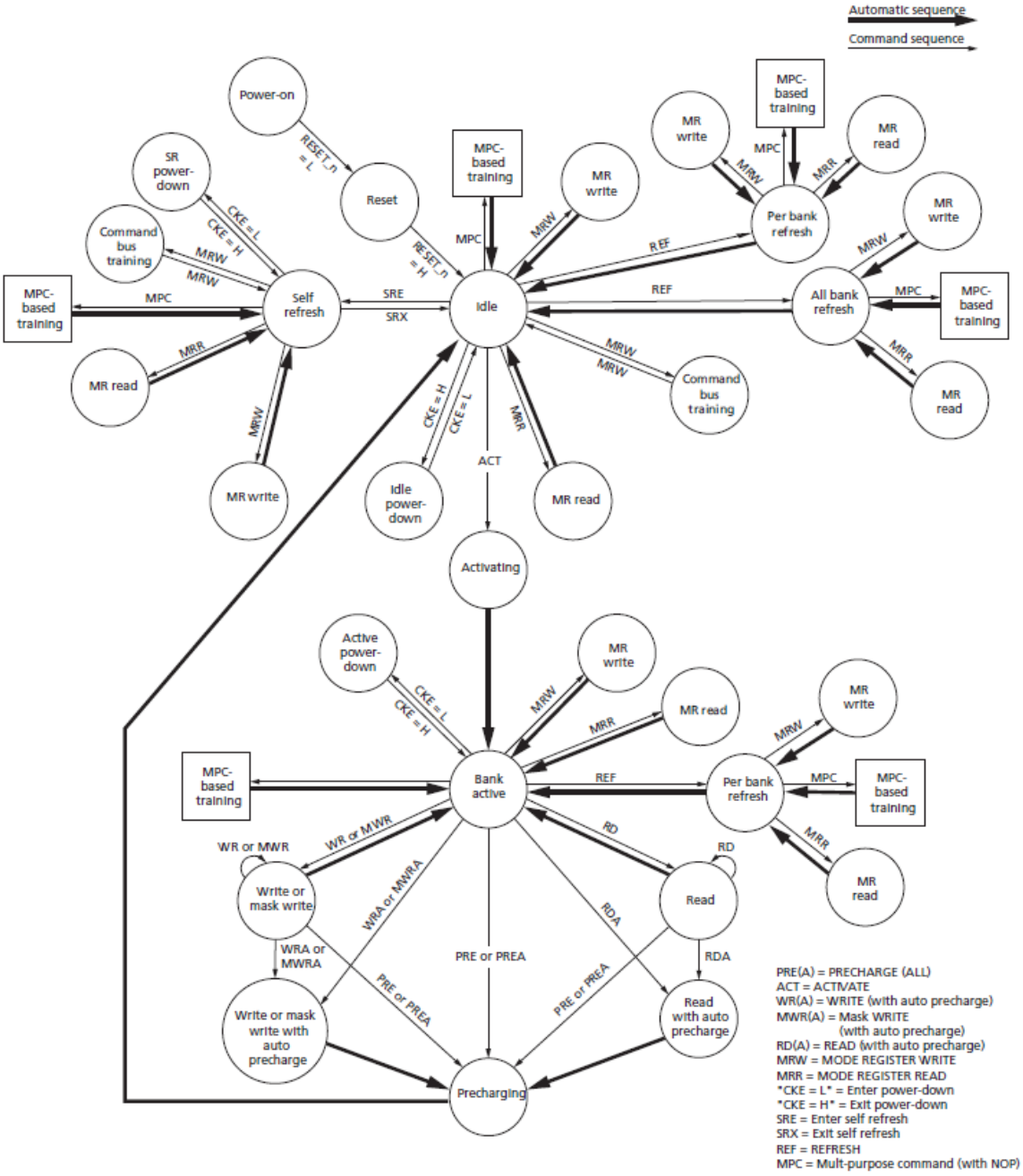


Figure 3-1 — Simplified Bus Interface State Diagram

Note: 1. From the self-refresh state, the device can enter power-down, MRR, MRW, or any of the training modes initiated with the MPC command. See the Self Refresh section.
2. All banks are pre-charged in the idle state.
3. In the case of using an MRW command to enter a training mode, the state machine will not automatically return to the idle state at the conclusion of training. See the applicable
4. In the case of an MPC command to enter a training mode, the state machine may not automatically return to the idle state at the conclusion of training. See the applicable

training section for more information.
5. This diagram is intended to provide an overview of the possible state transitions and commands to control them; however, it does not contain the details necessary to operate the device. In particular, situations involving more than one bank are not captured in complete detail.
6. States that have an "automatic return" and can be accessed from more than one prior state (that is, MRW from either idle or active states) will return to the state where they were initiated (that is, MRW from idle will return to idle).
7. The RESET pin can be asserted from any state and will cause the device to enter the reset state. The diagram shows RESET applied from the power-on and idle states as an example, but this should not be construed as a restriction on RESET.
8. MRW commands from the active state cannot change operating parameters of the device that affect timing. Mode register fields which may be changed via MRW from the active state include: MR1-OP[3:0], MR1-OP[7], MR3-OP[7:6], MR10-OP[7:0], MR11-OP[7:0], MR13-OP[5], MR15-OP[7:0], MR16-OP[7:0

Electrical Conditions

Absolute Maximum Ratings

Table 3-2 Absolute Maximum Ratings

Parameter	Symbol	min.	max.	Unit	Note
VDD1 supply voltage relative to VSS	VDD1	-0.4	2.1	V	1
VDD2 supply voltage relative to VSS	VDD2	-0.4	1.5	V	1
VDDQ supply voltage relative to VSS	VDDQ	-0.4	1.5	V	1
Voltage on any ball relative to VSS	VIN, VOUT	-0.4	1.5	V	
Storage Temperature	TSTG	-55	125	°C	2

Notes:
1. For information about relationships between power supplies, see the Voltage Ramp and Device Initialization section.
2. Storage Temperature is the case surface temperature on the center/top side of the device. For measurement conditions, refer to the JESD51-2 standard.

7.1.1 Recommended DC Operating Conditions

Table 3-3 Recommended DC Operating Conditions (TC = -25°C to +85°C)

Parameter	Symbol	min.	Typ.	max.	Unit	Note
Core 1 power	VDD1	1.7	1.8	1.95	V	1, 2
Core 2 power/ Input buffer power	VDD2	1.06	1.1	1.17	V	1, 2, 3
I/O buffer power	VDDQ	0.57	0.6	0.65	V	2, 3

Notes:
1. VDD1 uses significantly less power than VDD2.
2. The voltage range is for DC voltage only. DC voltage is the voltage supplied at the DRAM and is inclusive of all noise up to 20 MHz at the DRAM package ball.
3. The voltage noise tolerance from DC to 20 MHz exceeding a peak-to-peak tolerance of 45mV at the DRAM ball is not included in the TdIVW.

AC and DC Input Measurement Levels

Table 3-4 Input Levels for CKE

Parameter	Symbol	min.	max.	Unit	Note
Input High Level (AC)	VIH (AC)	0.75 × VDD2	VDD2 + 0.2	V	1
Input Low Level (AC)	VIL (AC)	-0.2	0.25 × VDD2	V	1
Input High Level (DC)	VIH (DC)	0.65 × VDD2	VDD2 + 0.2	V	
Input Low Level (DC)	VIL (DC)	-0.2	0.35 × VDD2	V	

Note: 1. See the AC Overshoot and Undershoot section.

Figure 3-2: Input Timing Definition for CKE

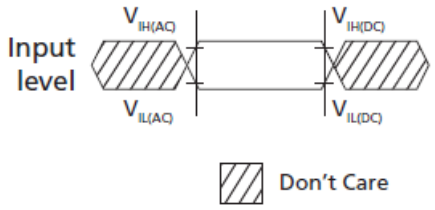
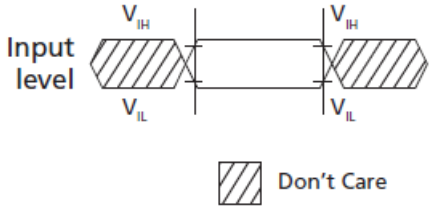


Table 3-5 Input Levels for RESET_n

Parameter	Symbol	min.	max.	Unit	Note
Input High Level	VIH	0.8 × VDD2	VDD2 + 0.2	V	1
Input Low Level	VIL	-0.2	0.20 × VDD2	V	1

Note: 1. See the AC Overshoot and Undershoot section.

Figure 3-3: Input Timing Definition for RESET_n

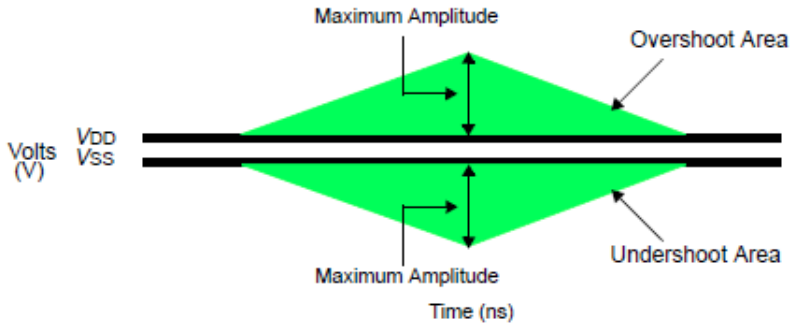


AC Overshoot and Undershoot Specifications

Table 3-6 — Overshoot/Undershoot Specification for CKE and RESET

Parameter		Specification	Unit
maximum peak amplitude allowed for overshoot area.	Max.	0.3	V
maximum peak amplitude allowed for undershoot area.	Max.	0.3	V
maximum overshoot area above VDD/VDDQ	Max.	0.8	V-ns
maximum undershoot area below VSS/VSSQ	Max.	0.8	V-ns

Figure 3-4 — AC Overshoot and Undershoot Definition



Differential Input Voltage

Differential Input Voltage for CK

The minimum input voltage needs to satisfy both Vindiff_CK and Vindiff_CK/2 specification at input receiver and their measurement period is 1tCK. Vindiff_CK is the peak-to-peak voltage centered on 0 volts differential and Vindiff_CK/2 is maximum and minimum peak voltage from 0 volts.

Figure 3-5: CK Differential Input Voltage

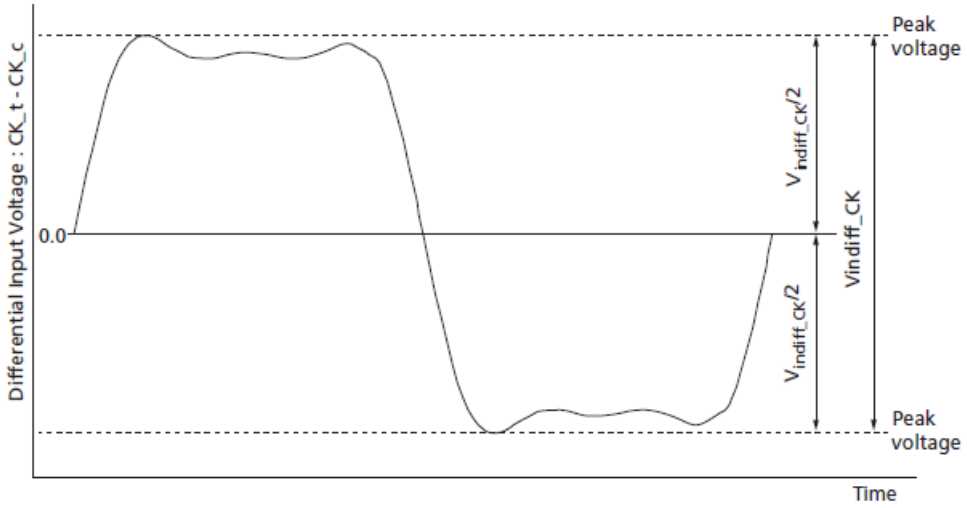


Table 3-7: CK Differential Input Voltage

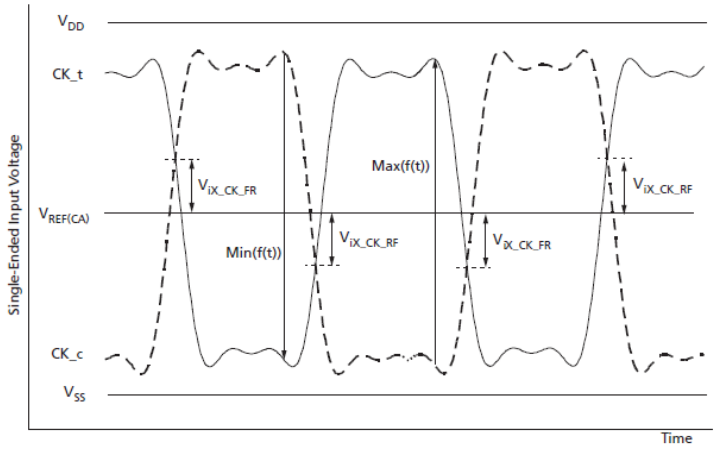
Parameter	Symbol	Data Rate						Unit	Notes
		1600/1867		2133/2400/3200		3733/4266			
		Min	Max	Min	Max	Min	Max		
CK differential input voltage	Vindiff_CK	420	-	380	-	360	-	mV	1

Note: 1. The peak voltage of differential CK signals is calculated in a following equation.
- Vindiff_CK = (Maximum peak voltage) - (Minimum peak voltage)
- Maximum peak voltage = MAX(f(t))
- Minimum peak voltage = MIN(f(t))
- f(t) = VCK_t - VCK_c

Differential Input Cross-Point Voltage

The cross-point voltage of differential input signals (CK_t, CK_c) must meet the requirements in table below. The differential input cross-point voltage VIX is measured from the actual cross-point of true and complement signals to the mid level that is VREF(CA).

Figure 3-6: Vix Definition (Clock)



Note: 1. The base levels of Vix_CK_FR and Vix_CK_RF are VREF(CA) that is device internal setting value by VREF training.

Table 3-8: Cross-Point Voltage for Differential Input Signals (Clock)

Notes 1 and 2 apply to entire table

Parameter	Symbol	Min / Max	2133	3200	4266	Unit	Note
CK Differential input cross-point voltage ratio	Vix_CK_ratio	Max	25	25	25	%	1,2

Notes: 1. Vix_CK_ratio is defined by this equation: Vix_CK_ratio = Vix_CK_FR/|MIN(f(t))|
2. Vix_CK_ratio is defined by this equation: Vix_CK_ratio = Vix_CK_RF/MAX(f(t))

Differential Input Voltage for DQS

The minimum input voltage needs to satisfy both Vindiff_DQS and Vindiff_DQS/2 specification at input receiver and their measurement period is 1UI (tCK/2). Vindiff_DQS is the peak to peak voltage centered on 0 volts differential and Vindiff_DQS/2 is maximum and minimum peak voltage from 0 volts.

Figure 3-7: DQS Differential Input Voltage

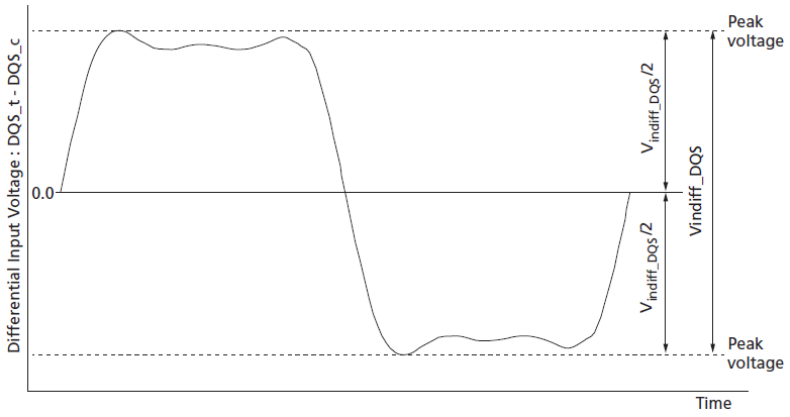


Table 3-9 : DQS Differential Input Voltage

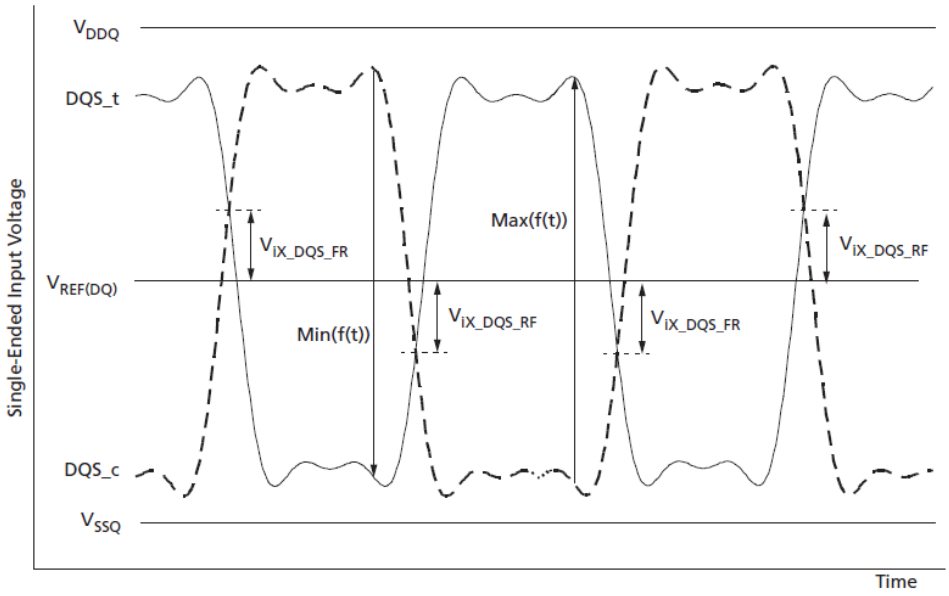
Parameter	Symbol	Data Rate						Unit	Notes
		1600/1867		2133/2400/3200		3733/4266			
		Min	Max	Min	Max	Min	Max		
DQS differential input	Vindiff_DQS	360	-	360	-	340	-	mV	1

Note: 1. The peak voltage of differential DQS signals is calculated in a following equation.
- Vindiff_DQS = (Maximum peak voltage) - (Minimum peak voltage)
- Maximum peak voltage = MAX(f(t))
- Minimum peak voltage = MIN(f(t))
- f(t) = VDQS_t - VDQS_c

Differential Input Cross-Point Voltage

The cross-point voltage of differential input signals (DQS_t, DQS_c) must meet the requirements in table below. The differential input cross-point voltage VIX is measured from the actual cross-point of true and complement signals to the mid level that is VREF(DQ).

Figure 3-8: Vix Definition (DQS)



Note: 1. The base levels of Vix_DQS_FR and Vix_DQS_RF are VREF(DQ) that is device internal setting value by VREF training.

Table 3-10: Cross-Point Voltage for Differential Input Signals (DQS)

Notes 1 and 2 apply to entire table

Parameter	Symbol	Min / Max	1600/1867	2133/2400/3200	3733/4266	Unit	Note
DQS Differential input crosspoint voltage ratio	Vix_DQS_ratio	Max	20	20	20	%	1,2

Notes: 1. Vix_DQS_ratio is defined by this equation: Vix_DQS_ratio = Vix_DQS_FR/|MIN(f(t))|
2. Vix_DQS_ratio is defined by this equation: Vix_DQS_ratio = Vix_DQS_RF/MAX(f(t))

Single-Ended Output Slew Rate

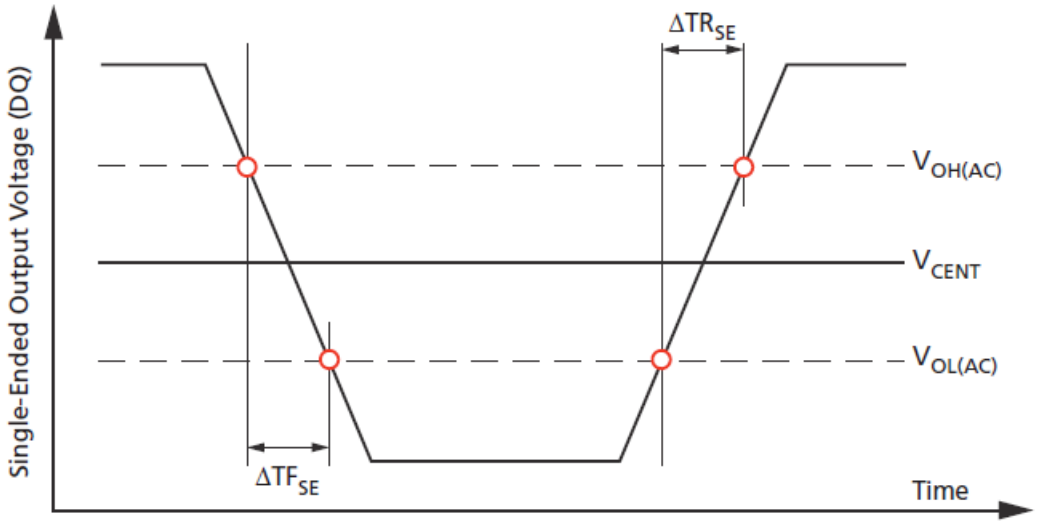
Table 3-11: Single-Ended Output Slew Rate

Note 1-5 applies to entire table

Parameter	Symbol	min.	max.	Unit
Single-ended Output Slew Rate (VOH = VDDQ *0.5)	SRQse	3.0	9.0	V/ns
Output slew-rate matching Ratio (Rise to Fall)		0.8	1.2	

Notes: 1. SR = Slew rate; Q = Query output; se = Single-ended signal.
2. Measured with output reference load.
3. The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.
4. The output slew rate for falling and rising edges is defined and measured between VOL(AC) = 0.2 × VOH(DC) and VOH(AC) = 0.8 × VOH(DC).
5. Slew rates are measured under average SSO conditions with 50% of the DQ signals per data byte switching.

Figure 3-9: Single-Ended Output Slew Rate Definition



Differential Output Slew Rate

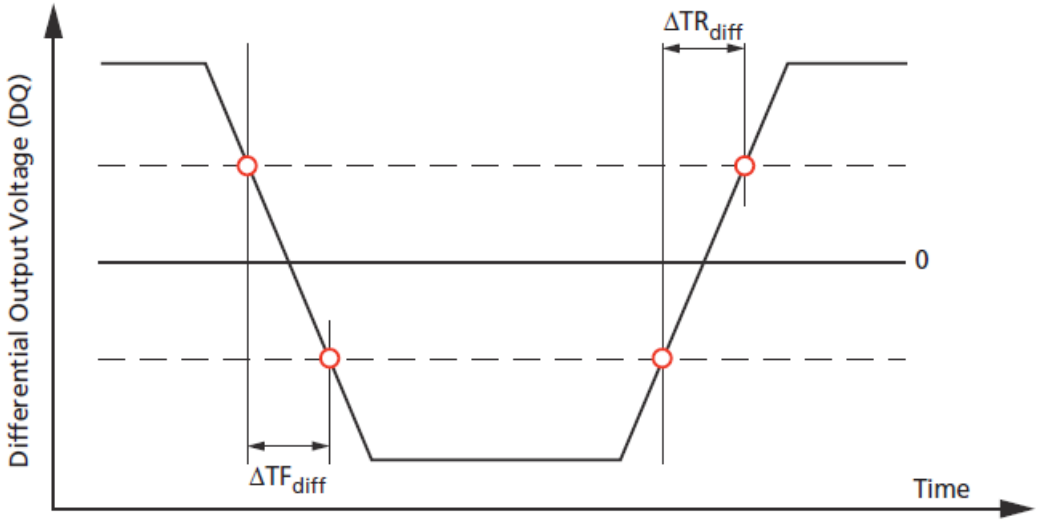
Table 3-12: Differential Output Slew Rate

Note 1-4 applies to entire table

Parameter	Symbol	min.	max.	Unit
Differential Output Slew Rate (VOH=VDDQ *0.5)	SRQdiff	6	18	V/ns

Notes: 1. SR = Slew rate; Q = Query output; se = Differential signal.
2. Measured with output reference load.
3. The output slew rate for falling and rising edges is defined and measured between VOL(AC) = -0.8 × VOH(DC) and VOH(AC) = 0.8 × VOH(DC).
4. Slew rates are measured under average SSO conditions with 50% of the DQ signals per data byte switching.

Figure 3-10: Differential Output Slew Rate Definition



AC and DC Input Measurement Levels for ODT input

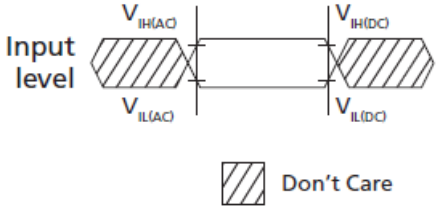
Input Levels for CKE

Table 3-13: Input Levels

Parameter	Symbol	min.	Max.	Unit	Note
Input high level (AC)	VIH(AC)	0.75*VDD2	VDD2+0.2	V	1
Input low level (AC)	VIL(AC)	-0.2	0.25*VDD2	V	1
Input high level (DC)	VIH(DC)	0.65*VDD2	VDD2+0.2	V	
Input low level (DC)	VIL(DC)	-0.2	0.35*VDD2	V	

Note: 1. See the AC Overshoot and Undershoot section

Figure 3-11: Input Timing Definition for CKE



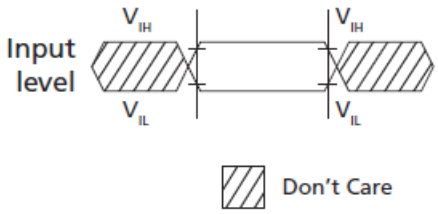
Input Levels for RESET_n

Table 3-14: Input Levels

Parameter	Symbol	min.	Max.	Unit	Note
Input high level	VIH	0.8*VDD2	VDD2+0.2	V	1
Input low level	VIL	-0.2	0.20*VDD2	V	1

Note: 1. See the AC Overshoot and Undershoot section.

Figure 3-12: Input Timing Definition for RESET_n



IDD Specification Parameters and Test Conditions

IDD Measurement Conditions

Table 3-15: IDD Measurement Conditions

Switching for CA								
CK_t edge	R1	R2	R3	R4	R5	R6	R7	R8
CKE	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
CS	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
CA0	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA1	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA2	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA3	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA4	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA5	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH

Notes: 1. LOW = VIN ≤ VIL(DC) MAX.
HIGH = VIN ≥ VIH(DC) MIN.
STABLE = Inputs are stable at a HIGH or LOW level.
2. CS must always be driven LOW.
3. 50% of CA bus is changing between HIGH and LOW once per clock for the CA bus.
4. The pattern is used continuously during IDD measurement for IDD values that require switching on the CA bus.

Table 3-16: CA Pattern for IDD4R

Clock Cycle Number	CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5
N	HIGH	HIGH	Read-1	L	H	L	L	L	L
N+1	HIGH	LOW		L	H	L	L	L	L
N+2	HIGH	HIGH	CAS-2	L	H	L	L	H	L
N+3	HIGH	LOW		L	L	L	L	L	L
N+4	HIGH	LOW	Deselect	L	L	L	L	L	L
N+5	HIGH	LOW	Deselect	L	L	L	L	L	L
N+6	HIGH	LOW	Deselect	L	L	L	L	L	L
N+7	HIGH	LOW	Deselect	L	L	L	L	L	L
N+8	HIGH	HIGH	Read-1	L	H	L	L	L	L
N+9	HIGH	LOW		L	H	L	L	H	L
N+10	HIGH	HIGH	CAS-2	L	H	L	L	H	H
N+11	HIGH	LOW		H	H	H	H	H	H
N+12	HIGH	LOW	Deselect	L	L	L	L	L	L
N+13	HIGH	LOW	Deselect	L	L	L	L	L	L
N+14	HIGH	LOW	Deselect	L	L	L	L	L	L
N+15	HIGH	LOW	Deselect	L	L	L	L	L	L

Notes: 1. BA[2:0] = 010; CA[9:4] = 000000 OR 111111; Burst order CA[3:2] = 00 or 11 (same as LPDDR3 IDDR3 specification).
2. CA pins are kept LOW with DES CMD to reduce ODT current (different from LPDDR3 IDDR3 specification).

Table 3-17: CA Pattern for IDD4W

Clock Cycle Number	CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5
N	HIGH	HIGH	Write-1	L	L	H	L	L	L
N+1	HIGH	LOW		L	H	L	L	L	L
N+2	HIGH	HIGH	CAS-2	L	H	L	L	H	L
N+3	HIGH	LOW		L	L	L	L	L	L
N+4	HIGH	LOW	Deselect	L	L	L	L	L	L
N+5	HIGH	LOW	Deselect	L	L	L	L	L	L
N+6	HIGH	LOW	Deselect	L	L	L	L	L	L
N+7	HIGH	LOW	Deselect	L	L	L	L	L	L
N+8	HIGH	HIGH	Write-1	L	L	H	L	L	L
N+9	HIGH	LOW		L	H	L	L	H	L
N+10	HIGH	HIGH	CAS-2	L	H	L	L	H	H
N+11	HIGH	LOW		L	L	H	H	H	H
N+12	HIGH	LOW	Deselect	L	L	L	L	L	L

N+13	HIGH	LOW	Deselect	L	L	L	L	L	L
N+14	HIGH	LOW	Deselect	L	L	L	L	L	L
N+15	HIGH	LOW	Deselect	L	L	L	L	L	L

Notes: 1. BA[2:0] = 010; CA[9:4] = 000000 or 111111 (same as LPDDR3 specification).
2. No burst ordering (different from LPDDR3 specification).
3. CA pins are kept LOW with DES CMD to reduce ODT current (different from LPDDR3 specification).

Table 3-18: Data Pattern for IDD4W (DBI Off)

	DBI OFF case									No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL0	1	1	1	1	1	1	1	1	0	8
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	1	1	1	1	1	1	0	0	0	6
BL7	1	1	1	1	0	0	0	0	0	4
BL8	1	1	1	1	1	1	1	1	0	8
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	1	1	1	1	1	1	0	0	0	6
BL15	1	1	1	1	0	0	0	0	0	4
BL16	1	1	1	1	1	1	0	0	0	6
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	1	1	0	2
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	0	0	0	0
BL21	0	0	0	0	1	1	1	1	0	4
BL22	1	1	1	1	1	1	1	1	0	8
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	1	1	0	2
BL25	0	0	0	0	1	1	1	1	0	4
BL26	1	1	1	1	1	1	0	0	0	6
BL27	1	1	1	1	0	0	0	0	0	4
BL28	1	1	1	1	1	1	1	1	0	8
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	0	0	0	0
BL31	0	0	0	0	1	1	1	1	0	4
No. of 1's	16	16	16	16	16	16	16	16		

Note: 1. Simplified pattern; same data pattern was applied to DQ[4], DQ[5], DQ[6], and DQ[7] to reduce complexity for IDD4W pattern programming.

Table 3-19: Data Pattern for IDD4R (DBI Off)

	DBI OFF case									No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL0	1	1	1	1	1	1	1	1	0	8
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	1	1	1	1	1	1	0	0	0	6
BL7	1	1	1	1	0	0	0	0	0	4
BL8	1	1	1	1	1	1	1	1	0	8
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	1	1	1	1	1	1	0	0	0	6
BL15	1	1	1	1	0	0	0	0	0	4
BL16	1	1	1	1	1	1	1	1	0	8
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	0	0	0	0
BL19	0	0	0	0	1	1	1	1	0	4
BL20	1	1	1	1	1	1	0	0	0	6
BL21	0	0	0	0	1	1	1	1	0	4
BL22	0	0	0	0	0	0	1	1	0	2
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	0	0	0	0
BL25	0	0	0	0	1	1	1	1	0	4
BL26	1	1	1	1	1	1	1	1	0	8
BL27	1	1	1	1	0	0	0	0	0	4
BL28	0	0	0	0	0	0	1	1	0	2
BL29	1	1	1	1	0	0	0	0	0	4
BL30	1	1	1	1	1	1	0	0	0	6
BL31	0	0	0	0	1	1	1	1	0	4
No. of 1's	16	16	16	16	16	16	16	16		

Note: 1. Simplified pattern; same data pattern was applied to DQ[4], DQ[5], DQ[6], and DQ[7] to reduce complexity for IDD4W pattern programming.

Table 3-20: Data Pattern for IDD4W (DBI On)

	DBI On case									No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL0	0	0	0	0	0	0	0	0	1	1
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	0	0	0	0	0	0	1	1	1	3
BL7	1	1	1	1	0	0	0	0	0	4
BL8	0	0	0	0	0	0	0	0	1	1
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	0	0	0	0	0	0	1	1	1	3
BL15	1	1	1	1	0	0	0	0	0	4
BL16	0	0	0	0	0	0	1	1	1	3
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	1	1	0	2
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	0	0	0	0
BL21	0	0	0	0	1	1	1	1	0	4
BL22	0	0	0	0	0	0	0	0	1	1
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	1	1	0	2
BL25	0	0	0	0	1	1	1	1	0	4
BL26	0	0	0	0	0	0	1	1	1	3
BL27	1	1	1	1	0	0	0	0	0	4
BL28	0	0	0	0	0	0	0	0	1	1
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	0	0	0	0
BL31	0	0	0	0	1	1	1	1	0	4
No. of 1's	8	8	8	8	8	8	16	16	8	

Table 3-21: Data Pattern for IDD4R (DBI On)

	DBI On case									No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL0	0	0	0	0	0	0	0	0	1	1
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	0	0	0	0	0	0	1	1	1	3
BL7	1	1	1	1	0	0	0	0	0	4
BL8	0	0	0	0	0	0	0	0	1	1
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	0	0	0	0	0	0	1	1	1	3
BL15	1	1	1	1	0	0	0	0	0	4
BL16	0	0	0	0	0	0	0	0	1	1
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	0	0	0	0
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	1	1	1	3
BL21	0	0	0	0	1	1	1	1	0	4
BL22	0	0	0	0	0	0	1	1	0	2
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	0	0	0	0
BL25	0	0	0	0	1	1	1	1	0	4
BL26	0	0	0	0	0	0	0	0	1	1
BL27	1	1	1	1	0	0	0	0	0	4
BL28	0	0	0	0	0	0	1	1	0	2
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	1	1	1	3
BL31	0	0	0	0	1	1	1	1	0	4
No. of 1's	8	8	8	8	8	8	16	16	8	

IDD Specifications

IDD values are for the entire operating voltage range, and all of them are for the entire standard temperature range.

Table 3-22: IDD Specification Parameters for 8Gb (1Ch, x16/Ch) and Operating Conditions

VDD2= 1.06-1.17V; VDDQ = 0.57–0.65V; VDD1 = 1.70–1.95V

Parameter / Condition	Symbol	Power Supply	4266 Mbps	Units	Notes
Operating one bank active-precharge current: tCK = tCKmin; tRC = tRCmin; CKE is HIGH; CS is LOW between valid commands; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	IDD01	VDD1	4.00	mA	
	IDD02	VDD2	29.00	mA	
	IDD0Q	VDDQ	0.75	mA	2
Idle power-down standby current: tCK = tCKmin; CKE is LOW; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	IDD2P1	VDD1	1.10	mA	
	IDD2P2	VDD2	1.80	mA	
	IDD2PQ	VDDQ	0.75	mA	2
Idle power-down standby current with clock stop: CK_t =LOW, CK_c =HIGH; CKE is LOW; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable ODT is disabled	IDD2PS1	VDD1	1.10	mA	
	IDD2PS2	VDD2	1.80	mA	
	IDD2PSQ	VDDQ	0.75	mA	2
Idle non power-down standby current: tCK = tCKmin; CKE is HIGH; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable	IDD2N1	VDD1	1.20	mA	
	IDD2N2	VDD2	16.00	mA	
	IDD2NQ	VDDQ	0.75	mA	2

Table 3-23 — IDD Specification Parameters for 8Gb (1Ch, x16/Ch) and Operating Conditions

Parameter / Condition	Symbol	Power Supply	4266 Mbps	Units	Notes
Idle non power-down standby current with clock stopped: CK_t=LOW; CK_c=HIGH; CKE is HIGH; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable ODT is disabled	IDD2NS1	VDD1	1.20	mA	
	IDD2NS2	VDD2	12.00	mA	
	IDD2NSQ	VDDQ	0.75	mA	2
Active power-down standby current: tCK = tCKmin; CKE is LOW; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable ODT is disabled	IDD3P1	VDD1	1.10	mA	
	IDD3P2	VDD2	4.80	mA	
	IDD3PQ	VDDQ	0.75	mA	2
Active power-down standby current with clock stop: CK_t=LOW, CK_c=HIGH; CKE is LOW; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable ODT is disabled	IDD3PS1	VDD1	1.10	mA	
	IDD3PS2	VDD2	4.80	mA	
	IDD3PSQ	VDDQ	0.75	mA	3
Active non-power-down standby current: tCK = tCKmin; CKE is HIGH; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable ODT is disabled	IDD3N1	VDD1	1.50	mA	
	IDD3N2	VDD2	22.00	mA	
	IDD3NQ	VDDQ	0.75	mA	3

Table 3-24 — IDD Specification Parameters for 8Gb (1Ch, x16/Ch) and Operating Conditions

Parameter / Condition	Symbol	Power Supply	4266 Mbps	Units	Notes
Active non-power-down standby current with clock stopped: CK_t=LOW, CK_c=HIGH; CKE is HIGH; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable ODT is disabled	IDD3NS1	VDD1	1.50	mA	
	IDD3NS2	VDD2	18.00	mA	
	IDD3NSQ	VDDQ	0.75	mA	3
Operating burst READ current: tCK = tCKmin; CS is LOW between valid commands; One bank is active; BL = 16 or 32; RL = RL(MIN); CA bus inputs are switching; 50% data change each burst transfer ODT is disabled	IDD4R1	VDD1	2.50	mA	9,10
	IDD4R2	VDD2	263.00	mA	9,10
	IDD4RQ	VDDQ	73.88	mA	4, 9,10
Operating burst WRITE current: tCK = tCKmin; CS is LOW between valid commands; One bank is active; BL = 16 or 32; WL = WLmin; CA bus inputs are switching; 50% data change each burst transfer ODT is disabled	IDD4W1	VDD1	1.50	mA	10
	IDD4W2	VDD2	195.00	mA	10
	IDD4WQ	VDDQ	0.75	mA	3, 10

All-bank REFRESH Burst current:
tCK = tCKmin;
CKE is HIGH between valid commands;
tRC = tRFCabmin;
Burst refresh;
CA bus inputs are switching;
Data bus inputs are stable;
	IDD51	VDD1	9.00	mA	

	IDD52	VDD2	90.00	mA	
	IDD5Q	VDDQ	0.75	mA	3

Table 3-25 — IDD Specification Parameters for 8Gb (1Ch, x16/Ch) and Operating Conditions

Parameter / Condition	Symbol	Power Supply	4266 Mbps	Units	Notes
All-bank REFRESH Average current:	IDD5AB1	VDD1	1.70	mA	
tCK = tCKmin;	IDD5AB2	VDD2	22.00	mA	
CKE is HIGH between valid commands; tRC = tREFI; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	IDD5ABQ	VDDQ	0.75	mA	3
Per-bank REFRESH Average current:	IDD5PB1	VDD1	1.70	mA	
tCK = tCKmin;	IDD5PB2	VDD2	22.00	mA	
CKE is HIGH between valid commands; tRC = tREFI/8; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	IDD5PBQ	VDDQ	0.75	mA	3
Self refresh current (85°C):	IDD61	VDD1	1.50	mA	5, 6, 11
CK_t=LOW, CK_c=HIGH; CKE is LOW; CA bus inputs are stable;	IDD62	VDD2	6.00	mA	5, 6, 11
Data bus inputs are stable; Maximum 1x self refresh rate ODT is disabled	IDD6Q	VDDQ	0.75	mA	3, 5, 6, 11
Self refresh current (25°C):	IDD61	VDD1	0.19	mA	5, 6, 11
CK_t=LOW, CK_c=HIGH; CKE is LOW; CA bus inputs are stable;	IDD61	VDD2	0.46	mA	5, 6, 11
Data bus inputs are stable; Maximum 1x self refresh rate ODT is disabled	IDD6Q	VDDQ	0.01	mA	3, 5, 6, 11

Notes:
1. ODT disabled: MR11[2:0] = 000b.
2. IDD current specifications are tested after the device is properly initialized.
3. Measured currents are the summation of VDDQ and VDD2.
4. Guaranteed by design with output load = 5pF and RON = 40 ohm.
5. The 1x self refresh rate is the rate at which the device is refreshed internally during self refresh before going into the

elevated temperature range.
6. This is the general definition that applies to full-array self refresh.
7. For all IDD measurements, VIHCKE = 0.8 × VDD2; VILCKE = 0.2 × VDD2.
8. Published IDD values except IDD4RQ are the maximum of the distribution of the arithmetic mean. Refer to the following note for IDD4RQ; refer to IDD6 Full-Array Self Refresh Current table for IDD6.
9. IDD4RQ value is reference only. Typical value. DBI disabled, VOH = 0.5 × VDDQ, TC = 25°C.
10. Measurement conditions of IDD4R and IDD4W values: DBI disabled, BL = 16.
11. IDD6 25°C is the typical value in the distribution with nominal VDD and a reference-only value. IDD6 85°C is the maximum IDD guaranteed value considering the worst-case conditions of process, temperature, and voltage.

AC Timing Parameters

Table 3-26: Core Timing Parameters (Continued)

Refresh rate is determined by the value in MR4 OP[2:0]

Parameter	Symbol	min/ max	Data Rate								Unit	Note
			533	1066	1600	2133	2667	3200	3733	4266		
ACTIVE to ACTIVE command period	tRC	min	tRAS + tRPab (with all-bank precharge) tRAS + tRPpb (with per-bank precharge)								ns	
Minimum Self-Refresh Time (Entry to Exit)	tSR	min	max(15ns, 3nCK)								ns	
Self Refresh exit to next valid command delay	tXSR	min	max(tRFCab + 7.5ns, 2nCK)								ns	
Exit power down to next valid command delay	tXP	min	max(7.5ns, 5nCK)								ns	
CAS to CAS delay	tCCD	min	8								tCK(avg)	
CAS to CAS delay (Masked Write w/ECC)	tCCDMW	min	32								tCK(avg)	
Internal Read to Precharge command delay	tRTP	min	max(7.5ns, 8nCK)								ns	
RAS to CAS Delay	tRCD	min	max(18ns, 4nCK)								ns	
Row Precharge Time (single bank)	tRPpb	min	max(18ns,3nCK)								ns	
Row Precharge Time (all banks) - 8-bank	tRPab	min	max(21ns, 3nCK)								ns	
Row Active Time	tRAS	min	max(42ns, 3nCK)								ns	
		max	min(9 * tREFI * Refresh Rate, 70.2)								us	
Write Recovery Time	tWR	min	max{18ns, 4nCK}								ns	
Write to Read Command Delay	tWTR	min	max(10ns, 8nCK)								ns	
Active bank A to Active bank B	tRRD	min	max(10ns, 4ncK)							max (7.5 ns, 4nc K)	ns	1
Precharge to Precharge Delay	tPPD	min	4								tCK	2
Four Bank Activate Window	tFAW	min	40							30	ns	1
Delay from SRE command to CKE input LOW	tESCKE	min	Max (1.75ns, 3nCK)									3

Notes:
1. 4266 Mbps timing value is supported at lower data rates if the device is supporting 4266Mbps speed grade.

2. Precharge to precharge timing restriction does not apply to AUTO PRECHARGE commands.
3. Delay time has to satisfy both analog time(ns) and clock count (*n*CK). It means that tESCKE will not expire until CK has toggled through at least three full cycles (3 tCK) and 1.75ns has transpired. The case which 3*n*CK is applied to is shown below.

Figure 3-13: tESCKE Timing

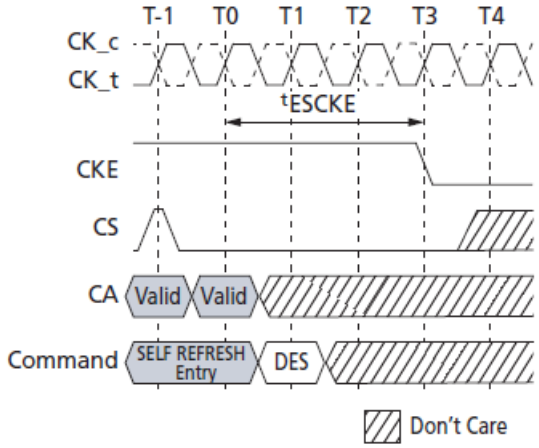


Table 3-27 — Clock timings

Parameter	Symbol	min/ max	1600	3200	3733	4266	Unit	Note
Average Clock Period	tCK(avg)	min	1.25	0.625	0.535	0.468	ns	
		max	100	100	100	100		
Average high pulse width	tCH(avg)	min	0.46				tCK(avg)	
		max	0.54					
Average low pulse width	tCL(avg)	min	0.46				tCK(avg)	
		max	0.54					
Absolute Clock Period	tCK(abs)	min	tCK(avg)min + tJIT(per)min				ns	
		max	-					
Absolute clock HIGH pulse width	tCH(abs)	min	0.43				tCK(avg)	
		max	0.57					
Absolute clock LOW pulse width	tCL(abs)	min	0.43				tCK(avg)	
		max	0.57					
Clock Period Jitter	tJIT(per)	min	-70	-40	-34	-30	ps	
		max	70	40	34	30		
Maximum Clock Jitter between two consecutive clock cycles	tJIT(cc)	min	-				ps	
		max	140	80	68	60		

Table 3-28: Read Output Timing

Parameter	Symbol	min/ max	1600	3200	3733	4266	Unit	Note
DQS output access time from CK/CK#	tDQSCK	min	1.5				ns	1
		max	3.5					
DQS output access time from CK_t/CK_c – temperature variation	tDQSCK_temp	max	4				ps/C	3
DQS output access time from CK_t/CK_c – voltage variation	tDQSCK_volt	max	7				ps/mV	2
CK to DQS rank to rank variation	tDQSCK_rank2rank	max	1				ns	4, 5
DQS_t, DQS_c to DQ skew total, per group, per access (DBI Disabled)	tDQSQ	max	0.18				UI	6
DQ output hold time total from DQS_t, DQS_c (DBI-Disabled)	tQH	min	min(tQSH, tQSL)				UI	6
DQ output window time total, per pin (DBI-Disabled)	tQW_total	min	0.75	0.7			UI	6, 11
DQS_t, DQS_c to DQ Skew total, per group, per access (DBI-Enabled)	tDQSQ_DBI	max	0.18				UI	6
DQ output hold time total from DQS_t, DQS_c (DBIenabled)	tQH_DBI	min	min(tQSH_DBI, tQSL_DBI)				UI	6
DQS Output Low Pulse Width (DBI Enabled)	tQSL_DBI	min	tCL(abs)-0.045				tCK(avg)	9, 11
DQS Output High Pulse Width (DBI Enabled)	tQSH_DBI	min	tCH(abs)-0.045				tCK(avg)	10, 11
Read preamble	tRPRE	min	1.8				tCK(avg)	
Read postamble	tRPST	min	0.4				tCK(avg)	
DQS Low-impedance time from CK_t, CK_c	tLZ(DQS)	min	(RL x tCK) + tDQSCK(Min) - (tPRE(Max) x tCK) - 200ps				ps	
DQS High-impedance time from CK_t, CK_c	tHZ(DQS)	max	(RL x tCK) + tDQSCK(Max) + (RPST(Max) x tCK) - 100ps				ps	
DQ Low-impedance time from CK_t, CK_c	tLZ(DQ)	min	(RL x tCK) + tDQSCK(Min) - 200ps				ps	
DQ High-impedance time from CK_t, CK_c	tHZ(DQ)	max	(RL x tCK) + tDQSCK(Max) + tDQSQ(Max)+ (BL/2 x tCK) - 100ps				ps	

Notes: 1. This parameter includes DRAM process, voltage, and temperature variation. It also includes the AC noise impact for frequencies >20 MHz and a max voltage of 45mV peakto-peak from DC-20 MHz at a fixed temperature on the package. The voltage supply noise must comply with the component MIN/MAX DC operating conditions.
2. t_{DQSCK_volt} max delay variation as a function of DC voltage variation for V_{DDQ} and V_{DD2}. The voltage supply noise must comply with the component MIN/MAX DC operating conditions. The voltage variation is defined as the max[abs(t_{DQSCK}(MIN)@V1-t_{DQSCK}(MAX)@V2), ABS(t_{DQSCK}(MAX)@V1-t_{DQSCK}(MIN)@V2)]/ABS(V1-V2).

3. tDQSCK_temp MAX delay variation as a function of temperature.
4. The same voltage and temperature are applied to tDQSCK_rank2rank.

5. tDQSCK_rank2rank parameter is applied to multi-ranks per byte lane within a package consisting of the same design dies.
6. DQ-to-DQS differential jitter where the total includes the sum of deterministic and random timing terms for a specified BER.
7. The deterministic component of the total timing.
8. This parameter will be characterized and guaranteed by design.
9. tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as measured from one falling edge to the next consecutive rising edge.
10. tQSH describes the instantaneous differential output high pulse width on DQS_t -DQS_c, as measured from one falling edge to the next consecutive rising edge.
11. This parameter is a function of input clock jitter. These values assume MIN tCH(ABS) and tCL(ABS). When the input clock jitter MIN tCH(ABS) and tCL(ABS) is 0.44 or greater than tCK(AVG), the MIN value of tQSL will be tCL(ABS) - 0.04 and tQSH will be tCH(ABS) - 0.04.

Table 3-29: Write Timing

Note UI = tCK(AVG)(MIN)/2

Parameter	Symbol	min/max	1600	3200	3733	4266	Unit	Note
Rx timing window total (At VdIVW voltage levels)	TdIVW_total	max	0.22	0.25			UI	1, 2, 3
DQ input pulse width (At Vcent_DQ)	TdIPW	min	0.45				UI	7
DQ to DQS offset	TDQS2DQ	min	200				ps	6
		max	800					
DQ to DQ offset	TDQDQ	max	30				ps	7
DQ to DQS offset temperature variation	TDQS2DQ_temp	max	0.6				ps/oC	8
DQ to DQS offset voltage variation	TDQS2DQ_volt	max	33				ps/50mV	9
DQ to DQS offset rank to rank	TDQS2DQ_rank2rank	max	200				ps	10,11
Write command to 1st DQS latching transition	tDQSS	min	0.75				tCK(avg)	
		max	1.25					
DQS input high-level width	tDQSH	min	0.4				tCK(avg)	
DQS input low-level width	tDQSL	min	0.4				tCK(avg)	
DQS falling edge to CK setup time	tDSS	min	0.2				tCK(avg)	
DQS falling edge hold time from CK	tDSH	min	0.2				tCK(avg)	
Write postamble	tWPST	min	0.4 (or 1.4 if extra postamble is programmed in MR)				tCK(avg)	
Write preamble	tWPRE	min	1.8				tCK(avg)	

Notes:
1. Data Rx mask voltage and timing parameters are applied per pin and include the DRAM DQ-to-DQS voltage AC noise impact for frequencies >20 MHz with a maximum voltage of 45mV peak-to-peak at a fixed temperature on the package. The voltage supply noise must comply to the component MIN/MAX DC operating conditions.
2. Rx differential DQ-to-DQS jitter total timing window at the VdIVW voltage levels.
3. Defined over the DQ internal VREF range. The Rx mask at the pin must be within the internal VREF(DQ) range irrespective of the input signal common mode.
4. Rx mask defined for one pin toggling with other DQ signals in a steady state.
5. DQ-only minimum input pulse width defined at the VCENT_DQ(pin_mid).
6. DQ-to-DQS offset is within byte from DRAM pin to DRAM internal latch. Includes all DRAM process, voltage, and temperature variations.
7. DQ-to-DQ offset defined within byte from DRAM pin to DRAM internal latch for a given component.
8. tDQS2DQ (MAX) delay variation as a function of temperature.
9. tDQS2DQ (MAX) delay variation as a function of the DC voltage variation for VDDQ and VDD2. It includes the VDDQ and VDD2 AC noise impact for frequencies >20 MHz and MAX voltage of 45mV peak-to-peak from DC-20 MHz at a fixed temperature on the package.
10. The same voltage and temperature are applied to tDQS2DQ_rank2rank.
11. tDQS2DQ_rank2rank parameter is applied to multi-ranks per byte lane within a package consisting of the same design dies.

Table 3-30: CKE Input Timing

Parameter	Symbol	min/max	1600	3200	3733	4266	Unit	Note
CKE minimum pulse width (HIGH and LOW pulse width)	tCKE	min	Max(7.5ns,4nCK)				-	1
Delay from valid command to CKE input LOW	tCMDCKE	min	Max(1.75ns,3nCK)				ns	1
Valid Clock Requirement after CKE Input low	tCKELCK	min	Max(5ns,5nCK)				ns	1
Valid CS Requirement before CKE Input Low	tCSCKE	min	1.75				ns	
Valid CS Requirement after CKE Input low	tCKELCS	min	Max(5ns, 5nCK)				ns	1
Valid Clock Requirement before CKE Input High	tCKCKEH	min	Max(1.75ns, 3nCK)				ns	1
Exit power- down to next valid command delay	tXP	min	Max(7.5ns, 5nCK)				ns	1
Valid CS Requirement before CKE Input High	tCSCKEH	min	1.75				ns	
Valid CS Requirement after CKE Input High	tCKEHCS	min	Max(7.5ns, 5nCK)				ns	1
Valid Clock and CS Requirement after CKE Input low after MRW Command	tMRWCKEL	min	Max(14ns, 10nCK)				ns	1
Valid Clock and CS Requirement after CKE Input low after ZQ Calibration Start Command	tZQCKE	min	Max(1.75ns, 3nCK)				ns	1

Note: 1. Delay time has to satisfy both analog time(ns) and clock count (*n*CK). For example, tCMDCKE will not expire until CK has toggled through at least 3 full cycles (3tCK) and 3.75ns has transpired. The case that 3*n*CK is applied to is shown below.

Figure 3-14: tCMDCKE Timing

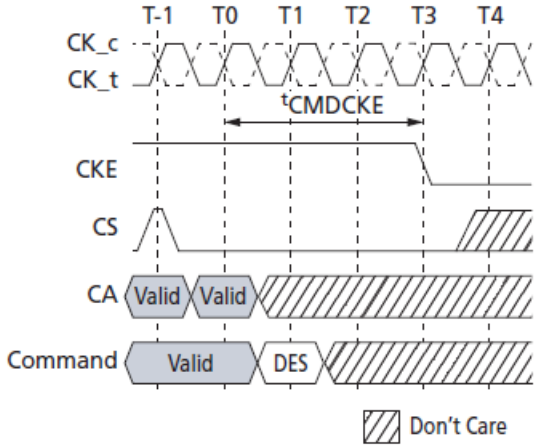


Table 3-31: Post-Package Repair Timing Parameters

Parameter	Symbol	min	max	Unit	Note
PPR Programming Time	tPGM	1000	-	ms	
PPR Exit Time	tPGM_Exit	15	-	ns	
New Address Setting Time	tPGMPST	50	-	us	

Table 3-32 — ZQ Calibration timings

Parameter	Symbol	min/max	Value	Unit	Note
ZQCAL START to ZQCAL LATCH command interval	tZQCAL	max	1	us	
ZQCAL LATCH to next valid command interval	tZQLAT	max	max(30ns, 8nCK)	ns	
ZQCAL RESET to next valid command interval	tZQRESET	max	max(50ns, 3nCK)	ns	

Table 3-33: Temperature Derating Parameters

Parameter	Symbol	min/max	1600	3200	3733	4266	Unit	Note
DQS Output access time from CK_t/CK_c (derated)	tDQSCKd	max	3600				ps	1
RAS-to-CAS delay (derated)	tRCDd	min	tRCD + 1.875				ns	1
Activate-to-Activate command period (derated)	tRCd	min	tRC + 3.75				ns	1
Row active time (derated)	tRASd	min	tRAS + 1.875				ns	1
Row precharge time (derated)	tRPd	min	tRP + 1.875				ns	1
Active bank A to Active bank B (derated)	tRRDd	min	tRRD + 1.875				ns	1

Note: 1. At higher temperatures (>85°C), AC timing derating may be required. If derating is required the device will set MR4 OP[2:0] = 110b.

Truth Tables

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the LPDDR4X device must be powered down and then restarted through the specified initialization sequence before normal operation can continue.

Table 3-34 — Command Truth Table

Command	CS_n	DDR CA Pins (10)						CK_tedge	Notes
		CA0	CA1	CA2	CA3	CA4	CA5		
Deselect (DES)	L	X						R1	1,2
Multi Purpose Command (MPC)	H	L	L	L	L	L	OP6	R1	1,2,9
	L	OP0	OP1	OP2	OP3	OP4	OP5	R2	
Precharge (Per Bank, All Bank)	H	L	L	L	L	H	AB	R1	1,2,3,4
	L	BA0	BA1	BA2	V	V	V	R2	
Refresh (Per Bank, All Bank)	H	L	L	L	H	L	AB	R1	1,2,3,4
	L	BA0	BA1	BA2	V	V	V	R2	
Self Refresh Entry	H	L	L	L	H	H	V	R1	1,2
	L	V						R2	
Write-1	H	L	L	H	L	L	BL	R1	1,2,3,6,7,9
	L	BA0	BA1	BA2	V	C9	AP	R2	
Self Refresh Exit	H	L	L	H	L	H	V	R1	1,2
	L	V						R2	
Mask Write-1	H	L	L	H	H	L	BL	R1	1,2,3,5,6,9
	L	BA0	BA1	BA2	V	C9	AP	R2	
RFU	H	L	L	H	H	H	V	R1	1,2
	L	V						R2	
Read-1	H	L	H	L	L	L	BL	R1	1,2,3,6,7,9
	L	BA0	BA1	BA2	V	C9	AP	R2	
CAS-2 (Write-2 or Mask Write-2 or Read-2 or MRR-2)	H	L	H	L	L	H	C8	R1	1,8,9
	L	C2	C3	C4	C5	C6	C7	R2	
RFU	H	L	H	L	H	L	V	R1	1,2
	L	V						R2	
RFU	H	L	H	L	H	H	V	R1	1,2
	L	V						R2	
MRW-1	H	L	H	H	L	L	OP7	R1	1,2,11
	L	MA0	MA1	MA2	MA3	MA4	MA5	R2	
MRW-2	H	L	H	H	L	H	OP6	R1	1,2,11
	L	OP0	OP1	OP2	OP3	OP4	OP5	R2	
MRR-1	H	L	H	H	H	L	V	R1	1,2,12
	L	MA0	MA1	MA2	MA3	MA4	MA5	R2	

RFU	H	L	H	H	H	H	V	R1	1,2
	L	V						R2	
Activate-1	H	H	L	R12	R13	R14	R15	R1	1,2,3,10
	L	BA0	BA1	BA2	R16	R10	R11	R2	
Activate-2	H	H	H	R6	R7	R8	R9	R1	1,10
	L	R0	R1	R2	R3	R4	R5	R2	

Notes

1. All LPDDR4X commands except for Deselect are 2 clock cycle long and defined by states of CS and CA[5:0] at the first rising edge of clock. Deselect command is 1 clock cycle long.
2. "V" means "H" or "L" (a defined logic level). "X" means don't care in which case CS, CK_t, CK_c and CA[5:0] can be floated.
3. Bank addresses BA[2:0] determine which bank is to be operated upon.
4. AB "HIGH" during Precharge or Refresh command indicates that command must be applied to all banks and bank address is a don't care.
5. Mask Write-1 command supports only BL 16. For Mark Write-1 command, CA5 must be driven LOW on first rising clock cycle (R1).
6. AP "HIGH" during Write-1, Mask Write-1 or Read-1 commands indicates that an auto-precharge will occur to the bank associated with the Write, Mask Write or Read command.
7. If Burst Length on-the-fly is enabled, BL "HIGH" during Write-1 or Read-1 command indicates that Burst Length should be set on-the-Fly to BL=32. BL "LOW" during Write-1 or Read-1 command indicates that Burst Length should be set on-the-fly to BL=16. If Burst Length on-the-fly is disabled, then BL must be driven to defined logic level "H" or "L".
8. For CAS-2 commands (Write-2 or Mask Write-2 or Read-2 or MRR-2 or MPC (Only Write FIFO, Read FIFO & Read DQ Calibration), C[1:0] are not transmitted on the CA[5:0] bus and are assumed to be zero. Note that for CAS-2 Write-2 or CAS-2 Mask Write-2 command, C[3:2] must be driven LOW.
9. Write-1 or Mask Write-1 or Read-1 or Mode Register Read-1 or MPC (Only Write FIFO, Read FIFO & Read DQ Calibration) command must be immediately followed by CAS-2 command consecutively without any other command in between. Write-1 or Mask Write-1 or Read-1 or Mode Register Read-1 or MPC (Only Write FIFO, Read FIFO & Read DQ Calibration) command must be issued first before issuing CAS-2 command. MPC (Only Start & Stop DQS Oscillator, Start & Latch ZQ Calibration) commands do not require CAS-2 command; they require two additional DES or NOP commands consecutively before issuing any other commands.
10. Activate-1 command must be immediately followed by Activate-2 command consecutively without any other command in between. Activate-1 command must be issued first before issuing Activate-2 command. Once Activate-1 command is issued, Activate-2 command must be issued before issuing another Activate-1 command.
11. MRW-1 command must be immediately followed by MRW-2 command consecutively without any other command in between. MRW-1 command must be issued first before issuing MRW-2 command.
12. MRR-1 command must be immediately followed by CAS-2 command consecutively without any other command in between. MRR-1 command must be issued first before issuing CAS-2 command.

Section 4

Revision History

Revision History

Rev.	History	Date
1.0	Initial Release	03 / 2023
1.1	Removed 5.0 reference	05 / 2023
1.2	Added Kingston contact info	06 / 2023

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