**Notification Number:** 20220222001.0 **Notification Date:** April 27, 2022

Title: Datasheet for DS90UH948-Q1 and DS90UB948-Q1

**Customer Contact:** Notification Manager **Quality Services** Dept:

Change Type: Electrical Specification

## **Description of Change:**

Texas Instruments Incorporated is announcing an information only notification.

The product datasheet(s) is being updated as summarized below.

The following change history provides further details.



DS90UH948-Q1

SNLS473D - OCTOBER 2014 - REVISED FEBRUARY 2022

С	hanges from Revision C (December 2020) to Revision D (February 2022)	Page
•	Clarified max channel insertion loss over frequency	1
•	Clarified the description of the clock and data differential output pins	
•	Changed IDx pin voltage from VDD18 to VDD33	
•	Removed normal mode PASS function since PASS is used only in BIST mode	
•	Updated the inclusive termonologies for SPI and I2C by changing "master" and "slave" wording	
•	Updated the SPI pin names from "MOSI" to "PICO", "MISO" to "POCI", and "SS" to "CS"	
•	Changed the I2S mode names from Slave Mode to Surround Sound Mode, and from Master Mode to Auxiliary Audio Mode	
	Added some missing units for current and voltage	
	Modified the list of compatible devices	
	Removed PASS from the table since PASS functionality is only used for BIST mode	
	Corrected the Nyquist Frequency for PCLK 192MHz	
	Added clarification for I2S transport modes	
	Added clarifying notes for BIST function.	
	Added a clarifying note on using I2C while PATGEN is enabled	
	Added new section "Dual Swap"	
	Clarified LVDS mapping names.	
	LVDS Formats table added	
	Added clarifying notes to LUT contents.	
	Added LUT Programming Example	
	Added clarifying notes about I2C access over the BCC	
	Specified which registers are not being reset when digital reset is applied	
	Changed default value of register 0x01[2] and added clarifying notes	
	Changed default value of register 0x03[7]	
	Changed reset value of register 0x1D, and changed default value for bits [7:4]	
	Changed reset value for registers 0x1E and 0x1F to 0x00	
•	Added clarifying note to register 0x22, that surround audio is not supported in repeater mode when 18 video mode is enabled	3-bit
	Added minimum value to register 0x26	
•	Changed default value for register 0x45[7:5] and changed to R/W. Added clarifying note.	
•	Changed default value for register 0x4B[3:2] and changed to R/W. Added clarifying note	
•	Added clarifying note to CMLOUT function in register 0x57	
•	Changed default value for register 0xF4	
•	Corrected the name of the Pattern Generation Application Note in the Related Documentation section	106



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•	Changed default value for register 0xF4					
•	Corrected the name of the Pattern Generation Application Note in the Related Documentation section99					
— he	datasheet number will be changing.					
Device Family		Change From:	Change To:			
DS90UH948-Q1		SNLS473C	SNLS473D			
DS90UB948-Q1		SNLS477C	SNLS477D			

These changes may be reviewed at the datasheet links provided.

http://www.ti.com/product/DS90UH948-Q1

http://www.ti.com/product/DS90UB948-Q1

### **Reason for Change:**

To accurately reflect device characteristics.

# Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

No anticipated impact. This is a specification change announcement only. There are no changes to the actual device.

## Changes to product identification resulting from this notification:

None.

Product Affected:					
DS90UH948TNKDRQ1	DS90UH948TNKDTQ1	DS90UB948TNKDTQ1	DS90UB948TNKDRQ1		

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