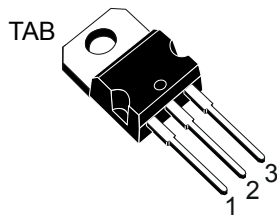
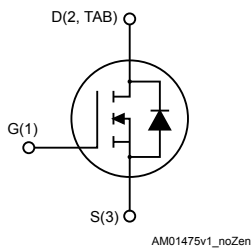


N-channel 40 V, 1.7 mΩ typ., 160 A, STripFET™ F6 Power MOSFET in a TO-220 package


TO-220


Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STP318N4F6	40 V	2.2 mΩ	160 A

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the STripFET™ F6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low R_{DS(on)} in all packages.

Product status	
STP318N4F6	
Device summary	
Order code	STP318N4F6
Marking	318N4F6
Package	TO-220
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	40	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	160	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	160	A
$I_{DM}^{(2)}$	Drain current (pulsed)	640	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	341	W
E_{AS}	Single pulse avalanche energy (starting $T_J=25\text{ }^\circ\text{C}$, $I_D=60\text{ A}$, $V_{DD}=35\text{ V}$)	1100	mJ
T_J	Operating junction temperature range	-55 to 175	$^\circ\text{C}$
T_{stg}	Storage temperature range		

1. Limited by wire bonding.
2. Pulse width limited by safe operating area.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.44	$^\circ\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-amb	62.5	$^\circ\text{C/W}$

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 3. On/Off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0\ \text{V}$	40			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\ \text{V}$, $V_{DS} = 40\ \text{V}$			1	μA
		$V_{GS} = 0\ \text{V}$, $V_{DS} = 40\ \text{V}$, $T_C = 125\text{ °C}$ ⁽¹⁾			100	μA
I_{GSS}	Gate-body leakage current	$V_{GS} = \pm 20\ \text{V}$, $V_{DS} = 0\ \text{V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\ \text{V}$, $I_D = 80\ \text{A}$		1.7	2.2	m Ω

1. Defined by design, not subject to production test.

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\ \text{V}$, $f = 1\ \text{MHz}$, $V_{GS} = 0\ \text{V}$	-	13800	-	nF
C_{oss}	Output capacitance		-	1870	-	nF
C_{riss}	Reverse transfer capacitance		-	1095	-	nF
Q_g	Total gate charge	$V_{DD} = 20\ \text{V}$, $I_D = 160\ \text{A}$,	-	240	-	nC
Q_{gs}	Gate-source charge	$V_{GS} = 0$ to $10\ \text{V}$	-	59	-	nC
Q_{gd}	Gate-drain charge	(see Figure 15. Test circuit for gate charge behavior)	-	75.2	-	nC

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 20\ \text{V}$, $I_D = 80\ \text{A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\ \text{V}$ (see Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform)	-	28	-	ns
t_r	Rise time		-	98	-	ns
$t_{d(off)}$	Turn-off delay time		-	190	-	ns
t_f	Fall time		-	95	-	ns

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on-voltage	$I_{SD} = 160\ \text{A}$, $V_{GS} = 0\ \text{V}$	-		1.1	V

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{rr}	Reverse recovery time	$I_{SD} = 160 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$	-	58.7		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 32 \text{ V}$, (see Figure 16 . Test circuit for inductive load switching and diode recovery times)	-	99.2		nC
I_{RRM}	Reverse recovery current		-	3.38		A

1. Pulsed: pulse duration=300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 3. Safe operating area

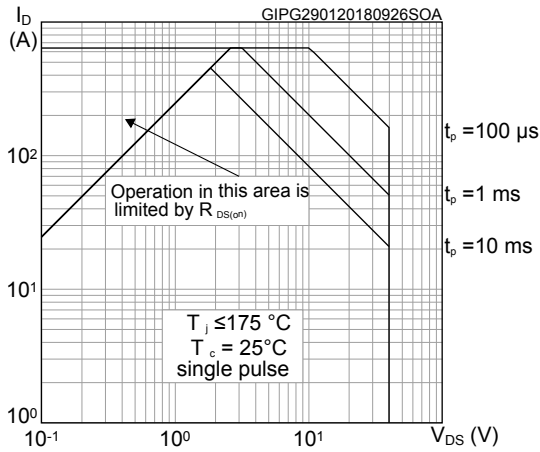


Figure 4. Normalized thermal impedance

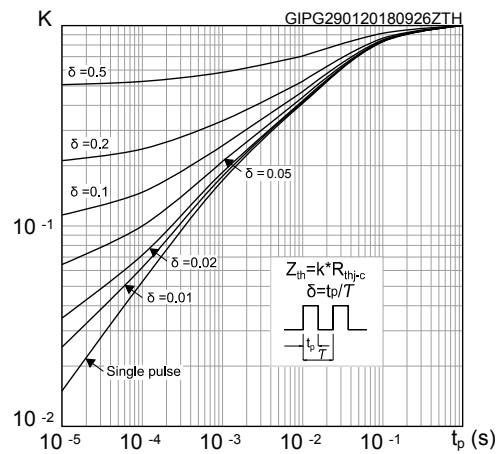


Figure 5. Output characteristics

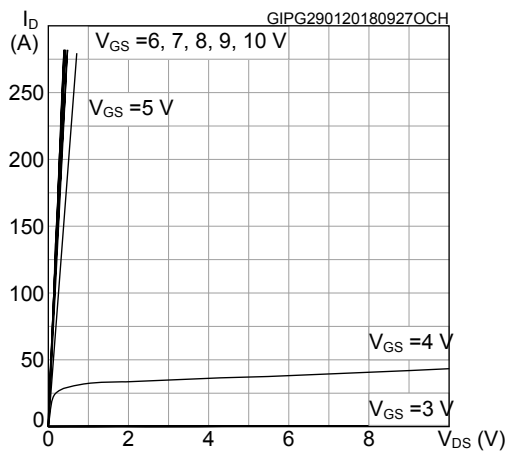


Figure 6. Transfer characteristics

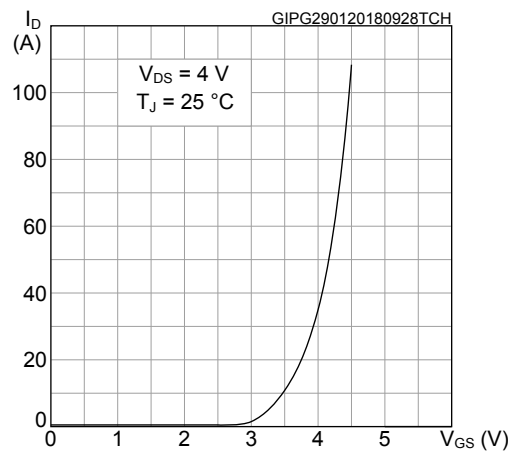


Figure 7. Static drain-source on-resistance

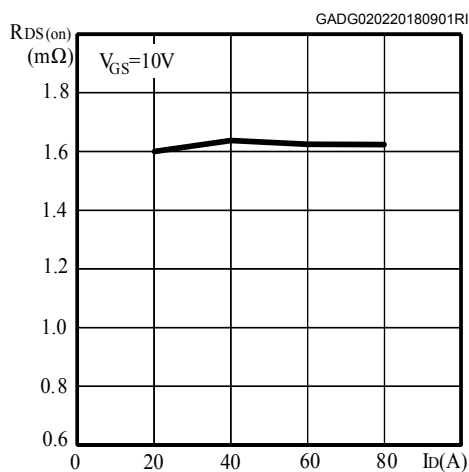


Figure 8. Normalized $V_{(BR)DSS}$ vs. temperature

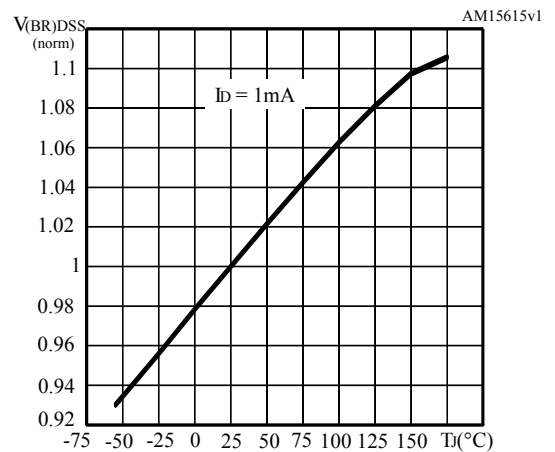


Figure 9. Capacitance variations

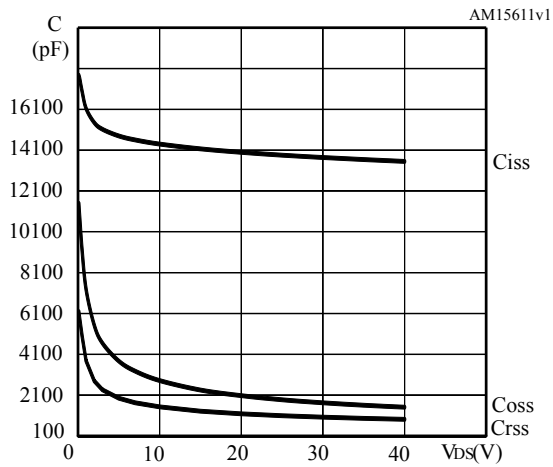


Figure 10. Gate charge vs gate-source voltage

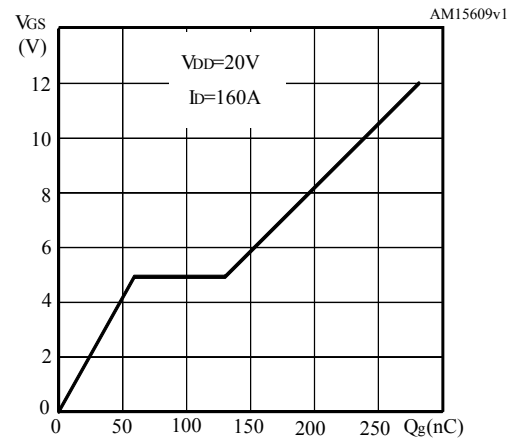


Figure 11. Normalized V_{GS(th)} vs. temperature

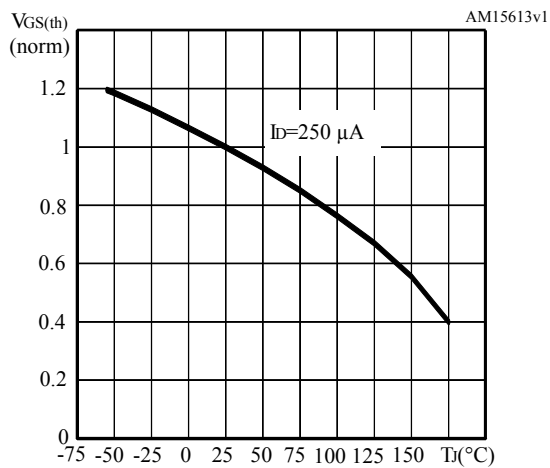


Figure 12. Normalized R_{DS(on)} vs. temperature

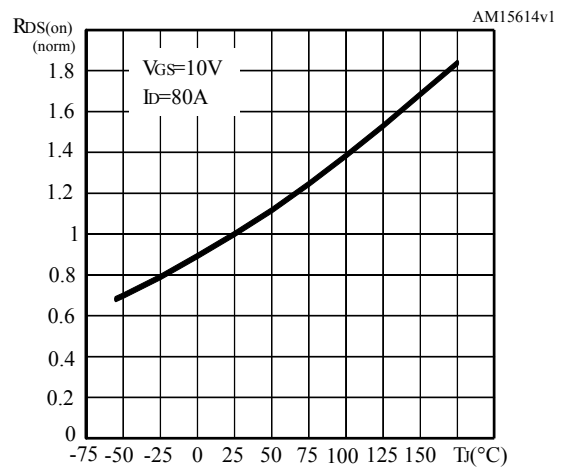
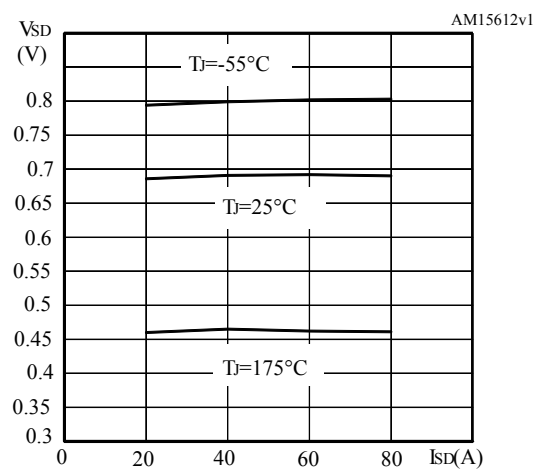
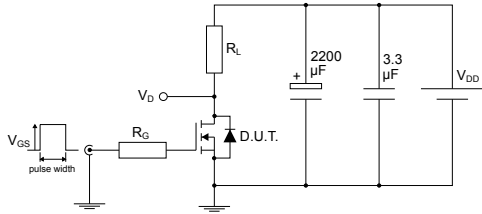


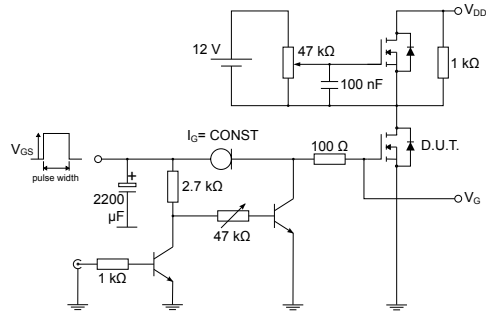
Figure 13. Source-drain diode characteristics



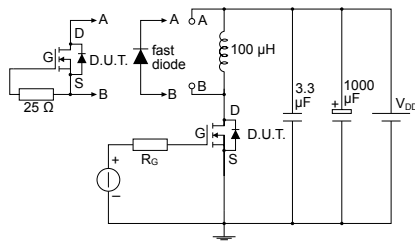
3 Test circuits

Figure 14. Test circuit for resistive load switching times


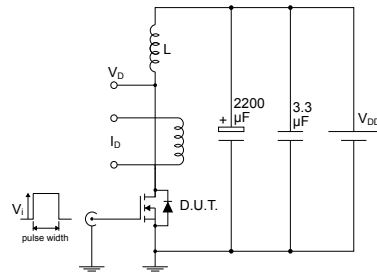
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Figure 15. Test circuit for gate charge behavior


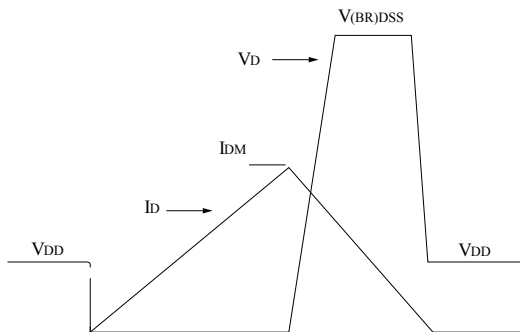
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Figure 16. Test circuit for inductive load switching and diode recovery times


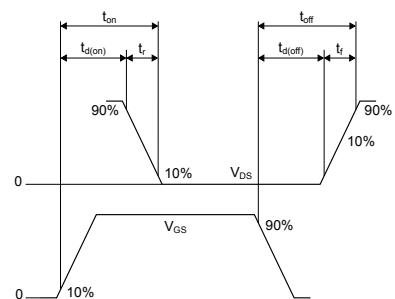
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Figure 17. Unclamped inductive load test circuit


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Figure 18. Unclamped inductive waveform


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Figure 19. Switching time waveform


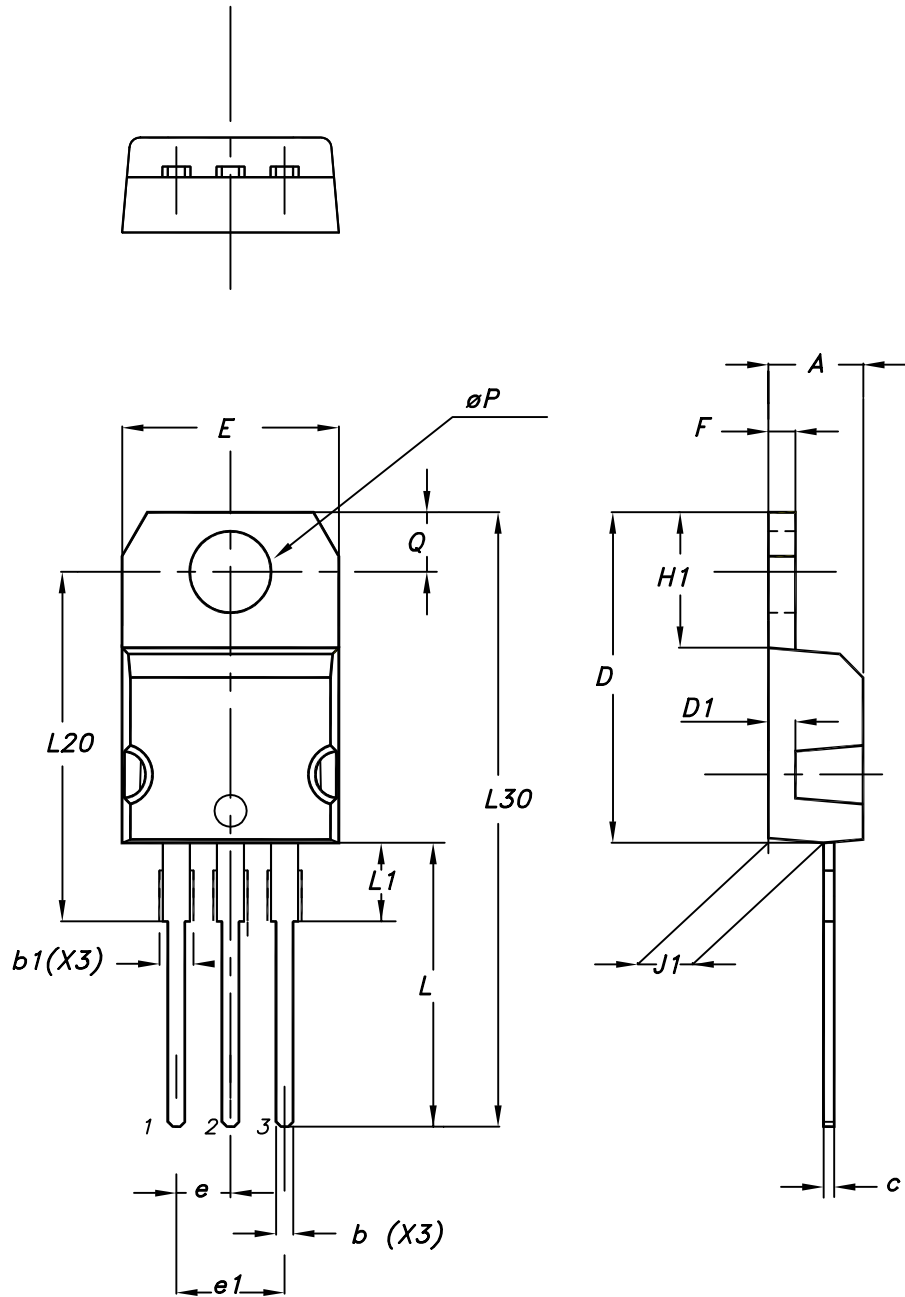
AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO-220 type A package information

Figure 20. TO-220 type A package outline



0015988_typeA_Rev_21

Table 7. TO-220 type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

Contents

1	Electrical ratings	2
2	Electrical characteristics	3
2.1	Electrical characteristics (curves)	5
3	Test circuits	7
4	Package information	8
4.1	TO-220 type A package information	8
	Revision history	12

Revision history

Table 8. Document revision history

Date	Version	Changes
08-Feb-2018	1	Initial release. Production data.

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