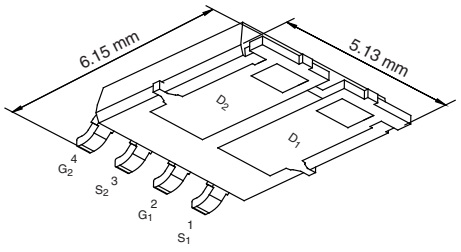
Automotive Dual N-Channel 40 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	40
$R_{DS(on)}$ (Ω) at V_{GS} = 10 V	0.0093
$R_{DS(on)}$ (Ω) at V_{GS} = 4.5 V	0.0111
I_D (A) per leg	30
Configuration	Dual

PowerPAK® SO-8L Dual



Bottom View

FEATURES

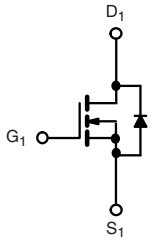
- TrenchFET® Power MOSFET
- 100 % R_g and UIS Tested
- AEC-Q101 Qualified[d]
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

AUTOMOTIVE GRADE

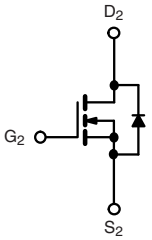
Pb-free

RoHS COMPLIANT

HALOGEN FREE



N-Channel MOSFET



N-Channel MOSFET

ORDERING INFORMATION	
Package	PowerPAK SO-8L
Lead (Pb)-free and Halogen-free	SQJ912AEP-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current[a]	T_C = 25 °C	I_D	30	A
	T_C = 125 °C		29	
Continuous Source Current (Diode Conduction)[a]		I_S	30	
Pulsed Drain Current[b]		I_{DM}	120	
Single Pulse Avalanche Current	L = 0.1 mH	I_{AS}	26	
Single Pulse Avalanche Energy		E_{AS}	34	mJ
Maximum Power Dissipation[b]	T_C = 25 °C	P_D	48	W
	T_C = 125 °C		16	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to + 175	°C
Soldering Recommendations (Peak Temperature)[e, f]			260	

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-Ambient	PCB Mount[c]	R_{thJA}	85	°C/W
Junction-to-Case (Drain)		R_{thJC}	3.1	

Notes

a. Package limited.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
c. When mounted on 1" square PCB (FR4 material).
d. Parametric verification ongoing.
e. See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
f. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

SPECIFICATIONS (T_C = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA		40	-	-	V
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		1.5	2	2.5	
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V	V_{DS} = 40 V	-	-	1	µA
		V_{GS} = 0 V	V_{DS} = 40 V, T_J = 125 °C	-	-	50	
		V_{GS} = 0 V	V_{DS} = 40 V, T_J = 175 °C	-	-	150	
On-State Drain Current[a]	$I_{D(on)}$	V_{GS} = 10 V	V_{DS} ≥ 5 V	30	-	-	A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 9.7 A	-	0.0077	0.0093	Ω
		V_{GS} = 4.5 V	I_D = 8.9 A	-	0.0093	0.0111	
		V_{GS} = 10 V	I_D = 9.7 A, T_J = 125 °C	-	-	0.0138	
		V_{GS} = 10 V	I_D = 9.7 A, T_J = 175 °C	-	-	0.0169	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 10 A		-	58	-	S
Dynamic[b]							
Input Capacitance	C_{iss}	V_{GS} = 0 V	V_{DS} = 20 V, f = 1 MHz	-	1438	1835	pF
Output Capacitance	C_{oss}			-	217	271	
Reverse Transfer Capacitance	C_{rss}			-	91	114	
Total Gate Charge[c]	Q_g	V_{GS} = 10 V	V_{DS} = 20 V, I_D = 11.3 A	-	25.6	38	nC
Gate-Source Charge[c]	Q_{gs}			-	4	-	
Gate-Drain Charge[c]	Q_{gd}			-	4	-	
Gate Resistance	R_g	f = 1 MHz		0.72	1.44	2.2	Ω
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 20 V, R_L = 20 Ω I_D ≅ 1 A, V_{GEN} = 10 V, R_g = 1 Ω		-	10	15	ns
Rise Time[c]	t_r			-	9	14	
Turn-Off Delay Time[c]	$t_{d(off)}$			-	23	35	
Fall Time[c]	t_f			-	11	17	
Source-Drain Diode Ratings and Characteristics[b]							
Pulsed Current[a]	I_{SM}			-	-	120	A
Forward Voltage	V_{SD}	I_F = 6.5 A, V_{GS} = 0 V		-	0.8	1.1	V

Notes

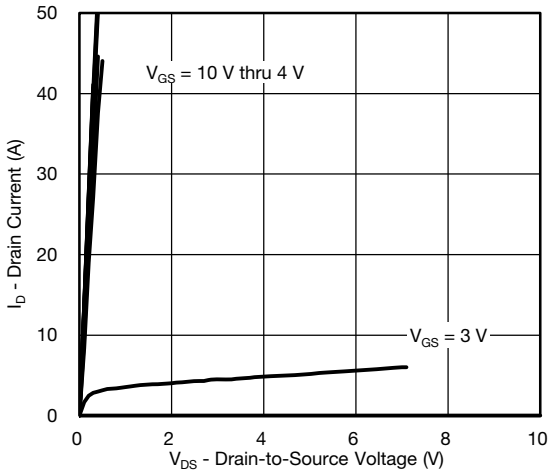
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.

b. Guaranteed by design, not subject to production testing.

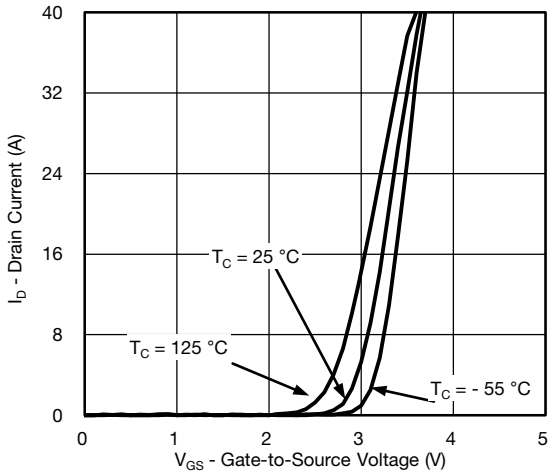
c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

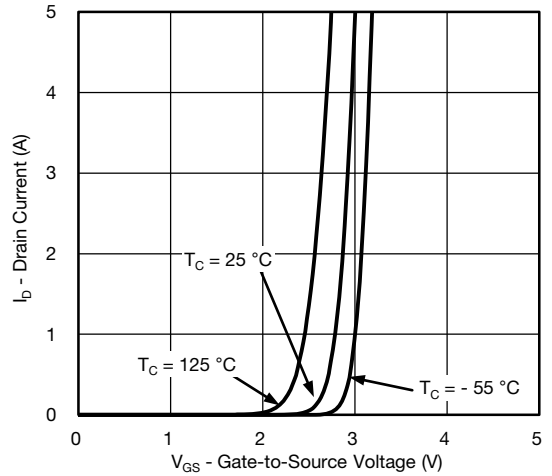
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



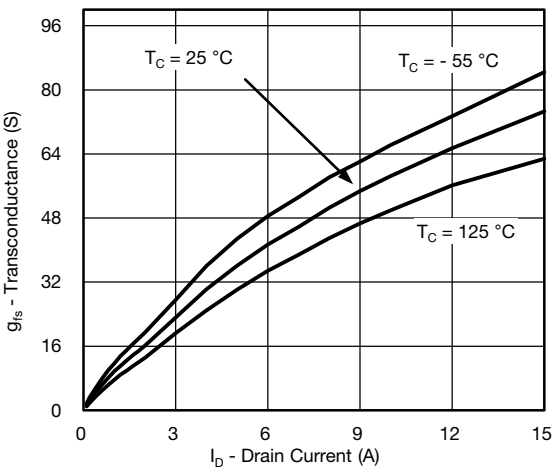
Output Characteristics



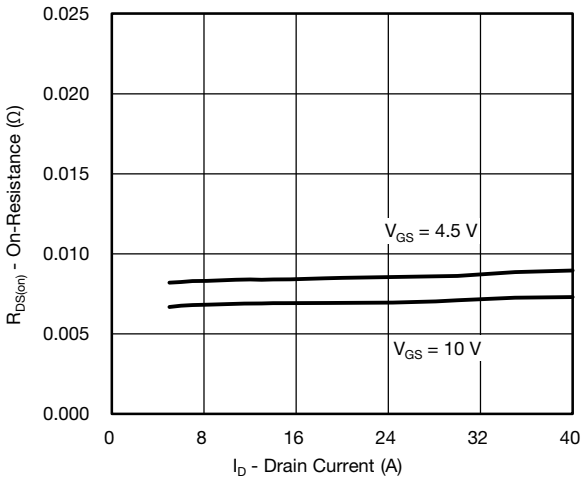
Transfer Characteristics



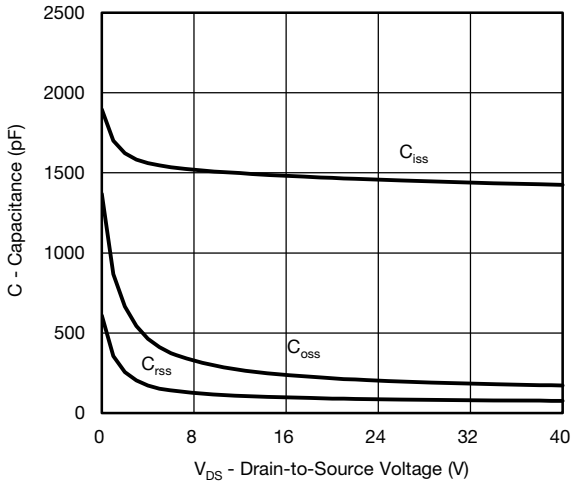
Transfer Characteristics



Transconductance

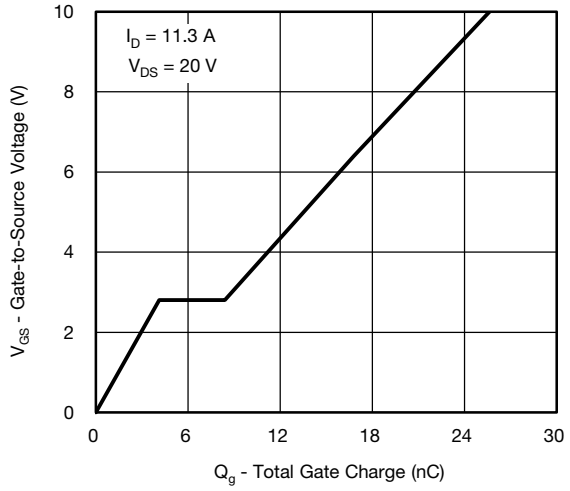


Capacitance

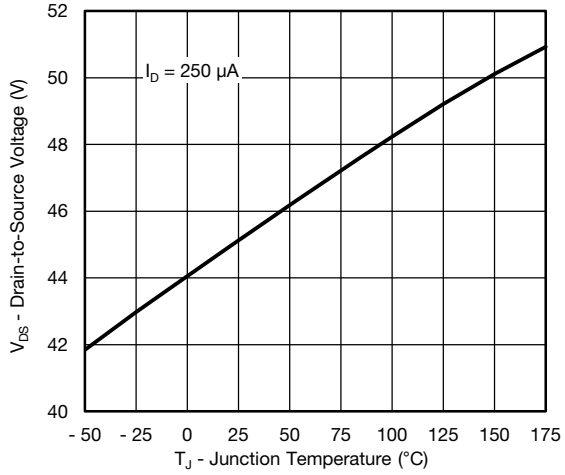


Gate Charge

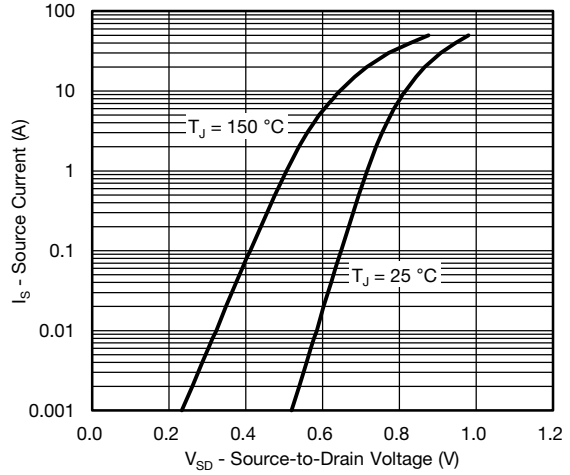
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



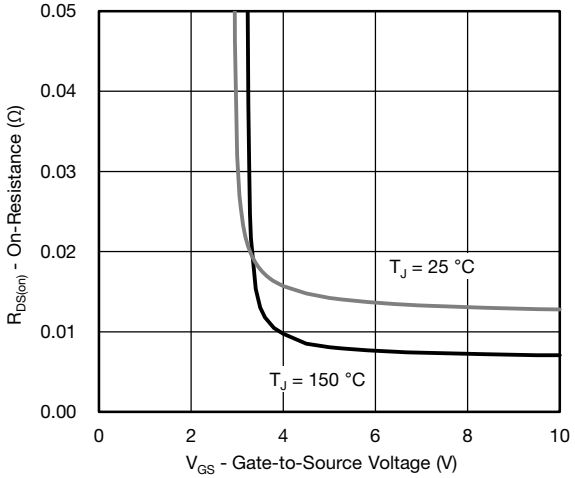
Gate Charge



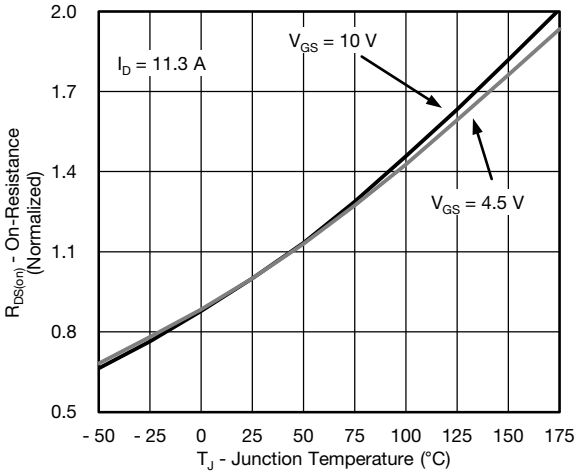
Drain-Source Breakdown vs. Junction Temperature



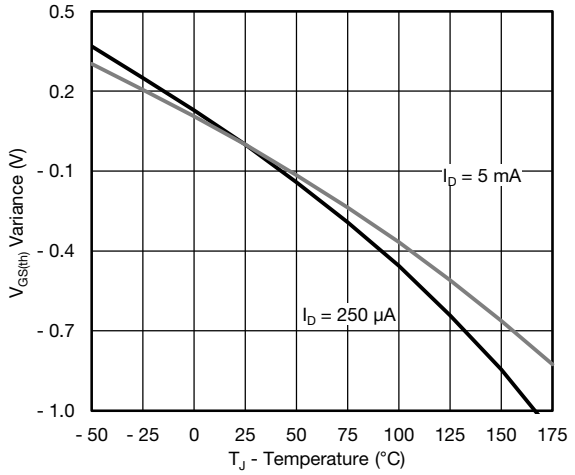
Source Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

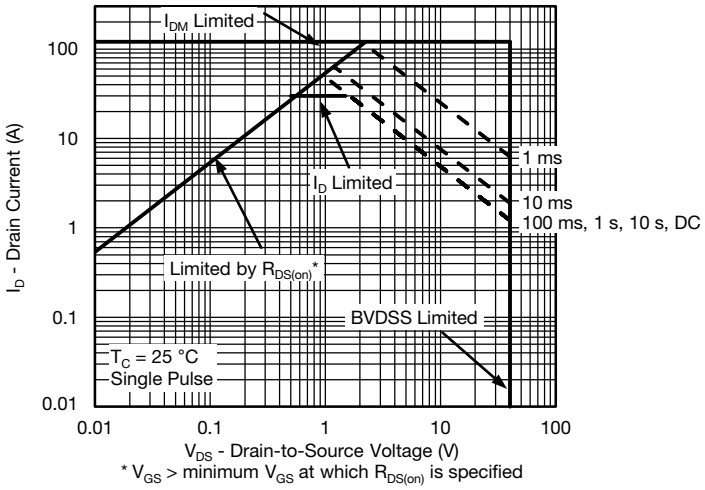


On-Resistance vs. Junction Temperature

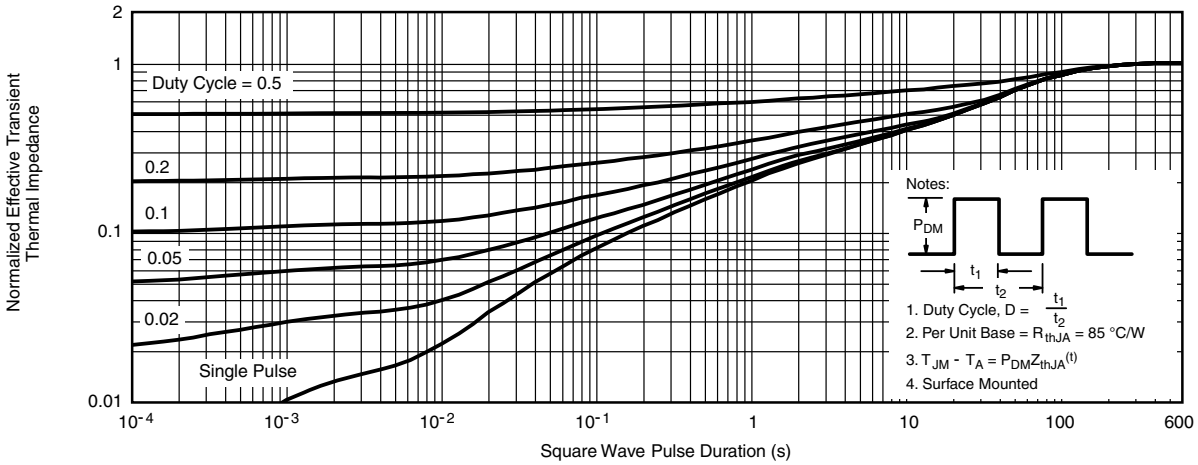


Threshold Voltage

THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)

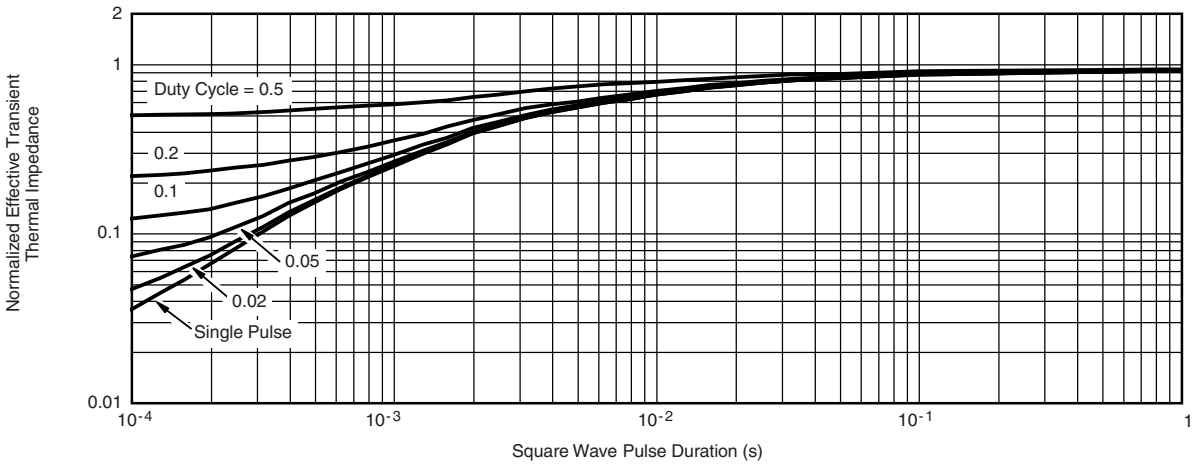


Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient

THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

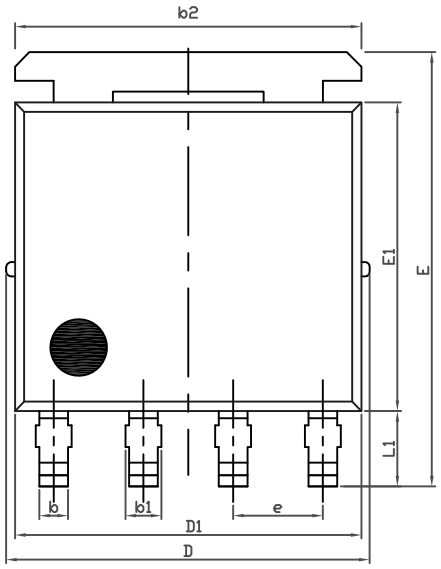
Note

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

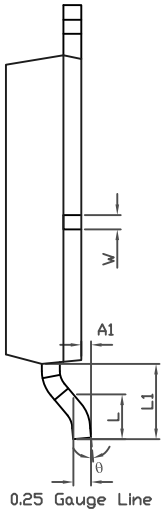
  are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

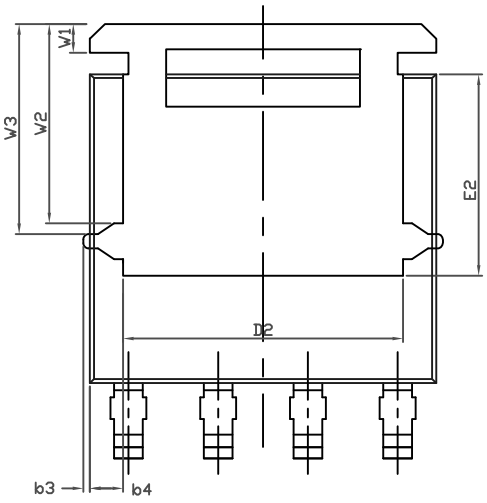
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62876.

PowerPAK® SO-8L Case Outline 2

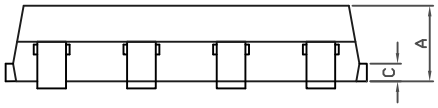


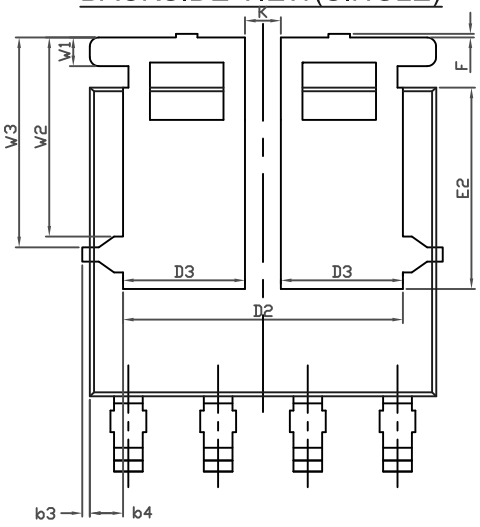
TOPSIDE VIEW





BACKSIDE VIEW(SINGLE)





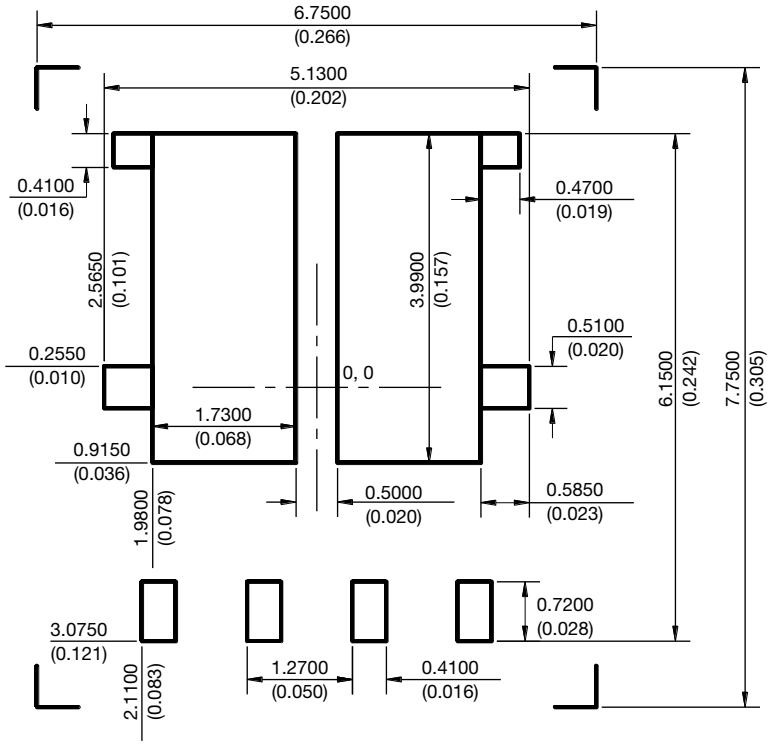
BACKSIDE VIEW(DUAL)

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	1.07	1.14	0.039	0.042	0.045
A1	0.00	-	0.127	0.00	-	0.005
b	0.33	0.41	0.48	0.013	0.016	0.019
b1	0.44	0.51	0.58	0.017	0.020	0.023
b2	4.80	4.90	5.00	0.189	0.193	0.197
b3	0.094			0.004		
b4	0.47			0.019		
c	0.20	0.25	0.30	0.008	0.010	0.012
D	5.00	5.13	5.25	0.197	0.202	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.86	3.96	4.06	0.152	0.156	0.160
D3	1.63	1.73	1.83	0.064	0.068	0.072
e	1.27 BSC			0.050 BSC		
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	4.27	4.37	4.47	0.168	0.172	0.176
E2	2.75	2.85	2.95	0.108	0.112	0.116
F	-	-	0.15	-	-	0.006
L	0.62	0.72	0.82	0.024	0.028	0.032
L1	0.92	1.07	1.22	0.036	0.042	0.048
K	0.51			0.020		
W	0.23			0.009		
W1	0.41			0.016		
W2	2.82			0.111		
W3	2.96			0.117		
q	0°	-	10°	0°	-	10°
ECN: S19-0643-Rev. B, 05-Aug-2019 DWG: 6044						

Note

- Millimeters will gover

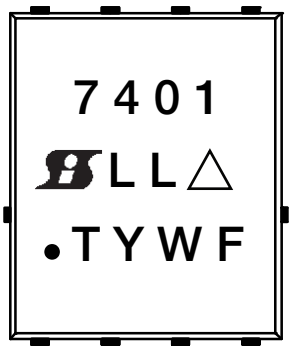
RECOMMENDED MINIMUM PAD FOR PowerPAK® SO-8L DUAL



Recommended Minimum Pads
Dimensions in mm (inches)
Keep-out 6.75 (0.266) x 7.75 (0.305)

PowerPAK® SO-8, PowerPAK® SO-8L, PowerPAK® 1212-8, PowerPAK® 1212-8S, PowerPAK® 1212-8W, PowerPAIR® 6 x 3.7, PowerPAIR® 6 x 5, PowerPAIR® 3 x 3

Single and Dual



7401 = example base part number or marking code [a]

= Siliconix logo

LL = lot code

△ = ESD symbol

● = pin 1 indicator

T = assembly factory code

Y = year ode

W = week code

F = wafer fab code

Note

a. These digits will be a code, if indicated on the datasheet. Otherwise, the digits will be the base number like indicated in the example

YEAR CODE			
YEAR	**CODE**	**YEAR**	**CODE**
2010	0	2020	0
2011	1	2021	1
2012	2	2022	2
2013	3	2023	3
2014	4	2024	4
2015	5	2025	5
2016	6	2026	6
2017	7	2027	7
2018	8	2028	8
2019	9	2029	9

WEEK CODE	
WORK WEEK	**CODE**
1 to 6	1
7 to 12	2
13 to 18	3
19 to 24	4
25 to 30	5
31 to 36	6
37 to 42	7
43 to 48	8
49 to 53	9

The current marking strategy is reflected. Contact your local sales representative for historical marking strategies for these packages.

Ordering Code for SQ Series Automotive MOSFET

Standard ordering code for SQ series of automotive MOSFETs can be derived per the following table:

PACKAGE TYPE	DATASHEET PART NUMBER	ORDERING SUFFIX	ORDERING PART NUMBER
PowerPAK® SC-70	Datasheet part number (example: SQA401EJ)	-T1_GE3	Datasheet part number + "-T1_GE3" (example: SQA401EJ-T1_GE3)
PowerPAK® 1212	Datasheet part number (example: SQ7415AENW)	-T1_GE3	Datasheet part number + "-T1_GE3" (example: SQ7415AENW-T1_GE3)
PowerPAK® SO-8L	Datasheet part number (example: SQJ459EP)	-T1_GE3	Datasheet part number + "-T1_GE3" (example: SQJ459EP-T1_GE3)
PowerPAK® 8 x 8L	Datasheet part number (example: SQJQ402E)	-T1_GE3	Datasheet part number + "-T1_GE3" (example: SQJQ402E-T1_GE3)
SC-70	Datasheet part number (example: SQ1431EH)	-T1_GE3	Datasheet part number + "-T1_GE3" (example: SQ1431EH-T1_GE3)
SOT-23	Datasheet part number (example: SQ2389ES)	-T1_GE3	Datasheet part number + "-T1_GE3" (example: SQ2389ES-T1_GE3)
TSOP-6	Datasheet part number (example: SQ3427EV)	-T1_GE3	Datasheet part number + "-T1_GE3" (example: SQ3427EV-T1_GE3)
SO-8	Datasheet part number (example: SQ4005EY)	-T1_GE3	Datasheet part number + "-T1_GE3" (example: SQ4005EY-T1_GE3)
TO-252 / DPAK, Reverse lead DPAK	Datasheet part number (example: SQD10N30-330H)	_GE3	Datasheet part number + "_GE3" (example: SQD10N30-330H_GE3)
TO-263 / D^2PAK, D^2PAK-7L	Datasheet part number (example: SQM40022EM)	_GE3	Datasheet part number + "_GE3" (example: SQM40022EM_GE3)
TO-220, TO-262	Datasheet part number (example: SQV120N10-3M8)	_GE3	Datasheet part number + "_GE3" (example: SQV120N10-3M8_GE3)

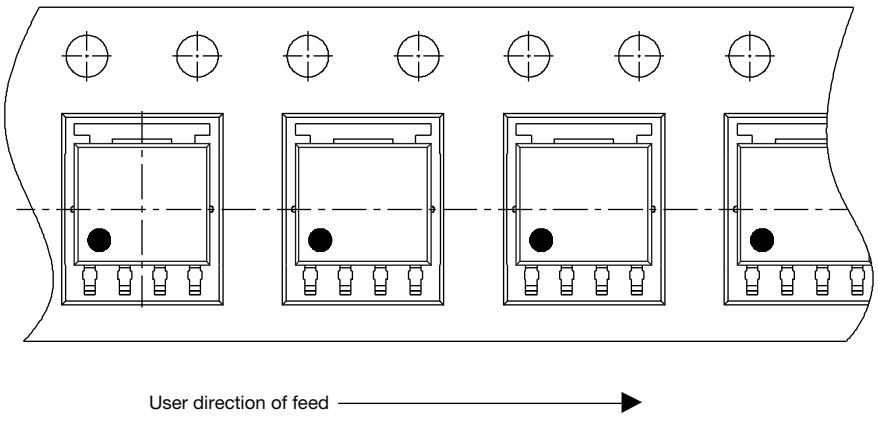
Note

- For bare die parts and for non-standard orientations in tape (such as T2, T4) please contact your local sales or marketing for ordering code information

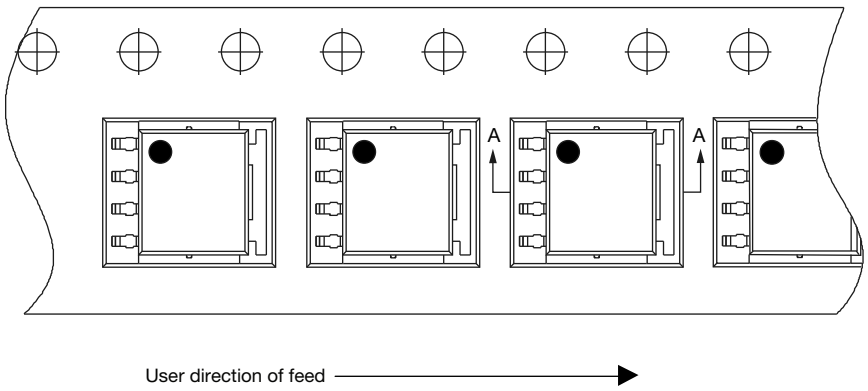
Device Orientation for PowerPAK® SO-8L

DEVICE ORIENTATION	
PACKAGE	**METHOD**
PowerPAK SO-8L/BWL auto/BWL 2mil auto	T1/T2

Method T1



Method T2



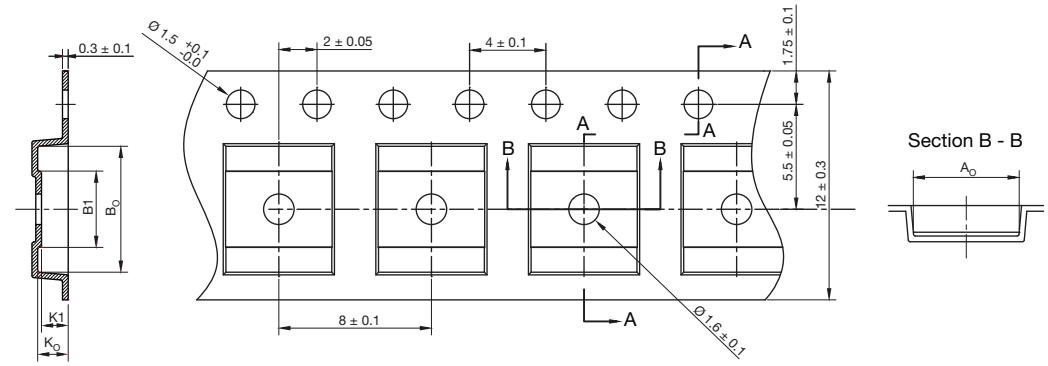
Revision control of this drawing is maintained through Document Control, Pack Specification-PACK-0007-24

Note

- For carrier tape drawing 93-5259-X, use version -1

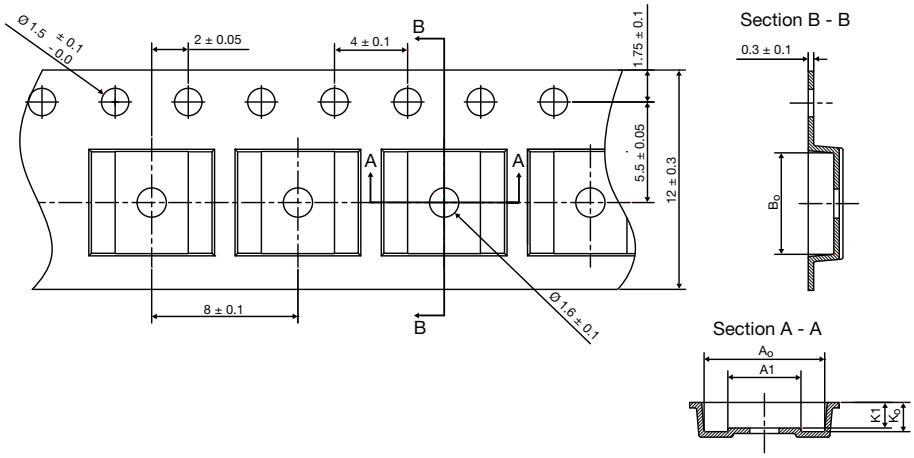
PowerPAK® SO-8L Carrier Tape

T1



Section A - A

T2



Version	A_O	A1	B_O	B1	K_O	K1	Quantity per reel
T1 / - 1	5.55 ± 0.1	-	6.60 ± 0.1	4 ± 0.15	1.6 ± 0.1	1.4 ± 0.1	3000
T2 / - 2 [a]	6.60 ± 0.1	4 ± 0.15	5.55 ± 0.1	-	1.6 ± 0.1	1.4 ± 0.1	

Notes

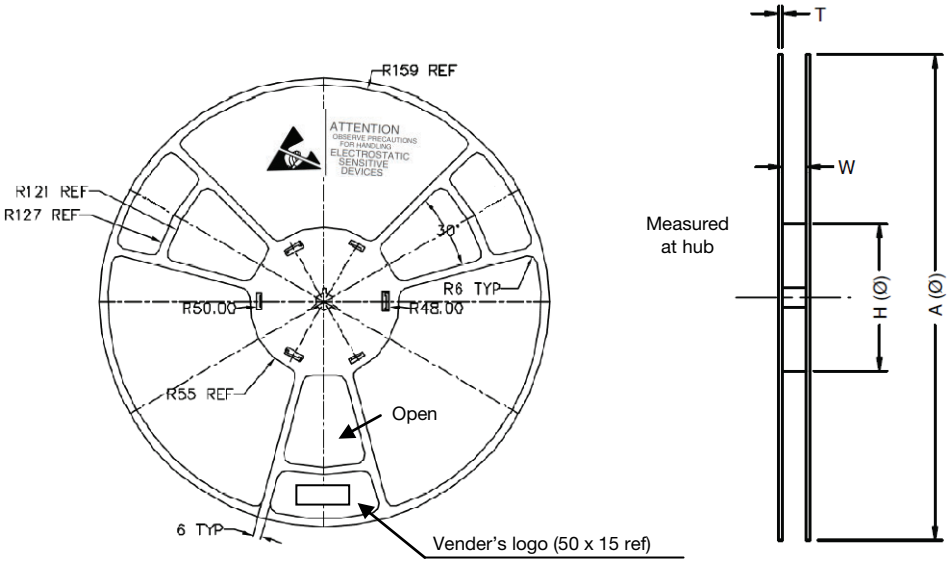
a. Not standard offering. Please contact local sales office for availability.

(1) 10 sprocket hole pitch cumulative tolerance ± 0.2 mm.
(2) Camber not to exceed 1 mm in 100 mm, also not to exceed 1.5 cm in 1 m actually.
(3) Material: black conductive or black static dissipative.
(4) A_o and B_o measured on a plane 0.3 mm above the bottom of the pocket.
(5) K_o measured from a plane on the inside bottom of the pocket to the top surface of carrier.
(6) It should be measured from:
  a. sprocket hole to pocket center.
  b. sprocket hole to pocket hole.
(7) All size in mm unless specified.
(8) Tolerance will be ± 0.1 mm unless specified.
(9) Vishay part number must be labeled at all reels of carrier tape.
(10) Surface resistivity: 10^4 to 10^{11} Ω.
(11) Version suffix as above table shown.

ECN: C15-1433-Rev. F, 02-Nov-15
DWG: 93-5259-X

Reel

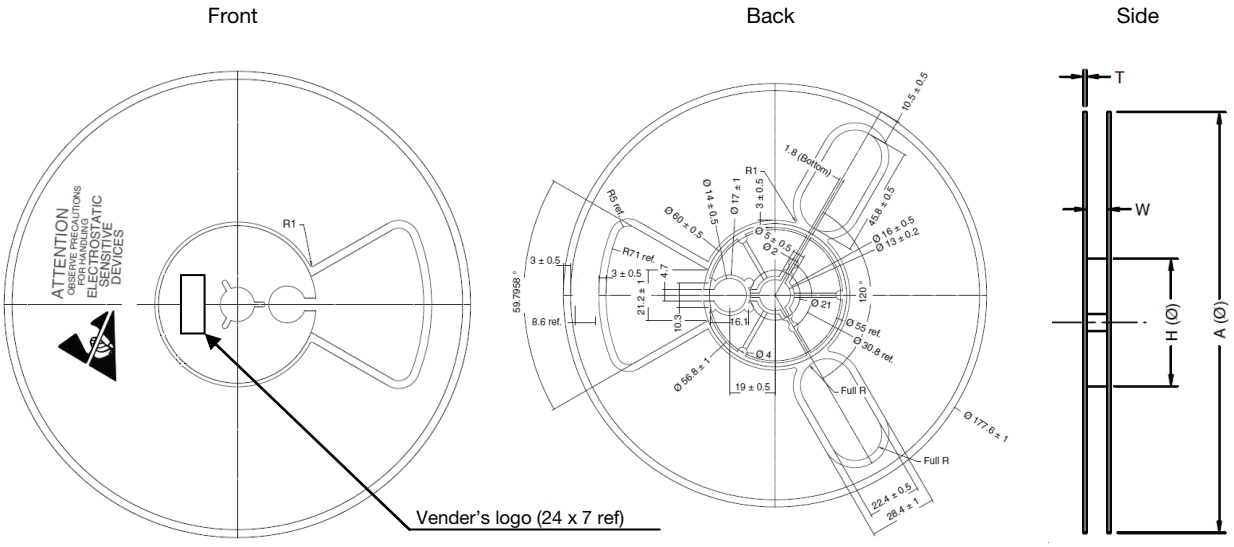
330 mm Reel (Lock Reel)



Notes
1. Material: antistatic or conductor plastic
2. All dimensions in mm
3. ESD-surface resistivity -10^4 Ω to 10^{11} Ω
4. Color: black

VER	APPLICATION		A	W	TAPE WIDTH	H	T
- 1	SOIC-14/16 TO-251 (Short Lead) TO-252/TO-252 (Reverse Lead) PLCC-20 TSSOP-8/14/16/20/28 SSOP-24 SOIC-16 (W) PLCC20	PowerPAK MLF 9 x 9 PowerPAK MLP 6 x 6 MLF 8 x 8 PowerPAK 8 x 8L PowerPAK 8 x 8 MLP57/MLP66/MLP77/MLP46 PowerPAK 5 x 9	330 ± 2	16.4 +2 -0	16	100 ± 1	2.5 ± 0.5
- 2	SOIC-8 (N), SOIC-8 (N) epad MSOP-8/10 PowerPAK® SO-8 PowerPAK 1212 PowerPAK 1212-8W MICRO FOOT® MLP33-5, MLP33-8, MLP33-10 QFN (4 x 4)/(3 x 3)/DFN-10 (3 x 3) MLP44/MLP4535/MLP55/MLP65/MLP56	PolarPAK® PowerPAIR® 6 x 5 PowerPAIR 6 x 3 J PowerPAIR SO-8L PolarPAK1215 PowerPAIR 6 x 3.7 PowerPAK SO-8L PowerPAK SO-8DCWL Power PAIR 3 x 3 S Power PAIR 3 x 3 F Power PAIR 3 x 3 FDC	330 ± 2	12.4 +2 -0	12	100 ± 1	2.5 ± 0.5
- 4	SOT-23/143 SC70 MICRO FOOT	TSOP-6, 1206-8 ChipFET PowerPAK SC70 PowerPAK SC75	330 ± 2	8.4 +1.5 -0	8.4	100 ± 1	2.5 ± 0.5
- 5	SOIC-20W/24W D2PAK SSOP-28 QSOP-36	PowerPAK MLF 10 x 10 MLPA6C PLCC28	330 ± 2	24.4 +2 -0	24	100 ± 1	2.5 ± 0.5
- 8	KGD		330 ± 2	16.4 +2 -0	16	130 ± 1	2.5 ± 0.5

178 mm Reel (Complete Reel)



Notes
1. Material: antistatic or conductor plastic
2. All dimensions in mm
3. ESD-surface resistivity -10^4 Ω to 10^{11} Ω
4. Color: black

VER	APPLICATION		A	W	TAPE WIDTH	H	T
- 3	SOT-23/143 TSOP-5/6/SC70JW-8L 1206-8 ChipFET® SC70/SC75A/SC89 MICRO FOOT SC-89 (SOT-666) SOT23-5, 6 KGD WCSP PowerPAK 0806 PowerPAK SC70	PowerPAK SC75 MiniQFN PowerPAK MLP22-5 PowerPAK ChipFET PowerPAK SC75-6L (PIC) PowerPAK TSC75-6L (PIC) TDFN4 1.2 x 1.6, TDFN8 2 x 2 Thin PowerPAK SC-70 Thin PowerPAK SC-75 µDFN-6L 1 x 1 µDFN-4L 1 x 1	178 ± 2	8.4 +1.5 -0	8.4	62 ± 2	1.5 ± 0.5
- 7	MICRO FOOT PowerPAK 2 x 5	KGD	178 ± 2	12.4 +2 -0	12	55 ± 2	1.6 ± 0.25
ECN: C21-0040-Rev. CA, 01-Feb-2021 DWG: 93-5211-X							

N-CHANNEL ACCELERATED OPERATING LIFE TEST RESULT	
Sample Size	15 334
Equivalent Device Hours	6 915 815 331
Failure Rate in FIT	0.132

Failure Rate in FIT is calculated according to JEDEC Standard JESD85, *Methods for Calculating Failure Rates in Units of FITs*, based on accelerated high temperature operating life test results by using an apparent activation energy of 0.7 eV. The junction temperature of the device at use is assumed to be 55 °C. A constant failure rate distribution is assumed. The upper confidence bound of the failure rate is 60 %.

300MC TrenchFET® PROCESS TECHNOLOGY	
Sample size	26 404
Equivalent device hours	3 449 960 047
Failure rate in FIT	0.264

Failure rate in FIT is calculated according to JEDEC® standard JESD85, Methods for calculating failure rates in units of FITs, based on accelerated high temperature operating life test results by using an apparent activation energy of 0.7 eV. The junction temperature of the device at use is assumed to be 55 °C. A constant failure rate distribution is assumed. The upper confidence bound of the failure rate is 60 %.

ENVIRONMENTAL AND PACKAGE TESTING DATA FOR POWERPAK® SO-8L					
STRESS	**SAMPLE SIZE**	**DEVICE HR./CYC**	**CONDITION**	**TOTAL FAILS**	**FAIL PERCENTAGE**
Bond int.	520	270 000	200 °C, N2	0	0.00
HAST	1394	155 800	130 °C, 85 % RH	0	0.00
Pressure pot	1886	236 160	121 °C, 15 PSIG	0	0.00
Temp. cycle	1968	2 501 000	-55 °C to +150 °C	0	0.00
Solderability	255	2 040	8 hours	0	0.00
Power cycle	1066	18 368 000	ΔT_J = 100 °C	0	0.00
Solder dunk	1099	3 297	260 °C, 10 s	0	0.00

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