



### DMP21D5UFD

#### P-CHANNEL ENHANCEMENT MODE MOSFET

## **Product Summary**

BV <sub>DSS</sub>	Rds(on) max	Package	Ι <sub>D</sub> T <sub>A</sub> = +25°C
	1.0Ω @ V <sub>GS</sub> = -4.5V		-600mA
001/	1.5Ω @ V <sub>GS</sub> = -2.5V		-500mA
-20V	2.0Ω @ V <sub>GS</sub> = -1.8V	X1-DFN1212-3	-400mA
	3.0Ω @ V <sub>GS</sub> = -1.5V		-250mA

# Description

This new generation MOSFET is designed to minimize the on-state resistance (R<sub>DS(ON)</sub>) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

# Applications

- **DC-DC** Converters
- **Power Management Functions**

### **Features**

- Low On-Resistance
- Very Low Gate Threshold Voltage V<sub>GS(TH)</sub>, 1.0V Max
- Low Input Capacitance
- Fast Switching Speed
- ESD Protected Gate
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- Qualified to AEC-Q101 Standards for High Reliability

# **Mechanical Data**

Case: X1-DFN1212-3 •

Gat

G pin

- Case Material: Molded Plastic. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: NiPdAu over Copper Leadframe. Solderable per MIL-STD-202, Method 208 @4)
- Terminal Connections: See Diagram
- Weight: 0.005 grams (Approximate)

Gate

Diode

Protection







Equivalent Circuit

Source

**Pin-Out Top View** 

# Ordering Information (Note 4)

Part Number	Case	Packaging
DMP21D5UFD-7	X1-DFN1212-3	3000/Tape & Reel

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant. Notes:

2. See http://www.diodes.com/quality/lead\_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.

3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and 41000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

# Marking Information

	KP2	
	YM	
)		

KP2 = Product Type Marking Code YM = Date Code Marking Y = Year (ex: E = 2017) M = Month (ex: 9 = September)

Date	Code	Key

Balo bodo hoy												
Year	201	1	2012		2013	20	14	2015		2016	2	2017
Code	Y		Z		А	E	3	С		D		E
Month	Jan	Feb	Mar	Apr	Мау	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	0	N	D



# Maximum Ratings (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Drain-Source Voltage	V <sub>DSS</sub>	-20	V
Gate-Source Voltage	V <sub>GSS</sub>	±8	V
Continuous Drain Current (Note 6) $V_{GS}$ = -4.5V	ID	-600 -500	mA
Continuous Drain Current (Note 6) V <sub>GS</sub> = -1.8V	ID	-400 -300	mA
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)	I <sub>DM</sub>	-2	А
Maximum Body Diode Continuous Current	Is	-800	mA

## **Thermal Characteristics**

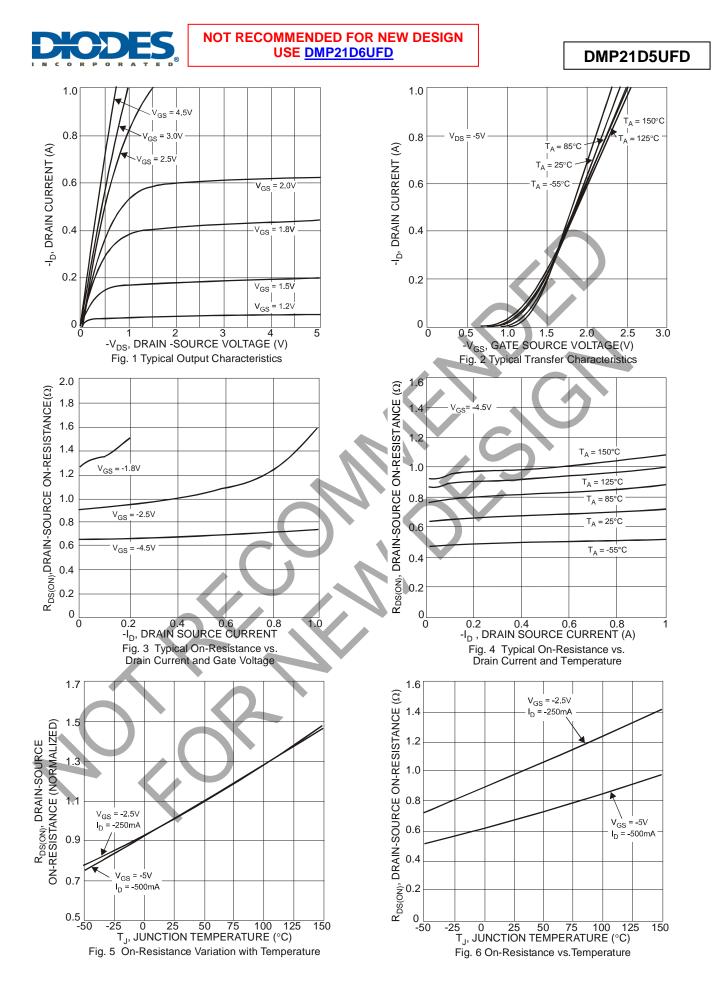
Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)		PD	0.4	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{ hetaJA}$	280	°C/W
Total Power Dissipation (Note 6)		PD	0.8	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	R <sub>θ</sub> JA	140	°C/W
Operating and Storage Temperature Range		T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C

### Electrical Characteristics (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 7)							
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	-20	-		V	$V_{GS} = 0V, I_D = -1mA$	
Zero Gate Voltage Drain Current $T_J = +25^{\circ}C$	I <sub>DSS</sub>			-80 -100	nA	$V_{DS} = -4.5V, V_{GS} = 0V$ $V_{DS} = -20V, V_{GS} = 0V$	
Gate-Source Leakage	I <sub>GSS</sub>			±10.0	μA	$V_{GS} = \pm 8V, V_{DS} = 0V$	
ON CHARACTERISTICS (Note 7)							
Gate Threshold Voltage	V <sub>GS(TH)</sub>	-0.5	-	-1.0	V	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	
		+	0.7	1.0		V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -100mA	
			0.9	1.5		V <sub>GS</sub> = -2.5V, I <sub>D</sub> = -80mA	
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	-	1.2	2.0	Ω	V <sub>GS</sub> = -1.8V, I <sub>D</sub> = -40mA	
		_	1.5	3.0		V <sub>GS</sub> = -1.5V, I <sub>D</sub> = -30mA	
		_ 5 _			$V_{GS} = -1.2V, I_{D} = -1mA$		
Forward Transfer Admittance	Y <sub>fs</sub>	—	0.7	_	S	$V_{DS} = -3V, I_{D} = -100mA$	
Diode Forward Voltage	VsD	—	-0.75	-1.2	V	$V_{GS} = 0V, I_{S} = -330mA$	
DYNAMIC CHARACTERISTICS (Note 8)							
Input Capacitance	Ciss	—	46.1	_			
Output Capacitance	Coss	_	7.2	_	pF	$V_{DS} = -10V, V_{GS} = 0V,$ f = 1.0MHz	
Reverse Transfer Capacitance	Crss	_	4.9	_		1 = 1.0MHZ	
Total Gate Charge V <sub>GS</sub> = -4.5V	Qg	_	0.5	_			
Total Gate Charge V <sub>GS</sub> = -8V	Qg	_	0.8	_	nC	101/1 050-04	
Gate-Source Charge	Q <sub>gs</sub>	_	0.1	_	no	$V_{DS} = -10V, I_D = -250mA$	
Gate-Drain Charge	Q <sub>qd</sub>	—	0.1	_			
Turn-On Delay Time	t <sub>D(ON)</sub>	—	8.5	_			
Turn-On Rise Time	t <sub>R</sub>	—	4.3	_		$V_{DD} = -3V, V_{GS} = -2.5V,$	
Turn-Off Delay Time	t <sub>D(OFF)</sub>	—	20.2	—	ns	$R_{\rm L} = 300\Omega, R_{\rm g} = 25\Omega,$	
Turn-Off Fall Time	tF		19.2	—		I <sub>D</sub> = -100mA	

 Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate. Notes:

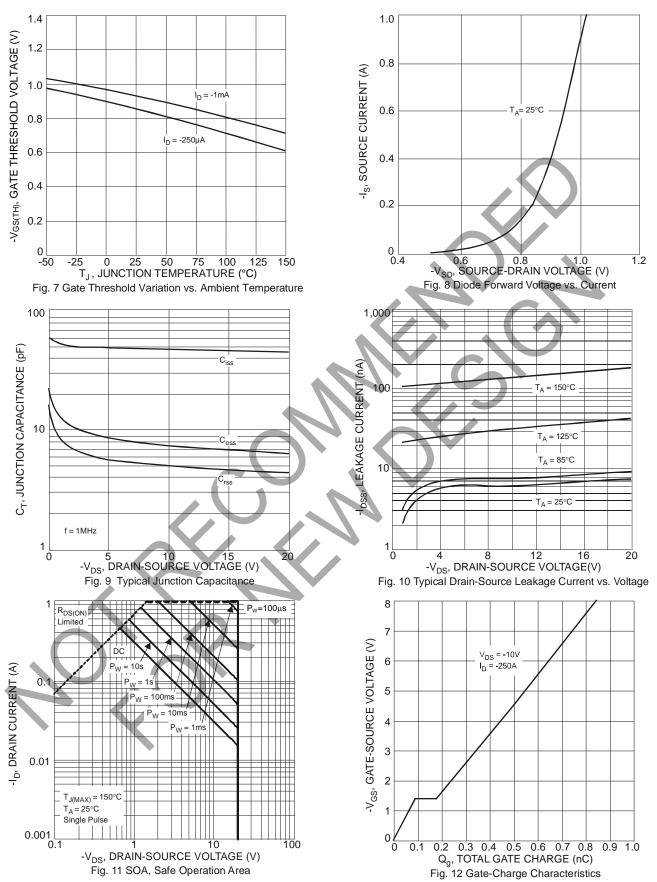
7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing.





## NOT RECOMMENDED FOR NEW DESIGN USE <u>DMP21D6UFD</u>

DMP21D5UFD

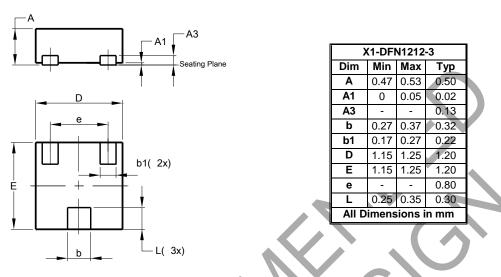




# Package Outline Dimensions

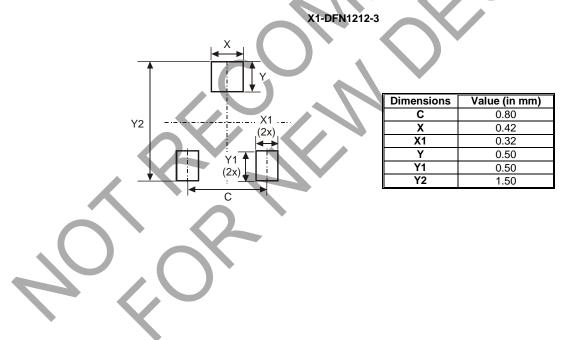
Please see http://www.diodes.com/package-outlines.html for the latest version.

#### X1-DFN1212-3



# Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.





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