8-CHANNELS SWITCH FOR MULTI-CELLS LI+/POLYMER BATTERY PACK

Description

AP9106 is 8-Channel analog switch which is suitable for up to 6-Cells in serial Li+/Polymer battery pack application.

AP9106 has four logic selection inputs (A/B/C/D). When all logic pins are set low, no channel is selected and the chip is turned off with shutdown mode. The A, B, C and D selection pins are compatible with TTL/CMOS logic level, can be connected to MCU I/O port directly to select the right channel respectively. The VOUT is output pin to indicate exactly the voltage of each battery cell.

AUX7, AUX8 pins are auxiliary channels, which can be connected to the NTC resistor to transfer the voltage variation into VOUT pin.

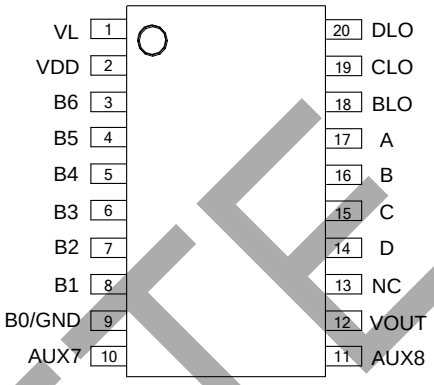
AP9106 is available in standard package of TSSOP-20.

Features

- ±1% Matching Error between any 2 Channels
- Up to 6-Cells in Serial Li+/Polymer Battery Pack Application with Single Chip
- Up to 11-cell in Serial Li+/Polymer Battery Pack Application with Dual Chip
- Ultra Low Current in Shutdown Mode: 1.0μA
- Compatible with TTL/CMOS for Logic Level
- Logic Level Shift Transfer
- Small Package: TSSOP-20

Pin Assignments

(Top View)

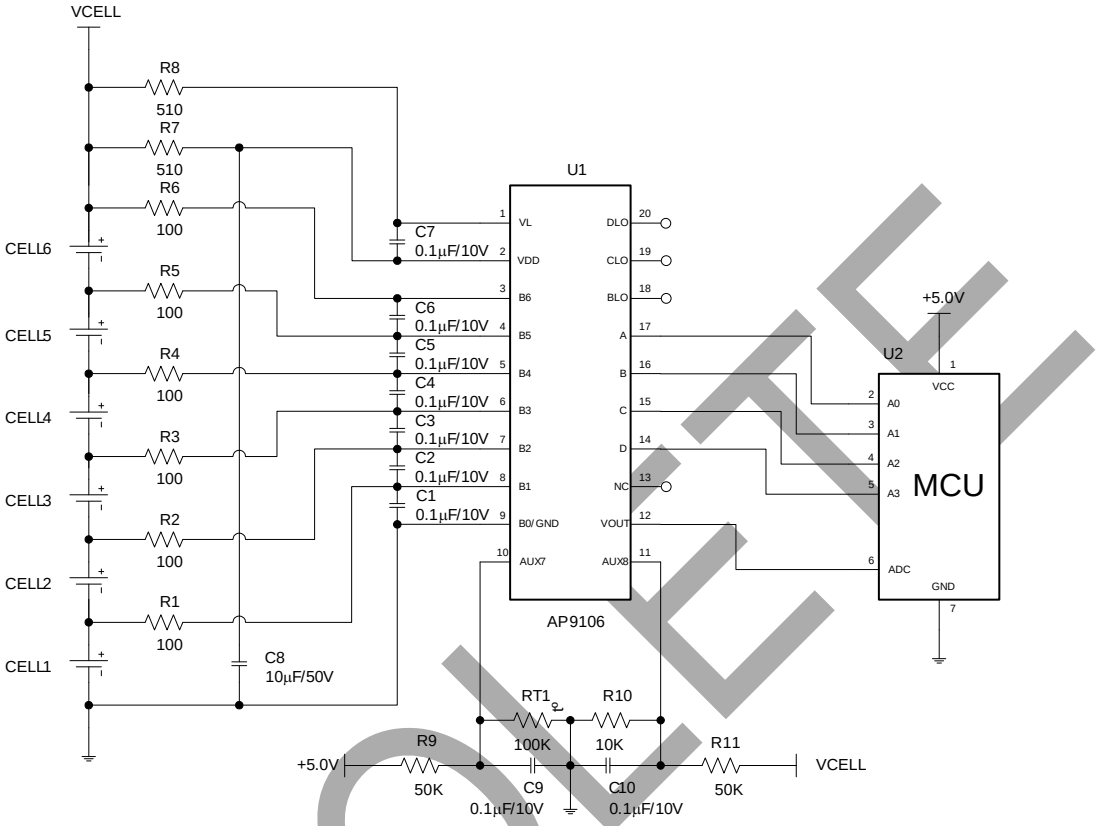


TSSOP-20

Applications

- E-Bike Li+ Battery Pack
- Electric Tool Battery Pack

Typical Applications Circuit

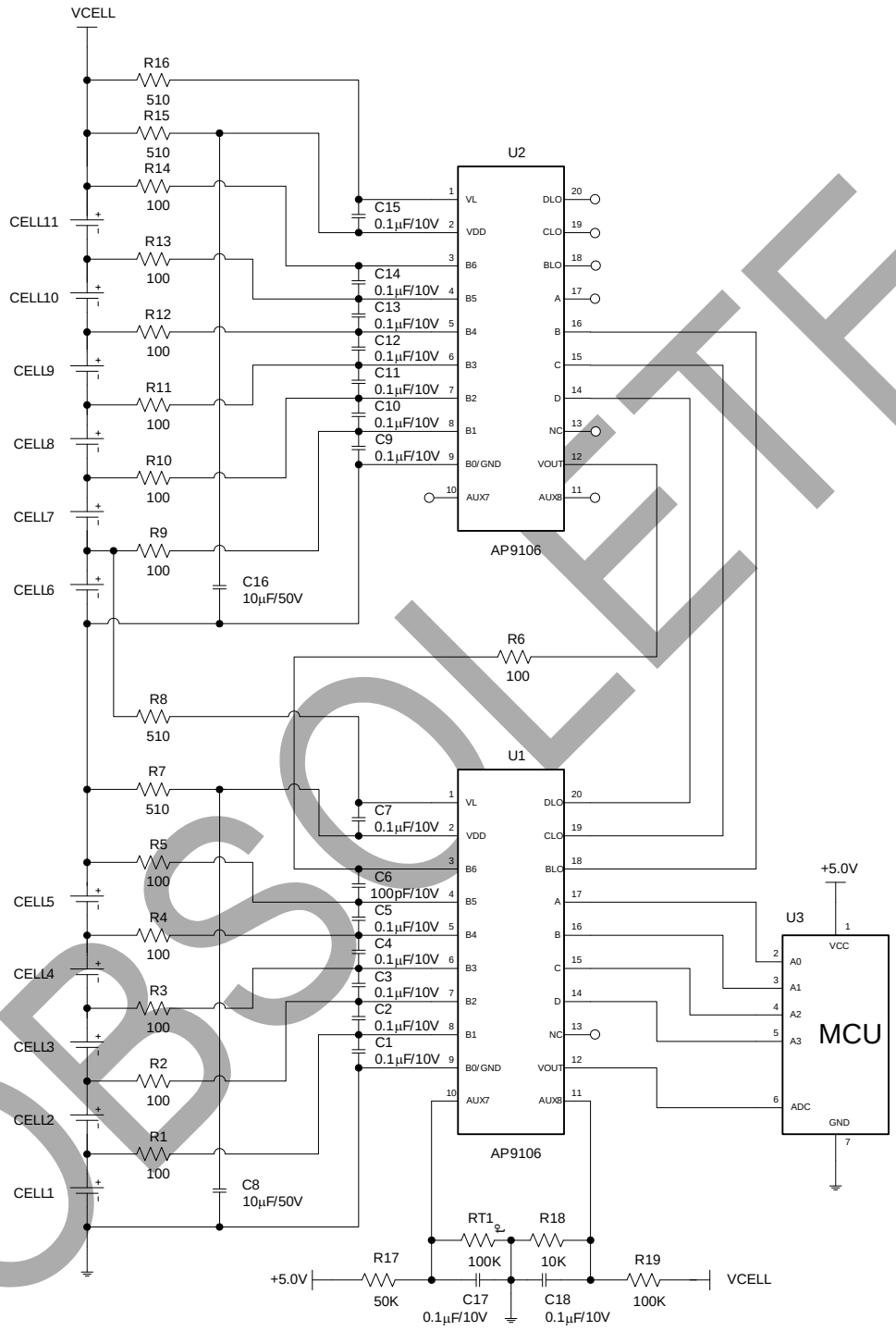


6-cell Battery (Single Chip) Application for AP9106

Truth Table for 6-cell (Single Chip) Battery Application

Logic Input				Active Channel	Output Voltage
A	B	C	D		
0	0	0	0	All channels OFF, chip is in shutdown mode	0V
0	0	0	1	QD1	VCELL1
0	0	1	0	QD2	VCELL2
0	0	1	1	QD3	VCELL3
0	1	0	0	QD4	VCELL4
0	1	0	1	QD5	VCELL5
0	1	1	0	QD6	VCELL6
0	1	1	1	QD7	VTEMP
1	0	0	0	QD8	VTCELL

Typical Applications Circuit (Cont.)



11-cell Battery (Dual Chips) Application for AP9106

Truth Table for 11-cell (Dual Chips) Battery Application

Logic Input				Active Channel (Lower Chip)	Active Channel (Upper Chip)	Output Voltage
A	B	C	D			
0	0	0	0	All channels OFF, chip is in shutdown mode	All channels OFF, chip is in shutdown mode	0V
0	0	0	1	QD1	Shutdown mode	VCELL1
0	0	1	0	QD2	Shutdown mode	VCELL2
0	0	1	1	QD3	Shutdown mode	VCELL3
0	1	0	0	QD4	Shutdown mode	VCELL4
0	1	0	1	QD5	Shutdown mode	VCELL5
0	1	1	0	QD6	Shutdown mode	0V
0	1	1	1	QD7	Shutdown mode	VTEMP
1	0	0	0	QD8	Shutdown mode	VTCELL
1	0	0	1	QD6	QD1	VCELL6
1	0	1	0	QD6	QD2	VCELL7
1	0	1	1	QD6	QD3	VCELL8
1	1	0	0	QD6	QD4	VCELL9
1	1	0	1	QD6	QD5	VCELL10
1	1	1	0	QD6	QD6	VCELL11
1	1	1	1	QD6	QD7	—

Pin Descriptions

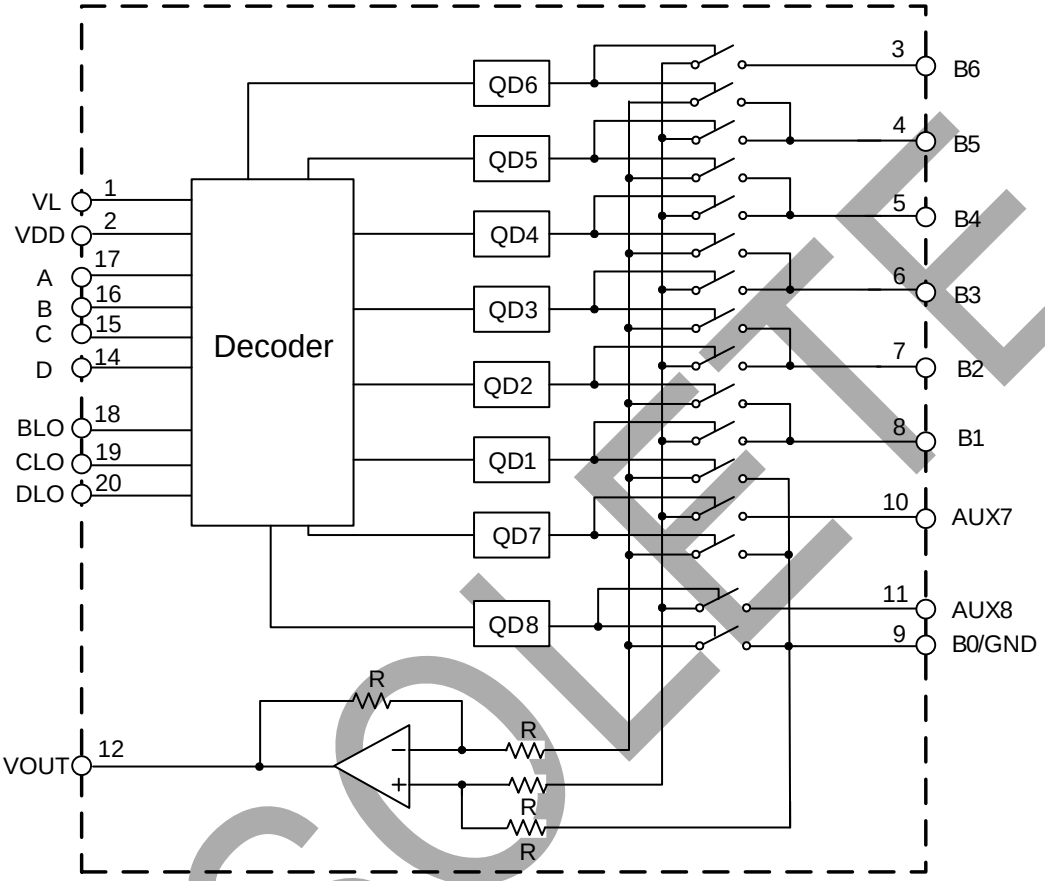
Pin Number	Pin Name	Function
1	VL	Level shift logic power supply
2	VDD	Power supply
3	B6	Positive node of sixth battery cell
4	B5	Positive node of fifth battery cell & negative node of sixth battery cell
5	B4	Positive node of fourth battery cell & negative node of fifth battery cell
6	B3	Positive node of third battery cell & negative node of fourth battery cell
7	B2	Positive node of second battery cell & negative node of third battery cell
8	B1	Positive node of first battery cell & negative node of second battery cell
9	B0(GND)	Ground and negative node of first battery cell
10	AUX7	Auxiliary channel 7
11	AUX8	Auxiliary channel 8
12	VOUT	Switch output pin
13	NC	No connected
14	D	Channel selection logic input D
15	C	Channel selection logic input C
16	B	Channel selection logic input B
17	A	Channel selection logic input A
18	BLO	Channel selection logic output B
19	CLO	Channel selection logic output C
20	DLO	Channel selection logic output D

Notes: 1. VDD pin should always be connected to the positive node of top battery.
2. Voltage of VL pin should be equal to or larger than that of VDD pin.

Truth Table and Relationship between Input Logic, Output Logic and Selected Channel

Logic Input				Logic Output			Active Channel	Output Voltage
A	B	C	D	BLO	CLO	DLO		
0	0	0	0	0	0	0	All channels OFF, chip is in shutdown mode	0V
0	0	0	1	0	0	0	QD1	B1 vs. B0(GND)
0	0	1	0	0	0	0	QD2	B2 vs. B1
0	0	1	1	0	0	0	QD3	B3 vs. B2
0	1	0	0	0	0	0	QD4	B4 vs. B3
0	1	0	1	0	0	0	QD5	B5 vs. B4
0	1	1	0	0	0	0	QD6	B6 vs. B5
0	1	1	1	0	0	0	QD7	AUX7 vs. GND
1	0	0	0	0	0	0	QD8	AUX8 vs. GND
1	0	0	1	0	0	1	QD6	B6 vs. B5
1	0	1	0	0	1	0	QD6	B6 vs. B5
1	0	1	1	0	1	1	QD6	B6 vs. B5
1	1	0	0	1	0	0	QD6	B6 vs. B5
1	1	0	1	1	0	1	QD6	B6 vs. B5
1	1	1	0	1	1	0	QD6	B6 vs. B5
1	1	1	1	1	1	1	QD6	B6 vs. B5

Functional Block Diagram



Absolute Maximum Ratings (Note 3)

Symbol	Parameter	Rating	Unit
V_{DD}	Supply Voltage	-0.3 to 35	V
V_{CELL}	Voltage between B_N and B_{N+1}, AUX7/AUX8 and GND	-0.3 to 5	V
T_J	Operating Junction Temperature Range	+150	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_{LEAD}	Lead Temperature (Soldering, 10sec)	+260	°C
θ_{JA}	Thermal Resistance	80	°C/W
—	ESD (Machine Model)	200	V
—	ESD (Human Body Model)	2000	V

Note 3: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability.

Recommended Operating Conditions

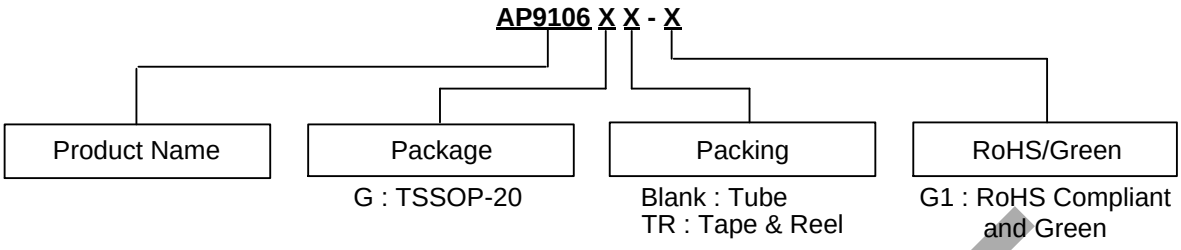
Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply Voltage	6.0	27	V
V_{CELL}	Battery Cell Voltage	2.0	4.5	V
V_{IN}	Input Voltage (B6 vs. B5, B5 vs. B4, B4 vs. B3, B3 vs. B2, B2 vs. B1, B1 vs. GND, AUX7/8 vs. GND)	2.0	4.5	V
T_A	Operating Ambient Temperature	-40	+85	°C
V_{IL}/V_{IH}	Input Logic Level	0	5.0	V

Electrical Characteristics

(V_{DD} = 21.6V, V_L = V_{DD}+4.4V = 26V, T_A = +25°C, **Bold** typeface applies over full temperature -40°C ≤ T_A ≤ +85°C ranges, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{DD}	Supply Voltage	—	6.0	—	27	V
I_Q	Quiescent Current	—	—	0.2	0.5	mA
I_{SHUT}	Shutdown Current	Set A, B, and C low	—	1.0	2.0	μA
OPAMP Output Voltage						
V_{OS}	Offset Voltage	Input DC voltage: 2.9V to 4.2V	-100	—	+100	mV
V_{OL}	Output Voltage Switching	—	2.0	—	—	V
V_{OH}		—	—	—	4.5	V
Switch						
I_{BIAS}	Bias Current	For B2, B3, B4, B5 and B6 Pin	—	10	15	μA
		For B1, AUX7, AUX8 Pin	—	—	1	
E_{MATCH}	Channel Matching Error between any 2 Channels	Set all channel DC: 2.9V to 4.2V, T_A = -40 to +85°C, (V_{MAX}-V_{MIN})/average(CH1 to CH7)	—	**±1**	—	%
—	Channel Isolation	f = 100Hz	—	-80	—	dB
V_{NO}	Output Noise	BW = 100Hz, CH1 to CH7, DC input: 2.9V to 4.2V	—	50	—	μV_{RMS}
t_{SET}	Channel Switching & Set-up Time	—	—	1.0	—	ms
Logic Input (Voltage Mode)						
V_{IH}	Logic Input High Level	A, B, C, D	1.0	—	5.0	V
V_{IL}	Logic Input Low Level	A, B, C, D	0	—	0.6	V
I_L	Input Leakage Current	Set A, B, C, D low	—	—	1.0	μA
$R_{PULL-DOWN}$	Pull Down Resistor	A, B, C, D	—	1.0	—	MΩ
Logic Output (Voltage Mode)						
V_{OL}	Logic Input Low Level	BLO, CLO, DLO	—	V_{DD}	—	V
V_{OH}	Logic Input High Level	BLO, CLO, DLO	—	V_L	—	V

Ordering Information

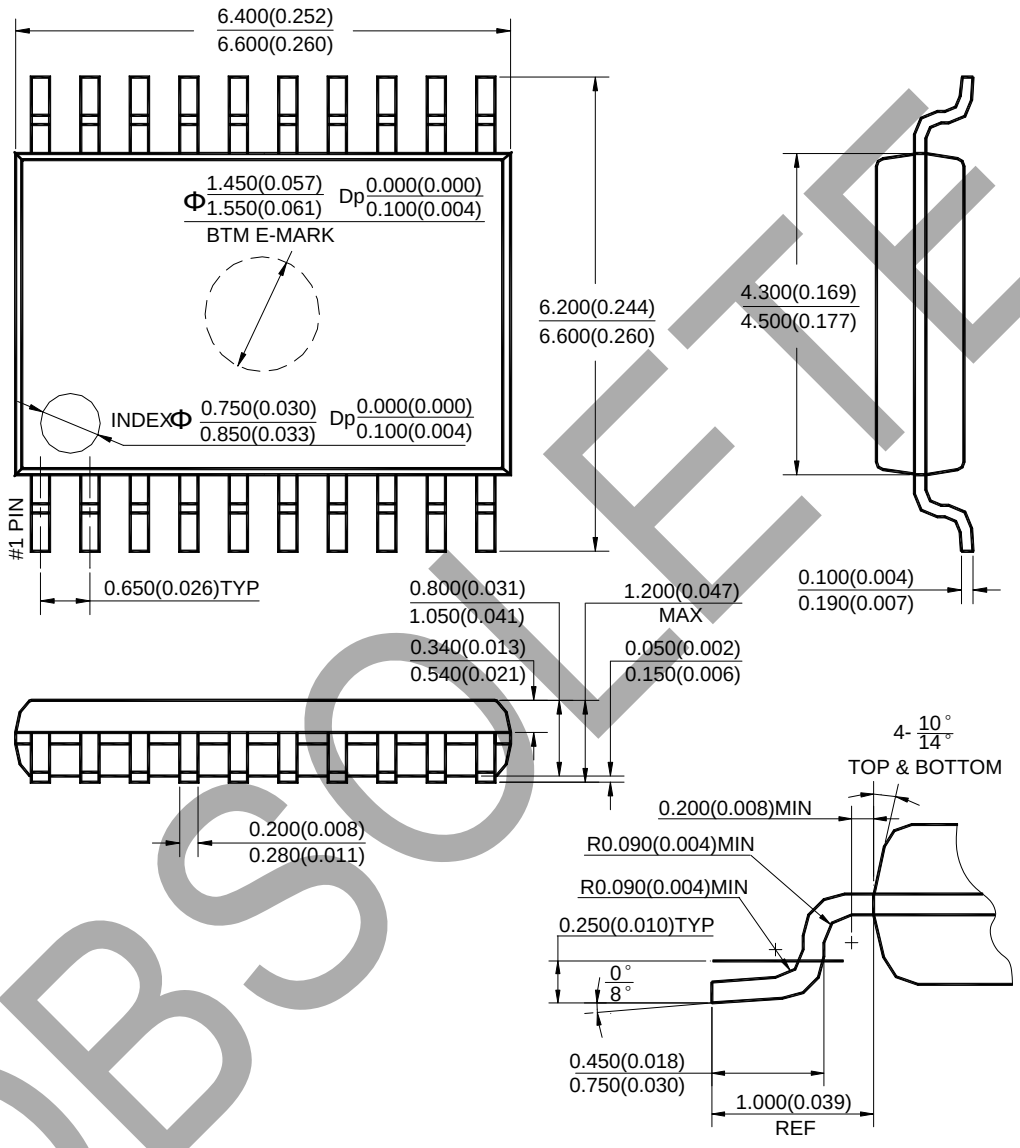


Package	Temperature Range	Part Number	Marking ID	Packing
TSSOP-20	-40 to +85°C	AP9106G-G1	AP9106GG	Tube
		AP9106GTR-G1	AP9106GG	Tape & Reel

OBSOLETE – PART DISCONTINUED

Package Outline Dimensions (All dimensions in mm(inch).)

(1) Package Type: TSSOP-20



Note: Eject hole, oriented hole and mold mark is optional.

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