

The S-5471 Series, developed by using CMOS technology, is a voltage monitoring IC with an ultra-low current consumption.

Since the feed-through current in the IC is extremely low, the error can be reduced when the voltage of a power supply with high impedance is detected. In addition, since the detection voltage is extremely low, a tiny amount of power generated by energy harvesting can also be detected.

Due to its ultra-low current consumption and low-voltage operation, the S-5471 Series is suitable for battery-operated small mobile devices.

■ Features

- Ultra-low current consumption: $I_{DD} \leq 10 \text{ nA typ.}$
- Detection voltage: $V_{DET} = 0.75 \text{ V typ.}$
- Wide operation voltage range: $V_{DD} = 0.7 \text{ V to } 5.5 \text{ V}$
- Operation temperature range: $T_a = -40^\circ\text{C to } +85^\circ\text{C}$
- Lead-free (Sn 100%), halogen-free

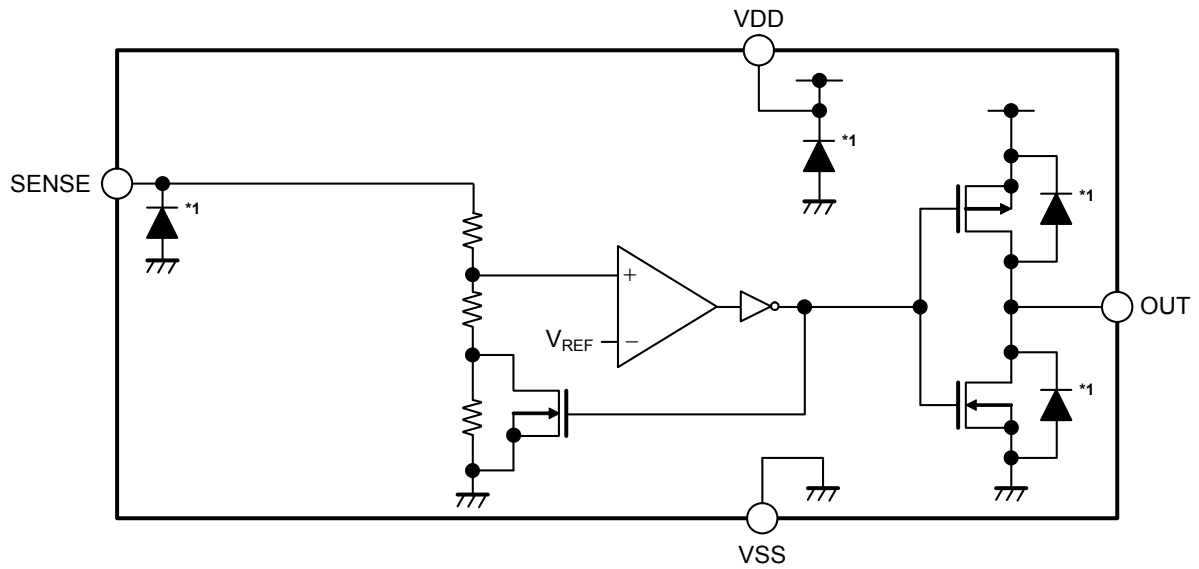
■ Applications

- Miniaturization and power consumption reduction for various sensors of portable and wireless devices
- Energy harvesting

■ Package

- SOT-23-5

■ Block Diagram



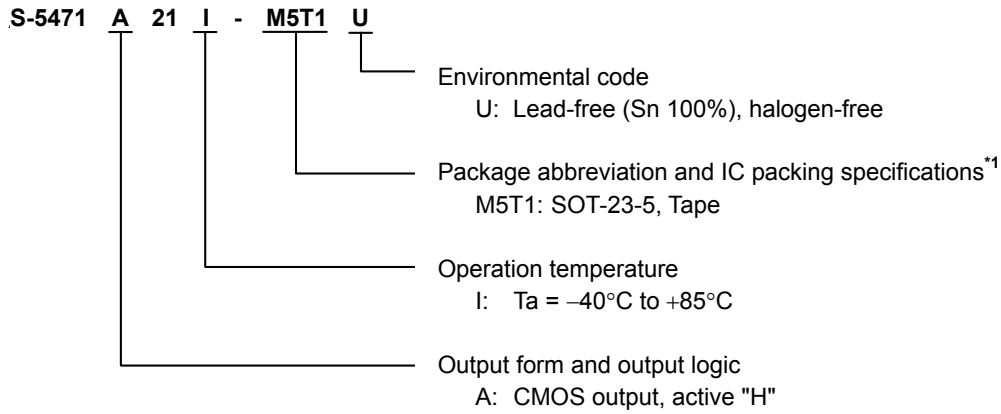
*1. Parasitic diode

Figure 1

■ **Product Name Structure**

Refer to "1. Product name" regarding the contents of the product name, "2. Package" regarding the package drawings.

1. **Product name**



*1. Refer to the tape drawing.

2. **Package**

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel
SOT-23-5	MP005-A-P-SD	MP005-A-C-SD	MP005-A-R-SD

■ Pin Configuration

1. SOT-23-5

Top view

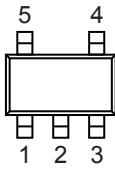


Figure 2

Table 2

Pin No.	Symbol	Description
1	VDD	Power supply pin
2	VSS	GND pin
3	TEST ^{*1}	Test pin
4	SENSE	Detection voltage input pin
5	OUT	Output pin

*1. Connect to GND.

■ Absolute Maximum Ratings

Table 3

(Ta = +25°C unless otherwise specified)

Item	Symbol	Absolute Maximum Rating	Unit
Power supply voltage	V _{DD}	V _{SS} – 0.3 to V _{SS} + 7.0	V
Input voltage	V _{SENSE}	V _{SS} – 0.3 to V _{SS} + 7.0	V
Output voltage	V _{OUT}	V _{SS} – 0.3 to V _{DD} + 0.3	V
Output pin current	I _{SOURCE}	20	mA
	I _{SINK}	20	mA
Operation ambient temperature	T _{opr}	–40 to +85	°C
Storage temperature	T _{stg}	–55 to +125	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 4

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	
Junction-to-ambient thermal resistance *1	θ _{JA}	SOT-23-5	Board A	–	192	–	°C/W
			Board B	–	160	–	°C/W
			Board C	–	–	–	°C/W
			Board D	–	–	–	°C/W
			Board E	–	–	–	°C/W

*1. Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "■ Power Dissipation" and "Test Board" for details.

■ Electrical Characteristics

Table 5

(Ta = +25°C, V_{DD} = 3.0 V unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit	
Power supply voltage	V _{DD}	Ta = -40°C to +85°C	0.7	-	5.5	V	-	
Current consumption	I _{DD}	V _{SENSE} = V _{SS}	-	1	150	nA	1	
		V _{SENSE} = 1.0 V	-	3	150	nA	1	
Detection voltage	V _{DET}	-	0.69	0.75	0.81	V	2	
Release voltage	V _{REL}	-	V _{DET} - 0.07	V _{DET} - 0.05	V _{DET} - 0.03	V	2	
Detection voltage temperature coefficient	V _{TC}	Ta = -40°C to +85°C	-	-0.24	-	%/°C	-	
Input current	I _{SENSE}	V _{SENSE} = 1.0 V	-	1.45	100	nA	3	
Source current	I _{SOURCE}	V _{OUT} = V _{DD} - 0.3 V	V _{DD} = 0.7 V	0.01	0.3	-	mA	4
			V _{DD} = 3.0 V	4.0	5.3	-	mA	4
Sink current	I _{SINK}	V _{OUT} = 0.3 V	V _{DD} = 0.7 V	0.01	0.6	-	mA	5
			V _{DD} = 3.0 V	8.0	10.2	-	mA	5
Output response time	t _{OD}	-	-	-	15	ms	-	

■ Test Circuits

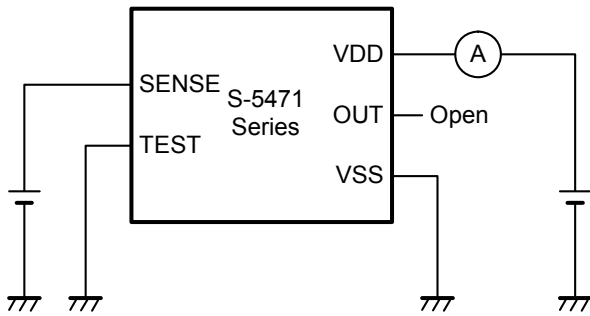


Figure 3 Test Circuit 1

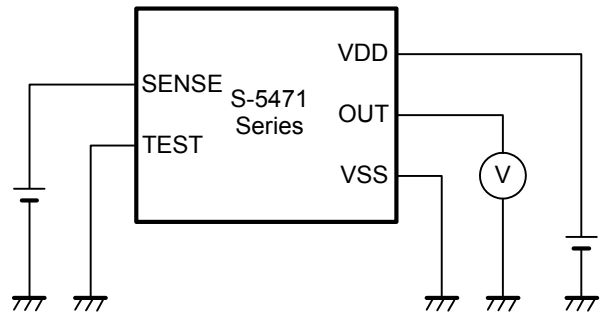


Figure 4 Test Circuit 2

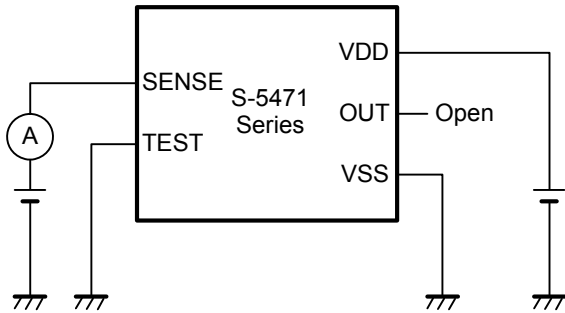


Figure 5 Test Circuit 3

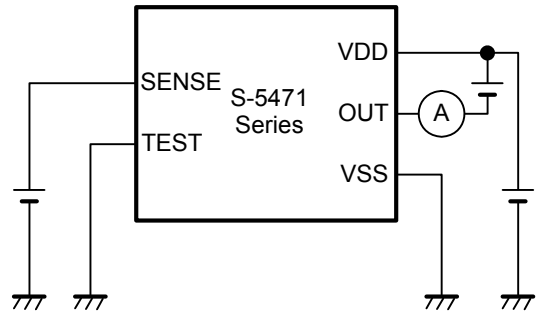


Figure 6 Test Circuit 4

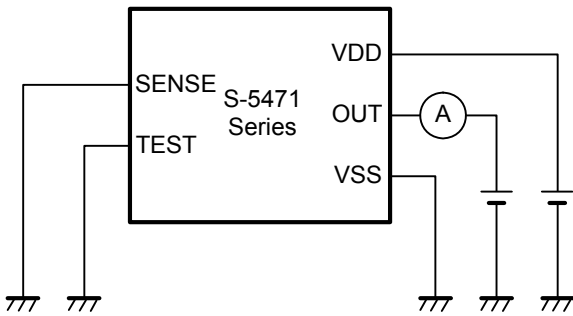


Figure 7 Test Circuit 5

■ Standard Circuit

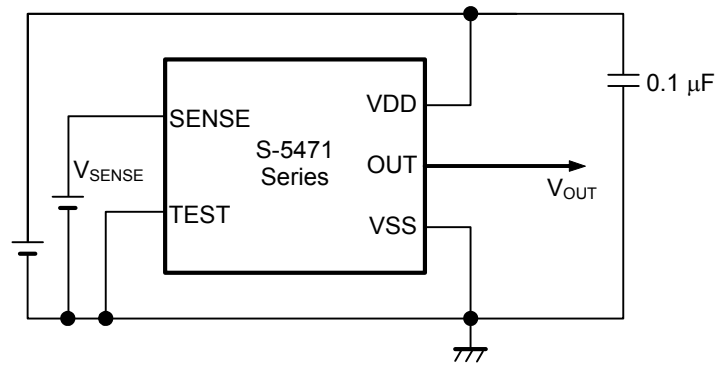


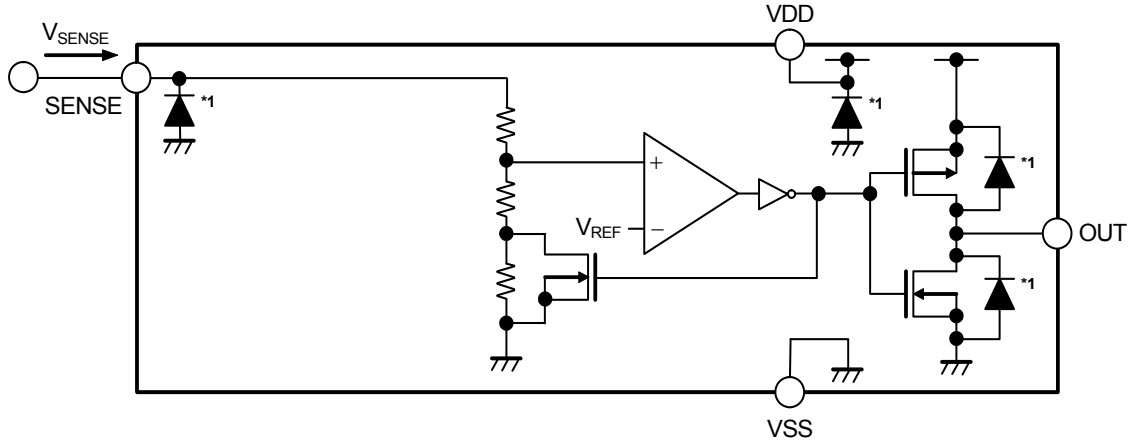
Figure 8

Caution The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.

■ Operation

1. Basic operation

Figure 9 shows an explanatory diagram for the operation at voltage detection.



*1. Parasitic diode

Figure 9 Explanatory Diagram for Operation at Voltage Detection

- (1) If V_{SENSE} is lower than V_{DET} , "L" is output from the OUT pin.
- (2) If V_{SENSE} increases and becomes equal to or higher than V_{DET} , "H" is output from the OUT pin (point A in Figure 10). Even if V_{SENSE} decreases and falls below V_{DET} , as long as V_{SENSE} is higher than V_{REL} , "H" is output from the OUT pin.
- (3) If V_{SENSE} then decreases further and becomes equal to or lower than V_{REL} , "L" is output from the OUT pin (point B in Figure 10).

Remark V_{SENSE} : Voltage input to the SENSE pin
 V_{DET} : Detection voltage (refer to "3. 1 Detection voltage (V_{DET})")
 V_{REL} : Release voltage (refer to "3. 2 Release voltage (V_{REL})")

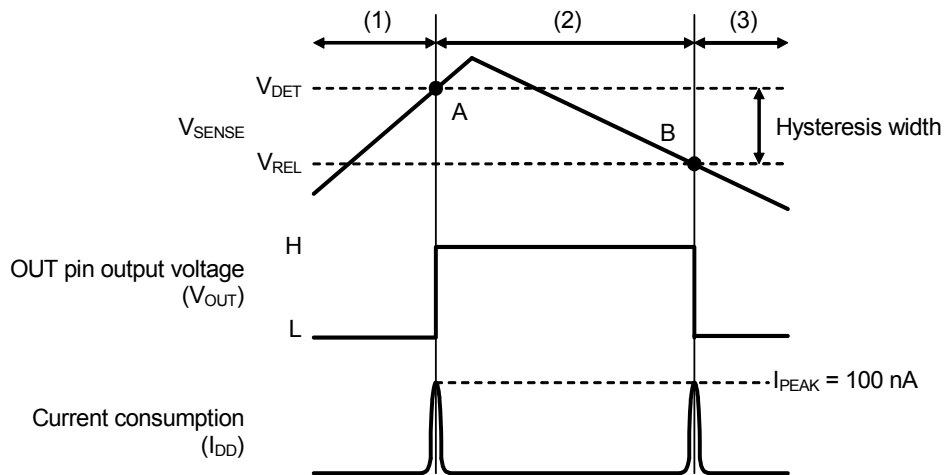
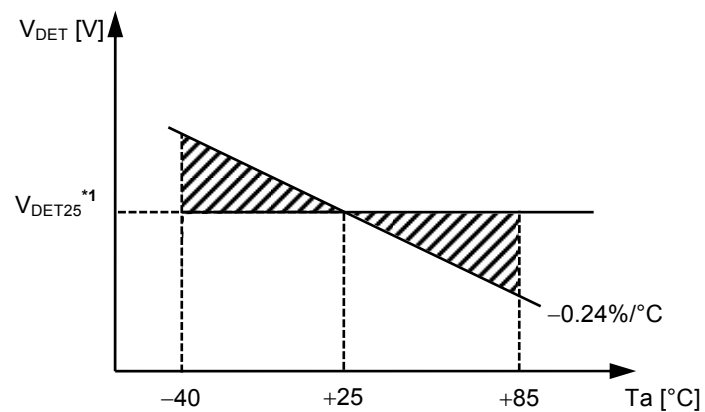


Figure 10 Operation at Voltage Detection

Caution Feed-through current ($I_{PEAK} = 100 \text{ nA}$) flows around the time when the OUT pin voltage switches, as shown in Figure 10. Therefore, if the V_{SENSE} is fixed around this time, the current consumption will increase.

2. Temperature characteristics of detection voltage

The shaded area in **Figure 11** shows the temperature characteristics of the detection voltage in the operation temperature range.



*1. V_{DET25} : Detection voltage value at $T_a = +25^{\circ}\text{C}$

Figure 11 Temperature Characteristics of Detection Voltage

3. Explanation of terms

3.1 Detection voltage (V_{DET})

The detection voltage (V_{DET}) is a voltage at which the output voltage (V_{OUT}) turns to "H".

The detection voltage varies slightly even among products with the same specification. The variation in detection voltage from the minimum detection voltage ($V_{DET\ min.}$) to the maximum detection voltage ($V_{DET\ max.}$) is called the detection voltage range (refer to **Figure 12**).

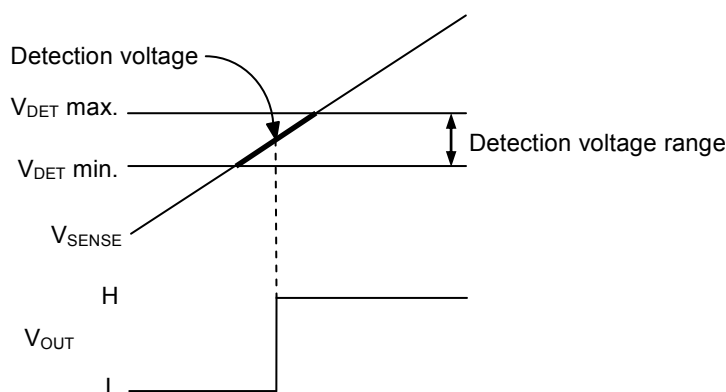


Figure 12 Detection Voltage

3.2 Release voltage (V_{REL})

The release voltage (V_{REL}) is a voltage at which the output voltage (V_{OUT}) turns to "L".

The release voltage varies slightly even among products with the same specification. The variation in release voltage from the minimum release voltage ($V_{REL\ min.}$) to the maximum release voltage ($V_{REL\ max.}$) is called the release voltage range (refer to **Figure 13**).

The range is calculated from the actual detection voltage (V_{DET}) of a product and is in the range of $V_{DET} - 0.07 \leq V_{REL} \leq V_{DET} - 0.03$.

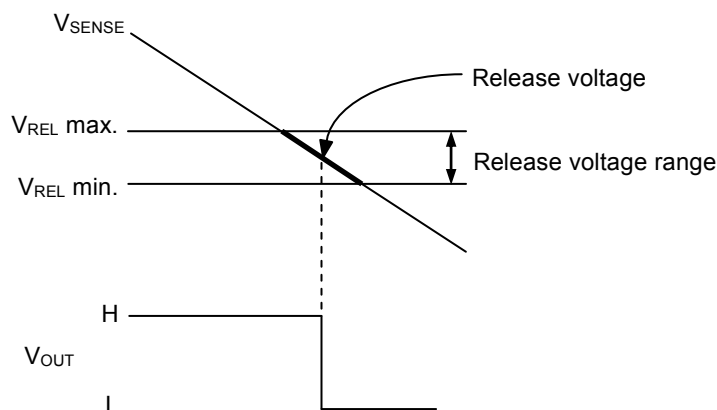


Figure 13 Release Voltage

3.3 Hysteresis width

The hysteresis width is the voltage difference between the detection voltage and the release voltage (voltage at point A – voltage at point B in "**Figure 10** Operation at Voltage Detection").

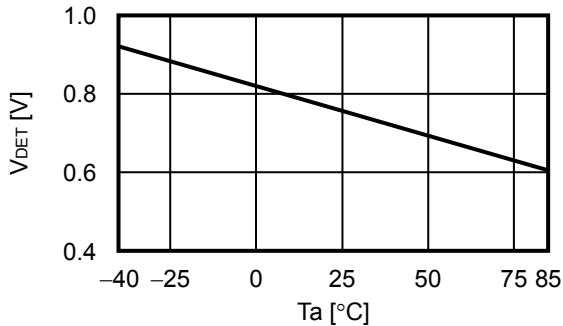
The hysteresis width between the detection voltage and the release voltage prevents malfunction caused by noise in the input voltage.

■ Precautions

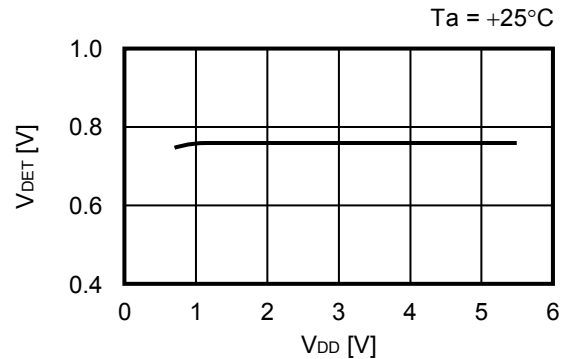
- Use the S-5471 Series with the output pin current of 20 mA or less.
- The S-5471 Series may malfunction if the power supply voltage changes steeply.
- The output in the S-5471 Series is unstable in lower voltage than the minimum operation voltage. At the time of power-on, use the S-5471 Series after output stabilization.
- Connect a capacitor of 0.1 μ F or more between the VDD pin and VSS pin for stabilization.
- Since the SENSE pin is easy to be affected by disturbance noise, perform countermeasures such as mounting external parts to the IC as close as possible.
- If the impedance of the power supply is high, the S-5471 Series may malfunction due to voltage drop caused by feed-through current. Make wire patterns very carefully so that the impedance of the power supply lowers.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
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■ Characteristics (Typical Data)

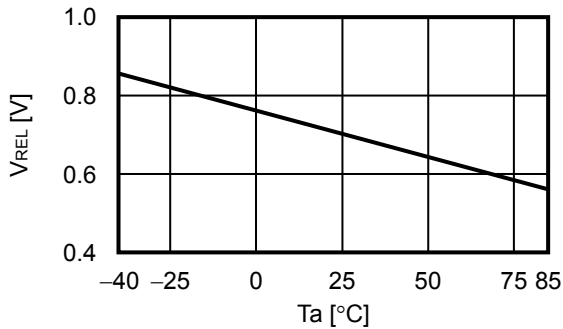
1. Detection voltage vs. Temperature



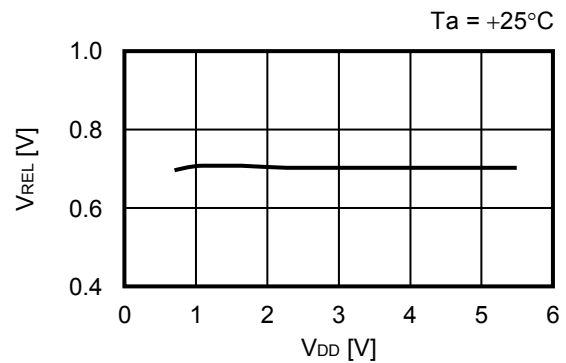
2. Detection voltage vs. Power supply voltage



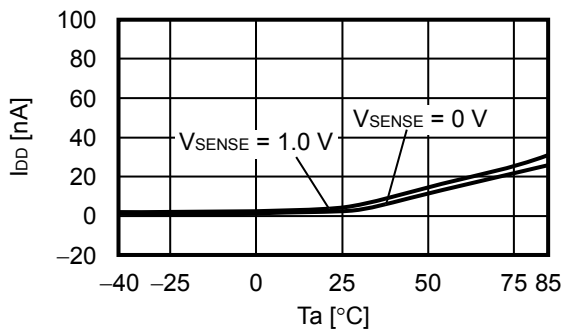
3. Release voltage vs. Temperature



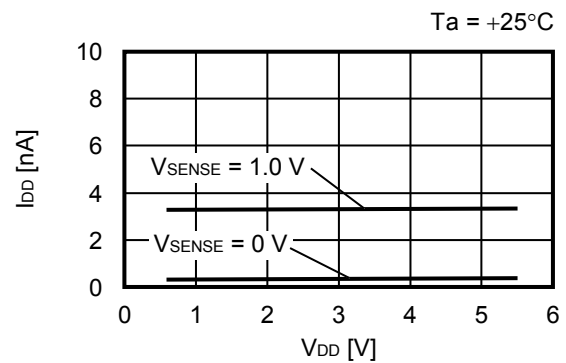
4. Release voltage vs. Power supply voltage



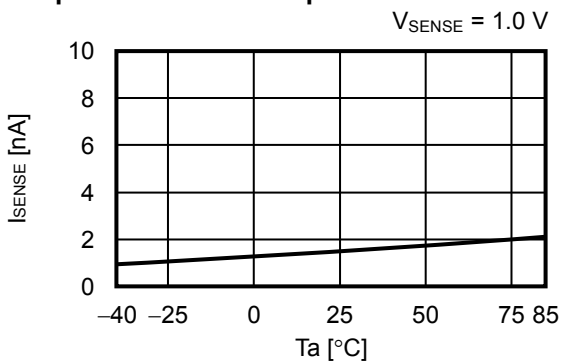
5. Current consumption vs. Temperature



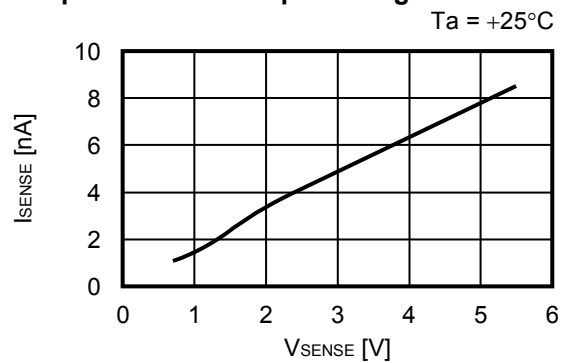
6. Current consumption vs. Power supply voltage



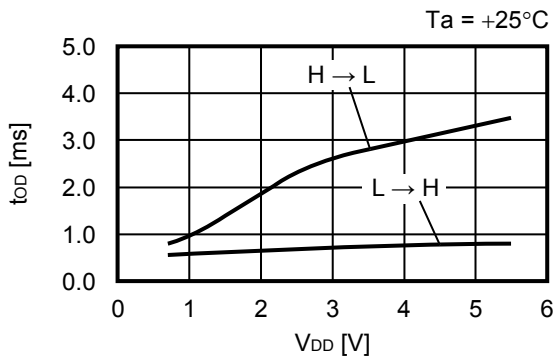
7. Input current vs. Temperature



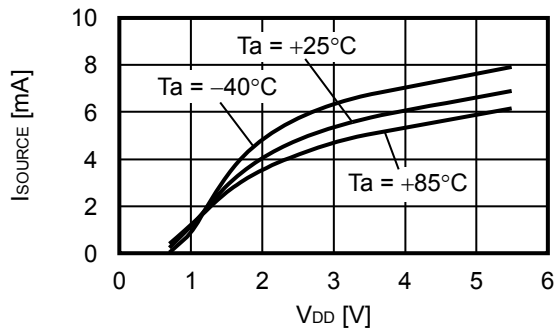
8. Input current vs. Input voltage



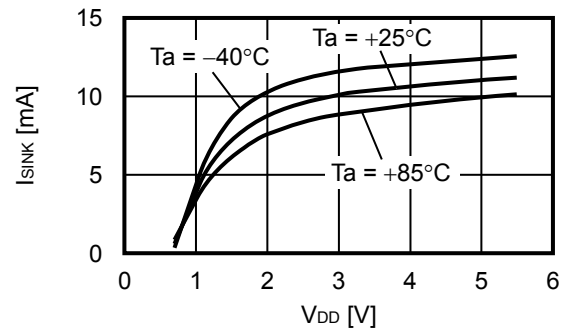
9. Output response time vs. Power supply voltage



10. Source current vs. Power supply voltage

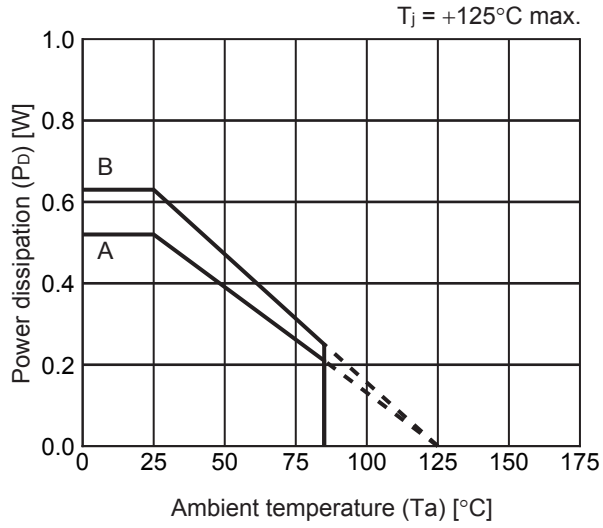


11. Sink current vs. Power supply voltage



■ Power Dissipation

SOT-23-5



Board	Power Dissipation (P_D)
A	0.52 W
B	0.63 W
C	-
D	-
E	-

SOT-23-3/3S/5/6 Test Board

 IC Mount Area

(1) Board A



Item	Specification	
Size [mm]	114.3 x 76.2 x t1.6	
Material	FR-4	
Number of copper foil layer	2	
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via	-	

(2) Board B



Item	Specification	
Size [mm]	114.3 x 76.2 x t1.6	
Material	FR-4	
Number of copper foil layer	4	
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via	-	

No. SOT23x-A-Board-SD-2.0



No. MP005-A-P-SD-1.3

TITLE	SOT235-A-PKG Dimensions
No.	MP005-A-P-SD-1.3
ANGLE	
UNIT	mm
ABLIC Inc.	



→ Feed direction

No. MP005-A-C-SD-2.1

TITLE	SOT235-A-Carrier Tape
No.	MP005-A-C-SD-2.1
ANGLE	
UNIT	mm
ABLIC Inc.	



Enlarged drawing in the central part



No. MP005-A-R-SD-1.1

TITLE	SOT235-A-Reel		
No.	MP005-A-R-SD-1.1		
ANGLE		QTY.	3,000
UNIT	mm		
ABLIC Inc.			

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