Notificatio	on Numbe	r: 202	210210000		Notificati	on Da	ate:	Mar.	. 16, 2021
			H941AS-Q1						,
Customer	Contact:	PCN Ma	nager				Dept:	(Quality Services
Change T	ype:		Electrical Spe	cificat	ion				
Notification Details									
Descriptio	on of Chan	ge:							
			d is announci	ng an	informatio	n only	/ notific	cation	
			ng updated a			elow.			
The followi	ng change	history pr	ovides furthe	er deta	ils.				
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Texa	S								DS90UH941AS-Q1
INST.	RUMENTS					SN	NLS633B - N	MAY 2019	- REVISED JANUARY 2021
Changes f	from Revisio	n A (Octob	er 2020) to Rev	vision I	3 (January 2	2021)			Page
									4
 Update 	AbsMax FPE	D-Link III out	put voltage to 1	.32V					9
 Update 	Analog volta	ge to 1.32V.							9
 Change 						9			
									15
	note to suppo	orted DSI Vio	deo Formats. Ea	ach vide	eo line is exp	ected t	o be sen	it as a	single DSI packet
26 Addadu									20
		-		-					
	 Updated internal pattern generation app note name								
				-					
	-								
-	-								61
	•								61
		-							61
		-			-				61
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•	-	-		•					61
-	-								61
-	_	_							61
	-		•						118
Added	Analog Indire	ct Registers	page						
Undated	d power up se	equence to	include initializa	ation of	internal DSL	clock s	ettings		148
-		-					-		
Included link to 941AS device bringup guide									

Changes from Revision B (October 2020) to Revision C (January 2021) Update RES1 pin description	Page
Update AbsMax FPD-Link III output voltage to 1.32V	
Update AbsMax Analog voltage to 1.32V	
Changed ESD HBM other pins rating to +/- 2500V	
Changed max DSI UI instantaneous to 6.67ns	
Added note to supported DSI Video Formats. Each video line is expected to be sent as a 25	single DSI packet
Added reference to splitter mode applications report	
Updated internal pattern generation app note name	
Revised Clock Mode description to align with register description	
Revised example code for 2:2 mode	
Updated device name to include -Q1	
Clarified how to enable replication mode	47
Update Asymmetric Splitting With Cropping graph	50
Update Asymmetric Splitting With VC-IDs graph	
Fixed register address format	
Update register 0x3[1] description	
Clarify for splitter mode register 0x3E[6:5] takes priority over register 0x56	
Update register 0x56[1:0] reset value to 0	
Clarify register 0x56[1:0] should not be used in splitter mode	
Changed register 0x5A[2] to reserved	
Clarify SLAVE_ID and SLAVE_ALIAS_ID registers are port specific	
Update register 0x56[1:0] description.	
Corrected DSI_ERR_COUNT register address	
Added Analog Indirect Registers page	
Updated power up sequence to include initialization of internal DSI clock settings	138
Included link to 941AS device bringup guide	

The datasheet number will be changing.

Device Family	Change From:	Change To:
DS90UH941AS-Q1	SNLS633A	SNLS633B
DS90UB941AS-Q1	SNLS640B	SNLS640C

These changes may be reviewed at the datasheet links provided. <u>http://www.ti.com/product/DS90UH941AS-Q1</u>

http://www.ti.com/product/DS90UB941AS-Q1

Reason for Change:

To accurately reflect device characteristics.

Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

No anticipated impact. This is a specification change announcement only. There are no changes to the actual device.

Changes to product identification resulting from this notification:						
None.						
Product Affected:						
DS90UB941ASRTDRQ1	DS90UB941ASRTDTQ1	DS90UH941ASRTDRQ1	DS90UH941ASRTDTQ1			

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