

Features

- ESD protection for one line with uni-directional
- Provide transient protection for one line to IEC 61000-4-2 (ESD) ±30kV (air/contact) IEC 61000-4-4 (EFT) 80A (5/50ns) IEC 61000-4-5 (Lightning) 170A (8/20μs)
- Suitable for, **15V and below,** operating voltage applications
- 2.0mm x 2.0mm DFN package saves board space
- High surge protection
- Protect one I/O line or one power line
- Fast turn-on and low clamping voltage
- Solid-state silicon-avalanche and active circuit triggering technology
- Green part

Applications

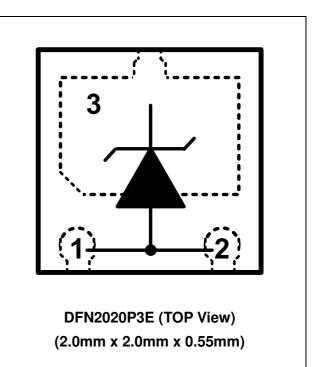
- Power supply protection
- USB VBUS protection
- Cellular handsets and accessories
- Panel modules
- Portable devices
- Touch panels
- Notebooks and handhelds
- Peripherals

Description

AZ4715-01F is a design which includes a uni-directional surge rated clamping cell to protect one power line, or one control line, or one low-speed data line in an electronic system. The AZ4715-01F has been specifically designed to protect sensitive components which are connected to power and control lines from over-voltage damage and latch-up caused by Electrostatic Discharging (ESD), Electrical Fast Transient (EFT), Lightning, and Cable Discharge Event (CDE). AZ4715-01F is a unique design which includes proprietary clamping cell in a single package. During transient conditions, the proprietary clamping cell prevents over-voltage on the power line or control/data lines, protecting any downstream component.

AZ4715-01F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

Circuit Diagram / Pin Configuration





SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, unless otherwise specified)				
PARAMETER	SYMBOL	RATING	UNIT	
Peak Pulse Current (tp=8/20µs)	I _{PP} (Note 1)	170	А	
Operating Supply Voltage (pin-3 to pin-1 and pin-2)	V_{DC}	16.5	V	
ESD per IEC 61000-4-2 (Air)	V_{ESD-1}	±30	kV	
ESD per IEC 61000-4-2 (Contact)	V_{ESD-2}	±30	κv	
Lead Soldering Temperature	T _{SOL}	260 (10 sec.)	°C	
Operating Temperature	T _{OP}	-55 to +125	°C	
Storage Temperature	T _{STO}	-55 to +150	°C	

ELECTRICAL CHARACTERISTICS						
PARAMETER	SYMBOL	CONDITION	MIN	ΤΥΡ	МАХ	UNIT
Reverse Stand-Off Voltage	V _{RWM}	pin-3 to pin-1 and pin-2, T = 25 $^{\circ}$ C.			15	V
Reverse Leakage Current	_{Leak}	$V_{RWM} = 15V, T = 25 \ ^{\circ}C,$ pin-3 to pin-1 and pin-2.			0.5	μA
Reverse Breakdown Voltage	V_{BV}	$I_{BV} = 1mA$, T = 25 °C, pin-3 to pin-1 and pin-2.	16.5		19.5	V
Forward Voltage	V_{F}	$I_F = 15mA$, T = 25 °C, pin-1 and pin-2 to pin-3.	0.6		1.2	V
Surge Clamping Voltage (Note 1)	$V_{CL-surge}$	$I_{PP} = 170A$, tp = 8/20µs, T = 25 °C, pin-3 to pin-1 and pin-2.		30		V
ESD Clamping Voltage (Note 2)	V_{CL-ESD}	IEC 61000-4-2 +8kV ($I_{TLP} = 16A$), T = 25 °C, Contact mode, pin-3 to pin-1 and pin-2.		18		V
ESD Dynamic Turn-on Resistance	R _{dynamic}	IEC 61000-4-2 0~+8kV, T = 25 $^{\circ}$ C, Contact mode, pin-3 to pin-1 and pin-2.		0.04		Ω
Channel Input Capacitance	C _{IN}	$V_R = 0V$, f = 1MHz, T = 25 °C, pin-3 to pin-1 and pin-2.		0.9	1.1	nF

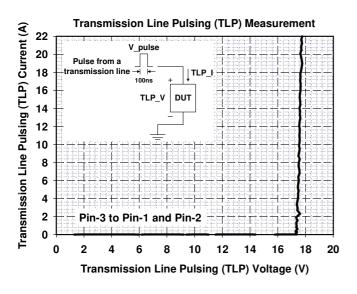
Note 1: The Peak Pulse Current measured conditions: $t_p = 8/20\mu s$, 2Ω source impedance.

Note 2: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.

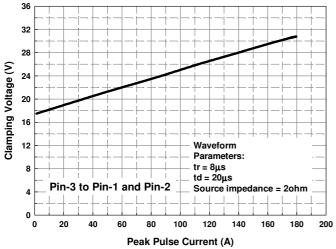
TLP conditions: $Z_0 = 50\Omega$, $t_p = 100$ ns, $t_r = 1$ ns.

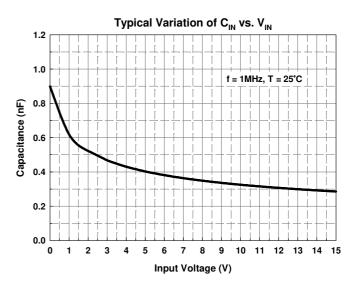


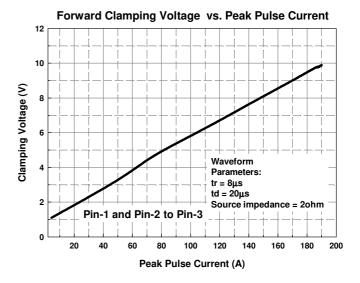
Typical Characteristics



Reverse Clamping Voltage vs. Peak Pulse Current









Application Information

The AZ4715-01F is designed to protect one line against system ESD/EFT/Lightning pulses by clamping them to an acceptable reference.

The usage of the AZ4715-01F is shown in Fig. 1. Protected lines, such as data lines, control lines, or power lines, are connected to pin 3. The pin 1 and pin 2 should be connected directly to a ground plane on the board. All path lengths connected to the pins of AZ4715-01F should be kept as short as possible to minimize parasitic inductance in the board traces. In order to obtain enough suppression of ESD induced transient, a good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ4715-01F.
- Place the AZ4715-01F near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

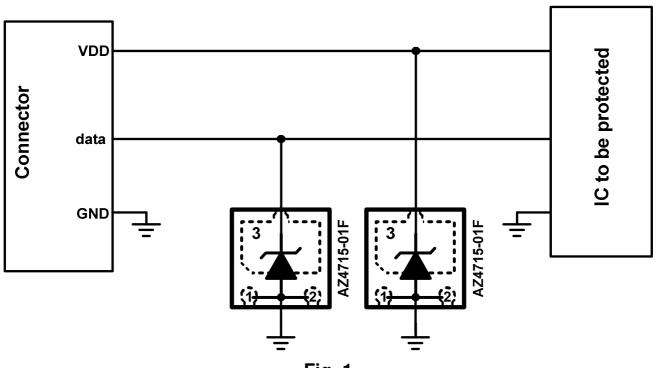


Fig. 1



Fig. 2 shows another simplified example of using AZ4715-01F to protect the control lines,

low-speed data lines, and power lines from ESD transient stress.

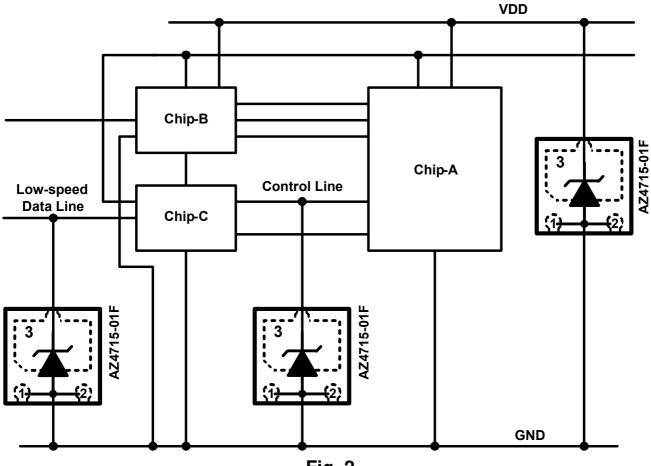
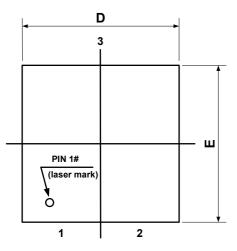


Fig. 2

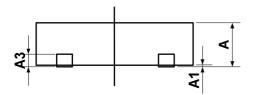


Mechanical Details

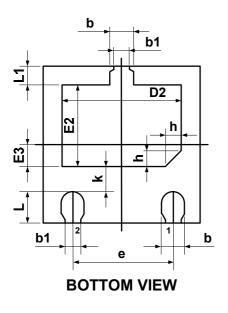
DFN2020P3E PACKAGE DIAGRAMS



TOP VIEW



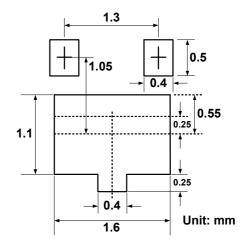




PACKAGE DIMENSIONS

Millimeters					
Symbol					
	MIN	NOM	MAX		
Α	0.50	0.55	0.60		
A1	0.00	0.02	0.05		
b	0.25	0.30	0.35		
b1	0.20BSC				
A3	0.152BSC				
D	1.90	2.00	2.10		
D2	1.40	1.50	1.60		
е		1.30BSC			
E	1.90	2.00	2.10		
E2	0.95	1.05	1.15		
E3	0.20	0.30	0.40		
L	0.35	0.40	0.45		
L1	0.20	0.25	0.30		
h	0.20REF				
k	0.20	0.30	0.40		

LAND LAYOUT

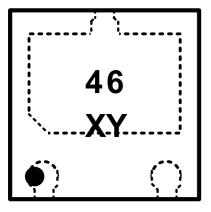


Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.



MARKING CODE



Part Number	Marking Code	
AZ4715-01F.R7G	46 XY	
(Green Part)		

Note : Green means Pb-free, RoHS, and Halogen free compliant.

46 = Device Code X = Date Code ; Y = Control Code

Ordering Information

PN#	Material	Туре	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ4715-01F.R7G	Green	T/R	7 inch	3,000/reel	4 reels = 12,000/box	6 boxes = 72,000/carton

Revision History

Revision	Modification Description
Revision 2018/03/06	Formal Release.