Features

- ESD protection for 4 high-speed I/O channels
- Provide transient protection for each channel to
  IEC 61000-4-2 (ESD) ±18kV (air/contact)
  IEC 61000-4-5 (Lightning) 6.5A (8/20μs)
- Low capacitance : 1.3pF typical
- Fast turn-on and low clamping voltage
- Array of surge rated diodes with internal equivalent TVS diode
- Small package saves board space
- Solid-state silicon-avalanche and active circuit triggering technology
- ***Green part***
- ***AEC-Q101 qualified***

Applications

- LVDS interface
- Video graphics cards
- USB2.0 power and data lines protection
- Monitors and flat panel displays
- Automotive application

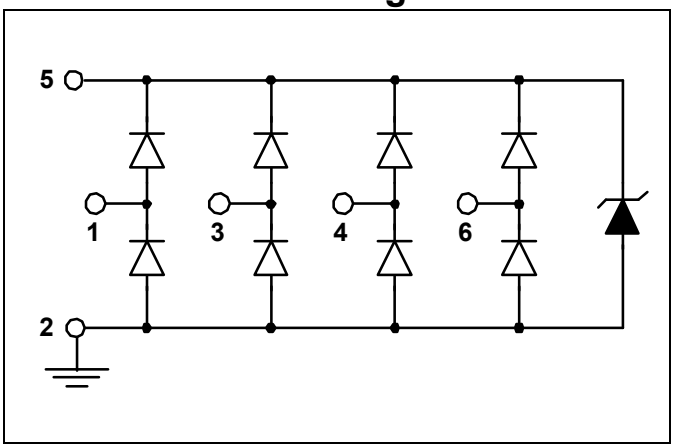
Description

AZ9C39-04S is a high performance design which includes surge rated diode arrays to protect high speed data interfaces. The AZ9C39-04S has been specifically designed to protect sensitive components, which are connected to data and transmission lines, from over-voltage caused by Electrostatic Discharging (ESD), and Lightning.

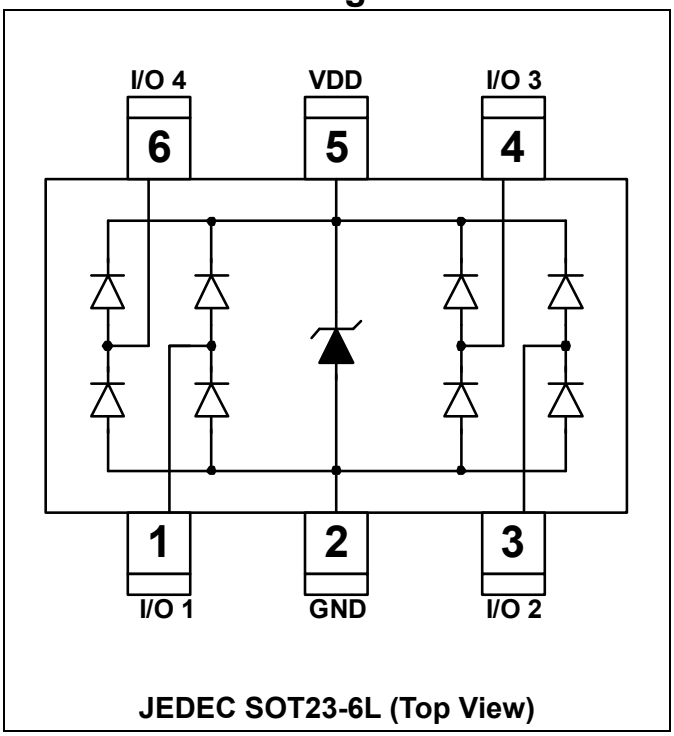
AZ9C39-04S is a unique design which includes surge rated, low capacitance steering diodes and a unique design of clamping cell which is an equivalent TVS diode in a single package. During transient conditions, the steering diodes direct the transient to either the power supply line or to the ground line. The internal unique design of clamping cell prevents over-voltage on the power line, protecting any downstream components.

AZ9C39-04S may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (± 15kV air, ±8kV contact discharge).

Circuit Diagram



Pin Configuration



JEDEC SOT23-6L (Top View)

Specifications

Absolute Maximum Ratings			
Parameter	**Symbol**	**Rating**	**Unit**
Peak Pulse Current (t_p =8/20μs)	I_{PP}	6.5	A
Operating Voltage	V_{DC}	5.5	V
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	±18 ±18	kV
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	°C
Operating Temperature	T_{OP}	-55 to +125	°C
Storage Temperature	T_{STO}	-55 to +150	°C

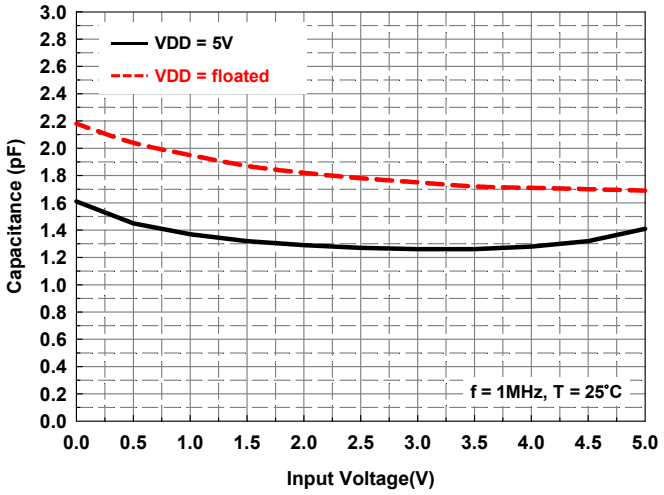
Electrical Characteristics						
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Reverse Stand-Off Voltage	V_{RWM}	Pin-5 to pin-2, T= 25 °C.			5	V
Reverse Leakage Current	I_{Leak}	V_{RWM} = 5V, T= 25 °C, pin-5 to pin-2.			5	μA
Channel Leakage Current	$I_{CH-Leak}$	V_{Pin-5} = 5V, V_{Pin-2} = 0V, T= 25 °C.			1	μA
Reverse Breakdown Voltage	V_{BV}	I_{BV} = 1mA, T= 25 °C, pin-5 to pin-2.	6		9	V
Forward Voltage	V_F	I_F = 15mA, T= 25 °C, pin-2 to pin-5.		0.8	1.2	V
ESD Clamping Voltage – I/O (Note 1)	$V_{CL-ESD\_I/O}$	IEC 61000-4-2 +8kV (I_{TLP} = 16A), T= 25 °C, contact mode, any I/O pin to GND.		10		V
ESD Clamping Voltage – VDD (Note 1)	V_{CL-ESD_VDD}	IEC 61000-4-2 +8kV (I_{TLP} = 16A), T= 25 °C, contact mode, VDD pin to GND.		7		V
ESD Dynamic Turn-on Resistance – I/O	$R_{dynamic\_I/O}$	IEC 61000-4-2 0~+8kV, T= 25 °C, contact mode, any I/O pin to GND.		0.23		Ω
ESD Dynamic Turn-on Resistance – VDD	$R_{dynamic\_VDD}$	IEC 61000-4-2 0~+8kV, T= 25 °C, contact mode, VDD pin to GND.		0.1		Ω
Surge Clamping Voltage – I/O	$V_{CL-Surge\_I/O}$	I_{PP} = 5A, t_p = 8/20μs, T= 25 °C, any I/O pin to GND.		7.5		V
Surge Clamping Voltage – VDD	$V_{CL-Surge\_VDD}$	I_{PP} = 5A, t_p = 8/20μs, T= 25 °C, VDD pin to GND.		6.5		V
Channel Input Capacitance – 1	C_{IN-1}	V_{Pin-5} = 5V, V_{Pin-2} = 0V, V_{IN} = 2.5V, f = 1MHz, T= 25 °C, any I/O pin to GND.		1.3	1.8	pF
Channel Input Capacitance – 2	C_{IN-2}	V_{Pin-5} = floated, V_{Pin-2} = 0V, V_{IN} = 2.5V, f = 1MHz, T= 25°C, any I/O pin to GND.		1.8	2.3	pF
Channel to Channel Input Capacitance – 1	$C_{I/O-to-I/O-1}$	V_{Pin-5} = 5V, V_{Pin-2} = 0V, V_{IN} = 2.5V, f = 1MHz, T= 25 °C , between I/O pins.		0.1	0.2	pF
Channel to Channel Input Capacitance – 2	$C_{I/O-to-I/O-2}$	V_{Pin-5} = floated, V_{Pin-2} = 0V, V_{IN} = 2.5V, f = 1MHz, T= 25 °C, between I/O pins.		0.2	0.3	pF

Note 1: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.

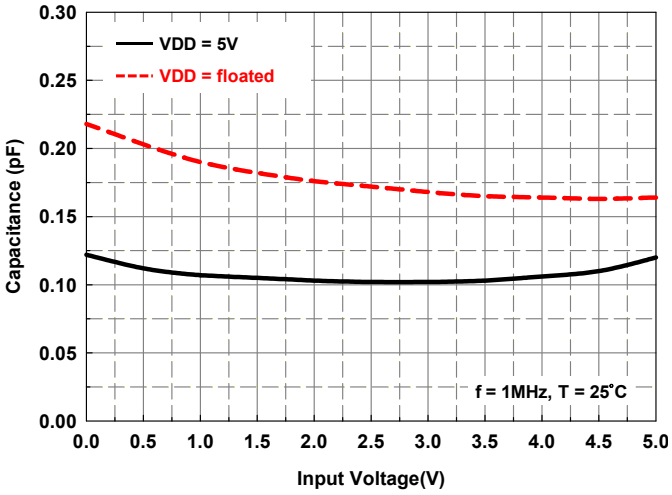
TLP conditions: Z_0 = 50Ω, t_p = 100ns, t_r = 1ns.

Typical Characteristics

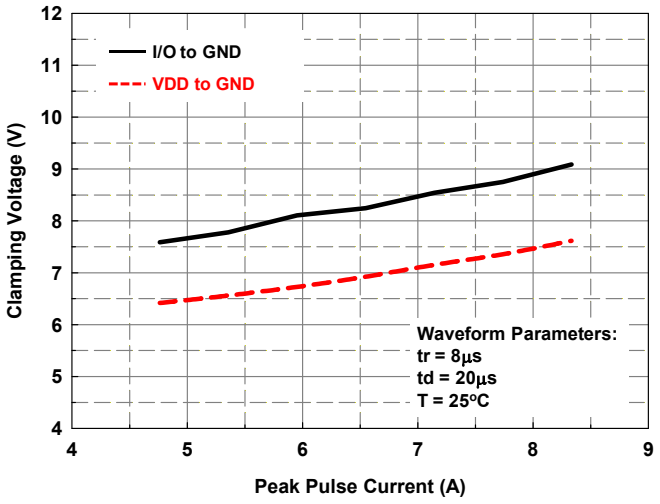
Typical Variation of C_{IN} v.s V_{IN}



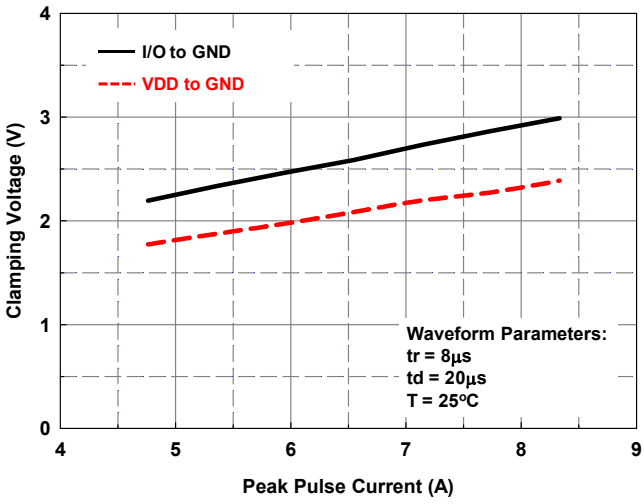
Typical Variation of $C_{I/O\ to\ I/O}$ v.s V_{IN}



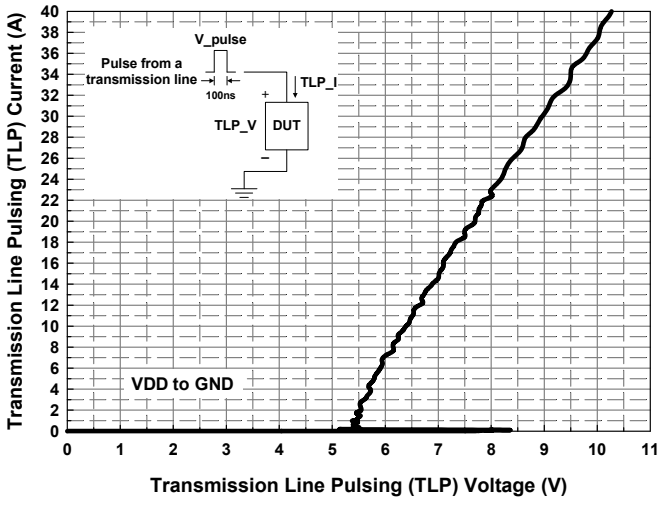
Reverse Clamping Voltage vs. Peak Pulse Current



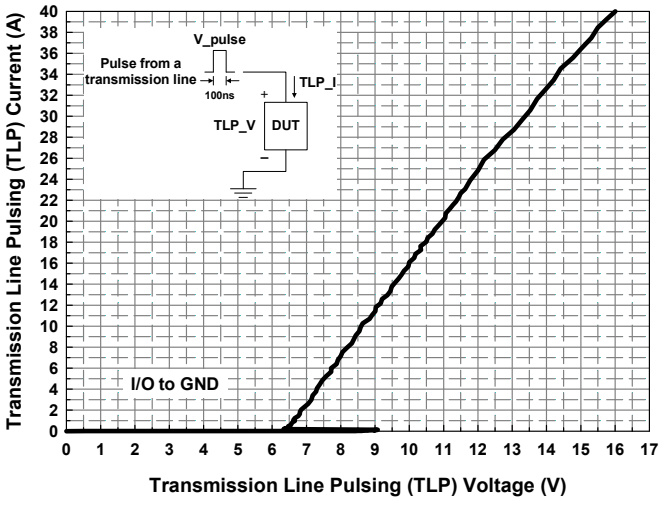
Forward Clamping Voltage vs. Peak Pulse Current



Transmission Line Pulsing (TLP) Measurement



Transmission Line Pulsing (TLP) Measurement



Applications Information

A. Device Connection

The AZ9C39-04S is designed to protect four data lines and power rails from transient over-voltage (such as ESD stress pulse). The device connection of AZ9C39-04S is shown in the Fig. 1. In Fig. 1, the four protected data lines are connected to the ESD protection pins (pin-1, pin-3, pin-4, and pin-6) of AZ9C39-04S. The ground pin (pin-2) of AZ9C39-04S is a negative reference pin. This pin should be directly connected to the GND rail of PCB (Printed Circuit Board). To get minimum parasitic inductance, the path length should keep as short as possible. In addition, the power pin (pin-5) of AZ9C39-04S is a positive reference pin. This pin should directly connect to the VDD rail of PCB., then the VDD rail also can be protected by the power-rail ESD clamped circuit (not shown) of AZ9C39-04S.

AZ9C39-04S can provide protection for 4 I/O signal lines simultaneously. If the number of I/O signal lines is less than 4, the unused I/O pins can be simply left as NC pins.

In some cases, systems are not allowed to be reset or restart after the ESD stress directly applying at the I/O-port connector. Under this situation, in order to enhance the sustainable ESD Level, a 0.1μF chip capacitor can be added between the VDD and GND rails. The place of this chip capacitor should be as close as possible to the AZ9C39-04S.

In some cases, there isn't power rail presented on the PCB. Under this situation, the power pin (pin-5) of AZ9C39-04S can be left as floated. The protection will not be affected, only the load capacitance of I/O pins will be slightly increased. Fig. 2 shows the detailed connection.

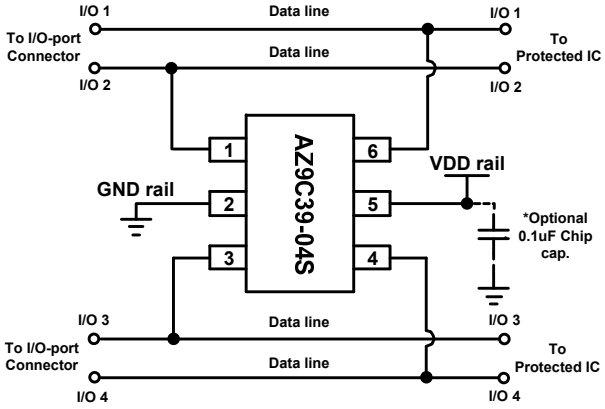


Fig. 1 Data lines and power rails connection of AZ9C39-04S.

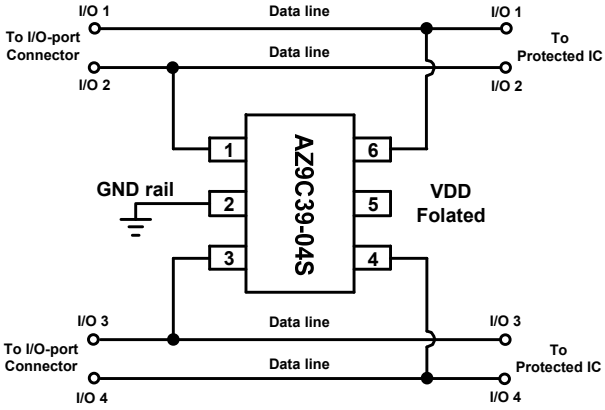
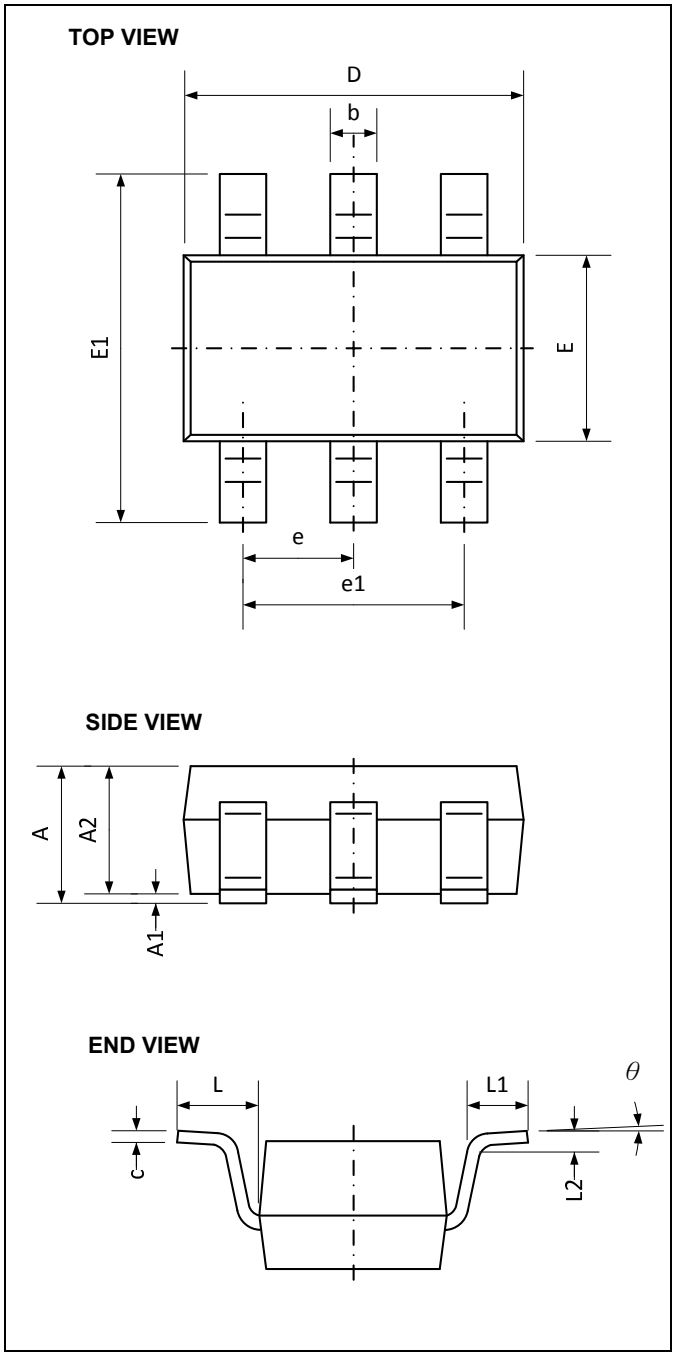


Fig. 2 Data lines and power rails connection of AZ9C39-04S. VDD pin is left as floating when no power rail presented on the PCB.

Mechanical Details

SOT23-6L

Package Diagrams



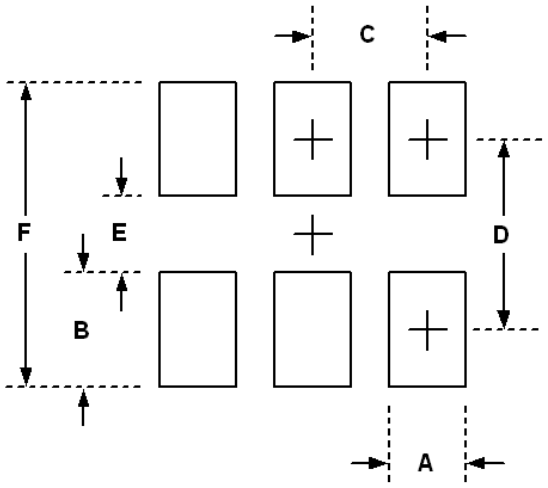
Package Dimensions

Symbol	Millimeters	
	Min.	Max.
A	-	1.25
A1	0.00	0.10
A2	0.90	1.20
b	0.30	0.50
c	0.08	0.21
D	2.72	3.12
E	1.40	1.80
E1	2.60	3.00
e	0.95 BSC	
e1	1.90 BSC	
L1	0.30	0.60
L	0.70 REF	
L2	0.25 BSC	
θ	0	8

Notes:

- This dimension complies with JEDEC outline standard MO-178 Variation AB.
- Dimensioning and tolerancing per ASME Y14.5M-1994.
- All dimensions are in millimeters, and the dimensions in inches are for reference only.
- 1mm = 40 mils = 0.04 inches.

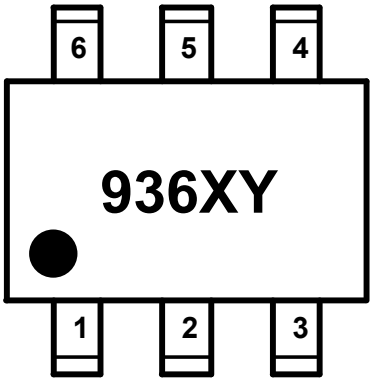
Land Layout



Dimensions		
Index	**Millimeter**	**Inches**
A	0.60	0.024
B	1.10	0.043
C	0.95	0.037
D	2.50	0.098
E	1.40	0.055
F	3.60	0.141

Notes:
This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

Marking Code



936 = Device Code
X = Date Code
Y = Control Code

Part Number	Marking Code
AZ9C39-04S.R7G (Green part)	936XY

Note : Green means Pb-free, RoHS, and Halogen free compliant.

Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ9C39-04S.R7G	Green	T/R	7 inch	3,000/reel	4 reels = 12,000/box	6 boxes = 72,000/carton

Revision History

Revision	Modification Description
Revision 2021/04/12	Formal release.